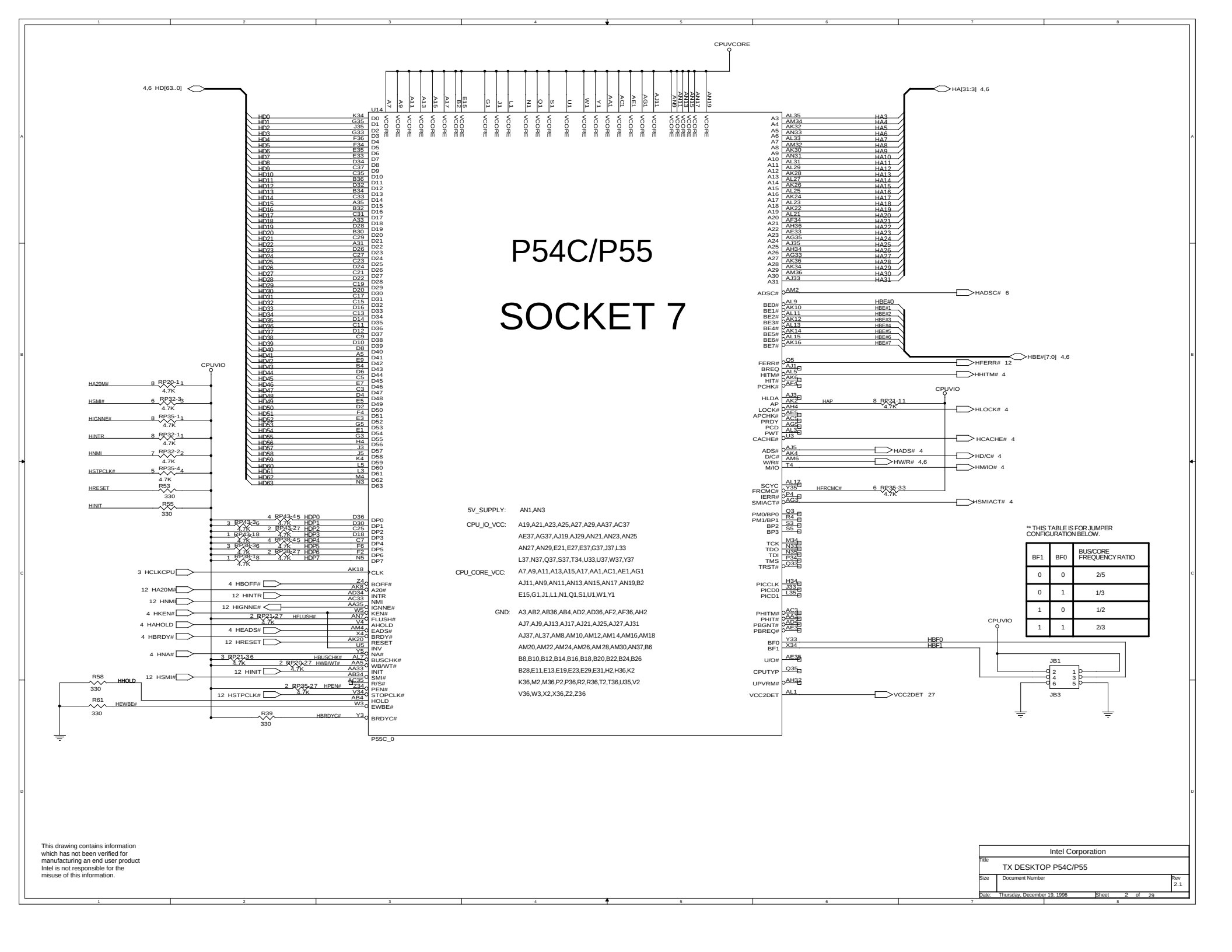
Intel Corporation		
Title: TX DESKTOP INDEX		
Size	Document Number	Rev 2.1
Date: Thursday, December 19, 1996	Sheet 1 of 29	


P54C/P55
SOCKET 7
CPUVCORE
CPUVIO
4,6 HD[63..0]
HA[31:3] 4,6
HBE#[7:0] 4,6
U14
P55C_0
5V_SUPPLY: AN1,AN3
CPU_IO_VCC: A19,A21,A23,A25,A27,A29,AA37,AC37
AE37,AG37,AJ19,AJ29,AN21,AN23,AN25
AN27,AN29,E21,E27,E37,G37,J37,L33
L37,N37,Q37,S37,T34,U33,U37,W37,Y37
CPU_CORE_VCC: A7,A9,A11,A13,A15,A17,AA1,AC1,AE1,AG1
AJ11,AN9,AN11,AN13,AN15,AN17 ,AN19,B2
E15,G1,J1,L1,N1,Q1,S1,U1,W1,Y1
GND: A3,AB2,AB36,AB4,AD2,AD36,AF2,AF36,AH2
AJ7,AJ9,AJ13,AJ17,AJ21,AJ25,AJ27,AJ31
AJ37,AL37,AM8,AM10,AM12,AM1 4,AM16,AM18
AM20,AM22,AM24,AM26,AM 28,AM30,AN37,B6
B8,B10,B12,B14,B16,B18,B20,B22,B24,B26
B28,E11,E13,E19,E23,E29,E31,H2,H36,K2
K36,M2,M36,P2,P36,R2,R36,T2,T36,U35,V2
V36,W3,X2,X36,Z2,Z36
** THIS TABLE IS FOR JUMPER CONFIGURATION BELOW.
BF1 BF0 BUS/CORE FREQUENCY RATIO
0 0 2/5
0 1 1/3
1 0 1/2
1 1 2/3
JB1
JB3
This drawing contains information which has not been verified for manufacturing an end user product Intel is not responsible for the misuse of this information.
Intel Corporation
Title
TX DESKTOP P54C/P55
Size
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Rev 2.1
Date: Thursday, December 19, 1996
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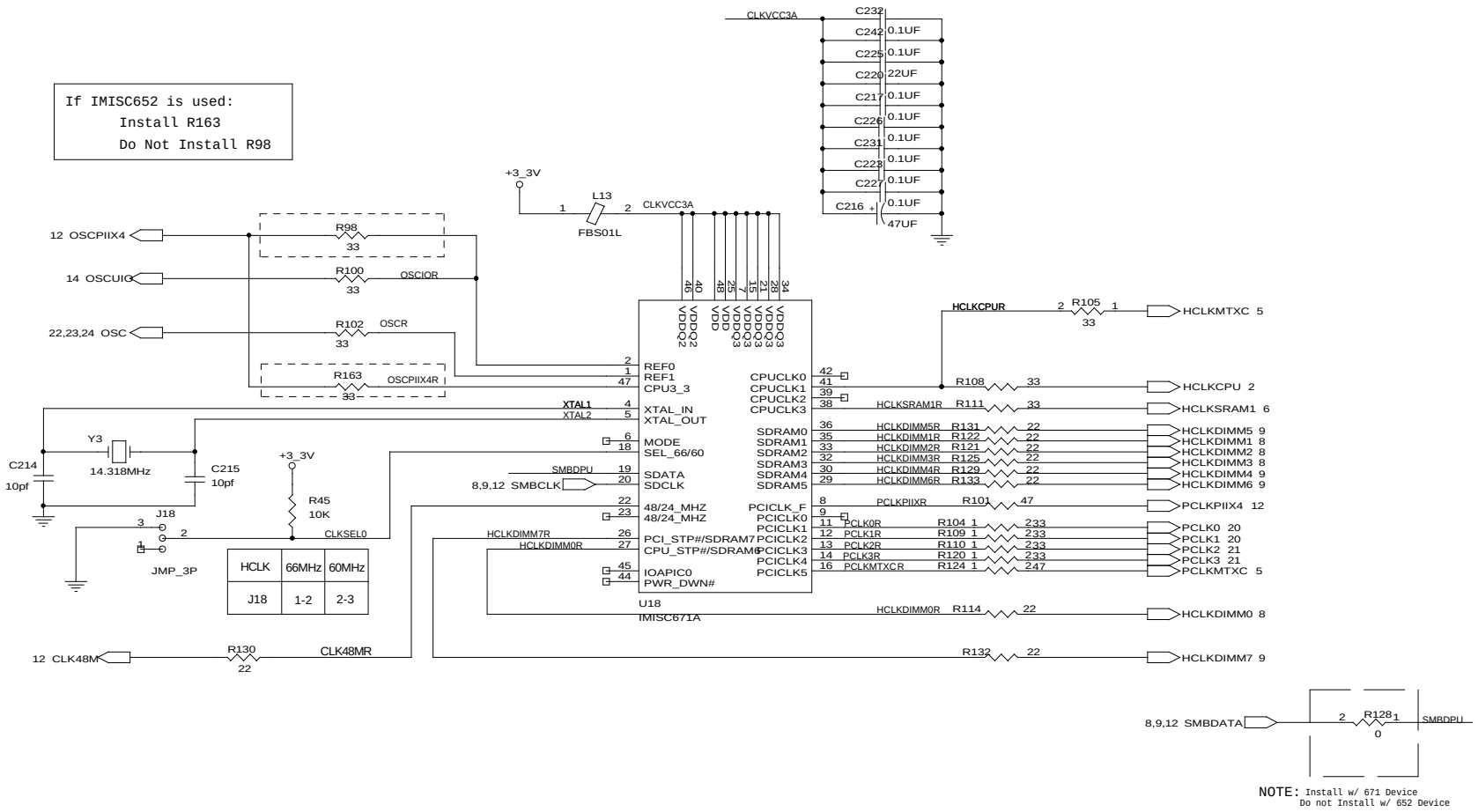
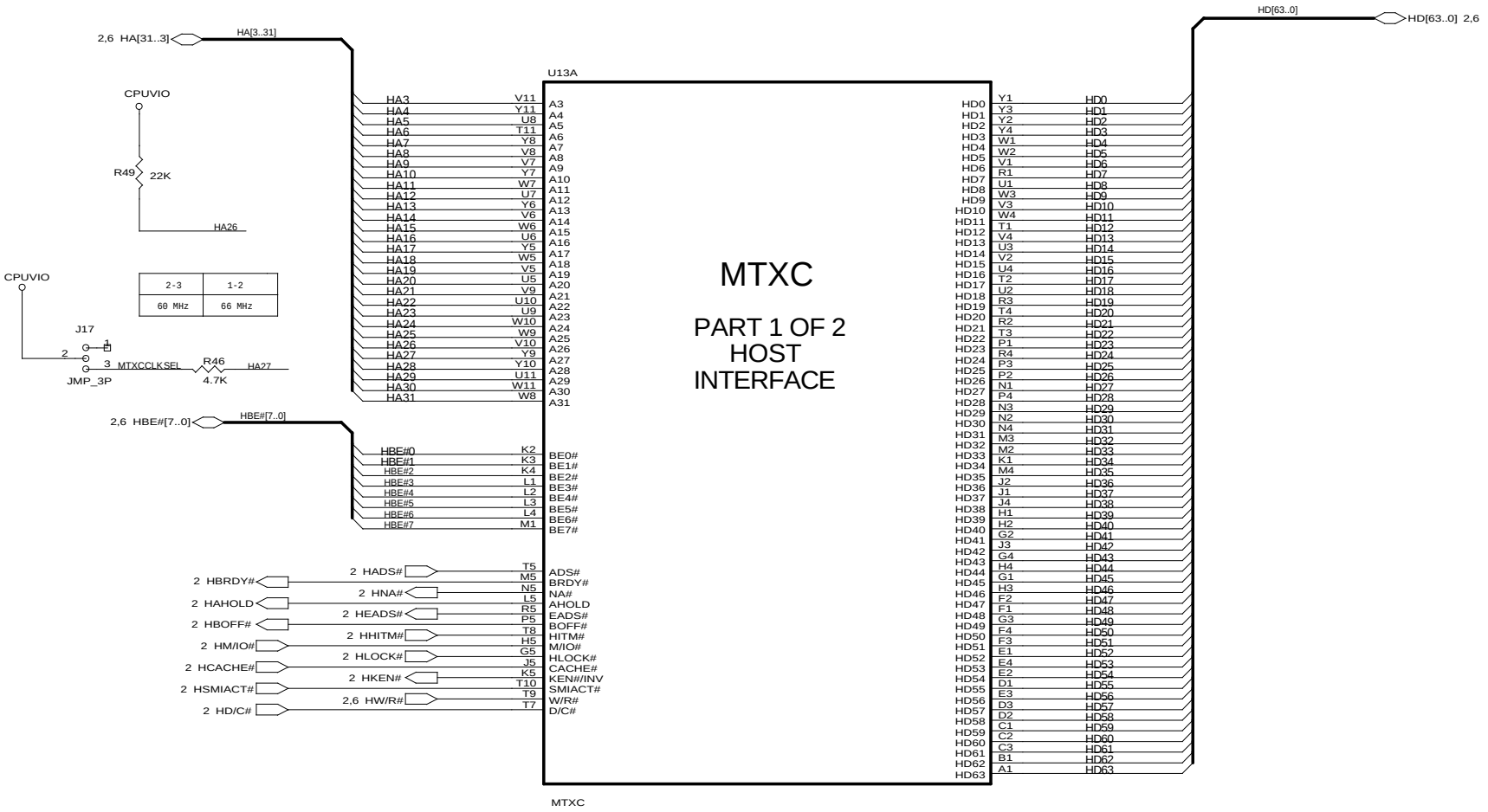
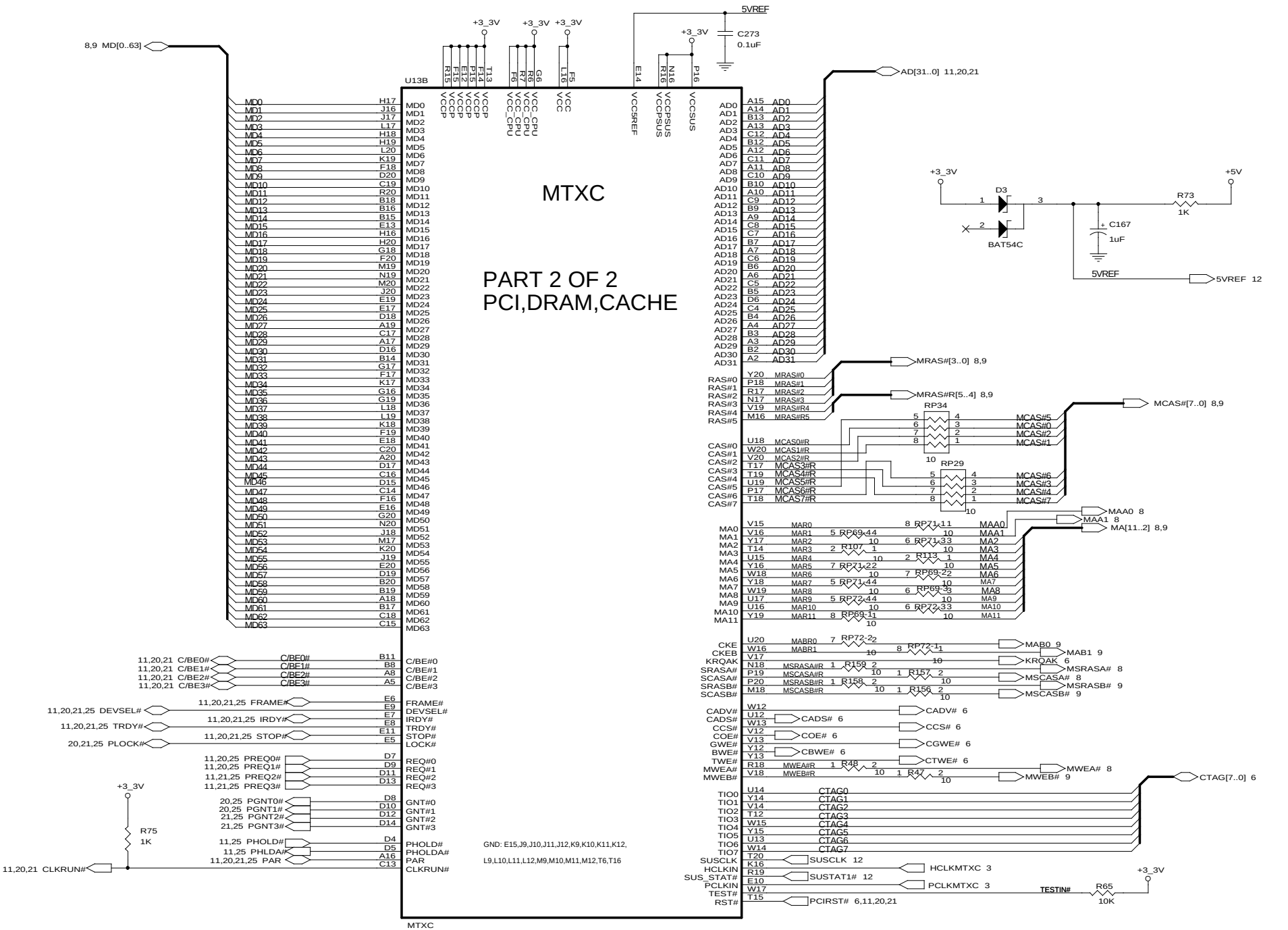


SYSTEM CLOCKS

Intel Corporation			
Title: TX DESKTOP SYSTEM CLOCKS			
Size	Document Number		Rev 2.1
Date: Thursday, December 19, 1996	Sheet 3 of 29		



Intel Corporation			
Title: TX DESKTOP MTXC MICRO CONTROLLER			
Size	Document Number		Rev 2.1
Date: Thursday, December 19, 1996	Sheet 4 of 29		


MTXC
PART 2 OF 2
PCI,DRAM,CACHE
U13B
8,9 MD[0..63]
AD[31..0] 11,20,21
MRAS#[3..0] 8,9
MRAS#R[5..4] 8,9
MCAS#[7..0] 8,9
MAA0 8
MAA1 8
MA[11..2] 8,9
CTAG[7..0] 6
5VREF
C273
0.1uF
D3
BAT54C
R73
1K
C167
1uF
RP34
RP29
R75
1K
R65
10K
TESTIN#
GND: E15,J9,J10,J11,J12,K9,K10,K11,K12,
L9,L10,L11,L12,M9,M10,M11,M12,T6,T16
This drawing contains information which has not been verified for manufacturing an end user product Intel is not responsible for the misuse of this information.
Intel Corporation
TX DESKTOP MTXC MICRO CONTROLLER
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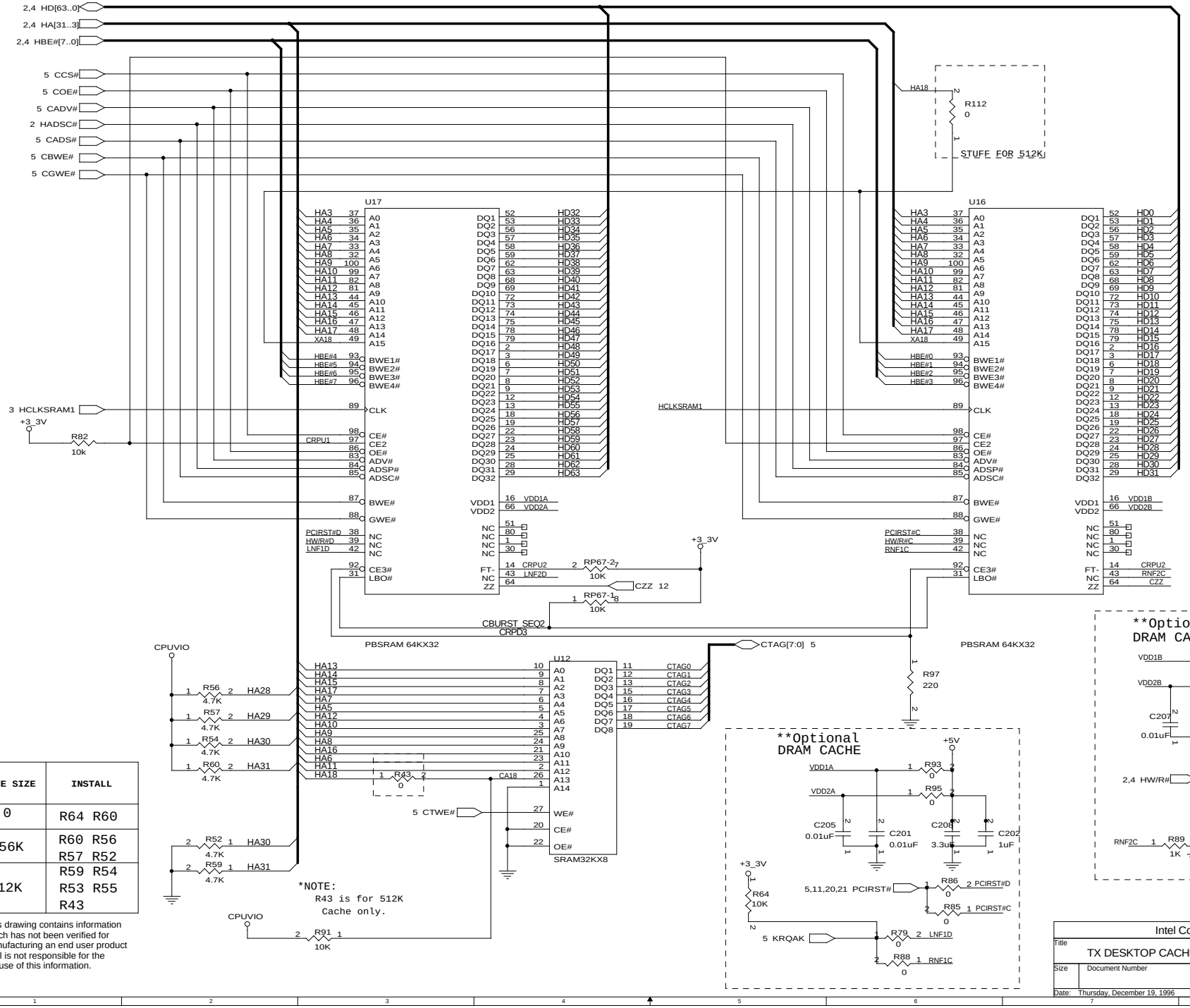
Sheet 5 of 29

NOTE: PIN 16, 38, 39, 42, 43 & 66 are no connects for PB SRAM



CACHE SIZE	INSTALL
0	R64 R60
256K	R60 R56 R57 R52
512K	R59 R54 R53 R55 R43

Intel Corporation	
Title	TX DESKTOP CACHE 1
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Intel Corporation			
Title	CACHE 2		
Size	Document Number		Rev 2.1
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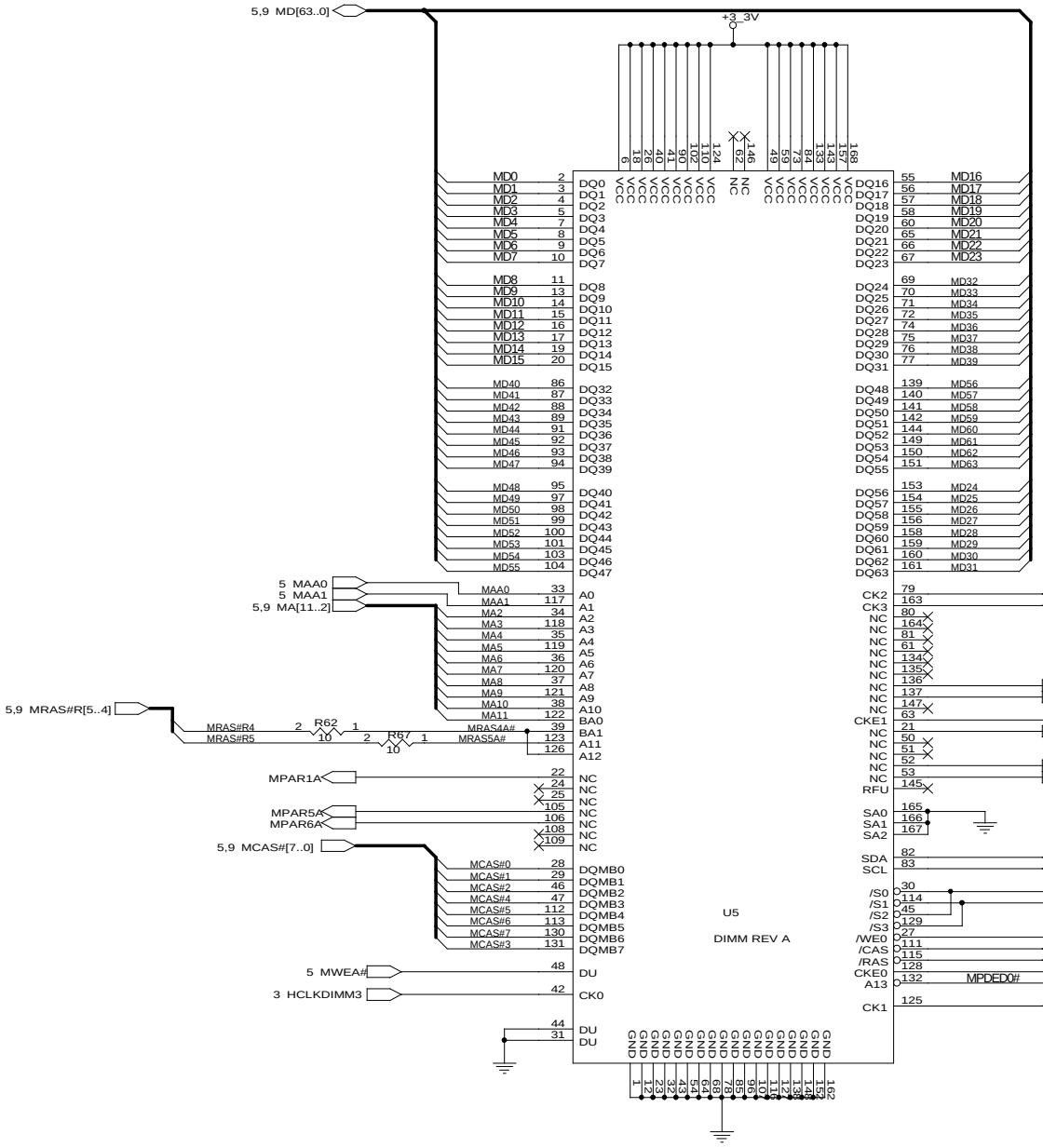

DIMM 0

(BANK 0)

NC:	62,146
+3_3V:	6,18,26,40,41,49,5973
	84,90,102,110,124,13[illegible]8
	143,157,168
GND:	1,12,23,31,32,43,44,5464
	68,78,85,96,107,116,127,[illegible]88
	148,152,162

Intel Corporation		
Title: TX DESKTOP DIMM 0		
Size	Document Number	Rev 2.1
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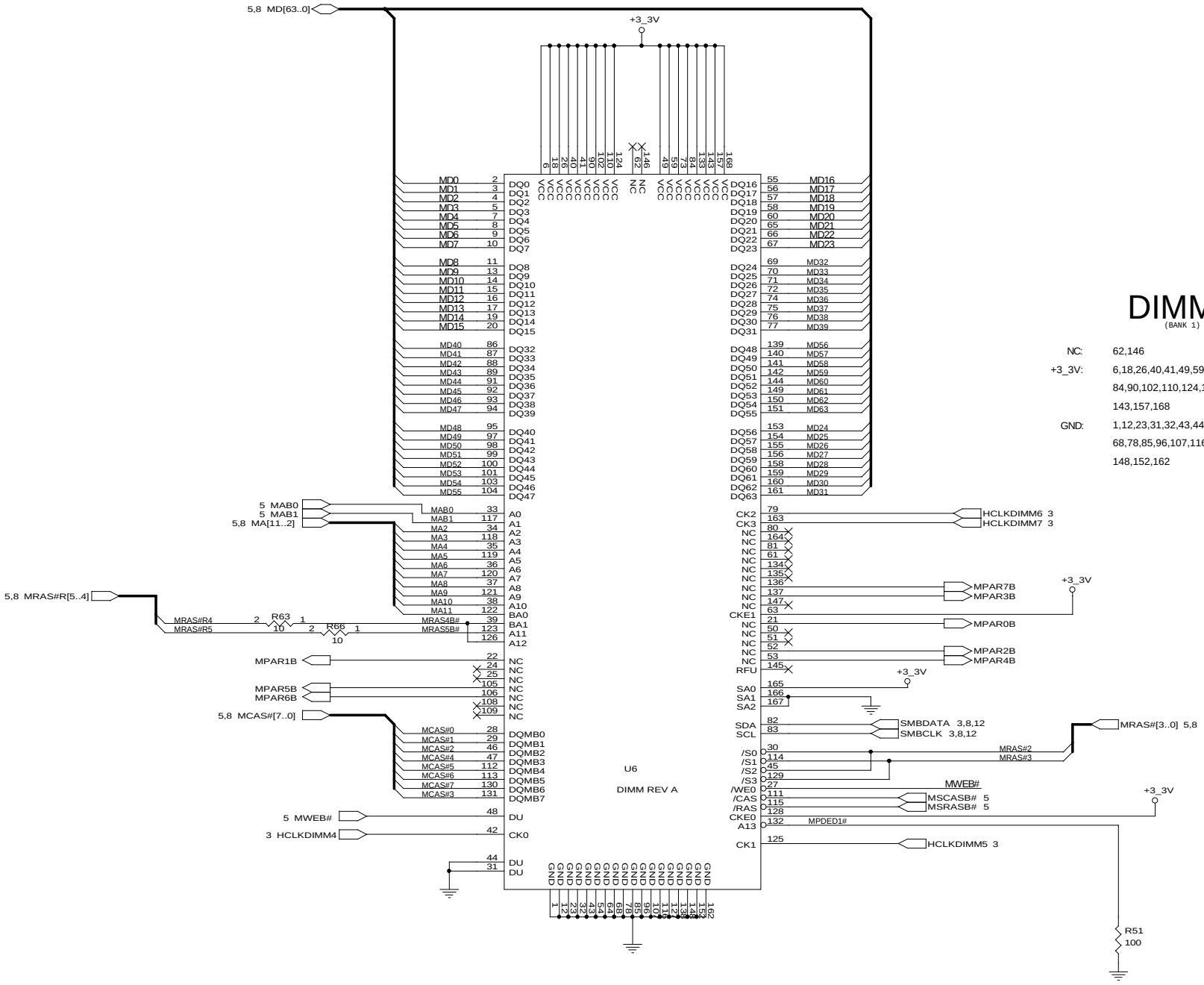

DIMM 1

(BANK 1)

NC: 62,146

+3_3V: 6,18,26,40,41,49,59,73
84,90,102,110,124,133
143,157,168

GND: 1,12,23,31,32,43,44,54,64
68,78,85,96,107,116,127,138
148,152,162

Intel Corporation		
Title: TX DESKTOP DIMM 1		
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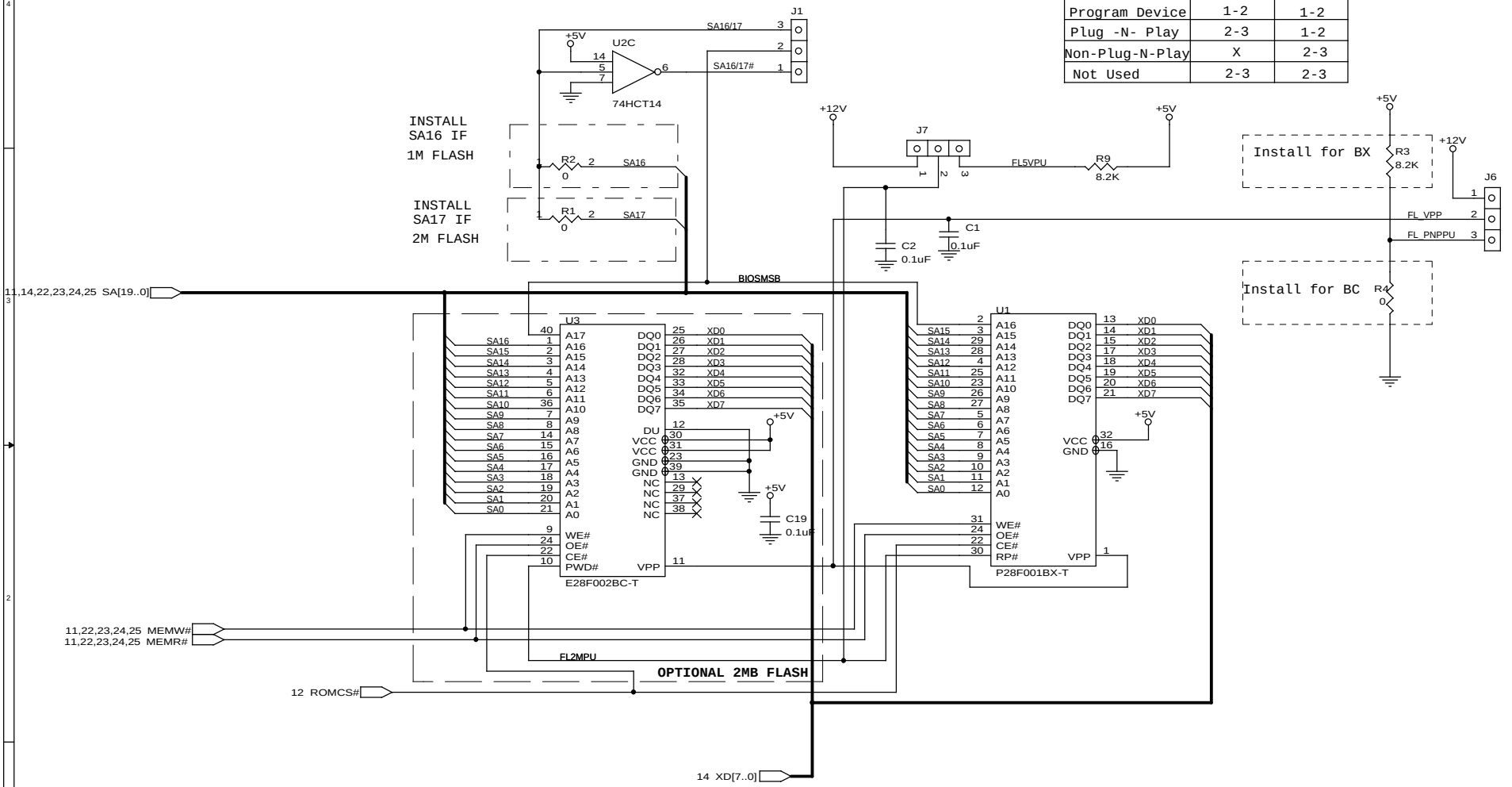
J11

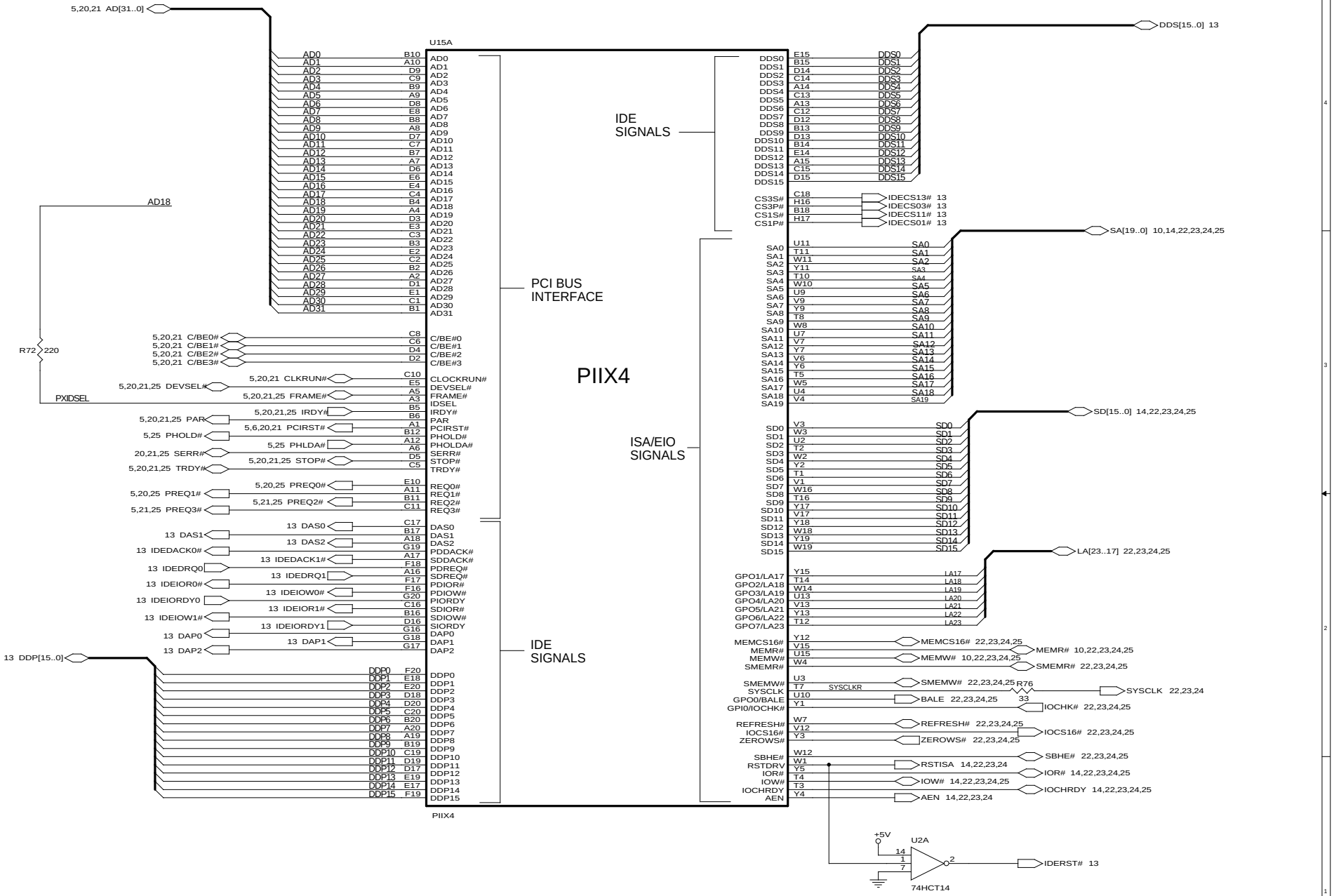
MODE	POS.
NORMAL	2-3
RECOVERY	1-2

Note: The X denotes a don't care.

MODE	J7	J6
Program Device	1-2	1-2
Plug -N- Play	2-3	1-2
Non-Plug-N-Play	X	2-3
Not Used	2-3	2-3



Intel Corporation	
Title	TX DESKTOP FLASH BIOS
Size	Document Number / Rev 2.1
Date: Thursday, December 19, 1996	Sheet 10 of 29



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Intel Corporation		
Title: TX DESKTOP PIIX4 (SOUTHBRIDGE)		
Size	Document Number	Rev 2.1
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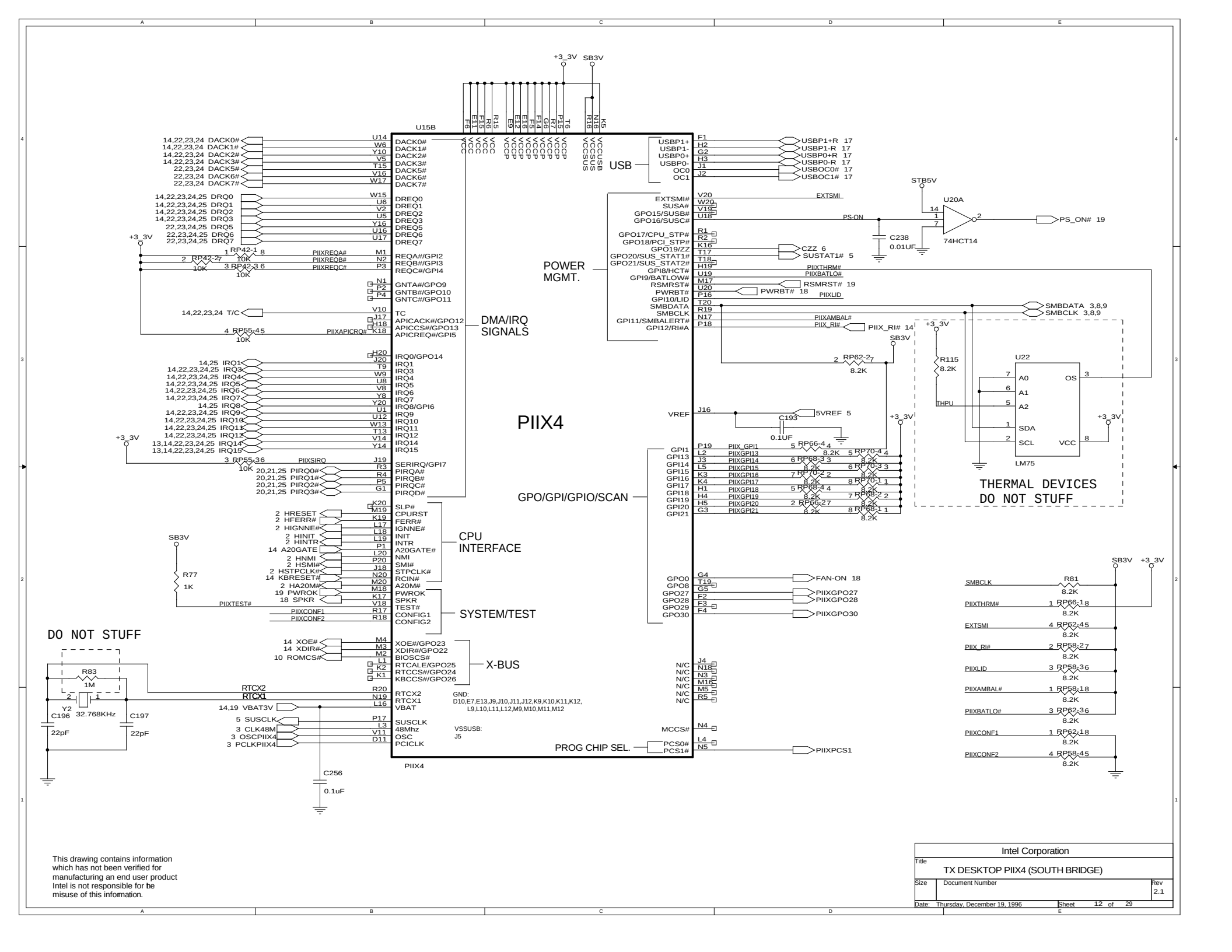

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Intel Corporation		
Title: TX DESKTOP PIIX4 (SOUTH BRIDGE)		
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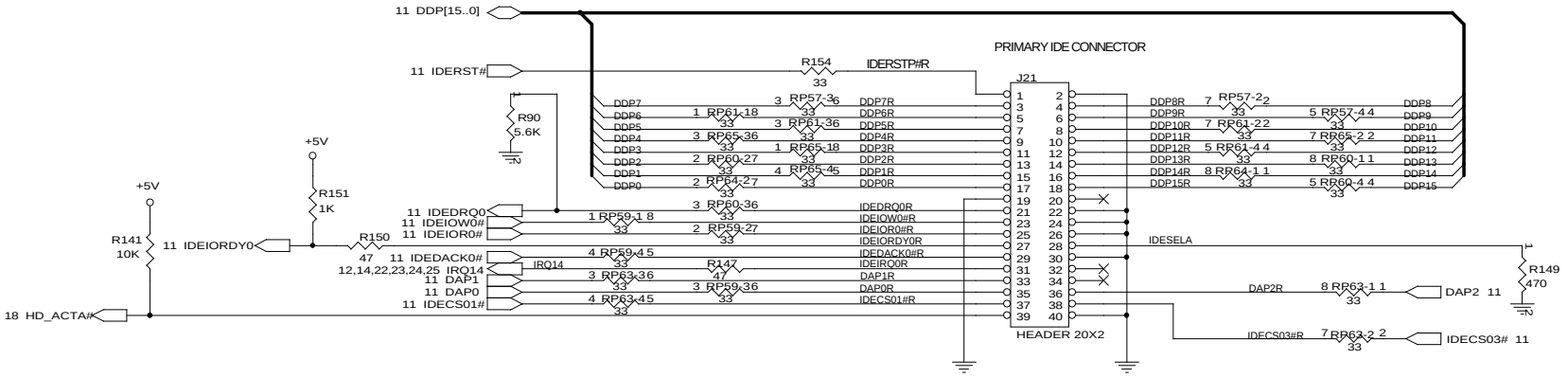
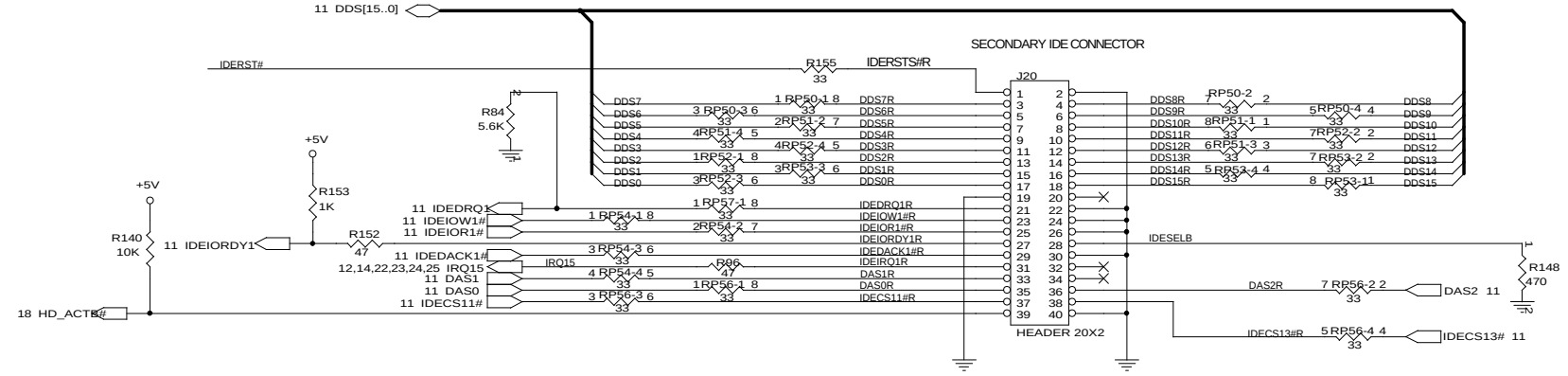
IDE CONNECTORS





Intel Corporation		
Title: TX DESKTOP IDE CONNECTORS		
Size	Document Number	Rev 2.1
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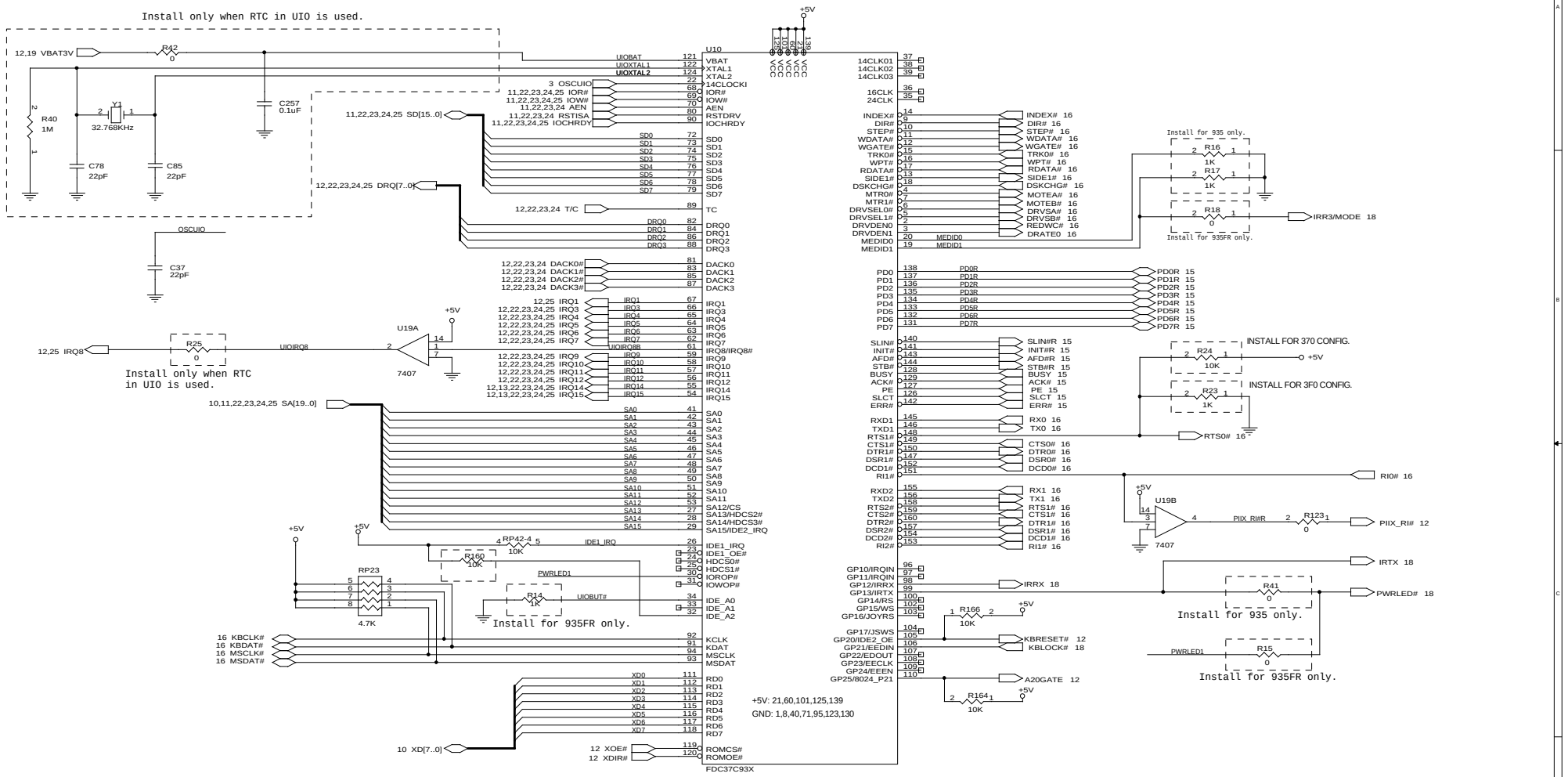
ULTRA IO



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Intel Corporation		
Title: TX DESKTOP ULTRA I/O		
Size	Document Number	Rev 2.1
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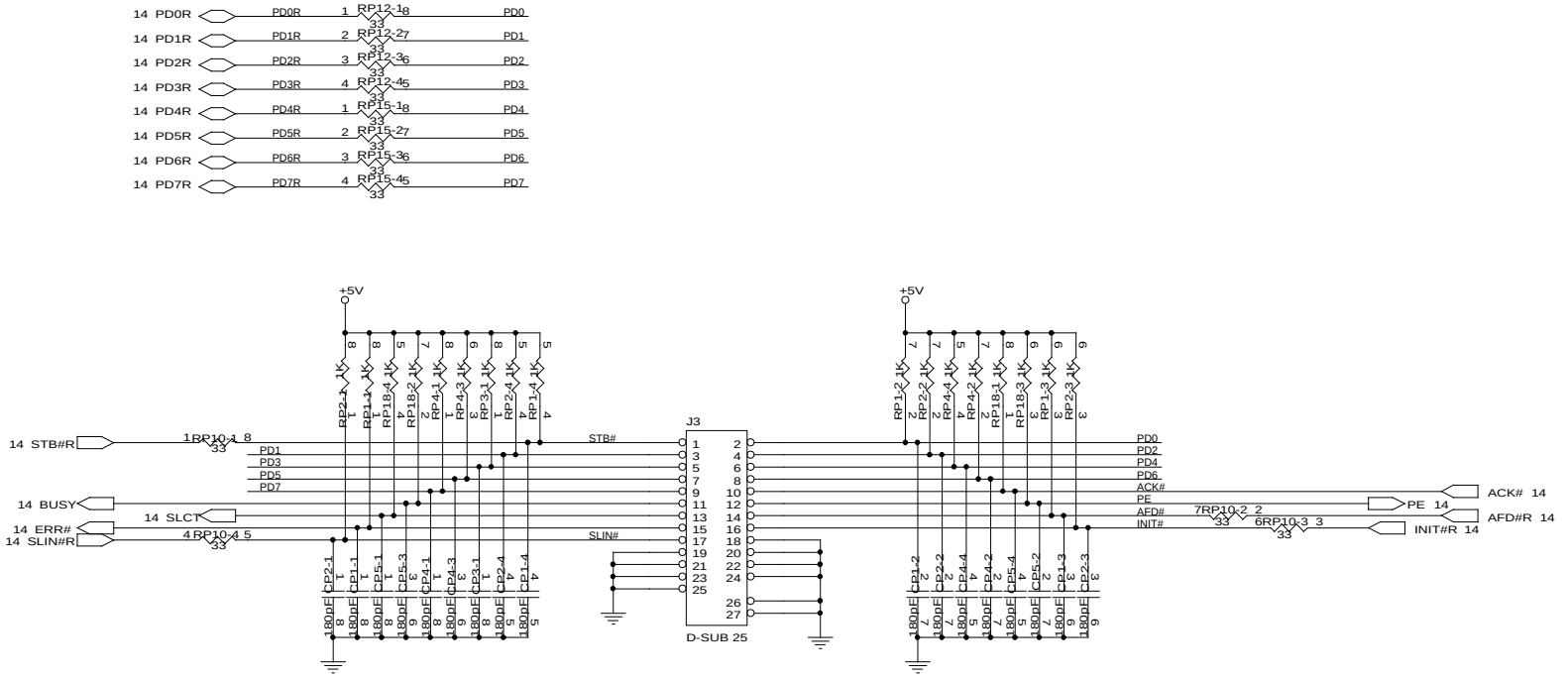

PARALLEL PORT CONNECTOR

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Intel Corporation		
Title: TX DESKTOP PARALLEL HEADER		
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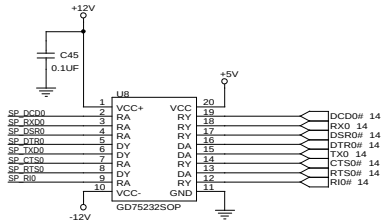
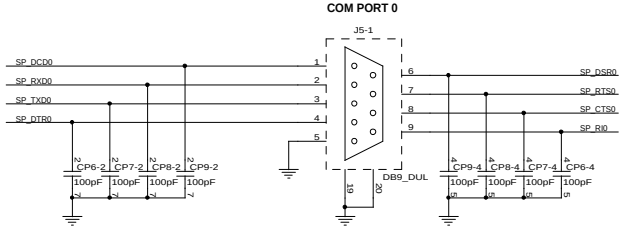
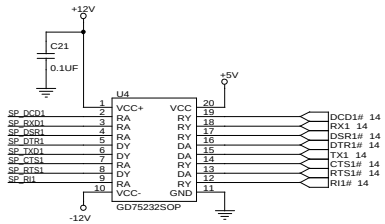
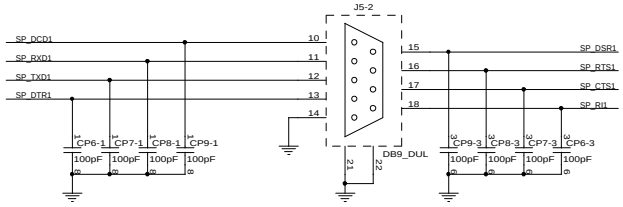


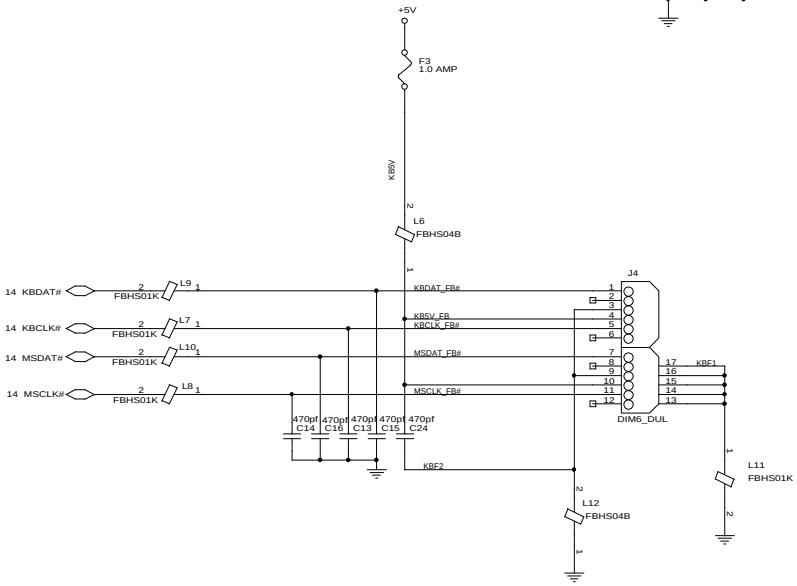
COM PORT 0

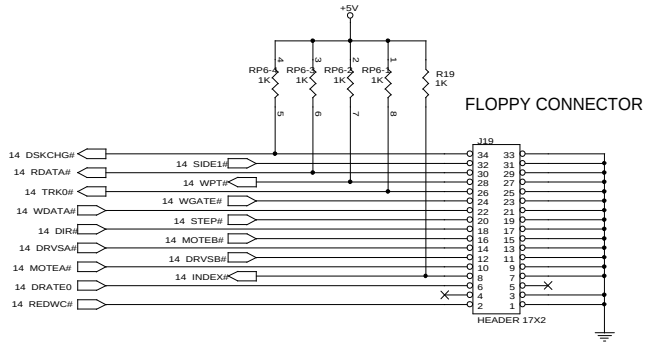




COM PORT 1

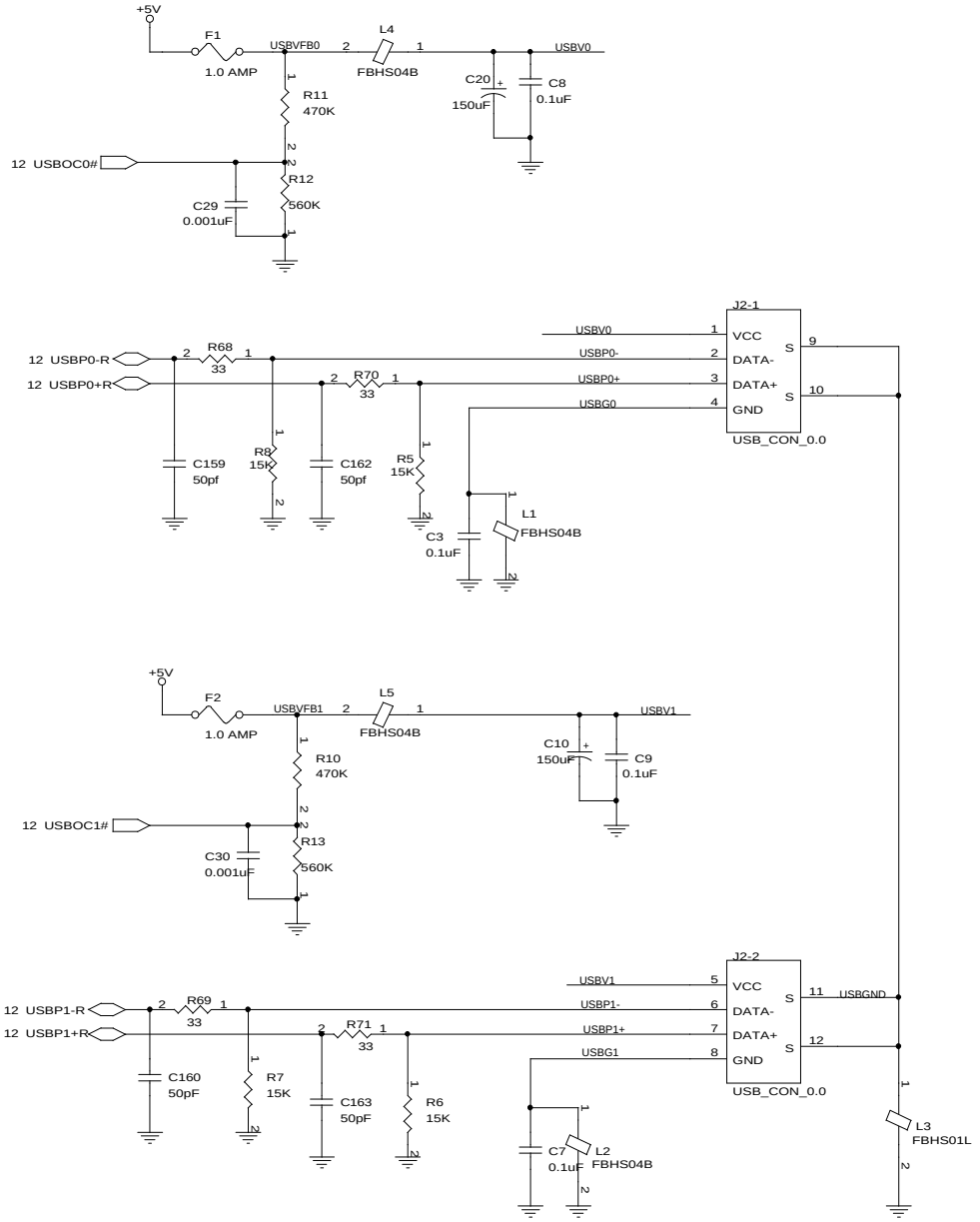






FLOPPY CONNECTOR

Intel Corporation			
Title: TX DESKTOP COM_PORT			
Size	Document Number		Rev 2.1
Date: Thursday, December 19, 1996	Sheet 16 of 29		



USB PORT INTERFACE

Intel Corporation		
Title: TX DESKTOP UNIVERSAL SERIAL BUS (USB)		
Size	Document Number	Rev 2.1
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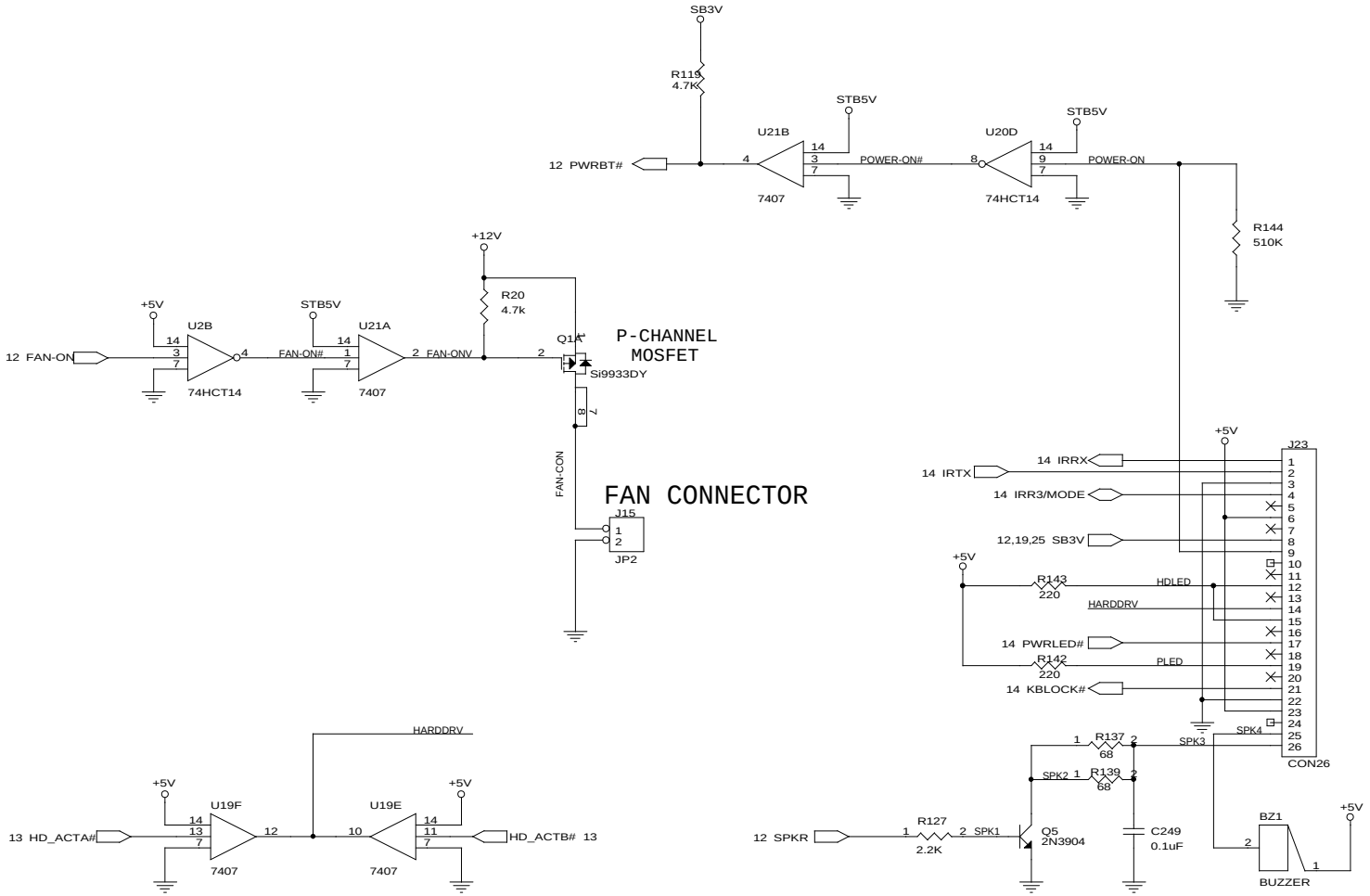

Intel Corporation		
Title: TX_DESKTOP FAN & FRONT PANEL CONNECTORS		
Size	Document Number	Rev 2.1
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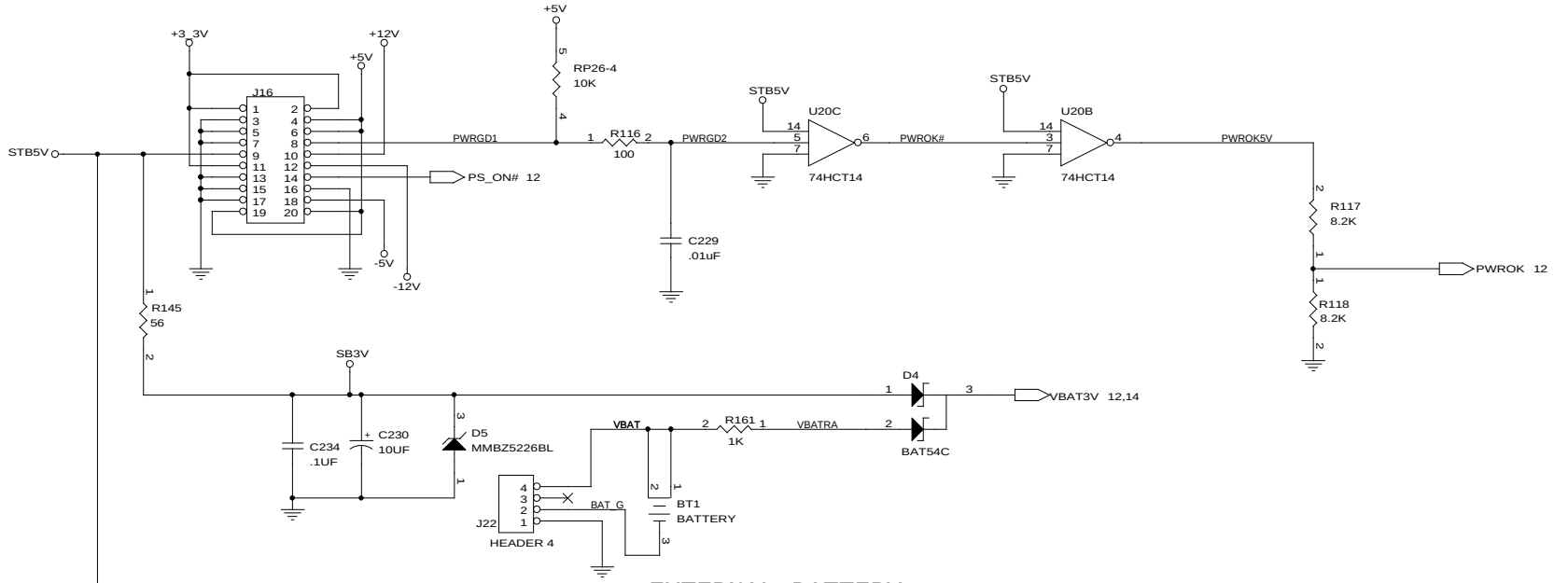
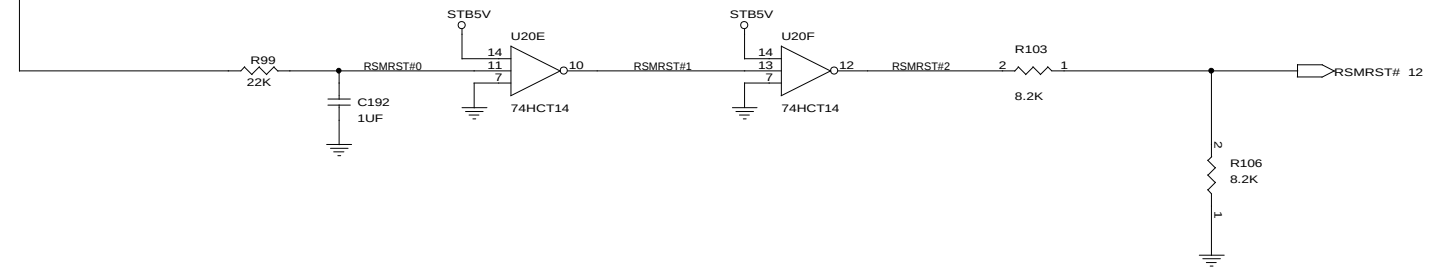


EXTERNAL BATTERY



Intel Corporation		
Title: TX DESKTOP POWER SUPPLY		
Size	Document Number	Rev 2.1
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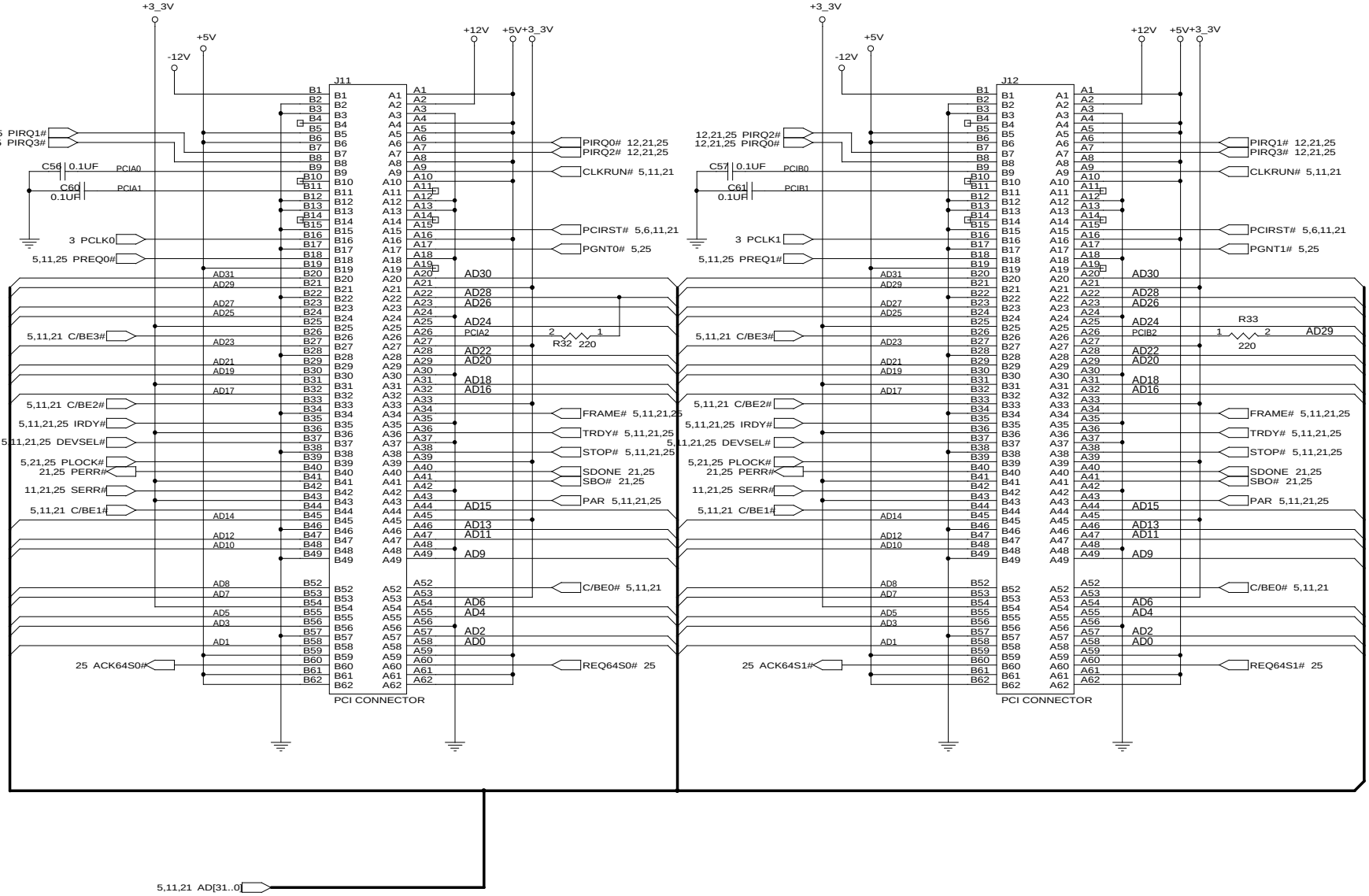
PCI SLOTS #1 & #2



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Intel Corporation		
Title: TX DESKTOP PCI SLOTS 1 & 2		
Size	Document Number	Rev 2.1
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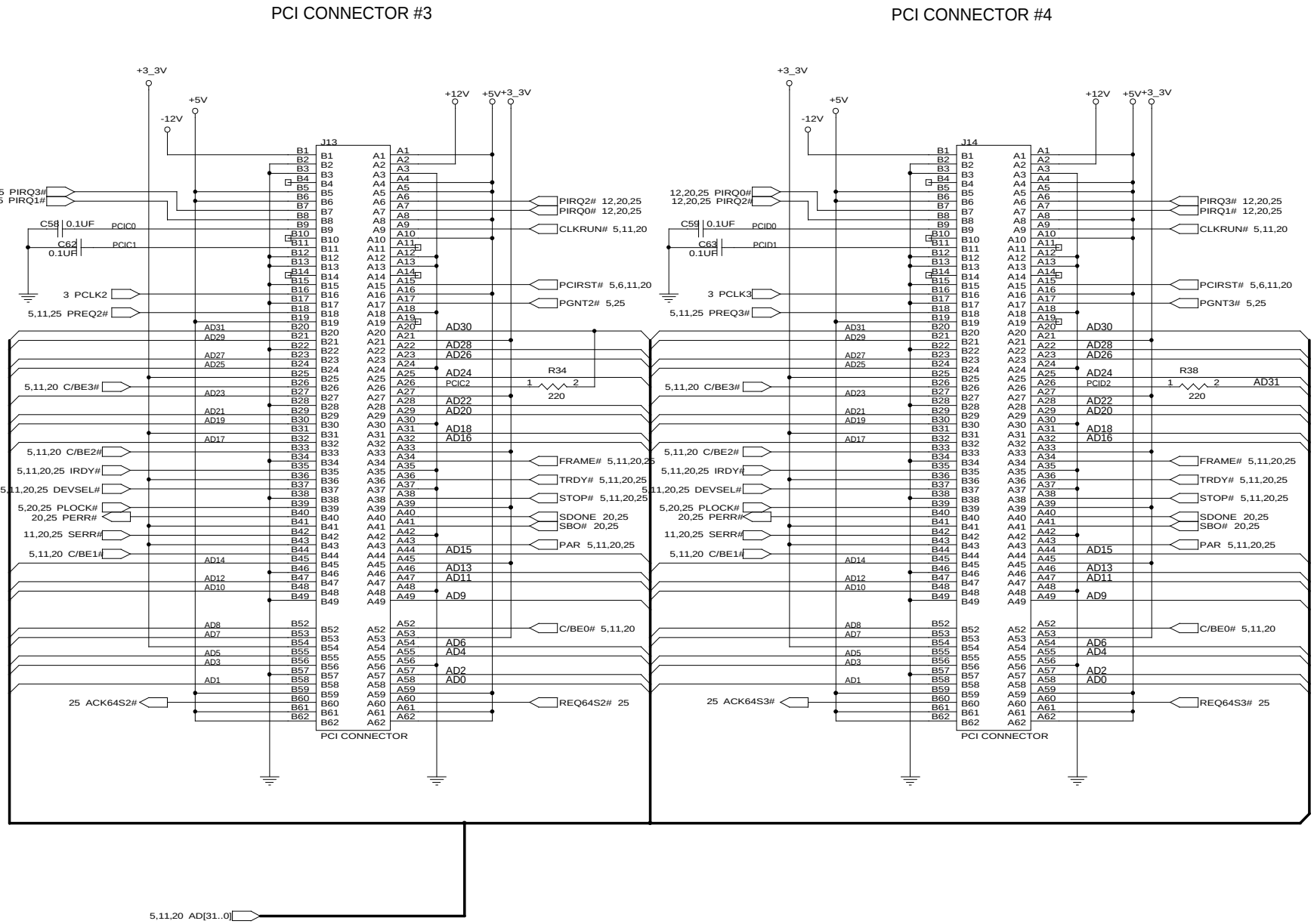
PCI SLOTS #3 & #4



Intel Corporation		
Title: TX DESKTOP PCI SLOTS 3 & 4		
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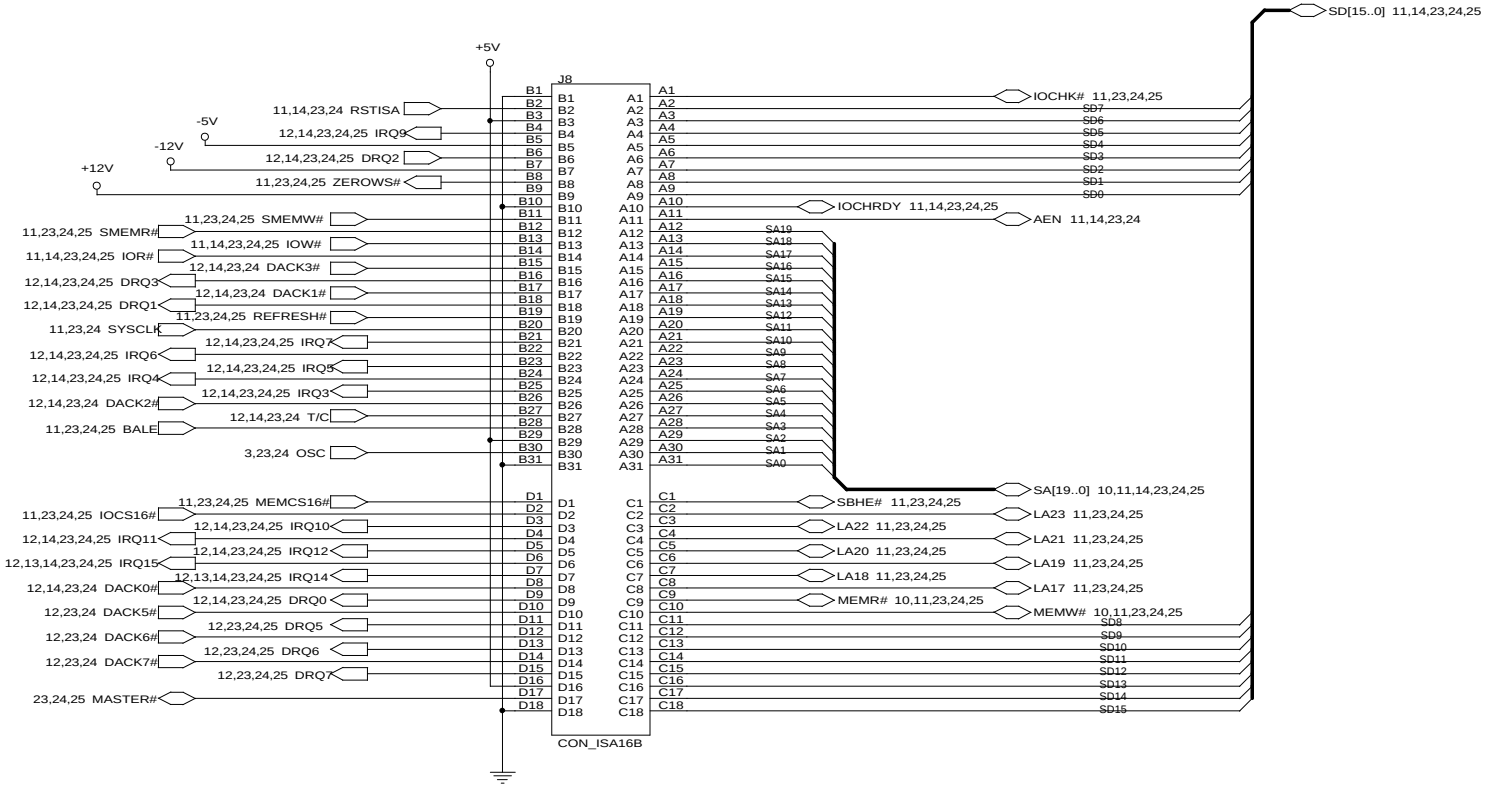
ISA
SLOT#1



Intel Corporation		
Title: TX DESKTOP ISA SLOT#1		
Size	Document Number	Rev 2.1
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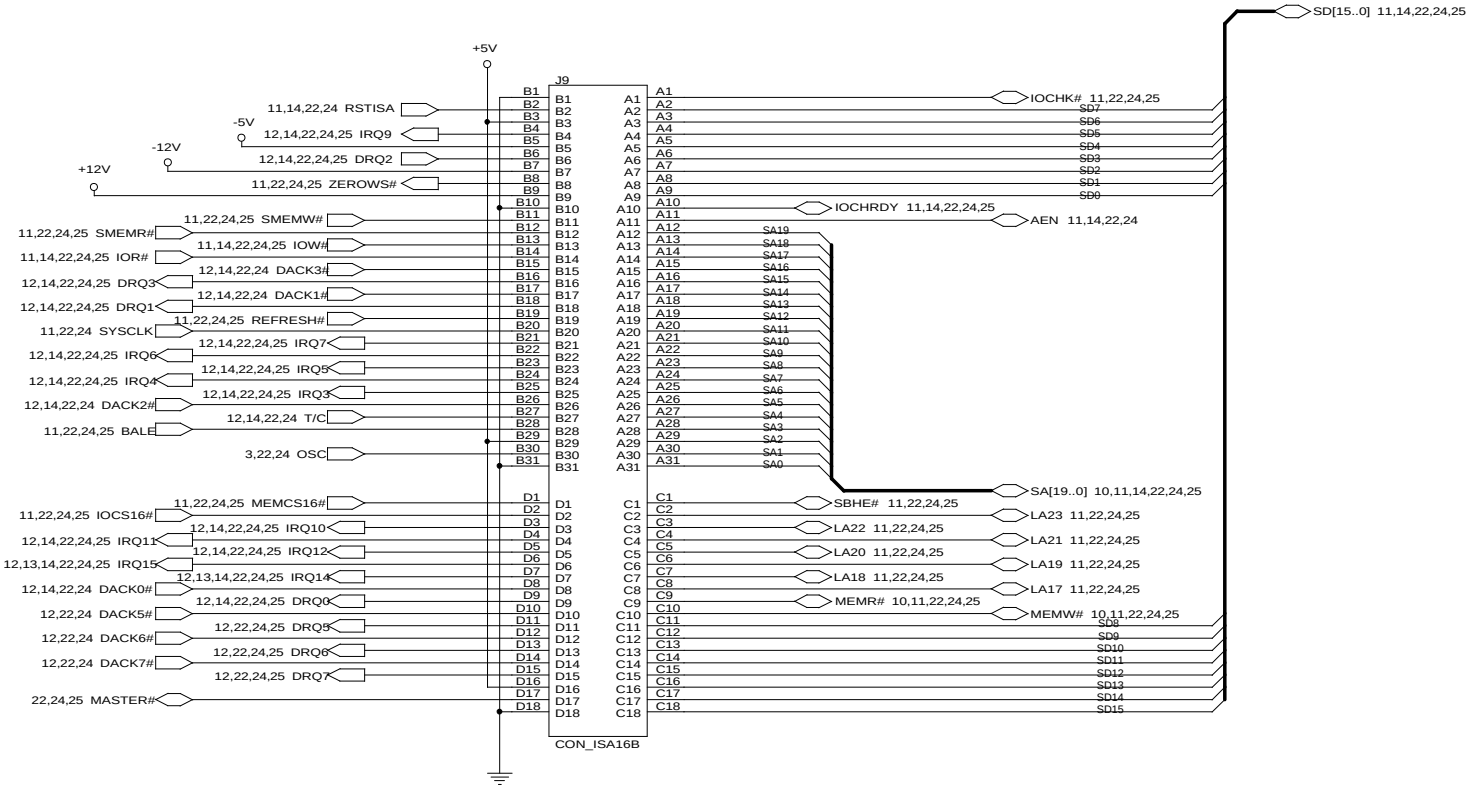
ISA
SLOT#2



Intel Corporation		
Title: TX DESKTOP ISA SLOT#2		
Size	Document Number	Rev 2.1
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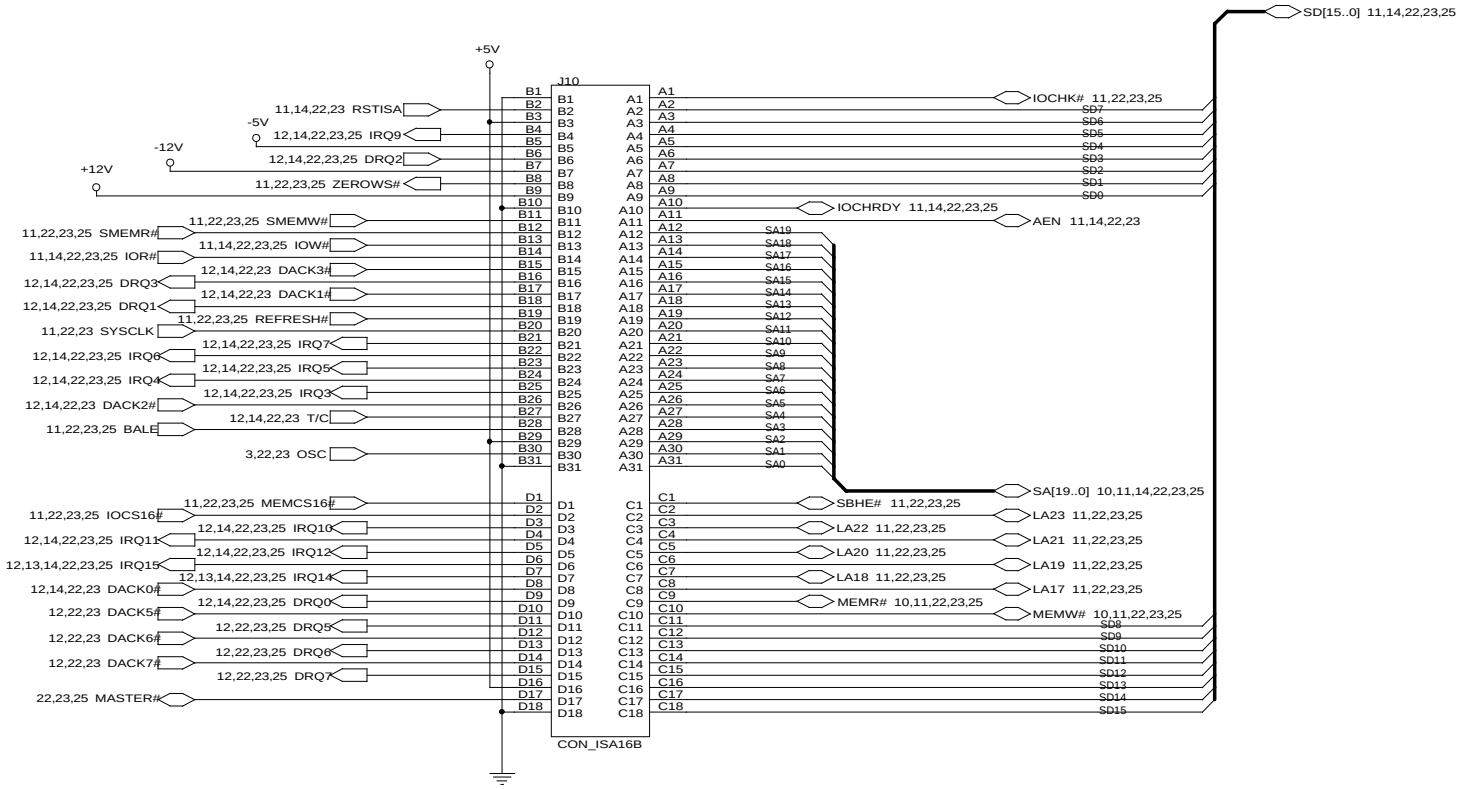
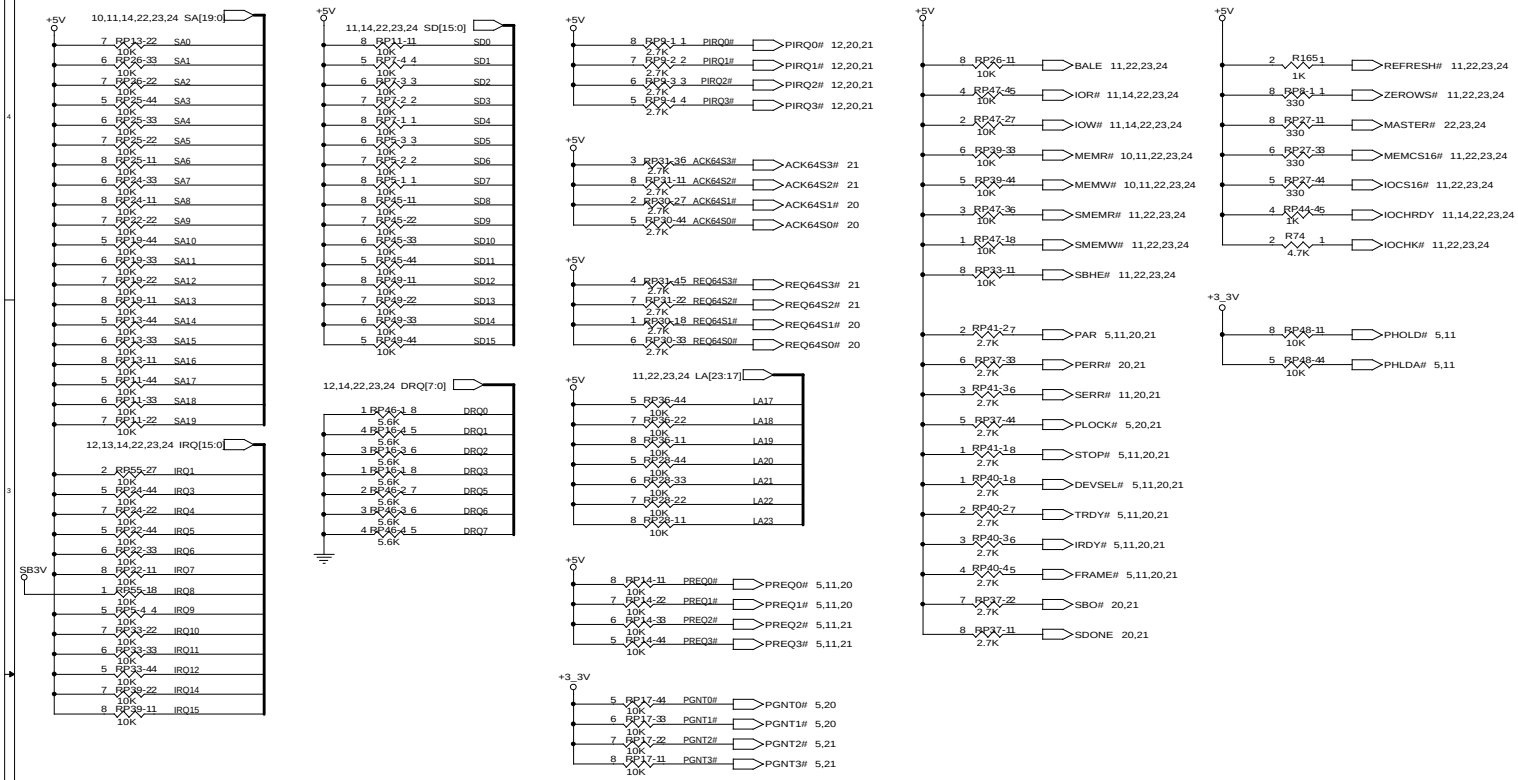
ISA
SLOT#3



This drawing contains information which has not been verified for manufacturing an end user product Intel is not responsible for the misuse of this information.

Intel Corporation		
Title: TX DESKTOP ISA SLOT#3		
Size	Document Number	Rev 2.1
Date: Thursday, December 19, 1996	Sheet 24 of 29	



Intel Corporation	
Title	TX DESKTOP PULL-UPS
Size	Document Number
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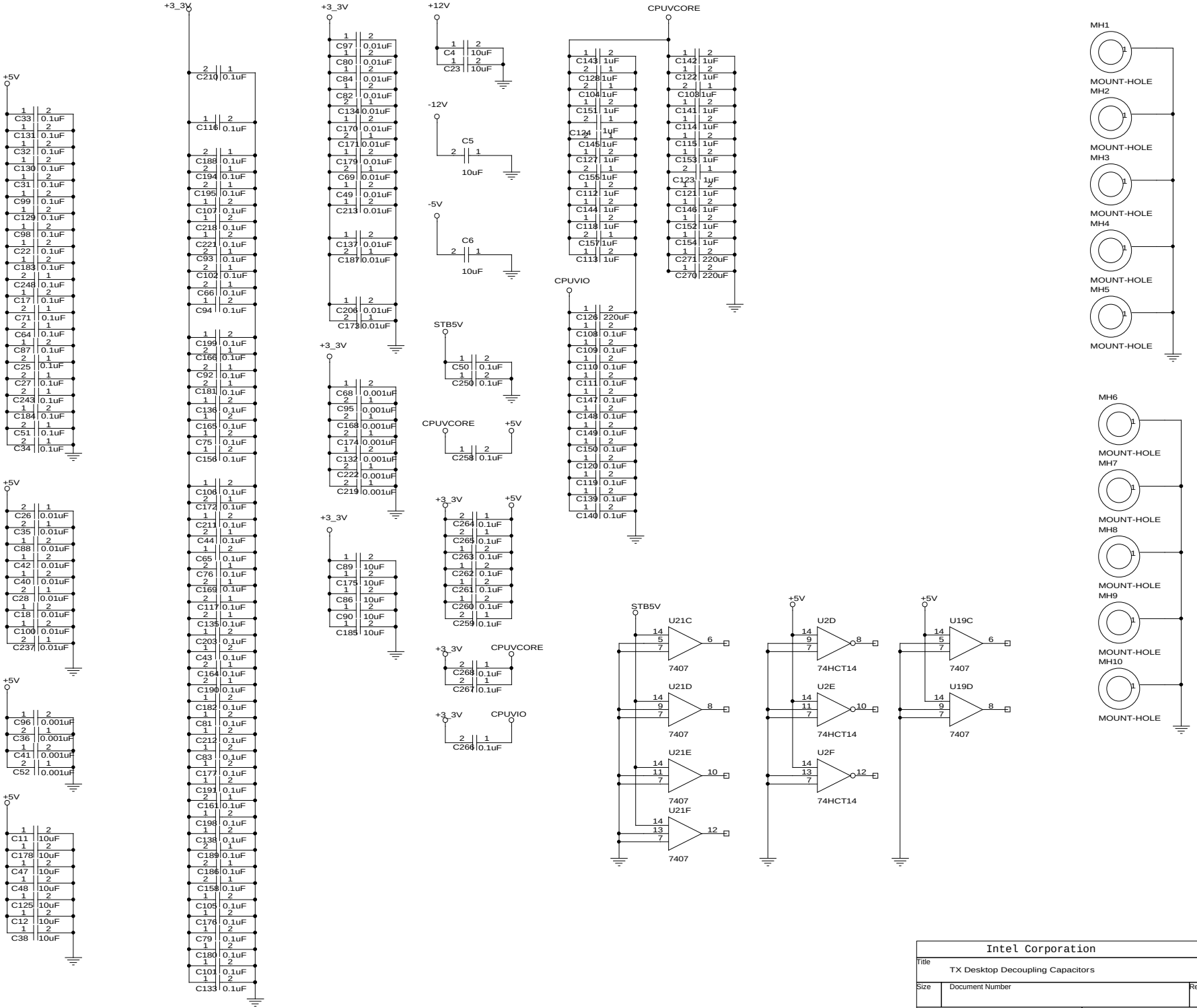
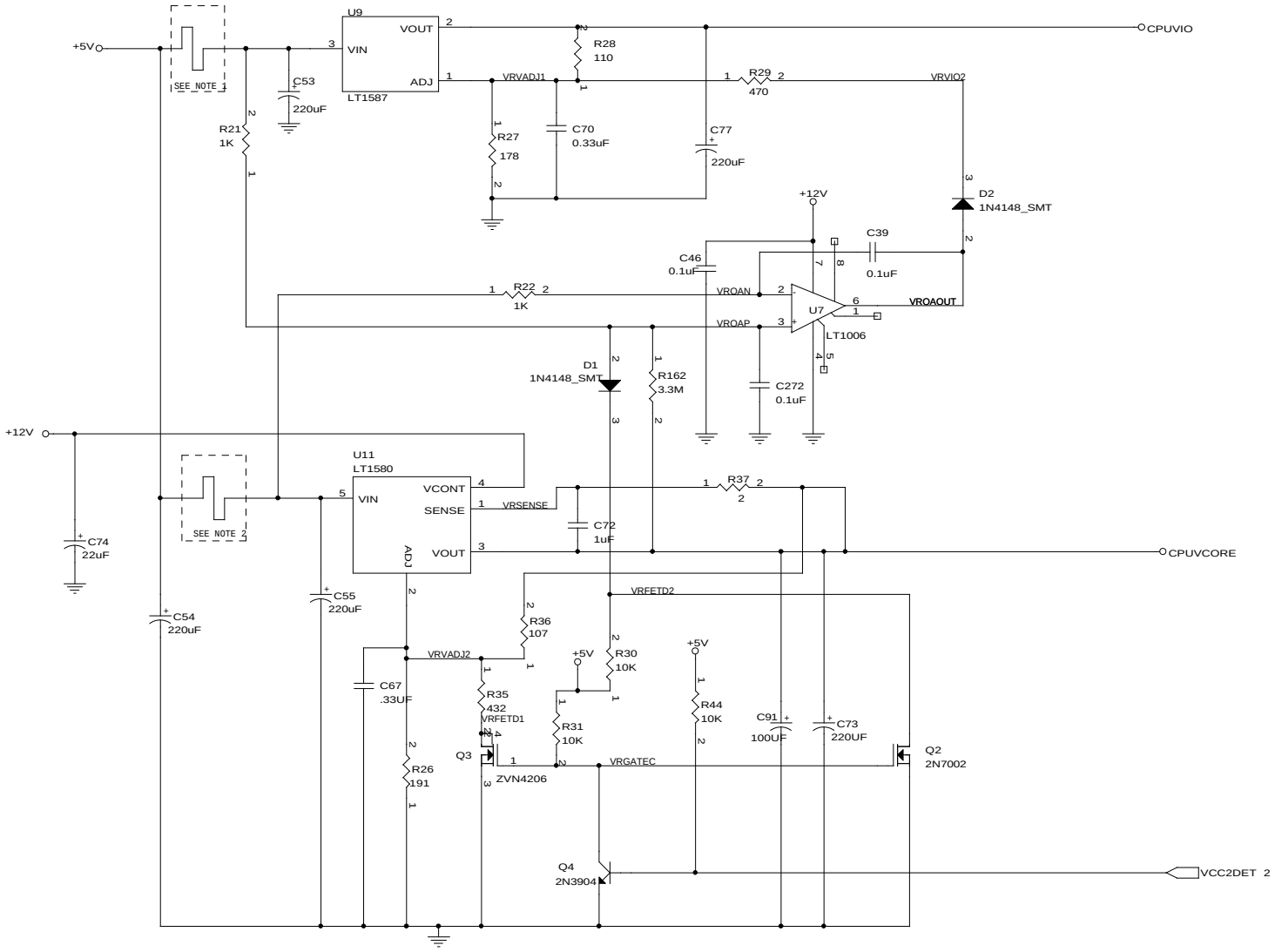
Date: Thursday, December 19, 1996	Sheet 25 of 29



Intel Corporation		
Title: TX Desktop Decoupling Capacitors		
Size	Document Number	Rev 2.1
Date: Thursday, December 19, 1996	Sheet 26 of 29	



Resistors are implemented as copper traces on inter layer:
For 1oz. copper:
Note 1: trace widths are 50 mils, 1.24" long.
Note 2: trace widths are 50 mils, 0.83" long.

Intel Corporation		
Title: TX DESKTOP VOLTAGE REGULATOR		
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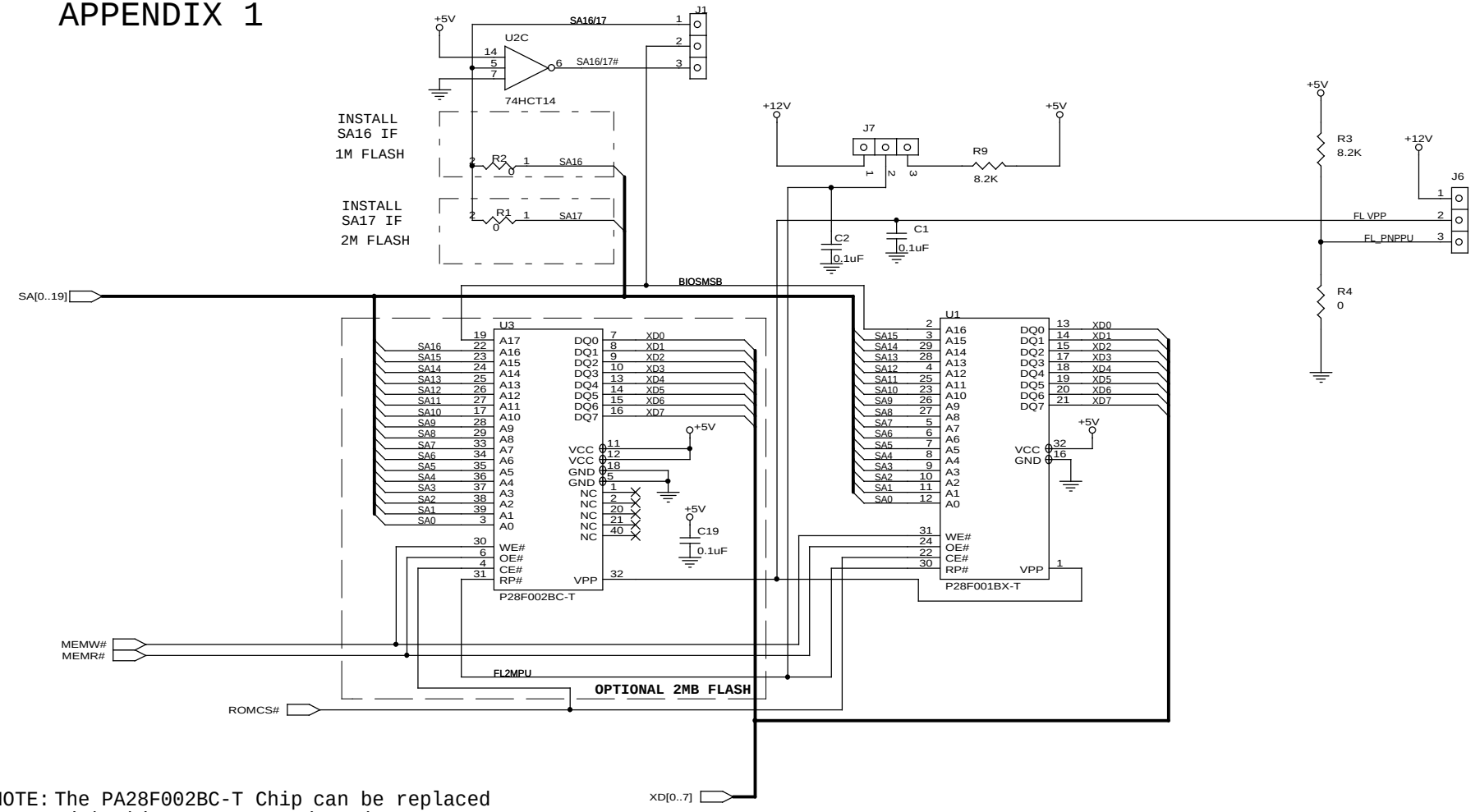
J1	
MODE	POS.
NORMAL	2-3
RECOVERY	1-2

MODE	J7	J6
Program Device	1-2	1-2
Plug -N- Play	2-3	1-2
Non-Plug-N-Play	X	2-3
Not Used	2-3	2-3

APPENDIX 1



**NOTE: The PA28F002BC-T Chip can be replaced with this P28F002BC-T (PDIP) Chip. When using the P28F002BC-T, simply replace page 10 of the TX_DESKTOP Design with this appendix page.

Intel Corporation		
Title: TX DESKTOP FLASH BIOS WITH P28F002BC-T PDIP		
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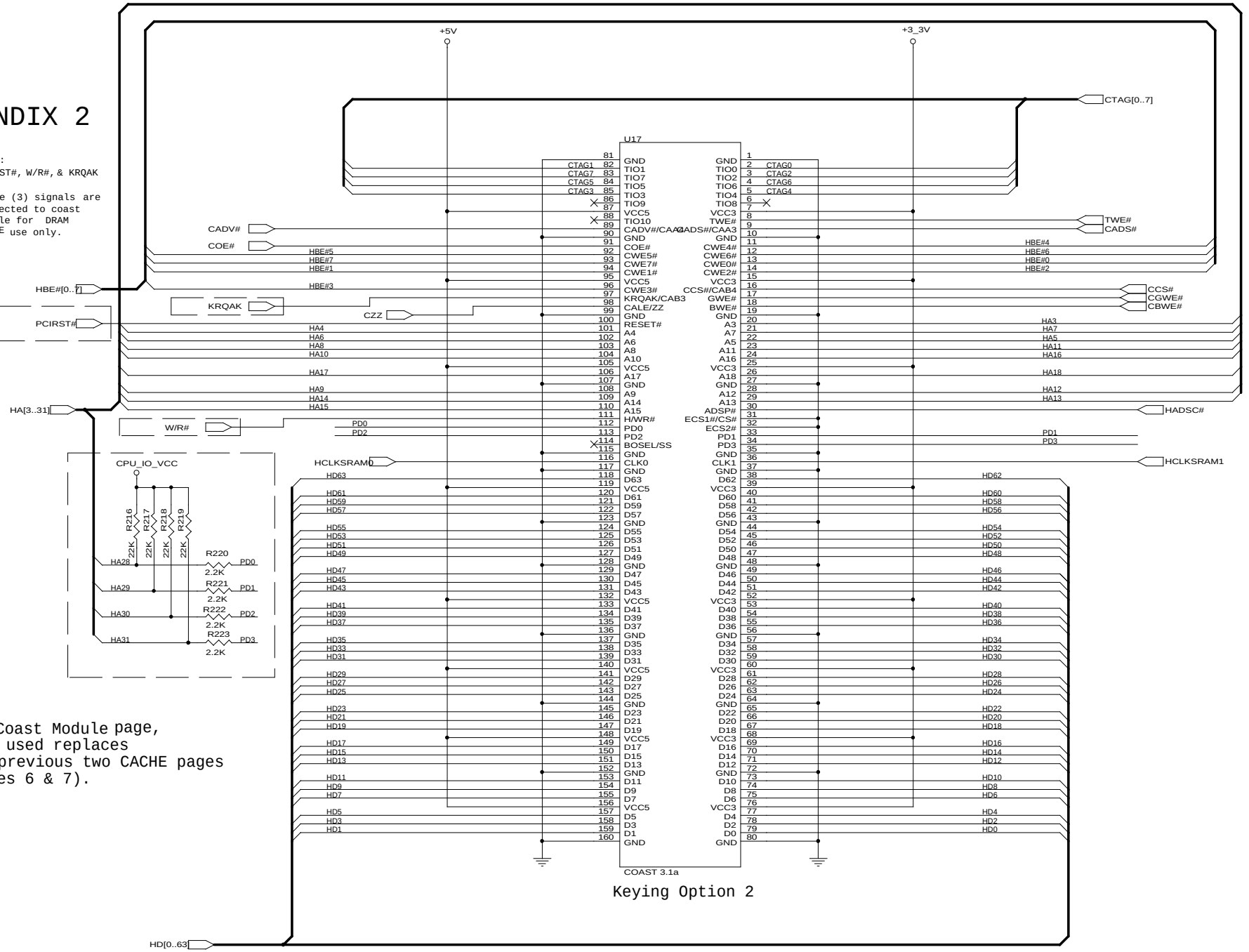
APPENDIX 2

Note:
PCIRST#, W/R#, & KRQAK

These (3) signals are connected to coast module for DRAM CACHE use only.



Keying Option 2

Note: The Coast Module page, when used replaces the previous two CACHE pages (pages 6 & 7).

Intel Corporation		
Title: TX DESKTOP COAST MODULE		
Size	Document Number	Rev 2.1
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The following are the changes from the Rev 2.0 to Rev 2.1 schematics:

1. Sheet 2: The value of the pull-up resistors on HRESET and HINIT (R53 and R55 respectively) changed from 4.7K to 330 ohms. These are timing critical, open collector outputs from the PIIX4 and need strong pull-ups.

2. Sheet 6,7: Cache topology changed from four 32Kx32 parts to two 64Kx32 parts. This reduces parts count and makes layout guidelines easier to meet.

3. Sheet 3,8,9: HCLKSRAM0 signal (R112) was removed due to change in cache topology. Clocks to DIMMs from clock synthesizer have also been moved to optimize layout. If SMBus is used to turn off the clocks, BIOS needs to be aware of the clock routing (i.e. which DIMM is connected to which clock). Signals that have moved include: HCLKDIMM0, HCLKDIMM5, HCLKDIMM6.

4. Sheet 10: PA28F002BC-T renamed to E28F002BC-T. The E prefix denotes the 40 pin TSOP part which is shown in the schematics and used on the customer reference board. (PA denotes a 44 pin PSOP package)

5. Sheet 12: An 8 pin thermal device U22 (not populated on the reference board) is added to the SMBus, located as close to the CPU as possible. This is for test purposes only.

6. Sheet 12: R83, a 1M ohm resistor in the PIIX4 RTC oscillator circuit is not required and therefore not installed.

7. Sheet 12: All unused GPIx inputs on the PIIX4 are tied high through 8.2K pull-up resistors to a power plane. GPI13 - GPI21 are tied to the 3.3v core power plane and GPI1 is tied to 3v Stand-by through 8.2k resistors. If GPI1 is left floating, this will violate ACPI compliance, preventing the GPI_STS bit (register base + 0Ch, bit 9) from functioning properly.

8. Sheet 12: PIIXTHRM is pulled to 3.3v (through resistor RP66-1) instead of SB3v. This signal is not part of the suspend well in the PIIX4.

9. Sheet 14: Open collector gate is added to the IRQ8# path to insure the voltage driven to the PIIX4 does not exceed a 3.3v level. The Super I/O device is a 5v part and could drive IRQ8# to 5v even if the pull-up on this pin is pulled to 3v Stand-by.

10. Sheet 14: Open collector driver U19B and 0 ohm resistor R123 was added to connect the PIIX4 and the Ultra I/O ring indicate lines. To implement ring indicate during STD/Soff, this part must be powered by the standby voltage.

11. Sheet 14: Capacitor C37 changed from 0 .1uF to 22pF.

12. Sheet 19: Bypass capacitor C234 changed from 1uF to .1uF.

13. Sheet 19: R145 changed from 390 ohms to 56 ohms to set SB3V correctly.

14. Sheet 19: R99 changed from 1K ohms to 22K ohms to provide adequate delay on RSMRST# at Schmitt triger (U20e) input.

The following are miscellaneous changes not reflected in the Rev 2.1 Schematics or Gerber files:

1. Sheet 8,9: Series resistors R62, R63, R66, and R67 should be 0 ohm stuffing option resistors, and MRAS[5..4] should have 10 ohm series termination resistors located as close as possible to the MTXC.

2. Sheet 12: SMBCLK and SMBDATA should be pulled up to the 3.3V core plane through 8.2K resistors. It follows that the SMBus cannot be used as a resume event during STD/Soff since it is not tied to a standby voltage. These should not be pulled up to 3VSB when used with devices being powered from the core voltage (e.g. SDRAM) due to excessive leakage when the core voltage is off. If they are pulled up to 3VSB then all the devices on the SMBus should be tied to 3VSB.

3. The PCI Boundary Scan signals on the PCI connector are: TRST#, TMS, TDI, TDO, and TCK. Pullup and pulldown resistor values for these signals should follow the recommendations listed in the PCI Specification, Rev 2.1. If boundary scan is not supported on the motherboard, then TMS (connector pin A3) and TDI (connector pin A4) should be independently bused and pulled up, each with ~ 5K ohm resistors. TRST# (connector pin A1) and TCK (connector pin B2) should be independently bused and pulled down, each with ~ 5K ohm resistors. TDO (connector pin B4) should be left open.

4. Sheet 25: Change pullups on the following ISA signals from 330 Ohms to 1K: ZEROWS#, MEMCS16#, IOCS16#.

5. (6/27/97) There is no internal pull-up or down on PDD7 or SDD7 of the PIIX4. The ATA3 specification requires a 10K ohm pull-down on DD7 in section 4.3.1. Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10K ohm pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up. It is intended that this recommendation become mandatory in the next revision of this standard.

INTEL CORPORATION

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