NEC Electronics Inc.

VR4111 (μPD30111)
64-Bit MIPS RISC Microprocessor

Product Brief

September 1997

Description

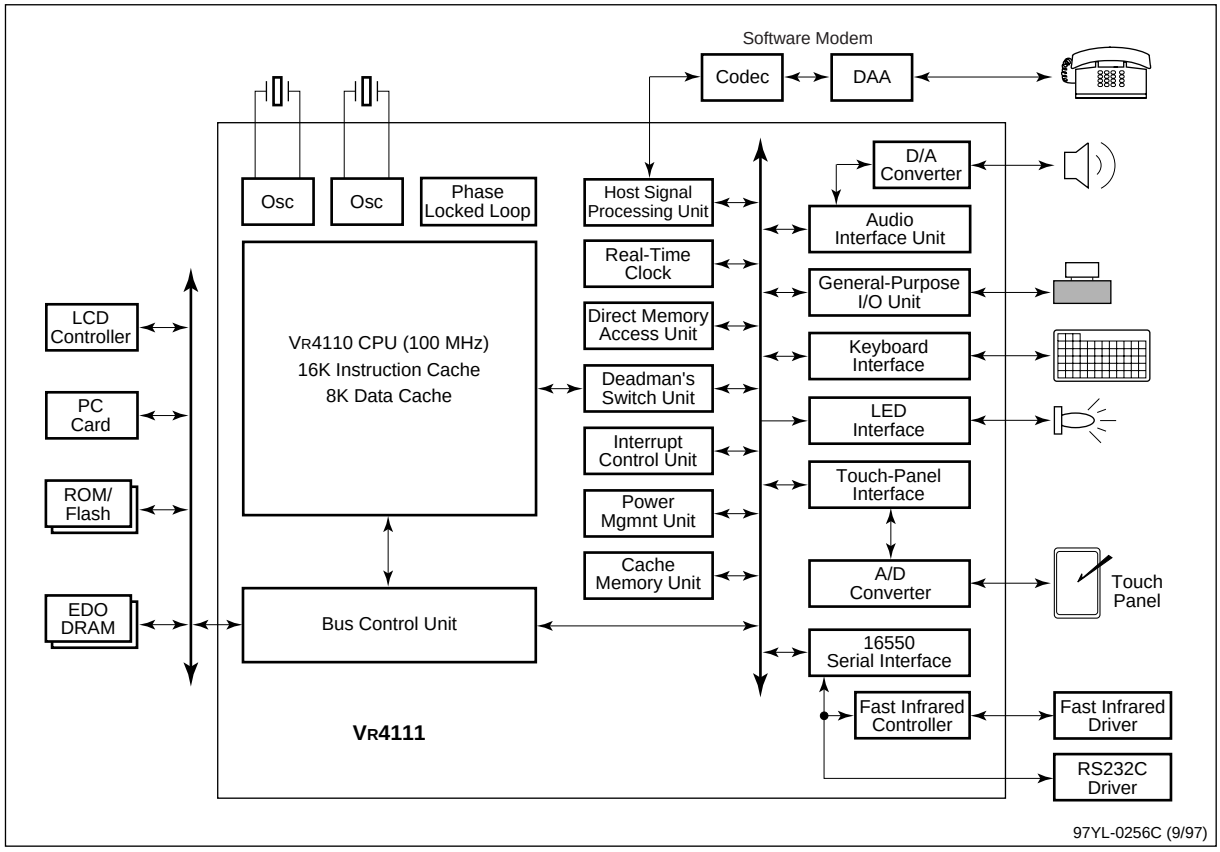
The 64-bit VR4111™(μPD30111) microprocessor is a member of NEC's VR Series™ devices created for Windows® CE-based embedded consumer applications. Designed around the popular MIPS® RISC architecture, the VR4111 offers excellent power consumption and performance in a high-integration, low-cost system on a chip.

This microprocessor is the first NEC device to use the VR4110™ CPU core, an ultra-low power consumption device based on advanced 0.25-micron technology. The VR4110 CPU has a 16K instruction cache, 8K data cache, multiply-and-accumulate (MAC) unit, memory management unit, and an optimized 100-MHz five-stage pipeline that deliver high performance in a compact, low-cost chip. Integrated peripherals include a power management unit, direct memory access unit, interrupt control unit, timers, real-time clock, serial interface, IrDA® interface, keyboard interface, touch-panel interface, LED interface, host signal processing unit (software modem), and A/D and D/A converters.

The VR4111 complies with MIPS I/II/III and MIPS16 instruction set architectures (ISAs).The MIPS16 ISA compliance enables the VR4111 to incorporate 16-bit instructions with conventional 32-bit instructions in a compact code size that reduces the memory requirement and thus system cost.

The VR4111 is an easy choice for VR4102™ customers in terms of upgrade because the VR4111 and VR4102 are fully pin compatible in the 224-pin FPBGA package. The VR4111 microprocessor's high speed, compact size, and low power consumption make it ideal for use in a battery-driven, portable handheld system.

Block Diagram



Features

- ❒ VR4110 CPU core
  - — MIPS I, II, III ISA-compliant (without FPU, LL, LLD, SC, and SCD instructions)
  - — MIPS16 ISA-compliant for compact code density
  - — Five-stage pipeline running at 100 MHz (130 Dhrystone MIPS)
  - — Single-cycle MAC instruction for DSP operations
- ❒ Memory management unit
  - — 32-bit physical addressing range of 4 GB with 40-bit virtual address space
  - — 32 double-entry TLBs supporting a 1K to 256K page size
  - — Up to 64 MB DRAM and 64 MB flash/mask ROM
- ❒ Cache memory unit
  - — 16K direct-mapped instruction cache
  - — 8K data cache
  - — Write-back cache for reducing store operations
- ❒ Bus control unit
  - — 32-bit and 16-bit addressing mode
  - — Dynamic bus sizing (subset of ISA bus)
- ❒ Power management unit
  - — 180 mW at full-speed power (typical)
  - — 30 mW in standby mode
  - — 10 mW in suspend mode
  - — 240 mW in hibernate mode
- ❒ Clock generator unit
  - — Built-in phase-locked loop for frequency multiplication
  - — External bus frequency of 16/33 MHz
  - — 32-kHz and 18-MHz resonators
- ❒ Real-time clock with four built-in timers
- ❒ Interrupt control unit with internal and external interrupts
- ❒ DMA address unit and DMA control unit with four different DMA channels
- ❒ General-purpose I/O unit with 49 general-purpose I/O pins
- ❒ Keyboard (96-key), touch-panel, and LED interface
- ❒ Serial interface unit (16550 compliant)
  - — Up to 115 kbps
  - — Separate serial debugging port
- ❒ Fast infrared unit operating at 0.5 to 4 Mbps (IrDA 1.1 standard communication)
- ❒ Audio interface unit and 10-bit D/A converter with audio output and microphone input sampling
- ❒ Host signal processing unit (software modem)
- ❒ AC/DC specifications
  - — 100-MHz maximum frequency
  - — 2.5-V and 3.3-V operation
  - — 180 mW typical power consumption
- ❒ 224-pin FPBGA package

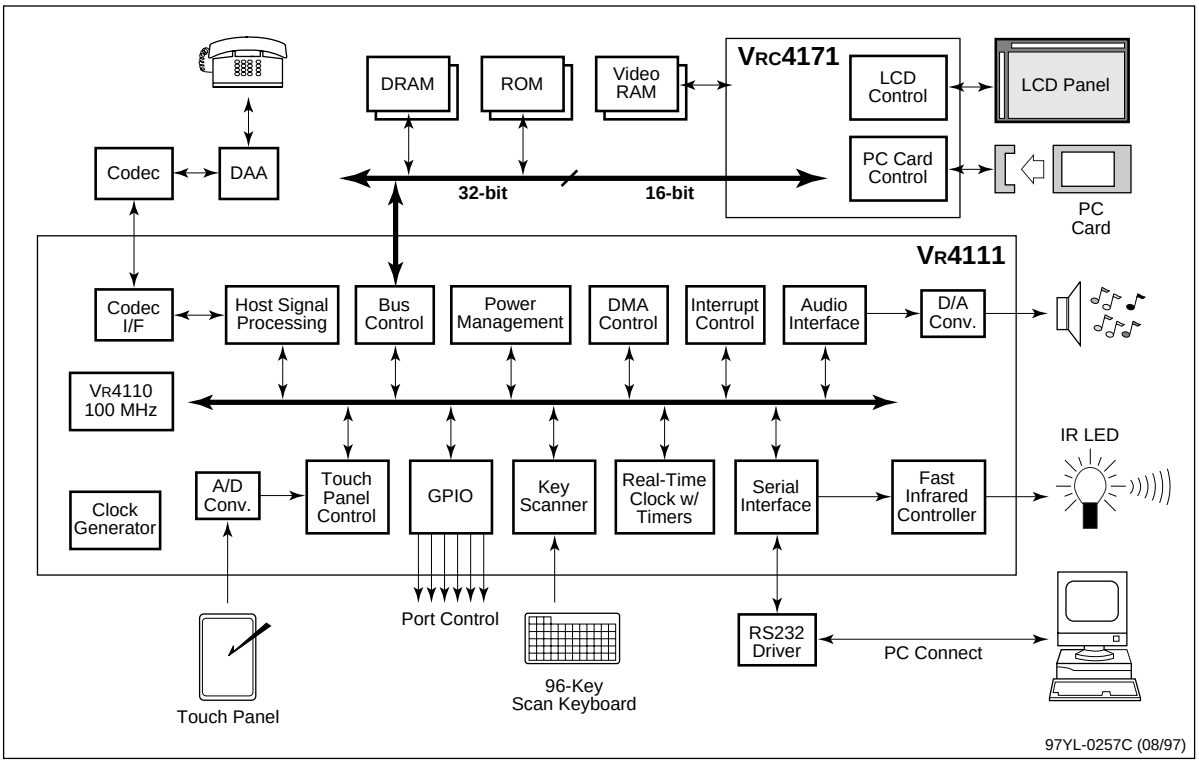
VR4102 and VR4111 Comparison

	VR4102	VR4111
CPU	VR4100	VR4110
Pipeline clock	66 MHz	100 MHz
Performance	80 Dhrystone MIPS	130 Dhrystone MIPS
Cache size	Instruction: 4K Data: 1K	Instruction: 16K Data: 8K
Instruction set	MIPS I, II, III	MIPS I, II, III MIPS16
Operating voltage	3.3 volts	2.5 volts (core), 3.3 volts
Integrated peripherals	Same	Same
Memory interface	32 M DRAM 32 M ROM	64 M DRAM 64 M ROM
Power consumption	250 mW	180 mW
Package	216-pin LQFP 224-pin FPBGA	224-pin FPBGA
Process technology	0.35 micron	0.25 micron

Ordering Information

Part Number	Package	Operating Frequency
μPD30111S1-100-3C	224-pin FPBGA	100 MHz
μPD30111S1-80-3C	224-pin FPBGA	80 MHz

Handheld PC Application Example



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