agere systems

Infrastructure Solutions

Function	Product	What It Is	What It Does	Key Features/Benefits
Amplifier	TLMA0110G	10 Gbits/s limiting amplifier	Used in optical receivers to provide additional amplification of the Rx signal from the TTIA.	–5.2 V power supply; 8 mV input sensitivity; adjustable threshold control; outputs limit to 550 mVp-p; small signal gain 32 dB; ceramic or low-cost plastic package.
Amplifier	TTIA0110G	10 Gbits/s limiting amplifier	Used in optical transceivers and receivers; takes current from a photodetecter (either PIN or APD) and generates an amplified voltage output. TTIA is available in die-form only.	–5.2 V power supply; 1 k Ω transimpedence; ac or dc coupled outputs 50 Ω; input overload 3.0 mAp-p; dc output offset control; up to 12.5 Gbits/s bandwidth.
ASICs	Application Specific Integrated Circuits/System on Chip	Custom solutions for computing communications and consumer applications	Speeds time-to-market with broad IP portfolio for customer IC solutions.	Lower cost per port, higher port densities, faster time-to-market.
ATM Access Processor	SAR-500	Complete ATM adaptation solution	Complete ATM adaptation solution. Implements any combination of 512 AAL2 CIDs/AAL5 VCs. Implements adaptation conversion of 512 AAL5/AAL2 flows into 512 AAL2/AAL5 flows.	Highly integrated ATM adaptation system on a chip + full-featured software + world-class support = fast time-to-market.
ATM Access Processor	SAR-1K	Complete ATM adaptation solution	Complete ATM adaptation solution. Implements any combination of 1024 AAL2 CIDs/AAL5 VCs. Implements adaptation conversion of 1024 AAL5/AAL2 flows into 1024 AAL2/AAL5 flows.	Highly integrated ATM adaptation system on a chip + full-featured software + world-class support = fast time-to-market.
ATM Access Processor	SAR-2K	High capacity device for ATM adaptation layer (AAL2 and AAL5)	Provides AAL2/5 SAR for 2K CIDs/VCs. Supports I.363.2 service, I.366.1 SSSAR service, I.366.1 SSTED service and I.363.5 CPCS service. Provides adaptation conversion of AAL5/AAL2 flows into AAL2/AAL5 flows (1300 flows). Maximum bandwidth = 155 Mbits/s.	Full feature ATM adaptation layer SoC, full-featured software and no external memory required provide low-cost system solution.

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ATM Access Processor	TAAD08JU2	Highly integrated device for ATM access (Layer 1 and Layer 2)	Provides QOS for a variety of ATM traffic types (on-chip APC). Support CBR, UBR, rt_VBR, nrt_VBR, and ABR. Provides AAL2/5 SAR for 2K CIDs/VC, integrated TC/IMA (4 Groups max) and framer for 8 T1/E1/J1s (PHY). Supports I.363.2 service, I.366.1 SSSAR service, I.366.1 SSTED service and I.363.5 CPCS service. Provides adaptation conversion of AAL5/AAL2 flows into AAL2/AAL5 flows (1300 flows). Maximum bandwidth = 155 Mbits/s through the SAR and APC. PHY bandwidth = 16 Mbits/s.	Unequaled HW/SW integration/density, no external memory required and price performance for target application provide low-cost system solution and fast time to market. Large number of flexible/modular interface ports provides multiple data paths for platform design.
ATM Access Processor	TAAD Lite	Low-speed ATM access solution	T1/E1/J1 framing (8 links). ATM transmission convergence. Inverse multiplexing for ATM (T1/E1/J1). ATM switching and control. ATM adaptation layer (AAL2 & AAL5), AAL segmentation and reassembly (SAR).	High functional integration targeted to the wireless 3G radio access network, multiservice access platforms and voice/multimedia gateways. Seamless, end-to-end multiservice hardware and applications software solutions. Highly flexible architectures. Flexible interfaces allows multiple/variable transport technologies to accommodate market requirements.
ATM Access Processor	TAAD UltraLite	Low-speed ATM access solution	T1/E1/J1 framing (8 links). ATM transmission convergence. Inverse multiplexing for ATM (T1/E1/J1). ATM switching and control. ATM adaptation layer (AAL2 & AAL5), AAL segmentation and reassembly (SAR).	High functional integration targeted to the wireless 3G radio access network, multiservice access platforms and voice/multimedia gateways. Seamless, end-to-end multiservice hardware and applications software solutions. Highly flexible architectures. Flexible interfaces allows multiple/variable transport technologies to accommodate market requirements.
ATM Interconnect	*CelXpres*™ T8207	Single-chip ATM switch and backplane I/F interconnecting UTOPIA Level 1/2 bus to a 1.7 Gbits/s ATM parallel cell bus backplane (OC-12 rate)	Performs cell routing between up to 32 line cards each supporting 32 MPHYs with 64 queues.	8-bit UTOPIA L1 and L2 I/F. 32 MPHY support. 64 queues available. VPI/VCI look-up and translation. 32-bit cell backplane with 66 MHz rate. Up to 32 devices supported on single bus.
ATM Interconnect	*CelXpres* T8208	Single-chip ATM switch and backplane I/F interconnecting UTOPIA Level 1/2 bus to a 1.7 Gbits/s ATM parallel cell bus backplane (OC-12 rate)	Performs cell routing between up to 32 line cards each supporting 64 MPHYs with 128 queues.	8/16-bit UTOPIA L1 and L2 I/F. 64 MPHY support. 128 queues available. VPI/VCI look-up and translation. 32-bit cell backplane with 66 MHz rate. Up to 32 devices supported on single bus.
Backplane Bridge	UB2G5AG	8 SerDes link aggregator to POSPHYL3 or CSIX L1 interface. Provides a low-cost aggregation and serial backplane interconnect solution.	Aggregates traffic from up to 8 2.5G SerDes to a POSPHYL3 or CSIX L1 compliant device. Seamlessly connects the APPxxx network processors to other universal bridge devices.	8/16/32-bit POSPHYL3 I/F. 32-bit CSIX level 1 fabric I/F. Programmable cell size for 64, 72, 80-byte user payloads to PI40. 8 pseudo SONET SerDes links operating at 1.25 Gbits/s or 2.5 Gbits/s. Packet extraction port. Cell insertion and capture functions. 8-bit asynchronous µP I/F.
Backplane Bridge	UB2G5LC	UTOPIA L2 protocol conversion engine to SONET SerDes. 2x OC-12 capacity backplane driver.	Interconnects UTOPIA L2 compliant devices to the PI40 fabric through 2.5G SerDes links. Support up to 256 MPHYs. Interconnects ADSL modems, DSPs, PHY devices into the PI40 fabric.	Four 8-bit UTOPIA L2 I/Fs (256 MPHYs). Two 16-bit UTOPIA L2 I/Fs (128 MPHYs). Programmable cell size for 64, 72, 80-byte user payloads to PI40. 4 pseudo SONET SerDes links operating at 1.25 Gbits/s or 2.5 Gbits/s. Cell insertion and capture functions. 8-bit asynchronous µP I/F.

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Backplane Bridge	UB2G5NP	POSPHYL3 and CSIX L1 protocol conversion engine to SONET SerDes. OC-48 (2.5G) capacity backplane driver.	Interconnects POSPHYL3 or CSIX L1 compliant devices to the PI40 fabric through 2.5G SerDes links. Seamlessly connects the APPxxx network processors to the PI40 fabric.	8/16/32-bit POSPHYL3 I/F. 32-bit CSIX level 1 fabric I/F. Programmable cell size for 64, 72, 80-byte user payloads to PI40. 8 pseudo SONET SerDes links operating at 1.25 Gbits/s or 2.5 Gbits/s. Packet extraction port. Cell insertion and capture functions. 8-bit asynchronous µP I/F.
Backplane Bridge	UBAPP500	POSPHYL3 protocol conversion engine to SONET SerDes. The UBAPP500 is IP code that can be loaded into the Lattice ORSO82G5 FPSC device.	Interconnects POSPHYL3 compliant devices to the PI40 fabric through 2.5G SerDes links. Seamlessly connects the APPxxx network processors to the PI40 fabric.	8/16/32-bit POSPHYL3 I/F. Support 256 MPHYs. Supports 72-byte cell size user payloads to PI40. 8 pseudo SONET SerDes links operating at 2.5 Gbits/s. Packet extraction port. 8-bit asynchronous µP I/F.
Backplane Bridge	UBAPC	APC conversion engine to SONET SerDes. The UBAPC is IP code that can be loaded into the Lattice ORSO82G5 FPSC device.	Seamlessly connects 2 APC devices to the PI40 fabric through 2.5G SerDes links.	Two 8-bit APC ATM I/F. Supports 72-byte cell size user payloads to PI40. 4 pseudo SONET SerDes links operating at 2.5 Gbits/s. 8-bit asynchronous µP I/F.
Backplane Bridge	UBCSIX	CSIX L1 protocol conversion engine to SONET SerDes. The UBCSIX is IP code that can be loaded into the Lattice ORSO82G5 FPSC device.	Interconnects CSIX L1 compliant devices to the PI40 fabric through 2.5G SerDes links. Seamlessly connects the *Motorola*® C5E network processors to the PI40 fabric.	32-bit CSIX L1 fabric I/F. Supports 1024 ports, 4 traffic classes. Supports 72-byte cell size user payloads to PI40. 4 pseudo SONET SerDes links operating at 2.5 Gbits/s. 8-bit asynchronous µP I/F.
CDR/Clock Synthesize/ MUX/DeMUX	*FlexPhy*™ (TSCV0110G)	CMOS 10 Gbits/s MUX/DeMUX transceiver	For SONET/SDH multiplexing at OC-192/STM-64 with FEC overhead capability.	Low-power, excellent jitter performance, integrated limiting amp with 10 mV input sensitivity, plastic package.
CDR/DeMUX	TRCV0110G	SiGe 10 Gbits/s DeMUX	For SONET/SDH demultiplexing at OC-192/STM-64 with limiting amp (7.5 mV input sensitivity).	10 Gbits/s data input, 16 x 622 MHz data output, integrated limiting amp with 7.5 mV input sensitivity, in both ceramic and plastic package.
CDR/DeMUX	TRCV0110G2	SiGe 10 Gbits/s deMUX	For SONET/SDH demultiplexing at OC-192/STM-64 with limiting amp (10 mV input sensitivity).	10 Gbits/s data input, 16 x 622 MHz data output, integrated limiting amp with 10 mV input sensitivity, in both ceramic and plastic package.
CDR/DeMUX	TRCV0111G	SiGe 10 Gbits/s deMUX	For SONET/SDH demultiplexing at OC-192/STM-64 with limiting amp (7.5 mV input sensitivity) 22 mV LOS threshold.	10 Gbits/s data input, 16 x 622 MHz data output, integrated limiting amp with 7.5 mV input sensitivity, 22 mV LOS threshold in both ceramic and plastic package.
CDR/DeMUX	TRCV0111G2	SiGe 10 Gbits/s deMUX	For SONET/SDH demultiplexing at OC-192/STM-64 with limiting amp (7.5 mV input sensitivity) 7 mV LOS threshold.	10 Gbits/s data input, 16 x 622 MHz data output, integrated limiting amp with 7.5 mV input sensitivity, 7 mV LOS threshold in both ceramic and plastic package.
CDR/DeMUX	TRCV0112G	SiGe 12.5 Gbits/s deMUX	For SONET/SDH demultiplexing at OC-192/STM-64 with limiting amp (10 mV input sensitivity).	12 Gbits/s data input, 16 x 622 MHz data output, integrated limiting amp with 10 mV input sensitivity, in both ceramic and plastic package.
Clock Driver	LCK4950	Low-voltage PLL clock driver	A PLL-based clock driver intended for high-performance clock tree designs.	Fully integrated PLL; oscillator or crystal reference input; output frequency up to 180 MHz; pin compatible with MPC950 types; low jitter, 70 ps typical cycle-to-cycle; low output-to-output skew of 150 ps typical; compatible with *PowerPC*™, *Intel*® and high-performance RISC microprocessors; 3.3 V system compatibility; 7 x 7 mm, 32-lead TQFP.

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Clock Driver	LCK4953	Low-voltage PLL clock driver	A PLL-based clock driver targeted at high-end computer workstations and network servers.	Output frequencies to 130 MHz in PLL mode; pin compatible with MPC953 types; low jitter, 50 ps cycle-to-cycle; low output-to-output skew of 75 ps; nine outputs with high impedance disable; zero delay performance; 3.3 V system compatibility; no external loop filter components needed; 32-lead TQFP.
Clock Driver	LCK4972	Low-voltage PLL clock driver	A 3.3 V and 2.5 V PLL-based clock driver for high-performance RISC or CISC processor based system.	Fully integrated PLL; output frequency up to 240 MHz; selectable 1 crystal input or 2 single ended TTI inputs; pin compatible with MPC972 types; compatible with *PowerPC* and *Pentium*® microprocessors; 52-pin LQFP; 3.3 V & 2.5 V power supply; 100 ps typical cycle-to-cycle jitter; low output-to-output skew of 250 ps.
Clock Driver	LCK4973	PLL clock driver	A 3.3 V and 2.5 V PLL-based clock driver for high-performance RISC or CISC processor based system.	Fully integrated PLL; output frequency up to 240 MHz; selectable 1 differential PECL or two single ended TTL inputs; pin compatible with MPC973 types compatible with *PowerPC* and *Pentium* microprocessors; 52-pin LQFP; 3.3 V and 2.5 V power supply; 100 ps typical cycle-to-cycle jitter; low output-to-output skew of 250 ps.
Clock Driver	LCK4973V	PLL clock driver	A 3.3 V and 2.5 V PLL-based clock driver for high-performance RISC or CISC processor based system.	Fully integrated PLL; 2.5 – 200 MHz output frequency; selectable 1 differential PECL or 2 single ended TTL inputs; pin compatible with CY7B9973 V; PLL lock indicator; 52-pin TQFP; 3.3 V power supply; 150 ps typical cycle-to-cycle jitter; low output-to-output skew of 250 ps.
Clock Driver	LCK4993KB/YH	PLL clock driver	A low-voltage PLL clock driver offering user-selectable control over system clock functions.	12/100 MHz output operation; matched pair output skew < 200 ps; zero input-to-output delay, 18 LVTTL 50% duty-cycle outputs capable of driving 50 Ω terminated lines; 3.3/2.5 V LVTTL/LV differential (LVPECL), fault tolerant and hot insertable reference inputs; available in 100-pin TQFP or 100-lead FSGBA packages.
Clock Driver	LCK4994KB/YH	PLL clock driver	A low-voltage PLL clock driver offering user-selectable control over system clock functions.	24/200 MHz output operation; matched pair output skew < 200 ps; zero input-to-output delay, 18 LVTTL 50% duty-cycle outputs capable of driving 50 Ω terminated lines; 3.3/2.5 V LVTTL/LV differential (LVPECL), fault tolerant and hot insertable reference inputs; available in 100-pin TQFP or 100-lead FSGBA packages.
Clock Synthesizer	LCK4801	Low-voltage PLL clock driver	A low-voltage, 3.3 V HSTL differential clock synthesizer.	Two fully integrated clock inputs; fully integrated PLL; HSTL outputs; HSTL and LVPECL reference clocks; 32-pin TQFP package; pin compatible with *Motorola* MPC998 types; operating frequency: 336 MHz to 1 GHz.
Clock Synthesizer	TSYN01622	Clock synthesis device	Synthesizes many different clock outputs as needed by downstream devices from a single clock input source; does not provide input clock protection switching.	Same features as TSWC01622, but no protection switch; meets OC-48 jitter specs; can apply to OC-192 systems with extra clock clean-up circuit; supports multiple input clock frequencies; provides a wide range of SONET/SDH output clock frequencies; multiple output clock levels, CMOS, LVPECL, LVDS; five frequency programmable outputs.

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Clock Synthesizer	TSYN03622	Clock synthesis device	Synthesizes many different clock outputs as needed by downstream devices from a single clock input source; does not provide input clock protection switching.	Same features as TSYN01622, but only meets OC-3/OC-12 jitter specs; meets OC-12 jitter specs; supports multiple input clock frequencies; provides a wide range of SONET/SDH output clock frequencies; multiple output clock levels, CMOS, LVPECL, LVDS; five frequency programmable outputs; targeted to work with Ultramapper and TSI's.
Clock Synthesizer & Protection Switch	TSWC01622	Full-featured clock synthesis and protection switch	Manages system timing on a line card or system board; provides hitless switching from master to secondary system clock; synthesizes many different clock outputs as needed by downstream devices on the line card or system board.	Meets OC-48 jitter specs; can apply to OC-192 systems with extra clock clean-up circuit; supports multiple input clock frequencies; provides a wide range of SONET/SDH output clock frequencies; hitless switch protection compliant with MTIE; multiple output clock levels, CMOS, LVPECL, LVDS; five frequency programmable outputs.
Clock Synthesizer & Protection Switch	TSWC02622	Clock synthesis and protection switch for OC-48 and OC-192	Same as TSWC01622 but with reduced number of clock outputs; manages system timing on a line card or system board; provides hitless switching from master to secondary system clock; synthesizes many different clock outputs as needed by downstream devices on the line card or system board.	Same features as TSWC01622 but only has 155 MHz, 622 MHz, and 8 KHz synch clock outputs; meets OC-48 jitter specs; can apply to OC-192 systems with extra clock clean-up circuit; supports multiple input clock frequencies; hitless switch protection compliant with MTIE; multiple output clock levels - LVPECL, LVDS.
Clock Synthesizer & Protection Switch	TSWC03622	Low cost clock synthesis and protection switch	Same as full-featured TSWC01622 but with relaxed output jitter specs; manages system timing on a line card or system board; provides hitless switching from master to secondary system clock; synthesizes many different clock outputs as needed by downstream devices on the line card or system board.	Same features as TSWC01622 but only meets OC-3/OC-12 jitter specs; meets OC-12 jitter specs; supports multiple input clock frequencies; provides a wide range of SONET/SDH output clock frequencies; hitless switch protection compliant with MTIE; multiple output clock levels, CMOS, LVPECL, LVDS; five frequency programmable outputs; targeted to work with Ultramapper and TSI's.
Clock Synthesizer/ MUX	TTRN0110G	SiGe 10 Gbits/s MUX	For SONET/SDH multiplexing at OC-192/STM-64 with FEC overhead capability.	16 x 622 MHz data input, 10 Gbits/s output, low jitter generation, in both ceramic and plastic package.
Clock Synthesizer/ MUX	TTRN0112G	SiGe 12 Gbits/s MUX	For SONET/SDH multiplexing at OC-192/STM-64 with FEC/Super FEC overhead capability.	16 x 622 MHz data input, 12 Gbits/s output, low jitter generation, in both ceramic and plastic package.
Clocking Solution - Fanout Buffer	LCK4310	Fanout buffer	A low-voltage, low skew 2:8 differential emitter-coupled logic (ECL) fanout buffer designed with clock distribution in mind.	100 ps maximum part-to-part skew; 40 ps maximum output-to-output skew; PECL mode operating range is VCC=2.4 V to 3.8 V with VEE = 0V; operating frequency: 1 MHz to 1250 MHz; Internal input pull down resistors; pin compatible with *ON Semiconductor*® MC100LVE310; 28-pin PLCC package.
Cross Connect	TDCS4810G	10G STS cross connect	10G aggregate bandwidth nonblocking STS-1/STM-1 granularity switch with 48 channels.	Nonblocking; TDM circuit grooming cross connect; migration path from TADM to standalone/ cascadable 40G TDM switch; enables higher bandwidth and ADM ring support at OC192 and greater. Software drivers available for reducing design time.

Function	Product	What It Is	What It Does	Key Features/Benefits
Cross Connect	TDCS6440G	40G cross connect	40G aggregate bandwidth non-blocking STS-1/STM-1 granularity switch.	Nonblocking; TDM Circuit grooming cross connect; Migration path from TADM to standalone/ cascadable 40G TDM switch; Enables higher bandwidth and ADM ring support at OC192 and greater. Software drivers available for reducing design time.
Data Engine	TSDE042G52 VC	2.5G Cell/packet data engine including virtual concatenation	4xSTS-3/12, or 1xSTS48 Cell/Packet Data engine with APS and cross connect with high order virtual concatenation.	Highly integrated, extremely versatile data engine with 12.5G integrated cross connect supports High-order (STS) virtual concatenation with LCAS, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, GeOS and IP. Software drivers available for reducing design time.
Driver	TCLD0110G	10 Gbits/s clocked laser driver	For direct modulated lasers up to 12.5 Gbits/s.	Same as TLAD0110G except with the additional feature of data retiming with 10G serial clock input.
Driver	TCMD0110G	10 Gbits/s clocked modulator driver	Drives either an EML or MZ modulator at 10 Gbits/s or 12.5 Gbits/s operation.	Same as TMOD0110G with the addition of clock retiming; available as die or low cost plastic package.
Driver	TLAD0110G	10 Gbits/s laser driver	For direct modulated lasers up to 12.5 Gbits/s.	-5.2 V power supply; operation to 12.5 Gbits/s; up to 100 mA drive current; 20 Ω to 50 Ω loads; 25ps rise/fall times; internal 50 Ω back term; laser modulation and bias controls; 1.2 ps rms jitter; available in die form.
Driver	TMOD0110G	10 Gbits/s modulator driver	Drives either an EML or MZ modulator at 10 Gbits/s or 12.5 Gbits/s operation.	-5.2 V power supply; operation to 12.5 Gbits/s; complementary outputs user adjustable to 3.0 Vp-p; 28 ps type; rise/fall times; 50 Ω input/output terminations; pulse width control, ceramic or low cost plastic package.
DSP	DSP16410	High-performance digital signal processor (DSP), 2 DSP16000 DSP cores, 800 MMACS, 388 kbit memory	2G/2.5G BTS: equalization, channel processing, speech processing.	Twin DSP16000 dual-MAC cores. Small package, low power consumption.
DSP	DSP16411	High performance Digital Signal Processor (DSP), 2 DSP16000 DSP cores, 960 MMACS, 644 kbit memory	2G/2.5G BTS: equalization, channel processing, speech processing.	Performance improvement/cost reduction DSP16410 software compatible, higher max clock rate and increased memory.
Framer	MARS1G2P (TADM021G2 V1B)	STS-3/12 SONET/SDH ADM with ATM and/or packet data engine	4xSTS-3, or 2xSTS12 SONET/SDH or POF/POS 16-channel framer with APS, cross connect and data engine.	Highly integrated, extremely versatile with 5G integrated cross connect, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, and IP. Software drivers available for reducing design time.
Framer	MARS1G2P (TADM021G2 V2)	STS-3/12 SONET/SDH ADM with ATM and/or packet data engine	Low power version of TADM V1B with 1.6 V core and enhanced data engine capabilities. This 792-pin PBGA package supports 4xSTS-3, or 2xSTS12 SONET/SDH/POF/POS with a 16 -channel Framer including APS,cross connect and enhanced data engine.	Highly integrated, extremely versatile with 5G integrated cross connect, proven technology, and very price competitive. Applications : POS, ATM, HDLS/PPP, and IP. Software drivers available for reducing design time.
Framer	MARS2G5 P-LT (TADM042G5 V1B)	STS-3/12/48 SONET/SDH ADM with ATM and/or packet data engine	4xSTS-3, or 4xSTS12, or 1xSTS48 SONET/SDH or POF/POS16 - channel framer with APS, and cross connect and data engine.	Highly integrated, extremely versatile with 12.5G integrated cross connect, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, and IP. Software drivers available for reducing design time.

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Framer	MARS2G5 P (TADM042G52 V2.2)	STS-3/12/48 SONET/SDH ADM with ATM and/or packet data engine	Low power version of TADM V1B with 1.6 V core and enhanced data engine capabilities. Available in 600-pin LBGA or 792-pin PBGA package. Supports 4xSTS-3, or 4xSTS12, or 1xSTS48 SONET/SDH /POF/POS with a 16- channel framer. APS, cross connect and enhanced data engine.	Highly integrated, extremely versatile with 12.5G integrated cross connect, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, and IP. Software drivers available for reducing design time.
Framer	MARS622 P (TADM04622 V1B)	STS-3/12 SONET/SDH ADM with ATM and/or packet data engine	4xSTS-3, or 1xSTS12 SONET/SDH or POF/POS 16-channel framer with APS, and cross connect and data engine.	Highly integrated, extremely versatile with 2.5 G integrated cross connect, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, and IP. Software drivers available for reducing design time.
Framer	MARS622 P (TADM04622 V2.2)	STS-3/12 SONET/SDH ADM with ATM and/or packet data engine	Low power version of TADM V1B with 1.6 V core and enhanced data engine capabilities. This 792-pin PBGA packages, supports 4xSTS-3, or 1xSTS12 SONET/SDH/POF/POS with a 16 -channel framer including APS, cross connect and enhanced data engine.	Highly integrated, extremely versatile with 12.5 G integrated cross connect, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, and IP. Software drivers available for reducing design time.
Framer	MARS622 P (TADM04622LT V1B)	792-Pin PBGA - STS-3/12 SONET/SDH ADM with ATM and/or packet data engine	4xSTS-3, or 1xSTS12 SONET/SDH or POF/POS 16-channel framer with APS, and cross connect and data engine.	Highly integrated, extremely versatile with 5 G integrated cross connect, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, and IP.
Framer	TADMVC1G2	STS-3/12 SONET/SDH ADM with ATM and/or packet data engine, and virtual concatenation	Low power version of TADM V1B with 1.6 V core and enhanced data engine capabilities including high order virtual concatenation. This 792-pin PBGA packages, supports 4xSTS-3, or 2xSTS12 SONET/SDH/POF/POS with a 16-channel framer including APS, cross connect and enhanced data engine.	Highly integrated, extremely versatile with 12.5 G integrated cross connect supports high-order (STS) virtual concatenation with LCAS, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, GeOS, and IP. Software drivers available for reducing design time.
Framer	MARS2G5 P-VC (TADMVC2G52 V2.2)	STS-3/12/48 SONET/SDH ADM with ATM and/or packet data engine, and virtual concatenation	Low power version of TADM V1B with 1.6 V core and enhanced data engine capabilities including high order virtual concatenation. Available in 600-pin LBGA or 792-pin PBGA package. Supports 4xSTS-3, or 4xSTS12, or 1xSTS48 SONET/SDH/POF/POS with a 16-channel framer. APS, cross connect and enhanced data engine.	Highly integrated, extremely versatile with 12.5 G integrated cross connect supports high-order (STS) virtual concatenation with LCAS, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, GeOS, and IP.
Framer	TADMVC622	STS-3/12 SONET/SDH ADM with ATM and/or packet data engine, and virtual concatenation	Low power version of TADM V1B with 1.6 V core and enhanced data engine capabilities including high order virtual concatenation. This 792-pin PBGA packages, supports 4xSTS-3, or 1xSTS12 SONET/SDH/POF/POS with a 16-channel framer including APS, cross connect and enhanced data engine.	Highly integrated, extremely versatile with 12.5 G integrated cross connect supports high-order (STS) virtual concatenation with LCAS, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, GeOS, and IP. Software drivers available for reducing design time.
Framer	TDAT021G2	STS-3/12 SONET/SDH interface with ATM data engine	4xSTS-3, or 2xSTS-12 SONET/SDH 4 channel framer with ATM path processing in data engine.	Highly integrated, proven technology, and very price competitive. Applications: ATM.

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Framer	MARS2G5 P-ProLT (TDAT042G5)	STS-3/12/48 SONET/SDH interface with ATM data engine	4xOC-3, or 4xOC12, or 1xOC-48 SONET/SDH 4-channel framer with ATM path processing in data engine.	Highly integrated, proven technology, and very price competitive. Applications: ATM.
Framer	TDAT04622	STS-3/12 SONET/SDH interface with ATM data engine	4xSTS-3, or 1xSTS-12 SONET/SDH 4 channel framer with ATM path processing in data engine.	Highly integrated, proven technology, and very price competitive. Applications : ATM.
Framer	MARS2G5 P-Pro (TDAT162G5 V1B)	STS-3/12/48 SONET/SDH Interface with ATM and or packet data engine	4xOC-3, or 4xOC12, or 1xOC-48 SONET/SDH 16-channel framer with ATM path processing in data engine.	Highly integrated, extremely versatile with 12.5G integrated cross connect, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, and IP. Software drivers available for reducing design time.
Framer	MARS2G5 P-Pro (TDAT162G52 VC)	STS-3/12/48 SONET/SDH Interface with ATM and or packet data engine with virtual concatenation	Low power version of TADM V1B with 1.6 V core and enhanced data engine capabilities including high order virtual concatenation. This device supports 4xOC-3, or 4xOC12, or 1xOC-48 SONET/SDH 16- channel framer with ATM path processing in data engine.	Highly integrated, extremely versatile supports high-order (STS) virtual concatenation with LCAS, proven technology, and very price competitive. Applications: POS, ATM, HDLS/PPP, GeOS and IP. Software drivers available for reducing design time.
Framer	MARS1G2 T-LT (TSOT021G2 V2.2)	STS-3/12 SONET/SDH ADM	Latest version TSOT with 1.6 V core. This device supports 4xOC-3, or 2xOC12, SONET/SDH framer.	Extremely versatile, proven technology, integrated cross connect, and very competitive. Access applications: POS, ATM, TDM data handle. Software drivers available for reducing design time.
Framer	MARS10G T-LT (TSOT0410G V1.4)	OC-192 framer/pointer processor	Supports 4xSTS-48, or 1xSTS192 SONET/SDH with a 4-channel framer.	Highly integrated, extremely versatile, proven technology, and very competitive. OTN applications: POS, ATM, TDM data handle. Software drivers available for reducing design time.
Framer	MARS2G5 T (TSOT042G5 V1B)	STS-3/12/48 SONET/SDH ADM	4xSTS-3/12, or 1xSTS48 SONET/SDH 16-channel framer with APS, and cross connect.	Highly integrated, extremely versatile with 5G integrated cross connect, proven technology, and very price competitive. Software drivers available for reducing design time.
Framer	MARS2G5 T (TSOT042G52 V2)	792-Pin PBGA - STS-3/12/48 SONET/SDH ADM	4xSTS-3/12, or 1xSTS48 SONET/SDH 16-channel framer with APS, and cross connect.	Extremely versatile with 12.5G integrated cross connect, proven technology, and very price competitive. Software drivers available for reducing design time.
Framer	MARS622 T-LT (TSOT04622 V2.2)	STS-3/12 SONET/SDH ADM	Latest version TSOT with 1.6 V core. This device supports 4xOC-3, or 1xOC12, SONET/SDH.	Extremely versatile, proven technology, integrated cross connect, and very competitive. Access applications: POS, ATM, TDM data handle. Software drivers available for reducing design time.
Framer	MARS5G TD-Pro (TSOT1605DP V1.0)	16xSTS-3, 8xSTS-12, or 2xSTS48 SONET/SDH framer	Supports 16 STS-3, 8xSTS-12, or 2xSTS48 SONET/SDH with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versatile 5G framer with integrated cross connect support, and price competitive. Applications: DWDM. Software drivers available for reducing design time.
Framer	MARS5G TD-Pro (TSOT1605DP8 V1.0)	8xSTS-3, 8xSTS-12, or 2xSTS48 SONET/SDH framer	Supports 8 STS-3, 8xSTS-12, or 2xSTS48 SONET/SDH with APS, cross connect, OH transparency and 622 MHz secondary line interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: DWDM. Software drivers available for reducing design time.
Framer	MARS5G T-Pro (TSOT1605GP V1.0)	16xSTS-3, 8xSTS-12, or 2xSTS48 SONET/SDH framer	Supports 16 STS-3, 8xSTS-12, or 2xSTS48 SONET/SDH with APS, cross connect, OH transparency and optional 2.5 G backplane interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: POS, ATM, TDM data handle. Software drivers available for reducing design time.

Function	Product	What It Is	What It Does	Key Features/Benefits
Framer	MARS5G T-Pro8 (TSOT1605GP8 V1.0)	8xSTS-3, 8xSTS-12, or 2xSTS48 SONET/SDH framer	Supports 8 STS-3, 8xSTS-12, or 2xSTS48 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5 G/622 MHz backplane interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: POS, ATM, TDM data handle. Software drivers available for reducing design time.
Framer	MARS10G TD-Pro (TSOT1610DP V1.0)	4xSTS48, or 1xSTS192 SONET/SDH framer	Supports 4xSTS-48, or 1xSTS192 SONET/SDH with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: DWDM. Software drivers available for reducing design time.
Framer	MARS2G5 TD-Pro16 (TSOT1610DP6 V1.0)	16xSTS-3, or 16xSTS-12, SONET/SDH framer	Supports 16 STS-3/12 SONET/SDH with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: DWDM. Software drivers available for reducing design time.
Framer	MARS10G T-Uni (TSOT1610G V1.0)	16xSTS-3/12, 4xSTS48, or 1xSTS192 SONET/SDH framer	Supports 16 STS-3/12, 4xSTS-48, or 1xSTS192 SONET/SDH with APS, cross connect, OH transparency and dual 2.5 G/622 MHz backplane interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: POS, ATM, TDM data handle. Software drivers available for reducing design time.
Framer	MARS10G TD-Uni (TSOT1610GD V1.0)	16xSTS-3/12, 4xSTS48, or 1xSTS192 SONET/SDH framer	Supports 16 STS-3/12, 4xSTS-48, or 1xSTS192 SONET/SDH with a 16 channel framer with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: DWDM. Software drivers available for reducing design time.
Framer	MARS10G T-Pro (TSOT1610GP V1.0)	4xSTS48, or 1xSTS192 SONET/SDH framer	Supports 4xSTS-48, or 1xSTS192 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5 G/622 MHz backplane interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: POS, ATM, TDM data handle. Software drivers available for reducing design time.
Framer	MARS10G T-Pro16 (TSOT1610GP6 V1.0)	16xSTS-3, or 16xSTS-12, SONET/SDH framer	Supports 16 STS-3/12 SONET/SDH with APS, cross connect, OH transparency, and dual 2.5 G/ 622 MHz backplane interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: POS, ATM, TDM data handle. Software drivers available for reducing design time.
Framer	MARS2G5 TD-Pro16 (TSOT162D5P6 V1.0)	16xSTS-3, 4xSTS-12, 1xSTS48 SONET/SDH framer	Supports 16xSTS-3, 4xSTS-12, 1xSTS-48 SONET/SDH with APS, cross connect, OH transparency, and 622 MHz secondary line interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: DWDM. Software drivers available for reducing design time.
Framer	MARS2G5 T-Pro16 (TSOT162G5P6 V1.0)	16xSTS-3, 4xSTS-12, 1xSTS48 SONET/SDH framer	Supports 16xSTS-3, 4xSTS-12, 1xSTS-48 SONET/SDH with APS, cross connect, OH transparency and dual 2.5 G/622 MHz backplane interface.	Highly integrated, extremely versitile, price competitive 5 G framer with cross connect support. Applications: POS, ATM, TDM data handle. Software drivers available for reducing design time.
Framer	TSOTLT2G5 V1B	792-Pin PBGA - STS-3/12/48 SONET/SDH ADM	4xSTS-3/12, or 1xSTS48 SONET/SDH 16-channel framer with APS, and cross connect.	Highly integrated, extremely versatile with 5G integrated cross connect, proven technology, and very price competitive. Software drivers available for reducing design time.
Mapper	Hypermapper (TMXF33625)	Integrated SONET/SDH mapper, MUX, and T1/E1/J1 framer. Used for OC3 or OC12 applications.	622/155 Mbit/s SONET/SDH interface for DS3/ E3 and DS0/E0 applications. Supports 1:1 and 1 + 1 protection schemes.	Extremely versatile device with tremendous integration and flexibility. Supports ITU, *Telcordia™ Technologies, ANSI®*, and Japanese standards.

Function	Product	What It Is	What It Does	Key Features/Benefits
Mapper	Supermapper (TMXF28155)	Integrated SONET/SDH mapper, MUX, and T1/E1/J1 framer. Used for OC3 or STS1/STM0.	155/51 Mbits/s SONET/SDH interface for DS3, DS2, DS1, E1, J1 and DS0/E0 applications. Supports 1 + 1 and ring protection with additional devices.	Extremely versatile device with tremendous integration and flexibility. Supports ITU, *Telcordia Technologies, ANSI, ETSI*, and Japanese standards.
Mapper	Ultramapper (TMXF84622)	Integrated SONET/SDH mapper, MUX, and T1/E1/J1 framer. Used for OC3 or OC12 applications.	622/155 Mbits/s SONET/SDH interface for DS3, E3, DS2, DS1, E1, J1 and DS0/E0 applications. Supports 1 + 1 and ring protection with additional devices.	Extremely versatile device with tremendous integration and flexibility. Supports ITU, *Telcordia Technologies, ANSI*, and Japanese standards.
Network Processors	*PayloadPlus*® 2.5G APP520	Highly integrated 2.5 Gbits/s network processors forEthernet bridging, VLANs, Ethernet over SONET	Programmable layer 2–4 plus protocol processing, traffic management/shaping/ modification, and policing & statistics. Optimized for Ethernet and packet/frame processing at aggressive price points.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line rate performance, and best in class traffic management. The APP520 integrates into the NP Ethernet MACs, full-featured traffic management, and a high-performance search engine.
Network Processors	*PayloadPlus* 2.5G APP530	Highly integrated 2.5 Gbits/s network processor for edge/access and multi-service applications	Programmable layer 2–4 plus protocol processing, traffic management/ shaping/modification and policing & statistics. Designed for full multiservice internetworking of ATM, Ethernet, IPv4, IPv6, frame relay, etc.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line rate performance, and best in class traffic management. The APP530 integrates into the NP ATM SAR and OAM engines, Ethernet MACs, full-featured, multiservice-capable traffic management, and a high-performance search engine.
Network Processors	*PayloadPlus* 2.5G APP530TM	Highly integrated 2.5 Gbits/s network processors for edge/access and multi-service applications. These devices include pre-written software to perform ATM SARing, traffic management, policing, and OAM.	Programmable layer 2–4 plus protocol processing, traffic management/shaping/ modification and policing & statistics. Designed for full multiservice internetworking of ATM, Ethernet, IPv4, IPv6, frame relay, etc.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line rate performance, and best in class traffic management. The APP530 integrates into the NP ATM SAR and OAM engines, Ethernet MACs, full-featured, multiservice-capable traffic management, and a high-performance search engine.
Network Processors	*PayloadPlus* 5G APP540	Highly integrated 5 Gbits/s network processors for Ethernet bridging, VLANs, Ethernet over SONET	Programmable layer 2–4 plus protocol processing, traffic management/shaping/ modification and policing & statistics. Optimized for Ethernet and packet/frame processing at aggressive price points.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line rate performance, and best in class traffic management. The APP540 integrates into the NP Ethernet MACs, full-featured, traffic management, and a high-performance search engine.
Network Processors	*PayloadPlus* 5G APP550	Highly integrated 5 Gbits/s network processor for edge/access and multi-service applications	Programmable layer 2–4 plus protocol processing, traffic management/shaping/ modification and policing & statistics. Designed for full multiservice internetworking of ATM, Ethernet, IPv4, IPv6, frame relay, etc.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line rate performance, and best in class traffic management. The APP550 integrates into the NP ATM SAR and OAM engines, Ethernet MACs, full-featured, multiservice-capable traffic management, and a high-performance search engine.

Function	Product	What It Is	What It Does	Key Features/Benefits
Network Processors	*PayloadPlus* 5G APP550TM	Highly integrated 5 Gbits/s network processors for edge/access and multi-service applications. These devices include prewritten software to perform ATM SARing, traffic management, policing, and OAM.	Programmable layer 2-4 plus protocol processing, traffic management/shaping/ modification and policing & statistics. Designed for full multiservice internet working of ATM, Ethernet, IPv4, IPv6, frame relay, etc.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for True line rate performance, and best in class traffic management. The APP550 integrates into the NP ATM SAR and OAM engines, Ethernet MACs, full-featured multiservice-capable traffic management, and a high-performance search engine.
Network Processors	*PayloadPlus* 10G (APP750NP, APP750TM)	10 Gbit/s multiprotocol network processor chipset	Programmable layer 2-4 plus protocol processing, traffic management/shaping/ modification and policing & statistics. Optimized for high performance high-value packet/frame applications.	Three key benefits of *PayloadPlus* network processors are simple software model, SoC approach for true line rate performance, and best in class traffic management. The APP750 chip set provides full line rate performance with any packet size and supports large 2M+ entry routing tables using low-cost, low-power DRAM.
RF Power	Transistors (AGRXXXXX)	Coolest temperature radio frequency power transistor that enable much cooler, smaller, and less expensive wireless base stations than are possible using any other RF power transistor technology	Boosts signals of voice, data, and video in various frequency ranges before the signals are delivered to wireless subscribers.	Transistors available for all frequency ranges. High-reliability gold-metalization process. Best-in-class thermal resistance. High gain, efficiency, and linearity. Integrated ESD protection.
SerDes	SDP3G06	6-channel, 1–3.2 Gbits/s serializer/deserializer interface	Recovers clock and data from high-speed serial signal and converts to parallel data and converts parallel data to high-speed serial differential signals.	Interoperable, high signal integrity, low power, configurable, handles 8b/10b coding.
SerDes	SDP3G08	8-channel, 1–3.2 Gbits/s serializer/deserializer interface	Recovers clock and data from high-speed serial signal and converts to parallel data and converts parallel data to high-speed serial differential signals.	Interoperable, high signal integrity, low power, configurable, handles 8b/10b coding.
Switch Fabric	APC Family (APC, APC Ultra-Lite)	Single-chip OC-12 ATM solution	Connection management, policing, traffic management, OAM.	Single-chip, complete ATM solution with a variety of price points. Software compatibility across all families.
Switch Fabric	ASX/ACE	Multidevice 40 x 40 port ATM switch fabric solution. The ASX is the 8 x 8 port queuing, buffering and arbitration device. The ACE is the 8 x 8 port crossbar device.	Switches 25 Gbits/s of ATM cell traffic in a 40 x 40 port matrix with user bandwidth of 622 Mbits/s per port. Seamlessly interconnects to the APC port managers.	25 Gbits/s user capacity. Eight 800 Mbits/s I/O ports. Nonblocking, loss-less, and self-routing switch fabric. No external memory required. Internal 512 cell size buffer. 4 traffic classes. Fabric redundancy supported. 16-bit asynchronous µP interface.
Switch Fabric	BCST1A	Single-device 8 x 8 port ATM switch fabric solution	Switches 5 Gbits/s of ATM cell traffic in an 8 x 8 port matrix with user bandwidth of 622 Mbits/s per port. Seamlessly interconnects to the APC port managers.	5 Gbits/s user capacity. Eight 800 Mbits/s I/O ports. Nonblocking and loss-less switch. No external memory required. Internal 512 cell size buffer. 4 traffic classes. Fabric redundancy supported. 16-bit asynchronous µP interface.

Function	Product	What It Is	What It Does	Key Features/Benefits
Switch Fabric	PI20SAX	Single-device 16 x 16 port protocol independent switch fabric solution	Switches 20 Gbits/s of user traffic in a 16 x 16 port matrix with flexible user port rates.	20 Gbits/s user capacity. 16 Integrated 1.25 Gbits/s or 2.5 Gbits/s Tx/Rx SerDes link pairs. Internal CDR and embedded link alignment. Port rates from OC-12 to OC-192 supported. Nonblocking, loss-less, and self-routing switch fabric. No external memory required. Internal 8k unicast cell size buffer. Internal 1k multicast cell size buffer. 512 queue support. 3 scheduling priorities. 4 traffic classes. 1+1 fabric redundancy supported. 16-bit asynchronous µP interface.
Switch Fabric	PI40SAX	Single-device 32 x 32 port protocol independent switch fabric solution	Switches 40 Gbits/s of user traffic in a 40 x 40 port matrix with flexible user port rates.	40 Gbits/s user capacity. 32 Integrated 1.25 Gbits/s or 2.5 Gbits/s Tx/Rx SerDes link pairs. Internal CDR and embedded link alignment. Port rates from OC-12 to OC-192 supported. Nonblocking, loss-less, and self-routing switch fabric. No external memory required. Internal 8k unicast cell size buffer. Internal 1k multicast cell size buffer. 1024 queue support. 3 scheduling priorities. 4 traffic classes. 1+1 fabric redundancy supported. 16-bit asynchronous µP interface.
Switch Fabric	PI40X/PI40C	Multi device 1024 x 1024 port protocol independent switch fabric solution. The PI40X is the 32 x 40 port aggregation, queuing, scheduling device. The PI40C is the 64 x 64 port crossbar switching and arbitration device.	Switches 2.5 Tbits/s of user traffic in a 1024 x 1024 port matrix with flexible user port rates.	2.5 Tbits/s user capacity. 1024 Integrated 1.25 Gbits/s or 2.5 Gbits/s Tx/Rx SerDes link pairs. Internal CDR and embedded link alignment. Port rates from OC-12 to OC-768 supported. Nonblocking, loss-less, and self-routing switch fabric. No external memory required. Internal 8k unicast cell size buffer per PI40X. Internal 1k multicast cell size buffer per PI40X. 1024 queue support. 3 scheduling priorities. 4 traffic classes. 1+1, 1:N and stackable fabric redundancy supported. 16-bit asynchronous µP interface.
TDM Interconnect	*Ambassador*® T8100A	Time-slot interchanger (TSI) with compliance to TDM backplane standards such as H.100, H.110, MVIP, HMVIP, etc.	Switches 1024 time slots (TSs) between 16I/16O streams and 256 time slots to 32 bidirectional backplane streams providing clock mastering capabilities to the system.	1024 local TS capacity. 256 TS backplane capacity. 16I/16O local streams. 32 bidirectional backplane streams. Supports local stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1, 2, or 4-bit subrate switching.
TDM Interconnect	*Ambassador* T8102	Time-slot interchanger (TSI) with compliance to TDM backplane standards such as H.100, H.110, MVIP, HMVIP, etc.	Switches 512 time slots (TSs) between 16I/16O streams and 32 bidirectional backplane streams providing clock mastering capabilities to the system.	512 TS backplane capacity. 16I/16O local streams. 32 bidirectional backplane streams. Supports local stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1, 2, or 4-bit subrate switching.
TDM Interconnect	*Ambassador* T8105	Time-slot interchanger (TSI) with compliance to TDM backplane standards such as H.100, H.110, MVIP, HMVIP, etc.	Switches 1024 time slots (TSs) between 16I/16O streams and 512 time slots to 32 bidirectional backplane streams providing clock mastering capabilities to the system.	1024 local TS capacity. 512 TS backplane capacity. 16I/16O local streams. 32 bidirectional backplane streams. Supports local stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1, 2, or 4-bit subrate switching.
TDM Interconnect	*Ambassador* T8110	Time-slot interchanger (TSI) with compliance to TDM backplane standards such as H.100, H.110, MVIP, HMVIP, etc.	Switches 4096 time slots (TSs) between 64 bidirectional local and backplane streams providing clock mastering capabilities to the system.	4096 local or backplane TS capacity. 64 bidirectional local and backplane streams. Supports local stream I/O rates of 2 Mbits/s, 4 Mbits/s, 8 Mbits/s or 16 Mbits/s. Supports 1, 2, or 4-bit subrate switching. PCI or µP I/F.
Time-Slot Interchanger	TTSI1K	1k x 1k DS0 time-space-time TDM switch	Switches 1024 time slots (TSs) between 16 Tx/Rx stream pairs.	1024 TS capacity. 16 Tx/16 Rx TDM streams. Supports TDM stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1, 2, or 4 bit subrate switching. Test pattern generation. Output enables for Tx streams. Frame integrity/low latency mode. 8-bit asynchronous µP I/F.

Function	Product	What It Is	What It Does	Key Features/Benefits
Time-Slot Interchanger	TTSI2K	2k x 2k DS0 time-space-time TDM switch	Switches 2048 time slots (TSs) between 32 Tx/Rx stream pairs.	2048 TS capacity. 32 Tx/32 Rx TDM streams. Supports TDM stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1, 2, or 4-bit subrate switching. Test pattern generation. Output enables for Tx streams. Frame integrity/low latency mode. 8-bit asynchronous µP I/F.
Time-Slot Interchanger	TTSI4K	4k x 4k DS0 time-space-time TDM switch	Switches 4096 time slots (TSs) between 32 Tx/Rx stream pairs.	4096 TS capacity. 32 Tx/32 Rx TDM streams. Supports TDM stream I/O rates of 2 Mbits/s, 4 Mbits/s, or 8 Mbits/s. Supports 1, 2, or 4-bit subrate switching. Test pattern generation. Output enables for Tx streams. Frame integrity/low latency mode. 8-bit asynchronous µP I/F.
Time-Slot Interchanger	TSI-8	8k x 8k DS0 time-space-time TDM switch	Switches 8192 time slots (TSs) between 32 Tx/Rx stream pairs.	8192 TS capacity. 32 Tx/32 Rx TDM streams. Supports TDM stream I/O rates of 2 Mbits/s, 4 Mbits/s, 8 Mbits/s or 16 Mbits/s. Test pattern generation/monitoring. 16 translation table look-ups. Frame integrity/low latency mode. 16-bit synchronous µP I/F.
Time-Slot Interchanger	STSI-144	Scalable TSI. 144k x 16k asymmetric DS0 time-space-time TDM switch.	Switches 16384 time slots (TSs) between 64 Tx/Rx stream pairs and 16 Tx/Rx high-speed serial link (HSL) pairs. Allows centralized and distributed 10G TDM switching.	147456 x 16384 TS capacity. 64 Tx/32 Rx TDM streams. 16 Tx/16 Rx HSL LVDS links (622 Mbits/s). Supports TDM stream I/O rates of 2 Mbits/s, 4 Mbits/s, 8 Mbits/s or 16 Mbits/s. Test pattern generation/monitoring. 16 translation table look-ups. Frame integrity/low latency mode. 16-bit synchronous µP I/F.
Transceiver	TTSV04622	STS-48 backplane transceiver with CDR	Supports a 2.5G interface for backplane connections. The 1.24 Gbits/s interface is implemented as quad 622 Mbits/s LVDS links. The device includes clock/data recovery (CDR) and MUX/deMUX between 77.76 MHz byte-wide internal data buses and the 622 Mbits/s external serial links.	Extremely versatile, proven technology, STS-48 backplane driver with CDR.

Function	Product	What It Is	What It Does	Key Features/Benefits
IP Core Library				
IP Core	10 Gigabit Ethernet	Various 10 Gigabit Ethernet cores	Library of cores for 10 Gigabit Ethernet support.	6 different cores available. Support for MAC, PCS, and XAUI interface functions.
IP Core	ARM7	ARM7 processor and peripherals	Embedded processor and peripherals for low-cost embedded applications.	Synthesizable core. Area and power efficient.
IP Core	ARM9	ARM9 processor and peripherals	Embedded processor and peripheral for mainstream applications.	Synthesizable and hard cores available. Up to 300 MHz and 300 MIPS. Configurable local memory sizes. Configurable instruction and data cache sizes. Supports *AMBA*™ bus (AHB) for integration of peripherals. 13 different peripheral cores available. Available memory management unit. Supports embedded trace modules and buffers for easier debug of software.
IP Core	ARM10	ARM10 processor and peripherals	Embedded processor and peripherals for high-end, performance applications.	Synthesizable and hard cores available. Up to 330 MHz and 400 MIPS. Integrated DSP and Java support. Configurable local memory sizes. Configurable instruction and data cache sizes. Supports *AMBA* bus (AHB) for integration of peripherals. 13 different peripheral cores available. Available memory management unit. Supports embedded trace modules and buffers for easier debug of software.
IP Core	CAM	Content addressable memories	Binary and ternary content addressable memories.	Configurable CAM sizes up to 144 kbits. Configurable TCAM sizes up to 1k x 144 TCAM. Single-cycle look- ups up to 200 MHz.
IP Core	FE MAC	10/100 Mbits/s Ethernet MAC IP core	Media access control for *IEEE*® 802.3 networks at 10 or 100 Megabits per second.	Simple FIFO style interface to a switch or customer ASIC. VLAN support. Half and full duplex support. Link level flow control via MAC control frames switch-based backpressure. Jumbo packet support.
IP Core	GigE MAC	Gigabit Ethernet MAC IP core	Media access control for *IEEE* 802.3 networks at 1 Gigabit per second.	Simple FIFO style interface to a switch or customer ASIC. VLAN support. Jumbo packet support.
IP Core	Memories	Compiled memories (SRAM)	Embedded memories for ASIC integration, replaces external SRAM memories.	Single-port and multiport configurations. Configurable sizes and widths available. Support for register file, conventional SRAM, and 1T SRAM.
IP Core	PCI Buffers	PCI 2.3 buffers	Buffers for conventional PCI link cores or customer logic.	Up to 66 MHz. Push/pull and PME/open drain available. Supports PME hot plug. Supports cardbus.
IP Core	PCI Link	PCI 2.3 link core	Universal PCI master/target link core.	32/64-bit PCI data bus support. 33/66 MHz PCI bus clock support. PCI 2.3 compliant. Zero wait-state and fast back-to-back transaction support.

Function	Product	What It Is	What It Does	Key Features/Benefits
IP Core Library				
IP Core	PCI-Express PHY	PCI-express PHY electrical core	PCI-express PHY electrical layer implementation.	2.5 Gbits/s data rate. Programmable TX signaling –550 to 1200 mV. 175–1200 mV RX range. 85 mV loss of signal detect. 0.5 UI RX jitter tolerance. 0.24 UI TX jitter generation. Pre-emphasis/de-emphasis equalization programmable up to 30% (3 dB).
IP Core	PCI-Express Protocol	PCI-express protocol core	PCI-express link and PHY logical implementation.	PHY, data link, and transaction layers in hardware, no transaction processing required in software. Complies with PCI-express base specification v1.0. Supports x1, x2, x4, x8, and x16 lane links. PCI type 0 and type 1 header and PCI express configuration and capability register space support. Supports extended PCI express capability structures: virtual channels, advanced error reporting, device serial number, and power budgeting. Configurable application dependent interface modules for ASIC integration. Power management and hot plug support. End-to-end CRC data integrity.
IP Core	PCI-X Buffers	PCI-X mode 1 and mode 2 buffers	Buffers for PCI-X link cores or customer logic.	Mode 1 and mode 2 (DDR) available. Push/pull and PME/open drain available. Backward compatible with PCI 2.2/2.3.
IP Core	PCI-X Link	PCI-X 1.0 link core	Universal PCI-X master/target link core.	32/64-bit PCI data bus support. 33/66/133 MHz PCI bus clock support. PCI-X 1.0 compliant. PCI 2.3 backwards compatible. Host bridge support. Split transaction support. 64-bit applications interface.
IP Core	SoC Support Cores	Various SoC support and peripheral cores	Library of cores for SoC peripheral support.	37 different cores available. Provides support for multimedia, security, and communications functions.
IP Core	SONET and Backplane Drivers	Various SONET and backplane driver cores	Library of cores for SONET support and interconnection of Agere SONET framers, switches, and mappers across backplanes.	13 different cores available. Support for SONET transport and framing functions. Supports backplane applications for scalable, chassis-based equipment.
IP Core	SPI-4	SPI-4 link and PHY core	Link and PHY for SPI-4 data interface.	Dynamic deskew support. Enhanced skew tolerance (±3 bit times). Full calendar scheduling support. Up to 800 Mbits/s per lane, 12 Gbits/s total bandwidth.
IP Core	Tri-Mode MAC	10/100/1000 Mbits/s Ethernet MAC IP core	Media access control for *IEEE* 802.3 networks at 10 or 100 Mbits/s, or 1 Gbits/s.	Support for PCI or native bus interfaces. Integrated DMA. Link level flow control via MAC control frames. Hardware assist for TCP checksum and offload. Jumbo packet support.
IP Core	WAN and ATM	Various WAN and ATM cores	Library of cores for WAN and ATM protocol and interface support.	15 different cores available. Support for ATM and T1 framing and transport functions. 13 different cores available. Support for SONET transport and framing functions. Supports backplane applications for scalable, chassis-based equipment.

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