CableNetwork

MOTOROLA

FEATURES

- **Up to eight controlled channels per enclosure**
- **Baseband encoded random dynamic scrambling**
- **Microprocessor controlled**
- **Dynamic event control with integral real-time clock**
- **Standard 19-inch equipment rack mount**

The HVP-III Headend Video Processor is a third generation processor that provides scrambling, encoding and addressing for baseband addressable terminals.
The HVP-III provides secure video scrambling using random dynamic baseband video inversion, compression and sync suppression. Descrambling data is encrypted for greater security and is constantly changed.

OPERATION

The HVP-III inserts both addressing and channel control information within the video bandwidth portion of each HVP-III channel. This information includes system ID, channel packages and event numbers on pay-per-view programs. Picture quality is enhanced by video clamps, AGC and a peak white clipper.
The HVP-III is controlled by the Micro-ACS headend computer. Alterable parameters may be changed through the addressing computer without a technician's presence at the headend location. HVPs may be co-located with the Micro-ACS or remotely located via a phone line or an RF communication link.

USER FEATURES

HVP-III channel controls may be reconfigured from the Micro-ACS or by direct HVP-III input through a terminal. A selectable alternate video generator may be set for addressing even in the absence of a video source following channel sign-off.

Specifications are subject to change without notice.   1027 S.W. 30th Avenue • Deerfield Beach, Florida 33442   HVPIII - 1
Phone: (954) 312-1200 • Fax: (954) 312-1077
Toll Free: 1-888-201-7200
www.cablenetwork.net

Standard BNC connectors serve as signal input-output points on the HVP-III rear panel. A third bank of rear-panel connectors also lets any channel serve as a loop-through source for another channel.

HVP-III multicolored LED indicators give the technician visual confirmation of Micro-ACS/HVP-III communication for test and calibration purposes. Adjustments, switch settings, and test points are also conveniently located along the front edge of each HVP-III for in-place testing.

Specifications

Analog Addressable Headend Video Processor[HVP-III]

Video Inputs:	Indicators:
Bridging Video Input Impedance:	ACS Receive and Transmit Data
> 3K Ohms (DC to 6 MHz)	Scrambling
Level:	White Clip
0.67 to 2.0 V pp	Detected Scene Change
Video Outputs:	Voltage Supply
Return Loss:	Self Test
> 16 dB (30 Hz to 6 MHz)	**User Adjustments:**
Impedance:	Reset
75 Ohms (Nominal)	Baud Rate
Level:	Hub ID
1 V pp into 75 Ohms (Nominal)	Channel ID
DC Offset:	Video Offset
Blanking Level = 0.0 Vdc (±0.25 Vdc)	Video Inverting Offset
Isolation Output One to Output Two:	AGC Level
< 60 dB (30 Hz to 6 MHz)	Sync Level
AGC Specifications:	Sync Pull Up
Output Level Change for 6 dB Input Change:	White Clip
< 0.5 dB	**Test Points:**
Manual Level Set Response Time:	Input Video
Less Than 5 Seconds	Composite Sync
Data Level at Video Output:	Power
80 IRE Nominal	Output Video

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Composite Sync Output:		AC Input:
Output Level:		110 Volts AC, 60 Hertz
0.28 V pp into 75 Ohms		**Mount:**
		Standard 19-Inch Rack Mount
		Size:
		19.0" Wide
		20.5" Deep
		10.5" High

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