Front Panel I/O Connectivity
Design Guide

October 2000

Order Number A29286-001

Revision History

Revision	Revision History	Date
V1.0	Release version	October 2000

Changes to this guide will be published in the Intel® Guide Update before being incorporated into a revision of this document.

Information in this document is provided in connection with Intel® products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to guidelines and product descriptions at any time, without notice.

This guide may contain errors known as errata. Current characterized errata are available on request.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 5937
Denver, CO 80217-9808

or call in North America 1-800-548-4725, Europe 44-0-1793-431-155, France 44-0-1793-421-777, Germany 44-0-1793-421-333, other Countries 708-296-9333.

† Third-party brands and names are the property of their respective owners.

Copyright © 2000, Intel Corporation. All rights reserved.

Preface

This guide describes connection and mechanical recommendations for all main boards having internal connectors requiring external connection. Recommendations include (among others): front panel I/O header pin-out definition, chassis I/O aperture size, I/O interface board dimensions and main board to front panel board I/O cable shielding and size. Front panel I/O legacy connectors, internal legacy and legacy-free connectors are also addressed. Specific to front panel I/O the goal is for any particular setup of main board, interface board, interface cable and chassis that meets the pinout and physical dimension recommendations of this design guide will be physically compatible with another setup that also meets the requirements of this design guide. Environmental and electrical compatibility testing should be conducted for all designs arising from use of this design guide.

Intended Audience

The guide is intended to provide detailed, technical information to vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	Supporting Documentation
2	Front Panel Legacy I/O
3	Front Panel High Speed Serial Bus
4	Cabling Design Guidelines
5	Interface Board Design Guidelines
6	Chassis and I/O Shield Guidelines
7	Internal Legacy Connectors (Reference)
8	Internal Legacy Free Connectors (Reference)

Typographical Conventions

This section contains information about the conventions used in this guide. Not all of these symbols and abbreviations appear in all guides of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions, which if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the board, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
GB	Gigabyte (1,073,741,824 bytes)
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. All voltages are DC unless otherwise specified.
†	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

1 Supporting Documentation 11
- 1.1 Online Support 11
- 1.2 Design Specifications 12
- 1.3 Recommended Roles for Suppliers 14
  - 1.3.1 Chassis Suppliers 14
  - 1.3.2 Mainboard Suppliers 14
  - 1.3.3 Third-Party Interface Board Suppliers 14

2 Front Panel Legacy I/O 15
- 2.1 Introduction 15
- 2.2 Switch/LED and IR Connectors 15
  - 2.2.1 Usage Models 15
  - 2.2.2 Switch/LED Connector Features 16
  - 2.2.3 IR Connector Features 17
  - 2.2.4 Header Design 17
  - 2.2.5 Pin Assignments 18
- 2.3 Audio Connector 19
  - 2.3.1 Usage Model 19
  - 2.3.2 Features 19
  - 2.3.3 Electrical Considerations 19
  - 2.3.4 Header Design 20
  - 2.3.5 Pin Assignments 20
  - 2.3.6 Jumpers 20

3 Front Panel High Speed Serial Bus 21
- 3.1 Introduction 21
- 3.2 USB Connectors 21
  - 3.2.1 Usage Model 21
  - 3.2.2 Features 21
  - 3.2.3 Header Design 22
  - 3.2.4 Pin Assignments 22
  - 3.2.5 Electrical Considerations 22
- 3.3 IEEE-1394 Connector 24
  - 3.3.1 Usage Model 24
  - 3.3.2 Features 24
  - 3.3.3 Header Design 25
  - 3.3.4 Pin Assignments 25

4 Cabling Design Guidelines 27
- 4.1 Introduction 27
- 4.2 Switch/LED Cable 27
- 4.3 Front Panel Audio Cable 28
  - 4.3.1 Introduction 28
  - 4.3.2 Cable Drawings 28
- 4.4 USB Cabling (Mainboard to Interface Board) 31

4.4.1 Introduction 31
4.4.2 Cable Drawings 32

5 Interface Board Design Guidelines 35

5.1 Introduction 35
5.2 Front Panel I/O Interface Board Dimensions 37

6 Chassis and I/O Shield Guidelines 39

6.1 Introduction 39
6.2 Front Panel I/O Board Placement 39
6.3 Front Panel I/O Reference Designs 42
6.3.1 I/O Shield Reference Design 42
6.3.2 Housing Reference Design 44
6.3.3 Housing and Shield Assembly Reference Design 45
6.3.4 Supporting Structure Reference Design 46
6.3.5 Supporting Structure and Shield Reference Design 47

7 Internal Legacy Connectors (Reference) 49

7.1 Introduction 49
7.2 Serial-WHQL Debug Connector 49
7.3 Parallel Connector 50

8 Internal Legacy Free Connectors (Reference) 53

8.1 Introduction 53
8.2 LPC (Low Pin Count) Debug Connector 53
8.2.1 Usage Model 53
8.2.2 Features 54
8.2.3 Header Design 56
8.2.4 Pin Assignments 58
8.2.5 LPC Debug Connector Pin Assignments 58

Figures

Figure 1. Front Panel Switch/LED and IR Headers 17
Figure 2. Front Panel Audio Header 20
Figure 3. Front Panel USB Connector 22
Figure 4. Front Panel IEEE-1394 Connector 25
Figure 5. Switch/LED Cable 27
Figure 6. Audio Cable Dimensions 28
Figure 7. Audio Cable Cross-section 29
Figure 8. Audio Cable Wiring Diagram 29
Figure 9. Mainboard to Interface Board USB Cable Cross Section 32
Figure 10. Mainboard to Interface Board USB Wiring Diagram 32
Figure 11. Front Panel I/O Aperture and Interface Board Placement Recommendations 35
Figure 12. Front Panel I/O Interface Board Placement Recommendations 36
Figure 13. Front Panel I/O Board Dimensions (Top and Front Views) 38
Figure 14. Front Panel I/O Board Dimensions (Bottom View) 38
Figure 15. Front Panel I/O Aperture and Interface Board Placement Recommendations 41
Figure 16. Front Panel I/O Interface Board Placement Recommendations 41
Figure 17. Front Panel I/O Shield Reference Design 42
Figure 18. I/O Shield Reference Design 43
Figure 19. Front Panel I/O Housing Reference Design 44
Figure 20. Front Panel I/O Housing and Shield Assembly Reference Design 45
Figure 21. Front Panel I/O Interface Board Support Structure Reference Design 46
Figure 22. Front Panel I/O Board Support Structure Reference Design 47
Figure 23. LPC Debug Connector Dimensions 56
Figure 24. LPC Debug Connector Hole Layout 57
Figure 25. LPC Debug Connector Keep-Out Zone 57
Figure 26. LPC Debug Connector Pin Numbering 58

Tables

Table 1. Specifications and Design Guidelines 12
Table 2. States for a Single-Color Power LED 16
Table 3. States for a Dual-Color Power LED 16
Table 4. IR Front Panel Electrical Connection 18
Table 5. Switch/LED Front Panel Electrical Connection 18
Table 6. Front Panel Audio Header Signal Names 20
Table 7. Front Panel USB Connector 22
Table 8. Front Panel IEEE-1394 Connector 25
Table 9. Audio Cable and Connector Pin Assignments 29
Table 10. Audio Cable Construction Recommendations 30
Table 11. Additional Audio Cable Recommendations 30
Table 12. Mainboard to Interface Board USB Cable and Connector Pin Assignments 33
Table 13. USB Cable Material List 33
Table 14. USB Cable Recommendations 34
Table 15. Serial Port Internal Connector 49
Table 16. Parallel Port Internal Connector 50
Table 17. Parallel Port Rear Panel Connector (Centronics Standard) 51
Table 18. LPC Debug Connector Part Numbers 56
Table 19. LPC Debug Connector Pin Assignment 58

1 Supporting Documentation

What This Chapter Contains

1.1 Online Support 11
1.2 Design Specifications 12
1.3 Recommended Roles for Suppliers 14

1.1 Online Support

Find information about Intel® mainboards under “Product Info” or “Customer Support” at these World Wide Web sites:
http://www.intel.com/design/motherbd
http://support.intel.com/support/motherboards/desktop

Find “Processor Data Sheets” or information about “Proper Data Access in Systems with Intel® Motherboards” at these World Wide Web sites:
http://www.intel.com/design/litcentr
http://support.intel.com/support/year2000

Find information about the ICH addressing at this World Wide Web site:
http://developer.intel.com/design/chipsets/datashts/

Find information about USB testing and compatibility at this World Wide Web site:
http://www.usb.org

Find information about USB 2.0 that can be downloaded from the USB-IF web site:
http://www.usb.org/developers/usb20.

Find white papers describing the signal quality compliance testing procedures for USB low speed and full speed signaling performed at USB Plugfests are available at:
http://www.usb.org/developers/complian.html#testing.

Find a design guide for integrating a discrete USB 2.0 host controller onto a four-layer desktop mainboard is available at:
http://developer.intel.com/technology/usb/techlit.htm.

1.2 Design Specifications

Table 1 lists the specifications applicable to the signals present on the front panel connectors.

Table 1. Specifications and Design Guidelines

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
AC '97	*Audio Codec '97*	Version 2.1, May 1998, Intel Corporation.	ftp://download.intel.com/ pc-supp/platform/ac97
ACPI	*Advanced Configuration and Power Interface Specification*	Version 2.0, July 27, 2000, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies, LTD, and Toshiba Corporation	http://www.teleport.com/ ~acpi/
APM	*Advanced Power Management BIOS Interface Specification*	Version 1.2, February 1996, Intel Corporation, Microsoft Corporation.	http://www.microsoft.com/ hwdev/busbios/amp_12.htm
ATA-3	*Information Technology - AT Attachment-3 Interface, X3T10/2008D*	Version 6, October 1995, ASC X3T10 Technical Committee	http://www.t13.org
ATAPI	*Information Technology AT Attachment with Packet Interface Extensions T13/1153D*	Version 18, August 19, 1998, Contact: T13 Chair, Seagate Technology	http://www.t13.org
ATX	*ATX Specification*	Version 2.03, February 1997, Intel Corporation.	http://developer.intel.com/ design/motherbd/atx.htm
IEEE† 1394	*IEEE-1394*	08-17-98	http://www.1394ta.org/ Technology/Specifications/ index.htm
OHCI	*OpenHCI Specification*	Release 1.0a 09/14/99 Compaq Computer Corporation Microsoft Corporation National Semiconductor, Inc.	ftp://ftp.compaq.com/pub/su pportinformation/papers/ hcir1_0a.pdf
PC-99	*PC 99 System Design Guideline*	Revision #: 36	http://emsd- rpe.dp.intel.com/files/ Useful%20Docs/ PC%2099%20Specs/ Pc_99_1.pdf

continued

Table 1. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
Plug and Play	*Plug and Play BIOS specification*	Version 1.0a, May 5, 1994, Compaq Computer Corp., Phoenix Technologies Ltd., and Intel Corporation.	http://www.microsoft.com/hwdev/respec/pnpspecs.htm
UHCI	*Universal Host Controller Interface Design Guide*	Version 1.1, March 1996, Intel Corporation.	http://developer.intel.com/design/USB/UHCI11D.htm
USB	*Universal Serial Bus Specification*	Version 1.1, September 23, 1998, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC. (This specification is superseded by the USB 2.0 Specification and should only be used for historical reference.)	http://www.usb.org/developers/docs.html
	Universal Serial Bus Specification	Version 2.0, April 27, 2000 Compaq Computer Corporation, Hewlett-Packard Co., Intel Corporation, Lucent Technologies, Inc, Microsoft Corporation, NEC, and Philips.	http://www.usb.org/developers/usb20
	USB 2.0 Platform Design Guideline	Version 0.9	See below*
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation	http://developer.intel.com/ial/WfM/wfmspecs.htm

* The USB 2.0 Platform Design Guideline, Rev. 0.9 provides guidelines for integrating a discrete USB 2.0 host controller onto a four-layer desktop mainboard. The material covered can be separated into three main categories:

- Board design guidelines
- EMI/ESD guidelines
- Front panel USB guidelines

The USB 2.0 Platform Design Guideline also covers some background information on the routing experiments and testing performed to validate the feasibility of 480 Megabits per second on an actual mainboard. Finally, it contains a design checklist that lists each design recommendation described in the document.

USB 1.1 drop/droop testing is available at: http://www.usb.org/developers/data/dropDroop_99.pdf

USB 1.1 signal quality testing is available at: http://www.usb.org/developers/data/usbsignalquality.pdf

1.3 Recommended Roles for Suppliers

1.3.1 Chassis Suppliers

The chassis supplier should provide the front panel I/O board support structure and attachment screws. Screws may not be necessary if a support structure implementing an I/O board with the "snap-in" feature is used. A filler panel (or panels) to close-up the opening in the chassis and bezel should also be provided in the event that the front panel I/O board feature is not used by a particular customer.

1.3.2 Mainboard Suppliers

The mainboard manufacturer should provide the interface board and the following items:

- Interface cable(s)
- Front panel I/O shield
- Appropriate decorative plastic sticker to cover any unused ports in the I/O shield

The mainboard manufacturer should also test the interface board and cable(s) with the mainboard to ensure compatibility.

1.3.3 Third-Party Interface Board Suppliers

A generic interface board provided by a third-party vendor may not function correctly with a particular mainboard. If a third-party supplier's interface board is to be used, the mainboard manufacturer should conduct testing to ensure the mainboard's compatibility.

2 Front Panel Legacy I/O

What This Chapter Contains

2.1 Introduction 15
2.2 Switch/LED and IR Connectors 15
2.3 Audio Connector 19

2.1 Introduction

This chapter contains feature descriptions of the signals assigned to the 2x3-pin and 2x5-pin front panel I/O connectors. This chapter also contains electrical connection information.

This guide does not specify designs for MIDI and diskette drive connectors. These interface types are stable and are well documented. Furthermore, as legacy reduction progresses, the functions of these connectors will be assumed by newer interfaces such as USB.

⚠ CAUTION

Voltages supplied to the front panel connector such as VCC (+5 V) are not overcurrent protected and should connect only to devices inside the computer's chassis. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by an external device could cause damage to the computer, the interconnecting cable, and the external device itself. It is strongly recommended that power provided to the external connector shall always implement overcurrent protection.

2.2 Switch/LED and IR Connectors

2.2.1 Usage Models

2.2.1.1 Switch/LED Connector

The 2x5-pin front panel connector's design supports the switch/LED compatibility among multiple mainboard-chassis combinations. See Figure 1 for header pin layout and function.

2.2.1.2 IR Connector

Figure 1 also shows the 2x3-pin front panel connector's IrDA† feature that supports wireless line-of-sight peripherals such as remote controls for internal DVD drives, and IR keyboard and mouse devices.

NOTE

The IrDA connector configuration described here may also be used to support consumer IR.

2.2.2 Switch/LED Connector Features

2.2.2.1 Hard Drive Activity LED

Connecting pins 1 and 3 to a front panel mounted LED provides visual indication that data is being read from or written to the hard drive. For the LED to function properly, an IDE drive should be connected to the onboard IDE interface. The LED will also show activity for devices connected to the SCSI (hard drive activity LED) connector.

2.2.2.2 Power / Sleep / Message Waiting LED

Connecting pins 2 and 4 to a single- or dual-color, front panel mounted LED provides power on/off, sleep, and message waiting indication. Table 2 shows the possible states for a single-color LED. Table 3 shows the possible states for a dual-color LED.

2.2.2.3 Reset Switch

Supporting the reset function requires connecting pins 5 and 7 to a momentary-contact switch that is normally open. When the switch is closed, the board resets and runs POST.

2.2.2.4 Power Switch

Supporting the power on/off function requires connecting pins 6 and 8 to a momentary-contact switch that is normally open. The switch should maintain contact for at least 50 ms to signal the power supply to switch on or off. The time requirement is due to internal debounce circuitry. After receiving a power on/off signal, at least two seconds elapses before the power supply recognizes another on/off signal.

Table 2. States for a Single-Color Power LED

LED State	Description	ACPI State
Off	Sleeping or power off (not running)	S1, S3, S5
Steady Green	Running	S0
Blinking Green	Running/message waiting	S0

Table 3. States for a Dual-Color Power LED

LED State	Description	ACPI State
Off	Power off	S5
Steady Green	Running	S0
Blinking Green	Running/message waiting	S0
Steady Yellow	Sleeping	S1, S3
Blinking Yellow	Sleeping/message waiting	S1, S3

NOTE

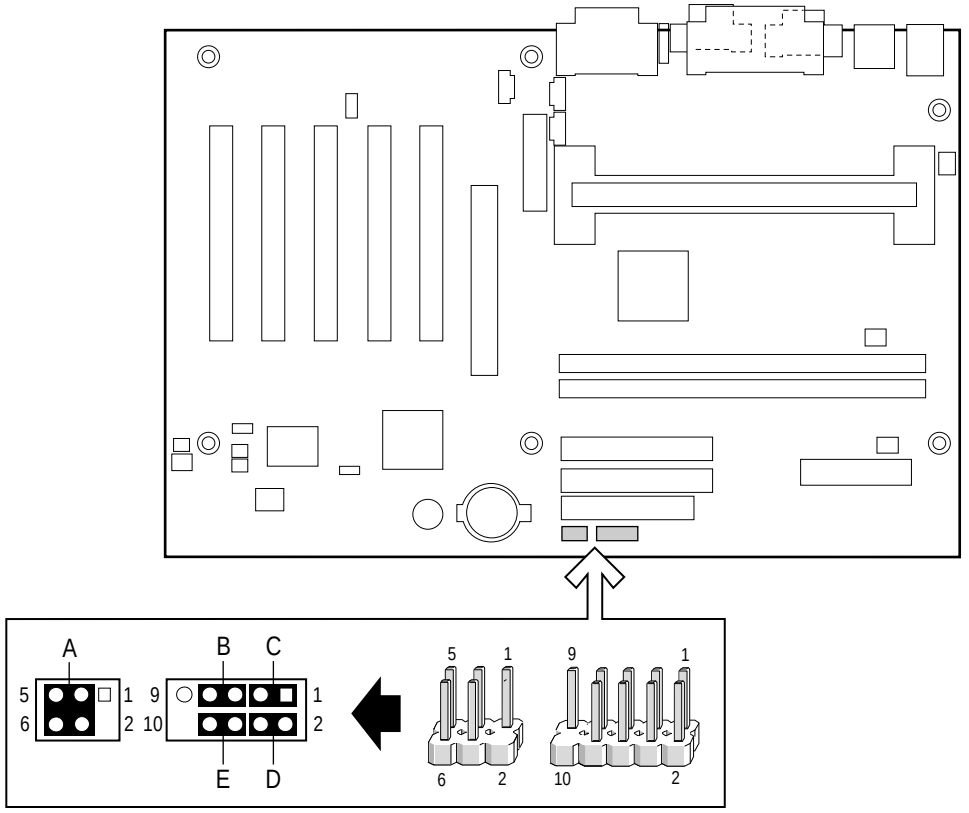
To use the message waiting function, ACPI should be enabled in the operating system and a message-capturing application should be invoked.

2.2.3 IR Connector Features

2.2.3.1 Infrared Port

Serial Port B can be configured to support an IrDA module connected to pins 3, 4, 5, and 6 of the 2x3-pin header connector.

2.2.4 Header Design



Connector Description	Item	Pins	Description
IR Front Panel Connector (see Table 4)	A	3, 4, 5, and 6	Infrared port
Switch/LED Front Panel Connector (see Table 5)	B	5 and 7	Reset switch
	C	1 and 3	Hard drive activity LED
	D	2 and 4	Power / Sleep / Message waiting LED
	E	6 and 8	Power switch

Figure 1. Front Panel Switch/LED and IR Headers

2.2.5 Pin Assignments

Table 4. IR Front Panel Electrical Connection

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
1	Not assigned	N/A	Not assigned	2	(No pin)	N/A	Key
3	+5 V	Out	IR Power	4	GND		Ground
5	IRTX	Out	IrDA serial output	6	IRRX	In	IrDA serial input

Table 5. Switch/LED Front Panel Electrical Connection

Pin	Signal	Description
1	HD_LED_P	Hard disk LED pullup (330 ohm) to +5 V
2	FP PWR/SLP	MSG LED pull-up (330 ohm) to +5 V
3	HD_LED_N	Hard disk active LED
4	FP PWR/SLP	MSG LED pull-up (330 ohm) to +5 V
5	RST_SW_N	Reset Switch low reference pull-down (100 ohm) to GND
6	PWR_SW_P	Power Switch high reference pull-up (10000 ohm) to +5 V
7	RST_SW_P	Reset Switch high reference pull-up (1000 ohm) to +5 V
8	PWR_SW_N	Power Switch high reference pull-down (100 ohm) to GND
9	RSVD_DNU	Reserved. Do not use

2.3 Audio Connector

2.3.1 Usage Model

This connector's design will support standard front panel microphone and headphone usage. The disabling hierarchy included in the design will enable a more intuitive audio usage model without software customization.

2.3.2 Features

The front panel audio connector is designed to support stereo audio output (headphone or amplified speakers) and a microphone input (mono).

The microphone inputs (mono) connect to a 1/8-inch ring-tip-sleeve mini-phone jack mounted on the front panel. The tip provides the Microphone In signal, and the ring provides the Audio Microphone Bias signal.

2.3.3 Electrical Considerations

The two front panel audio output sends (AUD_FPOUT_L and AUD_FPOUT_R) and the two front panel audio returns (AUD_RET_L and AUD_RET_R) connect to a switching-type, 1/8-inch ring-tip-sleeve mini-phone jack mounted on the front panel. The signal path is such that the mainboard output amplifier feeds the front panel jack via the AUD_FPOUT_L and AUD_FPOUT_R.

The signal passes through the front panel jack to the back panel jack via the AUD_RET_L and AUD_RET_R signal when the front panel jack is not in use. When headphones are plugged into the front panel jack, the return signals (AUD_RET_L and AUD_RET_R) that feed that back panel jack are disconnected muting the back panel output.

Note that the mainboard should not leave the back panel signal floating when front panel devices are connected. Allowing the back panel signals to float could result in excessive noise at the back panel jack when the front panel jack is in use.

The mainboard designer should put in weak pulldown on the AUD_RET_L and AUD_RET_R (10 k for example). The designer needs to make sure that these resistors are post output capacitor if using a single supply for the output amplifier. Doing so will avoid loading the amplifier bias down.

NOTE

Use headphones or amplified speakers only on the audio outputs. Poor audio quality may occur if passive (non-amplified) speakers are connected to the output.

2.3.4 Header Design

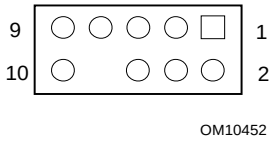


Figure 2. Front Panel Audio Header

2.3.5 Pin Assignments

Table 6. Front Panel Audio Header Signal Names

Pin	Signal Name	Description
1	AUD_MIC	Front Panel Microphone input signal
2	AUD_GND	Ground used by Analog Audio Circuits
3	AUD_MIC_BIAS	Microphone Power
4	AUD_VCC	Filtered +5 V used by Analog Audio Circuits
5	AUD_FPOUT_R	Right Channel Audio signal to Front Panel
6	AUD_RET_R	Right Channel Audio signal Return from Front Panel
7	HP_ON	RSVD for future use to control Headphone Amplifier
8	KEY	No Pin
9	AUD_FPOUT_L	Left Channel Audio signal to Front Panel
10	AUD_RET_L	Left Channel Audio signal Return from Front Panel

2.3.6 Jumpers

A feature of the front panel headphone jack is that rear panel audio output connectors are disabled when headphones are plugged in. This feature is implemented through the front panel audio header shown in Figure 2 and Table 6.

If the front panel interface board is *not* connected to the front panel audio header, pins 5 and 6, and 9 and 10 should be jumpered on the front panel audio header. If these jumpers are not installed, the rear panel audio connectors will be inoperative.

NOTE

Mainboards without a front panel audio header will have 0-ohm resistors installed on the board which duplicate the jumpers.

3 Front Panel High Speed Serial Bus

What This Chapter Contains

3.1 Introduction 21
3.2 USB Connectors 21
3.3 IEEE-1394 Connector 24

3.1 Introduction

This chapter contains electrical connection information for USB and IEEE 1394 front panel high-speed serial bus connectors.

3.2 USB Connectors

The USB 2.0 connector is the same as USB 1.1 connector. The USB 2.0 specification defines a new high-speed transfer rate of 480 Mb/sec., a 40x increase from the 1.1 specification.

3.2.1 Usage Model

Matching PC 99 guidelines, this design allows for a minimum of 2 front panel USB connections for access by frequent hot-plug devices (cameras, game controllers, etc.)

3.2.2 Features

The USB front panel can support multiple USB ports (USBFP_0,1.USBFP_N) that can be routed via a cable to the front panel. Each 2x5 header supports two ports. For an odd number of ports the lower numbered or even port should be enabled, PORT0, 2, 4, etc. In the physical layout where a dual-stack USB connector is used, arranging the ports such that the lower connector is the first Port (0) to be enabled allows for a single-port, single-connector implementation without modifying the electrical design. The connector fully supports UHCI (see Figure 3 and Table 7 for electrical connection information).

USB features include:

- Support for self-identifying peripherals that can be connected or disconnected while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

3.2.3 Header Design

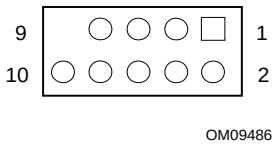


Figure 3. Front Panel USB Connector

3.2.4 Pin Assignments

Table 7. Front Panel USB Connector

Pin	Signal names	Description
1	VREG_FP_USBPWR0	Front Panel USB Power (Ports 0,1)
2	VREG_FP_USBPWR0	Front Panel USB Power (Ports 0,1)
3	USB_FP_P0-	Front Panel USB Port 0 Negative Signal
4	USB_FP_P1-	Front Panel USB Port 1 Negative Signal
5	USB_FP_P0+	Front Panel USB Port 0 Positive Signal
6	USB_FP_P1+	Front Panel USB Port 1 Positive Signal
7	Ground	
8	Ground	
9	Key	
10	USB_FP_OC0	Front Panel USB Overcurrent signal (Ports 0,1)

Note: USB ports may be assigned as needed.

3.2.5 Electrical Considerations

Care should be taken when implementing USB designs such that signal quality and power delivery are not compromised. Certain basic guidelines should be followed. First, there should be only one set of components used to provide fuse protection for the power supplied to the USB connector (see 3.2.5.1). Second, filtering and ESD components should be included (see 3.2.5.3 and 3.2.5.4). Third, front panel and rear panel USB connectors should use separate fuses.

The location of the Front Panel I/O header on the mainboard should take into account the trace lengths on the mainboard and interface board as well as the front panel cable length, otherwise signal quality could be affected. See the most recent USB specification for details and testing information.

3.2.5.1 Fuse Element

Defensive designs should always place the fuse element on the mainboard.

- This protects the mainboard from damage in the case where an unfused front panel cable solution is used.
- This fuse placement also provides some measure of protection from damage if an unkeyed cable is inadvertently plugged onto the front panel USB connector.
- It also provides protection to the mainboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between Vbus and ground.

3.2.5.2 Vbus Bypass Capacitance

Refer to the USB 1.1/2.0 Specifications for the details on the power distribution requirements. Voltage drop and droop testing procedures are also available at:
http://www.usb.org/developers/data/dropDroop_99.pdf

3.2.5.3 Filter Components

Filtering must be carefully addressed in order to enable the system to meet EMC requirements.

3.2.5.4 ESD Components

ESD suppression components should be included to enable the system to meet the applicable ESD requirements.

3.2.5.5 Mainboard Power Requirements

See the most recent USB specification for the voltage and current requirements that must be maintained at the front panel interface board's USB connector.

3.2.5.6 Mainboard Signal Quality Requirements

The signal quality as measured at the USB front panel connectors must meet the requirements given in the most recent USB Specification.

White papers describing the signal quality compliance testing procedures for USB Low Speed and Full Speed signaling performed at USB Plugfests are available. See Section 1.1, page 11 for additional information.

A design guide for integrating a discrete USB 2.0 host controller onto a four-layer desktop mainboard is also available. See Section 1.1, page 11 for additional information.

3.3 IEEE-1394 Connector

3.3.1 Usage Model

IEEE-1394 connectivity allows for data transfer between the PC and consumer electronic devices such as digital cameras and camcorders.

3.3.2 Features

This chapter summarizes the design recommendations for hardware using the IEEE 1394 standards. The IEEE 1394 high-speed serial bus complements USB by providing enhanced PC connectivity for a wide range of devices, including consumer audio/video (A/V) components, storage peripherals, other PCs, and portable devices.

IEEE 1394 has been adopted by the consumer electronics industry and is expected to provide a volume, Plug and Play-compatible expansion interface for the PC.

The 100-Mb/s, 200-Mb/s, and 400-Mb/s transfer rates currently specified in IEEE 1394 are well suited to multi-streaming I/O requirements. Figure 4 and Table 8 show the header and pin assignments.

3.3.2.1 Basic Requirements

The following is a summary of the IEEE 1394 design considerations related to PC systems:

- A front-panel port designed to support the IEEE 1394 standard
- Support for the 1394 Open HCI specification for controllers, specifically OHCI Revision 1.1
- Plug and Play support for device configuration, control and status registers (CSRs), connectors and cabling, and connection fault-handling
- Cable power distribution, including requirements for source devices, sink devices, self-powered devices, and supporting CSRs
- Device power management, CSRs, and soft-power protocols
- Device command protocols for audio, video imaging, still imaging, and storage device classes
- 12 Volt fused supply
- See the latest revision of the IEEE 1394 standard for voltage and current requirements.

3.3.3 Header Design

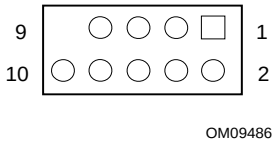


Figure 4. Front Panel IEEE-1394 Connector

3.3.4 Pin Assignments

Table 8. Front Panel IEEE-1394 Connector

Pin	Signal Name	Pin	Signal Name
1	TPA+	2	TPA-
3	Ground	4	Ground
5	TPB+	6	TPB-
7	+12V (Fused)	8	+12V (Fused)
9	Key (no pin)	10	Ground

Note: IEEE-1394 ports may be assigned as needed.

4 Cabling Design Guidelines

What This Chapter Contains

4.1 Introduction 27
4.2 Switch/LED Cable 27
4.3 Front Panel Audio Cable 28
4.4 USB Cabling (Mainboard to Interface Board) 31

4.1 Introduction

This chapter contains reference cable designs for the swith/LED and audio cable that are compatible with the connector pinouts described in chapters 2 and 3.

NOTE

To prevent cable unseating, cables should be secured within the system. Tie wraps and/or sheet metal features could be used to implement this. Cables that are permanently attached to the front panel interface board could also be implemented, however the interface to the mainboard should remain as specified.

4.2 Switch/LED Cable

Figure 5 shows the proper use of the switch/LED header. Great flexibility in cabling is permitted as long as this diagram is followed.

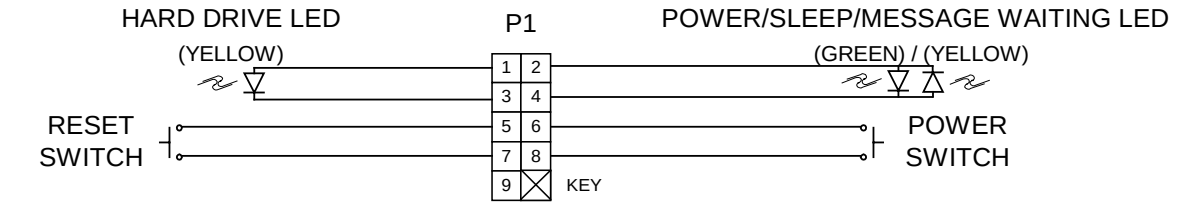


Figure 5. Switch/LED Cable

4.3 Front Panel Audio Cable

4.3.1 Introduction

This section details the design of an audio cable to be used in conjunction with the front panel I/O board.

The shielding in this cable is important to reduce crosstalk, signal degradation, and coupling of electromagnetic interference. The shielding is especially important for the microphone circuit since it is a low-level signal and is very sensitive to noise.

The suggested maximum length for this cable is 18 inches as shown in Figure 6. Figure 7 and Figure 8 show the cable shielding details. Table 9 and Table 10 lists the pin assignments and materials list. Table 11 provides additional information for the audio cable.

4.3.2 Cable Drawings

NOTE

Drawings are not shown to scale.

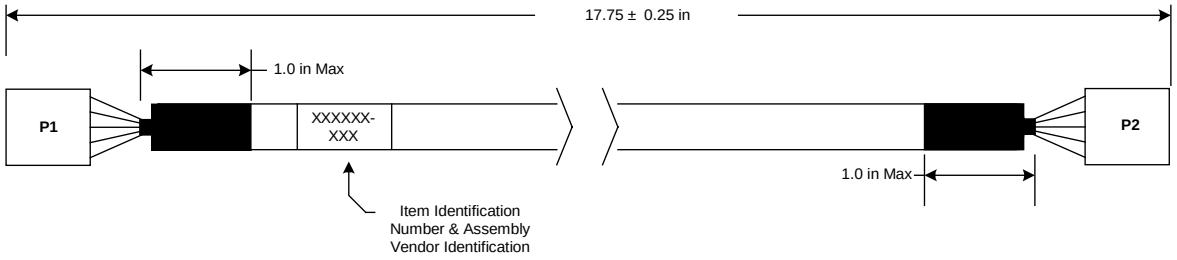


Figure 6. Audio Cable Dimensions

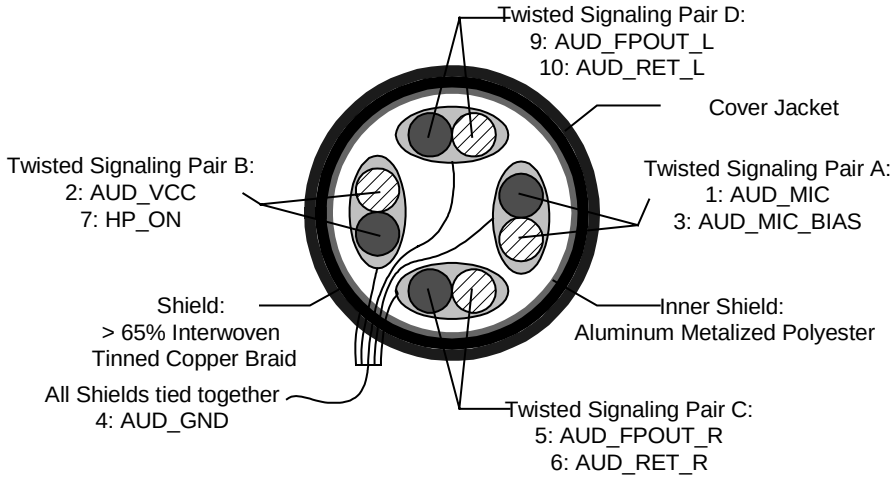


Figure 7. Audio Cable Cross-section

Figure 8. Audio Cable Wiring Diagram

Table 9. Audio Cable and Connector Pin Assignments

Signal	AWG	Pairing	PIN P1 / P2
AUD_MIC	26	A	1 /1
AUD_VCC	26	B	2 /2
AUD_MIC_BIAS	26	A	3 /3
AUD_GND	N/A		4 / 4
AUD_FPOUT_R	26	C	5 / 5
AUD_RET_R	26	C	6 /6
HP_ON	26	B	7 /7
KEY	N/A		8 /8
AUD_FPOUT_L	26	D	9 / 9
AUD_RET_L	26	D	10 /10

Table 10. Audio Cable Construction Recommendations

Part	Qty	Vendor/Part Number*	Material Description*
2X5 Header	2	Berg/65043-032	Header
Key	2	N/A	Key
Heat-Shrink Tubing	As req.	N/A	UL Heat-shrink Tube
26 AWG (4 twisted pair shielded wire)	As req.	N/A	UL Certified Conductor Wire
Part Label	1	N/A	Manufacturer's name and P/N

* Or approved equivalent.

Table 11. Additional Audio Cable Recommendations

Characteristic	Specification
Flammability Rating	UL-94 VW-1
Insulation Resistance	5000 ohms @ 300 VDC
Temperature Range	- 55 °C to + 80 °C
Withstand Voltage	1000 VDC @ 60 Hz
Plating	Per materials list.
Wire	Per materials list.
Workmanship	Parts shall be uniform in workmanship and appearance. There shall be no excessive nicks, deep scratches, excessive burrs, or defects in materials that may affect the function, serviceability, or appearance of this part. Contact retention equal to or greater than 2.0 oz. per contact, when unmated force: from the proper connector.
Maximum	Insertion Force: 10 pounds per connector.
Dimensioning and Tolerances	Per ANSI Y14.5M unless otherwise noted on drawing.
UL Marking	The cable manufacturer should supply UL recognized cables that are certified under the UL wiring harness program (ZPFW2). The UL recognition mark should be supplied with the smallest container or bundle of cables with each shipment.
Recognition Mark	The UL recognized wire's insulation will have surface printing identifying the style, flammability rating, manufacturer's name, voltage and temperature ratings, along with the UL mark.

4.4 USB Cabling (Mainboard to Interface Board)

4.4.1 Introduction

This chapter provides some details of the design for a front panel USB 1.1 and 2.0 interface cable to be used in conjunction with the front panel I/O interface board and main board. The interface cable must be shielded as specified in Figure 9, for two reasons:

- To ensure the cable data lines meet the required differential characteristic impedance as given in the most recent USB Specification. Cables with an impedance variation outside of the USB Specification limits will degrade signal quality and could cause front panel USB devices to fail to operate reliably.
- To shield the cable from RF emissions inside the chassis. Improperly shielded interface cables can pick up these internally radiated signals and cause the system to fail EMI testing.

Figure 9 and Figure 10 show the recommended USB interface cable shielding details and pin assignments. Pin assignments are further detailed in. The cable materials (including connectors) and construction should enable the system to meet the performance requirements of the most current USB 2.0 Specification and applicable safety and regulatory requirements. Table 13 and Table 14 show some current recommendations regarding cable parts and materials.

The cable length (in combination with the trace lengths on the main board and front panel I/O interface board) must be such that it will satisfy the signal quality requirements (propagation delay, etc.) given in the most recent version of the USB 2.0 Specification.

4.4.2 Cable Drawings

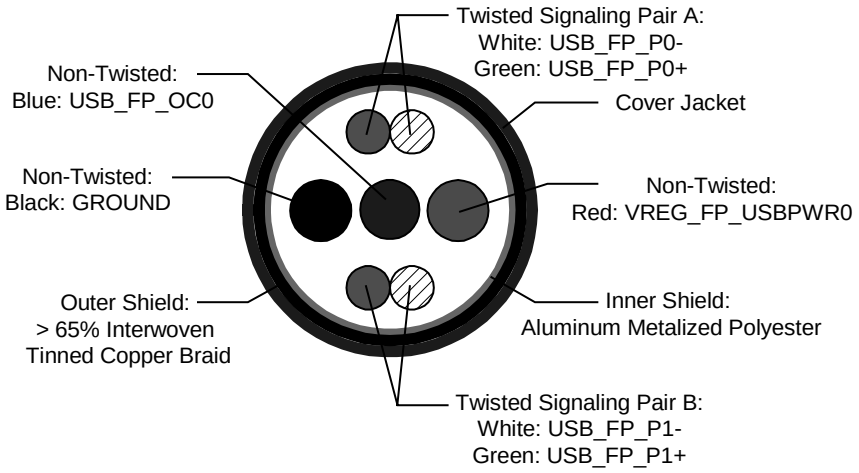


Figure 9. Mainboard to Interface Board USB Cable Cross Section

Figure 10. Mainboard to Interface Board USB Wiring Diagram

Table 12. Mainboard to Interface Board USB Cable and Connector Pin Assignments

Signal	AWG	Color	PIN P1 / P2
VREG_FP_USBPWR0	20	Red	1 /1
UNUSED	N/A	N/A	2 / 2
USB_FP_P0-	28	White	3 / 3
USB_FP_P1-	28	White	4 / 4
USB_FP_P0+	28	Green	5 / 5
USB_FP_P1+	28	Green	6 / 6
GROUND (Shield)	N/A	N/A	7 / 7
GROUND	20	Black	8 / 8
KEY	N/A	N/A	9 /9
USB_FP_OC0	20	Blue	10 / 10

Table 13. USB Cable Material List

Part	Qty	Vendor/Part Number*	Material Description*
2X5 Header	2	Berg/65043-032	Header
Key	2	N/A	Key
Heat-Shrink Tubing	As req.	N/A	UL Heat-shrink Tube
Shield cable consisting of: 2 28 AWG twisted pairs, 3 20 AWG discrete wires	As req.	Sunf Pu/Style 2835	UL Certified Conductor Wire
Part Label	1	N/A	Manufacturers name and P/N

* NOTE: Or approved equivalent.

Table 14. USB Cable Recommendations

Characteristic	Specification
Flammability Rating	UL-94 VW-1
Insulation Resistance	5000 ohms @ 300 VDC
Temperature Range	- 55 °C to + 80 °C
Withstand Voltage	1000 VDC @ 60 Hz
Plating	Per materials list.
Wire	Per materials list.
Workmanship	Parts shall be uniform in workmanship and appearance. There shall be no excessive nicks, deep scratches, excessive burrs, or defects in materials that may affect the function, serviceability, or appearance of this part.
Contact Retention Force	Equal to or greater than 2.0 ounces per contact, when unmated from the proper connector.
Maximum Insertion Force	10 pounds per connector.
Dimensioning and Tolerances	Per ANSI Y14.5M unless otherwise noted on drawing.
UL Marking	The cable manufacturer should supply UL Recognized cables that are certified under the UL wiring harness program (ZPFW2). The UL recognition mark should be supplied with the smallest container or bundle of cables with each shipment. The UL recognized wire's insulation will have surface printing identifying the style, flammability rating, manufacturer's name, operating voltage and temperature ratings, along with the UL recognition mark.

5 Interface Board Design Guidelines

What This Chapter Contains

5.1 Introduction 35
5.2 Front Panel I/O Interface Board Dimensions 37

5.1 Introduction

The following chapter defines the mechanical recommendations of a front-panel interface board. The definition includes physical raw board size, mounting holes, keep-out zones and recommended physical tolerances. A compliant front panel interface board can be used in any chassis design that supports these key features. Figure 11 shows recommended dimensions of the front panel aperture, and interface board placement.

The front panel I/O guideline defines an I/O aperture opening area that is 3.875+/- 0.008 inch (98.43+/- 0.20 mm) wide by 1.000+/- 0.008 inch (25.40+/- 0.20 mm) tall. To retain maximum flexibility, the exact positioning and configuration of the connectors within the I/O connector zone is left to the discretion of the designer. The connectors shown in Figure 11 are a reference design and are shown here only as examples.

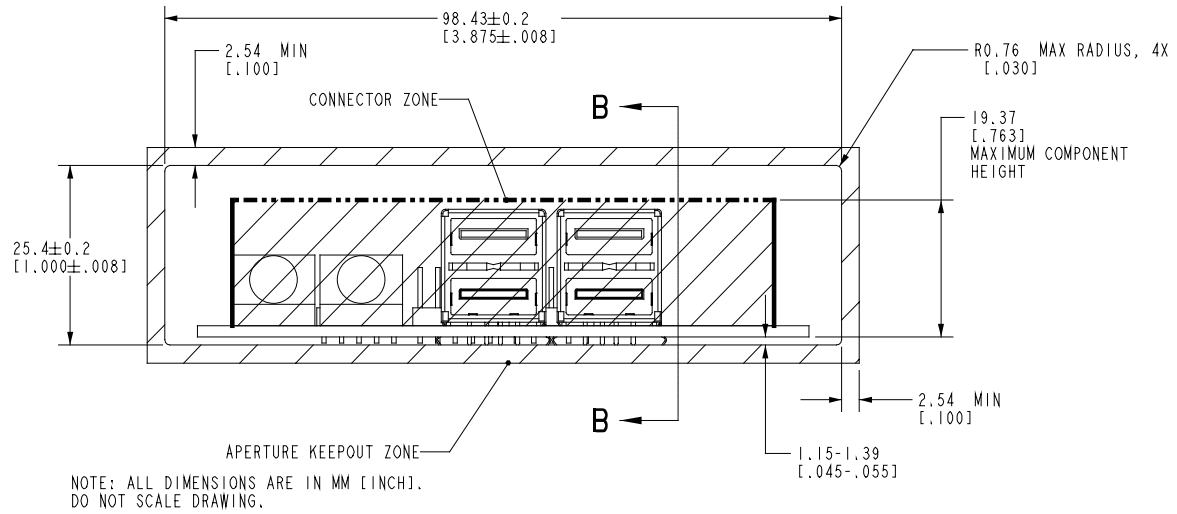


Figure 11. Front Panel I/O Aperture and Interface Board Placement Recommendations

Figure 12 shows the front panel I/O board interface recommendations. The face of the front panel I/O board edge should be placed 0.053 +/- 0.010 inch (1.35+/- 0.25 mm) from the inside of the chassis front panel I/O shield and/or chassis housing. The connectors shown here are only examples.

It is the front panel I/O board designer's responsibility to properly place the connector to meet front panel I/O aperture and interface recommendations. (The front panel I/O shield is not shown.)

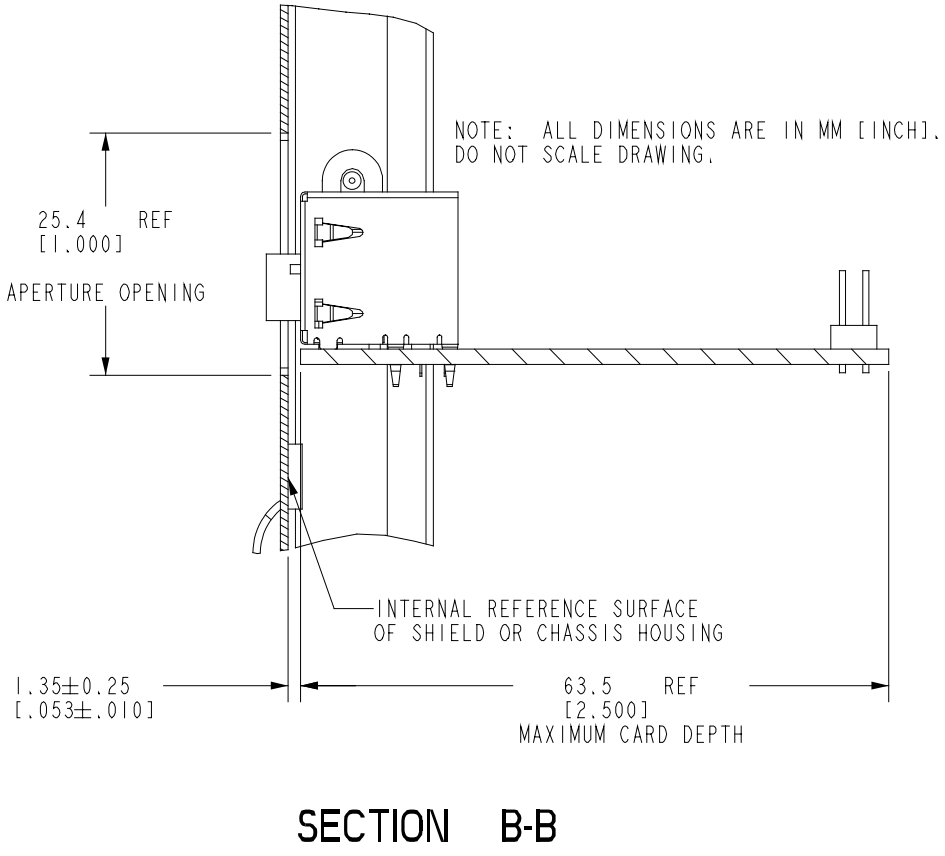


Figure 12. Front Panel I/O Interface Board Placement Recommendations

5.2 Front Panel I/O Interface Board Dimensions

The front panel I/O interface board guideline defines an I/O aperture opening area that is 3.875 +/- 0.008 inch (98.43 6 0.20 mm) wide by 1.000 6 0.008 inch (25.40 +/- 0.20 mm) tall. This area allows the use of stacked connectors on the board to maximize the amount of available I/O space.

As shown in Figure 13 and Figure 14, the front panel I/O board guideline defines several keep-out zones that are necessary for chassis interface features. A typical, 0.062-inch (1.57 mm) thick board has a 0.100 to 0.108-inch (2.5 to 2.7 mm) keepout zone defined around the perimeter of the board, and on both sides of the board. The keep-out zones provide reserved areas that can be used to interface with a chassis-dependent front I/O housing or supporting structures. The keep-out zones should be used as ground contact areas to increase ground return for EMI attenuation.

No components, connectors or other features should be placed within the keepout zones. The maximum component height on the primary component side of the board (including board thickness) is not to exceed 0.763 in. (19.37 mm). The maximum component height on the secondary side of the board is not to exceed 0.043 inches (1.09 mm). If the keepout zones are violated, the board forfeits compatibility with the front panel I/O board-compliant chassis as detailed in Figure 11 and Figure 12.

As shown in Figure 13 and Figure 14, the front panel I/O board guideline defines a board width of 3.500 +/- 0.008 in. (88.90 +/- 0.20 mm), a minimum board depth of 1.500 inches (38.10 mm) and a maximum board depth of 2.500 inches (63.50 mm). This variable board depth is intended to retain flexibility for present and future technologies.

For the best EMI attenuation and proper grounding performance, board connector placement should be limited as shown in Figure 11 and Figure 12 to allow enough clearance between the connectors and the chassis opening for the I/O shield and/or front I/O housing structures. The indented notches provided in the board definition may be used for a screw-less and/or clip retention method.

Refer to Figure 13 and Figure 14 for other front panel I/O board dimension and tolerance recommendations. The connectors shown here are only examples.

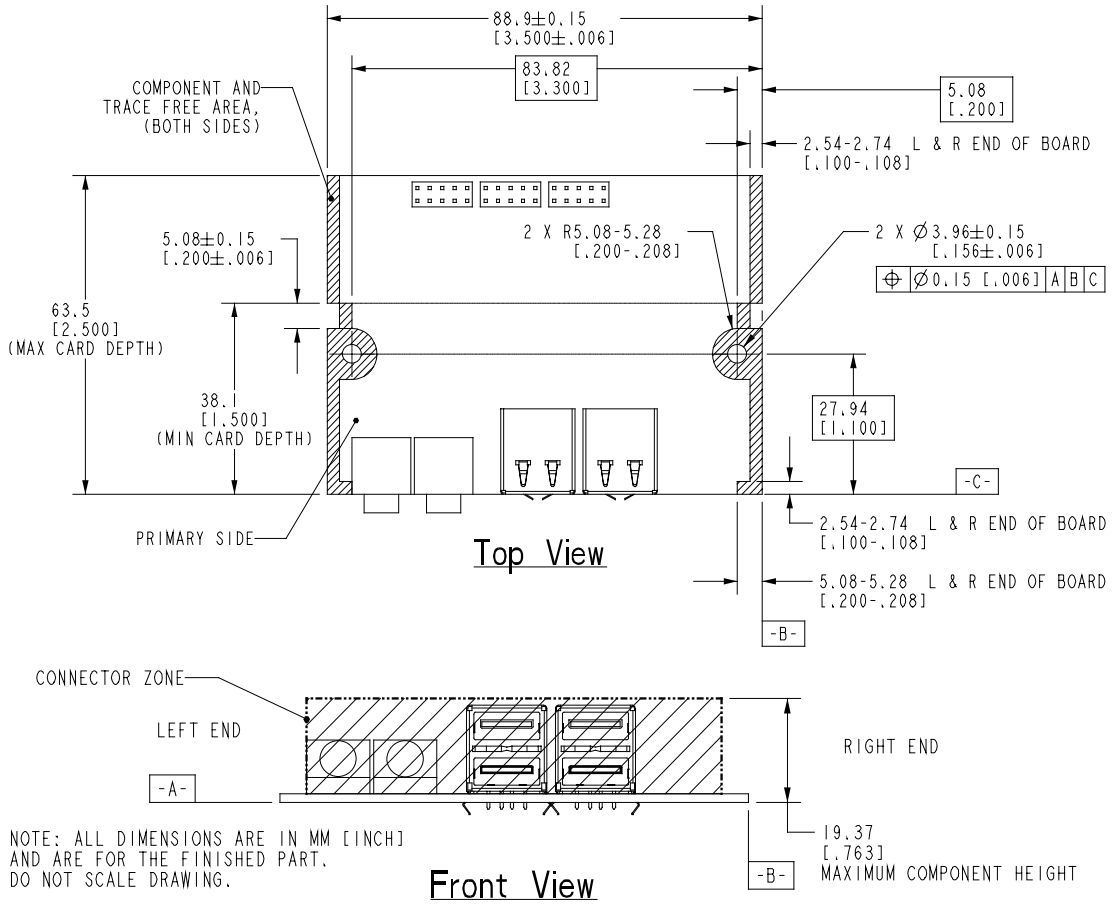


Figure 13. Front Panel I/O Board Dimensions (Top and Front Views)

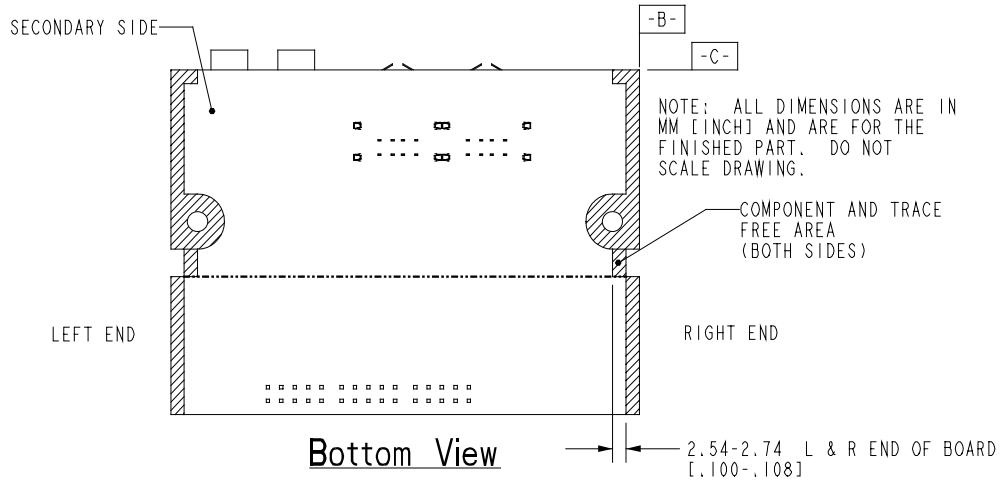


Figure 14. Front Panel I/O Board Dimensions (Bottom View)

6 Chassis and I/O Shield Guidelines

What This Chapter Contains

6.1 Introduction 39
6.2 Front Panel I/O Board Placement 39
6.3 Front Panel I/O Reference Designs 42

6.1 Introduction

This chapter defines the chassis and I/O shield mechanical guidelines for the front panel I/O interface. Typical chassis interfaces should adhere to the definitions of the front panel I/O board's keep-out zones, and mounting hole recommendations. Compliant front panel chassis interface boards can be used in any chassis design that supports these key features.

Beyond the specific aperture opening and keep-out zones, the chassis and bezel implementation of the front panel I/O board is not limited to specific features or locations.

NOTE

Figure 11 and Figure 12 are repeated as Figure 15 and Figure 16 in this chapter for convenience only.

6.2 Front Panel I/O Board Placement

The exact location of the front panel I/O board is not specified. It is recommended that it be placed in the front of the system in either a horizontal or a vertical orientation. When placing the front panel I/O board, the designer should consider that the proper clearance should be provided for the chassis peripheral bays and mainboard keepout recommendations. The system designer should also take into consideration impact to system front airflow, venting, and full-length add-in board retention features.

As shown in Figure 15, the bottom of the front panel opening is located 0.045 to 0.055 inches (1.15 to 1.39 mm) below the bottom of a typical, 0.062 inches (1.57 mm) thick board. Also, a 0.1 inches (2.54 mm) minimum keepout zone has been defined around the perimeter of the aperture area, on both inside and outside surfaces of the chassis front panel. The keepout zone provides a reserved space that can be used to attach a chassis-independent front I/O shield into the chassis front panel. No slots, tabs, notches, or other topographical features should be placed within the keepout zone. Interface board connector placement should be limited as shown in Figure 15 and Figure 16 to allow enough clearance between the connectors and the chassis opening for the I/O shield.

It is strongly recommended for the best EMI attenuation performance, paint should not be applied within the 0.1 inches (2.54 mm) minimum keepout zone on the inside and outside surfaces of the chassis front panel (Figure 15). Paint can prevent proper grounding of the I/O shield to the front chassis panel. The list below shows some front panel I/O board highlights.

- Cutout size = 3.875 +/- 0.008 inches (98.43 +/- 0.20 mm) wide by 1.00 +/- 0.008 inches (25.4 +/- 0.20 mm) tall. See Figure 15.
- Distance from bottom of typical 0.062 inches (1.57 mm) thick board to bottom of I/O cutout hole = 0.045 to 0.055 inches (1.14 to 1.39 mm). See Figure 15.
- Allowable thickness of the chassis front panel that the I/O shield can clip into is in the range 0.030 inches (0.76 mm) to 0.052 inches (1.32 mm).

The interface board's width is 3.500 +/- 0.008 inches (88.90 +/- 0.20 mm), its minimum depth is 1.500 inches (38.10 mm), and its maximum depth is 2.500 inches (63.50 mm), see Figure 13 and Figure 14.

- The corners of the I/O aperture can be rounded to a maximum radius of 0.030 inches (0.76 mm) as shown in Figure 15. This allowable rounding of the corners helps chassis manufactures extend the life of their hard tooling while still complying with this guide.
- The 0.1 inches (2.5 mm) minimum keepout zone around the I/O aperture area is used in a front panel I/O interface board compliant chassis (see Figure 15). This allows front panel I/O interface board- compliant I/O shields to fit into front panel I/O interface board compliant chassis. The keepout area is used for the shield attachment points. Avoid paint application in the area.
- The face of the Front Panel I/O board edge should be placed 0.053 +/- 0.010 inches (1.35 +/- 0.25 mm) from the inside of the chassis front panel I/O shield and/or chassis housing, as defined in Figure 16.
- Chassis manufactures are not limited to an I/O shield implementation only. As long as the chassis manufacturers comply with the definitions of this guide, they may choose to have alternate methods of implementation, i.e., I/O shield or chassis dependent housing.

Figure 15 and Figure 16 detail the I/O connector zone. Compliance with this recommendation is necessary to ensure enough clearance between the chassis aperture and the front panel I/O interface board connectors for the I/O shield structure. This recommendation may be waived if the shield provided with the board requires less than the recommended clearance. It is recommended that system designers implement a universal design that would support a standard front panel I/O aperture opening, as shown in Figure 15. To retain maximum flexibility, the exact positioning and configuration of the connectors within the I/O connector zone is left to the discretion of the designer. Connectors shown in Figure 15 are a reference design and are shown here only as an example. Though it is not recommended for reasons of flexibility, a system designer may choose to implement an integrated chassis housing and I/O shield to support and secure the front panel I/O interface board. Then a supplied I/O shield may not be required.

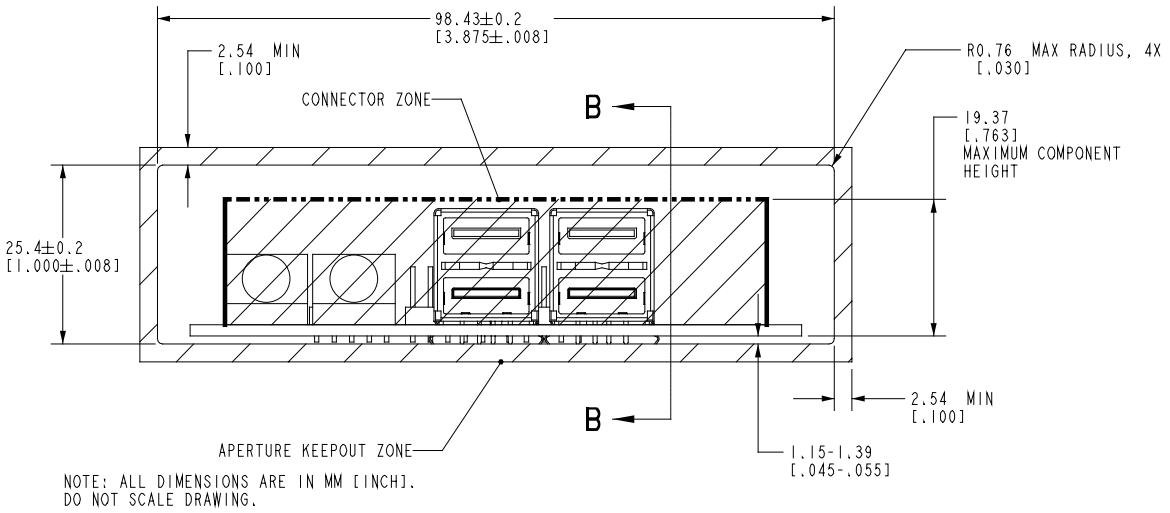


Figure 15. Front Panel I/O Aperture and Interface Board Placement Recommendations

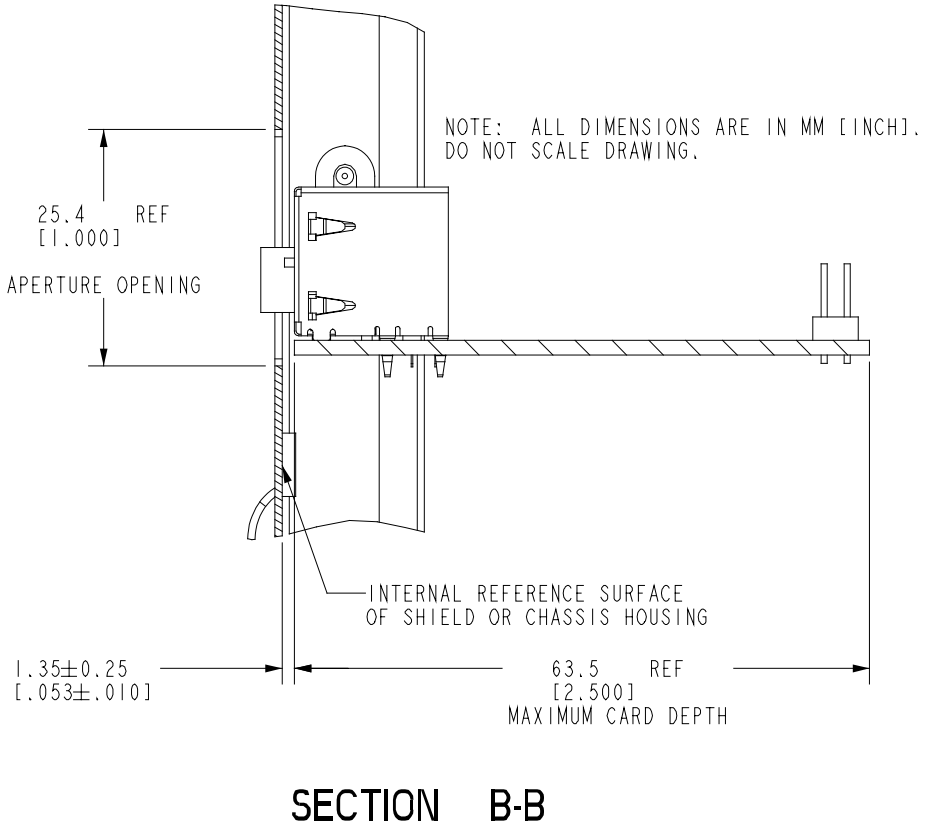


Figure 16. Front Panel I/O Interface Board Placement Recommendations

6.3 Front Panel I/O Reference Designs

Figure 17 through Figure 22 show several front panel I/O reference designs and implementations. Additional connectors could be added if desired. These reference designs are only examples. The front panel I/O interface board guide allows flexibility in the layout of the front panel I/O connectors within the connector zone.

6.3.1 I/O Shield Reference Design

Figure 17 shows an example of a standard front panel I/O shield. A standard shield may accommodate a complete connector layout to support several interface board definitions or stuffing options. Multiple label designs could then be used to fit within the face of the shield to accommodate board-specific layouts (label not shown).

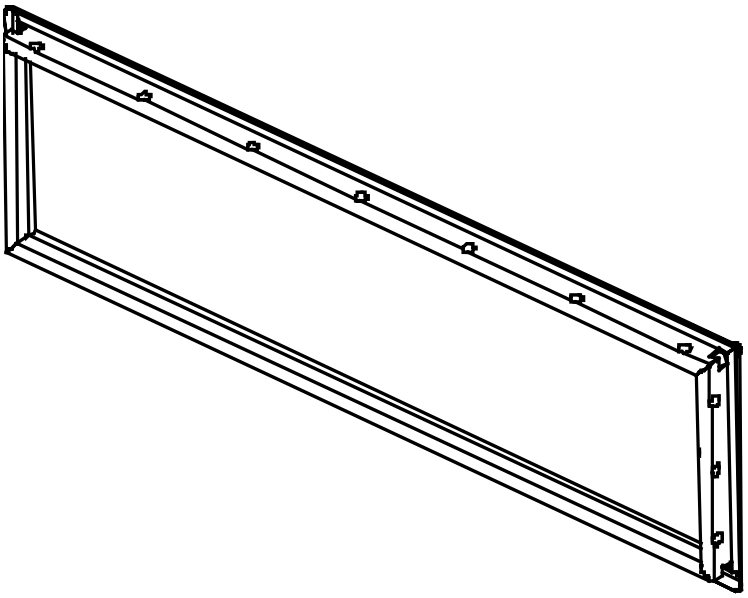


Figure 17. Front Panel I/O Shield Reference Design

Figure 18 shows an example of a standard I/O shield reference design. It is provided here as only a reference for key features that may be used to design and secure front panel I/O shields into a standard front panel I/O aperture opening. See Figure 11 and Figure 12 for recommended dimensions of the front panel aperture and interface board placement.

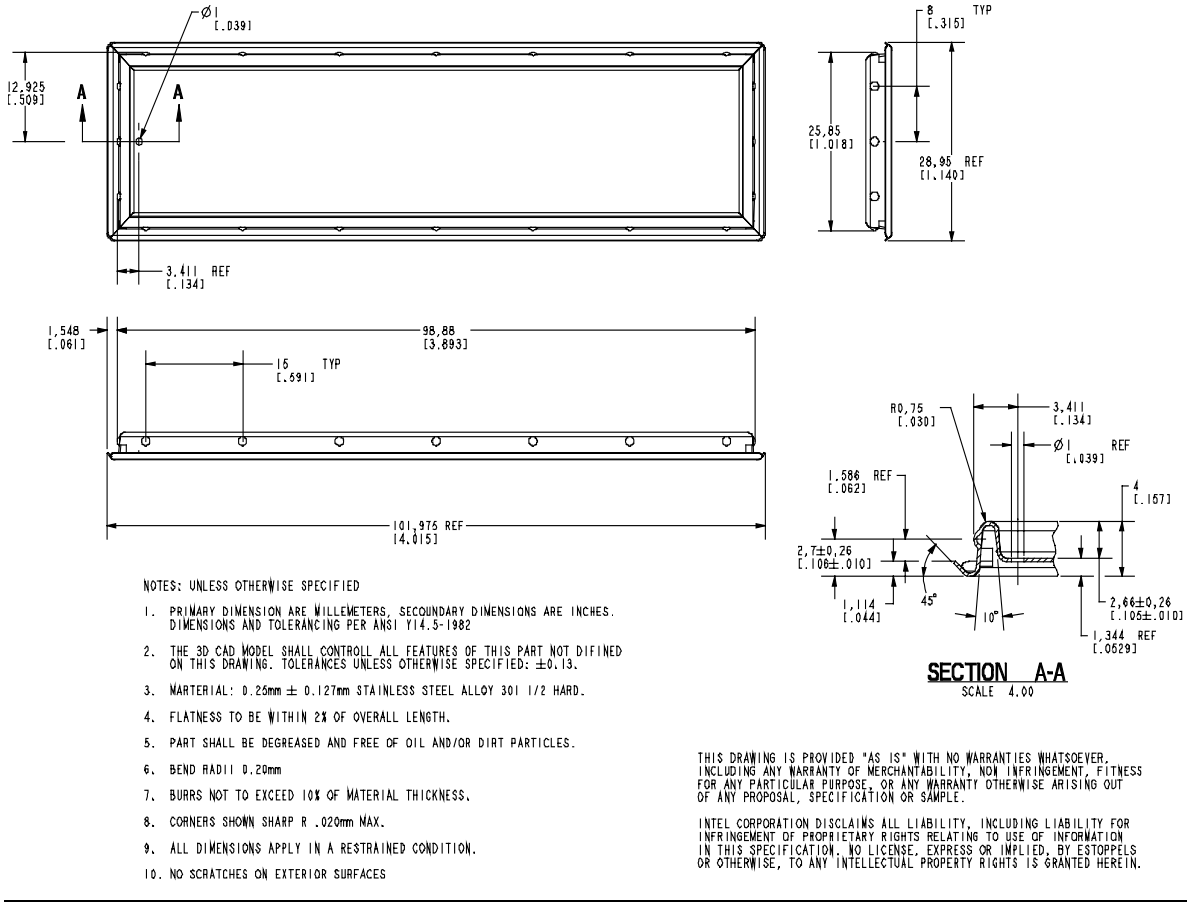


Figure 18. I/O Shield Reference Design

6.3.2 Housing Reference Design

Figure 19 shows an example of a chassis-dependant housing, featuring a standard front panel I/O aperture opening. The housing would support any board, shield, and specific label combination.

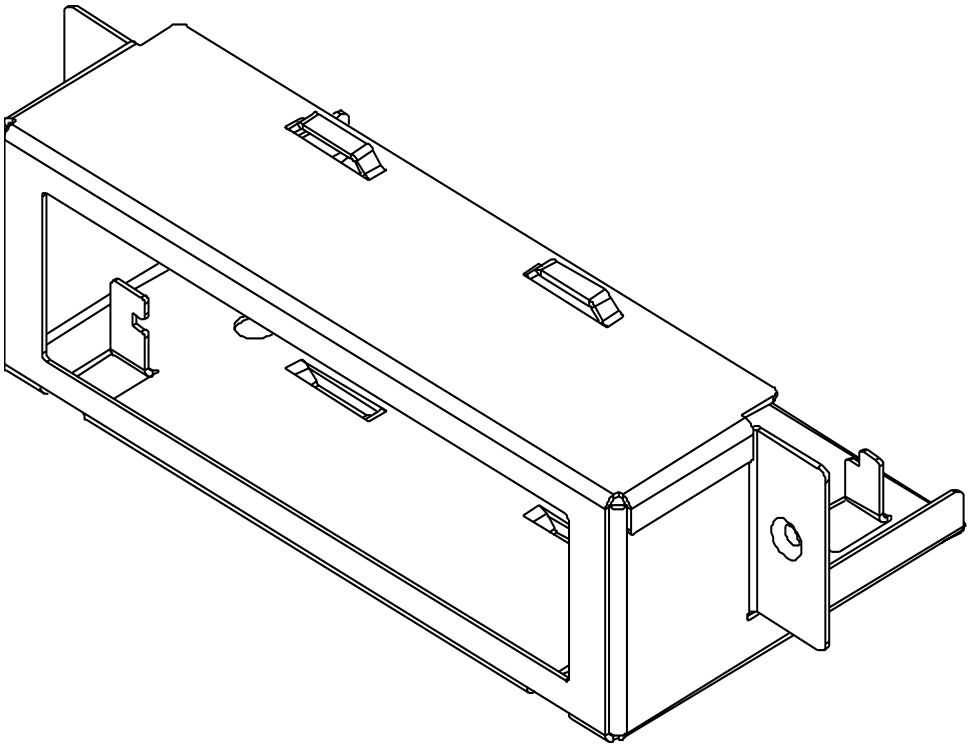


Figure 19. Front Panel I/O Housing Reference Design

6.3.3 Housing and Shield Assembly Reference Design

Figure 20 shows an example of a chassis-dependant housing assembly with standard front panel I/O board and shield. The label is not shown in this example.

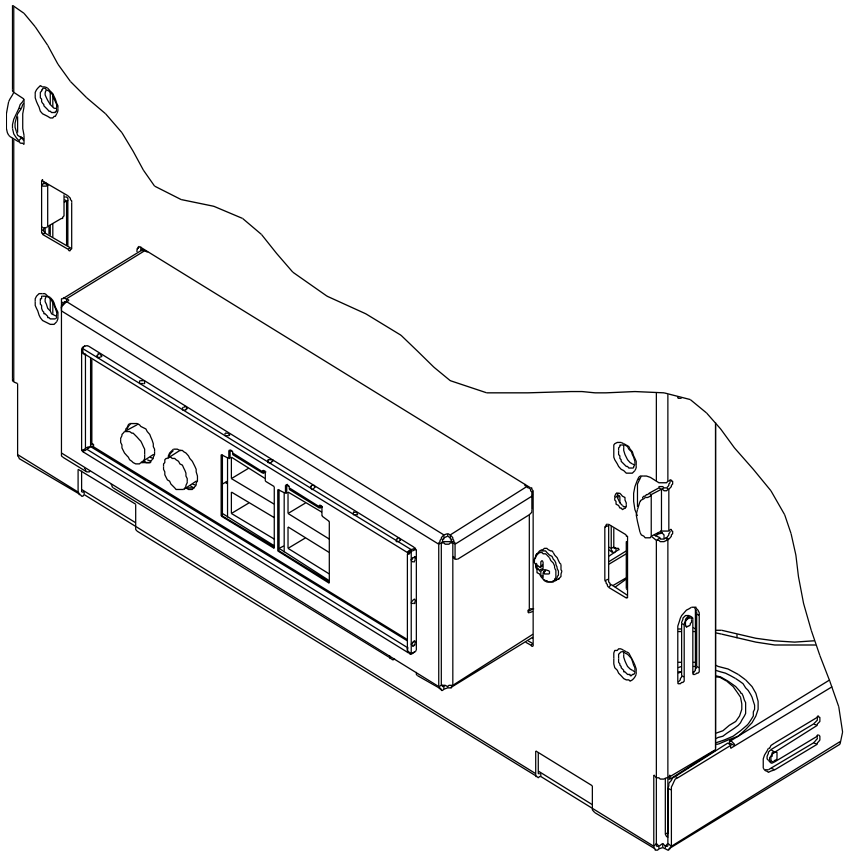


Figure 20. Front Panel I/O Housing and Shield Assembly Reference Design

6.3.4 Supporting Structure Reference Design

Figure 21 shows an example of a chassis-dependant support structure, which should be used in conjunction with a standard front panel I/O shield.

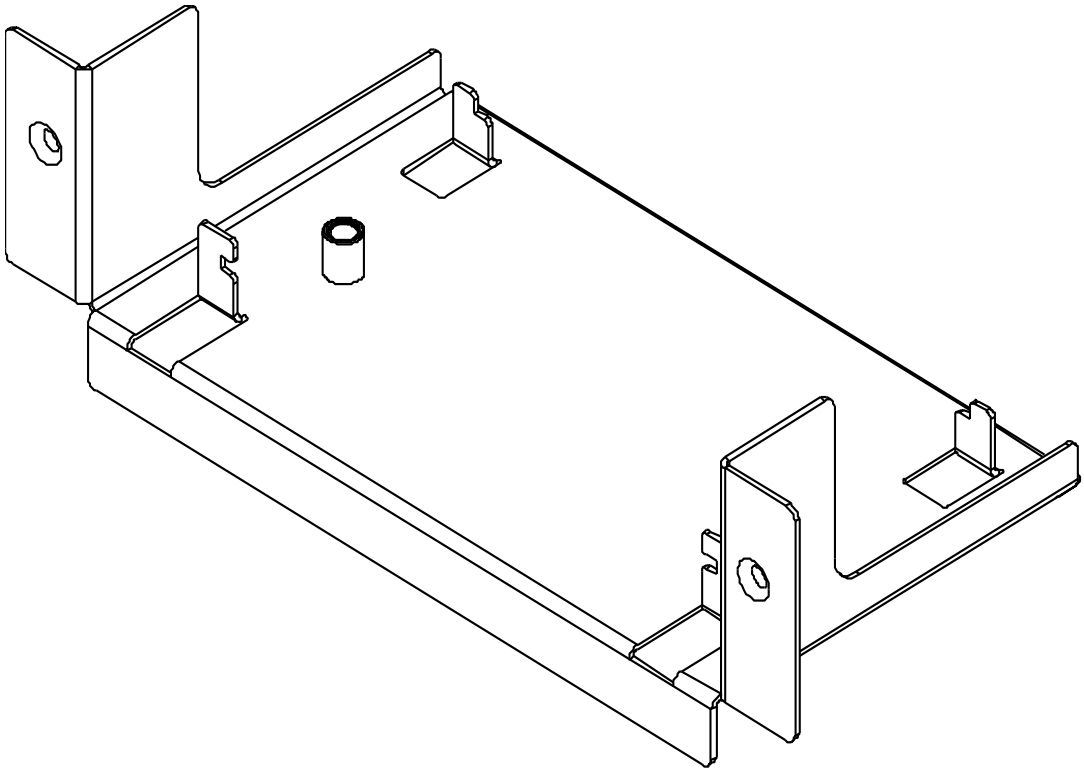


Figure 21. Front Panel I/O Interface Board Support Structure Reference Design

6.3.5 Supporting Structure and Shield Reference Design

Figure 22 shows an example of a chassis-dependant support structure and a standard front panel I/O shield assembled into a chassis front panel. This chassis front panel features a standard front panel I/O aperture opening. The support structure would support any front panel I/O interface board, shield, and specific label combination.

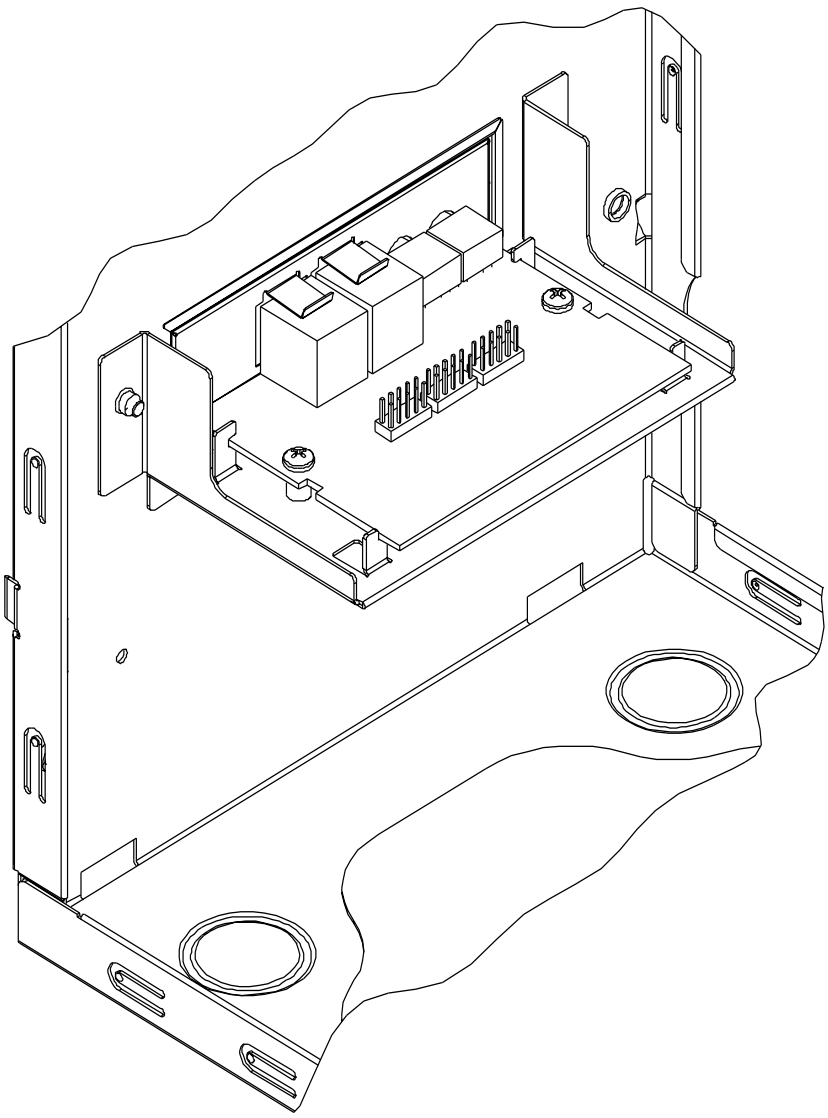


Figure 22. Front Panel I/O Board Support Structure Reference Design

7 Internal Legacy Connectors (Reference)

What This Chapter Contains

7.1 Introduction 49
7.2 Serial-WHQL Debug Connector 49
7.3 Parallel Connector 50

7.1 Introduction

This chapter contains feature descriptions of the signals assigned to the internal legacy connectors. This chapter also contains electrical connection information.

7.2 Serial-WHQL Debug Connector

The serial-WHQL debug connector is an internal 9-pin serial port the pinout for which is shown in Table 15. The port's NS16C550-compatible UART supports data transfers at speeds up to 115.2 kbits/sec with BIOS support. The port can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

Table 15. Serial Port Internal Connector

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	DSR (Data Set Ready)
3	SIN # (Serial Data In)
4	RTS (Request to Send)
5	SOUT # (Serial Data Out)
6	CTS (Clear to Send)
7	DTR (Data Terminal Ready)
8	RI (Ring Indicator)
9	Ground

7.3 Parallel Connector

Internal parallel port connection is made through a 26-pin stake-pin connector located on the mainboard. The pinouts are shown in Table 16 and Table 17.

Table 16. Parallel Port Internal Connector

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name
1	STROBE#	STROBE#	WRITE#
2	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#
3	PD0	PD0	PD0
4	FAULT#	FAULT#, PERIPHREQST#	FAULT#
5	PD1	PD1	PD1
6	INIT#	INIT#, REVERSERQST#	RESET#
7	PD2	PD2	PD2
8	SLCTIN#	SLCTIN#	ADDRSTB#
9	PD3	PD3	PD3
10	GND	GND	GND
11	PD4	PD4	PD4
12	GND	GND	GND
13	PD5	PD5	PD5
14	GND	GND	GND
15	PD6	PD6	PD6
16	GND	GND	GND
17	PD7	PD7	PD7
18	GND	GND	GND
10	ACK#	ACK#	INTR
20	GND	GND	GND
21	BUSY	BUSY#, PERIPHACK	WAIT#
22	GND	GND	GND
23	PERROR	PE, ACKREVERSE#	PE
24	GND	GND	GND
25	SELECT	SELECT	SELECT
26	N.C.	N.C.	N.C.

Table 17. Parallel Port Rear Panel Connector (Centronics Standard)

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name
1	STROBE#	STROBE#	WRITE#
2	PD0	PD0	PD0
3	PD1	PD1	PD1
4	PD2	PD2	PD2
5	PD3	PD3	PD3
6	PD4	PD4	PD4
7	PD5	PD5	PD5
8	PD6	PD6	PD6
9	PD7	PD7	PD7
10	ACK#	ACK#	INTR
11	BUSY	BUSY#, PERIPHACK	WAIT#
12	PERROR	PE, ACKREVERSE#	PE
13	SELECT	SELECT	SELECT
14	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#
16	INIT#	INIT#, REVERSERQST#	RESET#
17	SLCTIN#	SLCTIN#	ADDRSTB#
18 – 25	GND	GND	GND

8 Internal Legacy Free Connectors (Reference)

What This Chapter Contains

8.1 Introduction 53
8.2 LPC (Low Pin Count) Debug Connector 53

8.1 Introduction

This chapter contains feature descriptions of the signals assigned to the internal connectors found on legacy-free and legacy-reduced PC's. This chapter also contains electrical connection information.

8.2 LPC (Low Pin Count) Debug Connector

The PC-AT serial COM port has been used previously by low level debuggers (such as operating system KERNAL debuggers) as the connection point between the PC under test and the debugger console. Since the PC-AT serial COM port is no longer a feature on legacy-free and legacy-reduced PC's, an LPC debug connector has been introduced for inclusion on main boards to provide the debug interface.

8.2.1 Usage Model

Two types of debug connectors are considered here: the standard Debug Connector (16 pins) and the Debug Connector with Legacy Extension (20 pins).

The 16-pin Debug Connector is intended for systems that will run a legacy-free operating system. It consists of the minimum LPC bus signals, an I2C bus, a mechanical key, power, and ground.

The 20-pin Debug Connector with Legacy Extension is intended for use with both legacy and legacy-free operating systems. It adds the 8042 controller legacy signals (RC# and A20GATE) and a serial interrupt line which is used to route IRQ1 and IRQ12 to the main board. Power is required as follows:

- 5 VDC and 3.3 VDC
- 3.3 VDC (required for the LPC interface and for the serial EEPROM)
- 5 VDC (required for the RS-232C drivers and receivers on the module)

The power pins should be de-coupled with capacitors on both the module and the main board. De-coupling should take place at their respective connectors pins, to provide an AC signal return path for the signals in the connecting cable.

The main board connector is a non-shrouded pin header. The main board connector uses a missing pin at the position labeled KEYWAY to guarantee proper module cable alignment. The receptacle connector on the module cable should have the KEYWAY location plugged to guarantee correct installation.

8.2.2 Features

The following criteria were used to design the LPC debug module of which the LPC debug connector (described here) is a part. The LPC debug module is to:

- Be available on all production hardware which does not include the PC-AT serial COM port
- Use standard interfaces to connect the debug console to the PC under test
- Use a no-silicon design for quick industry enabling
- Not limit the hardware configurations of the PC system under test
- Minimize the processor and memory overhead of the debug data stream of the PC under test
- Be a private resource for the operating system
- Be easily discovered and enumerated by the operating system
- Support one full duplex 57,600 bits per second serial data pipe (minimum)

The module consists of a serial communications port, implemented with a standard 16550 UART register interface. The serial communications port registers are not allowed to appear at a legacy COM port I/O addresses, and should be reported to the operating system using a new ACPI table.

To minimize the impact to the main board, the module interface is placed on the Intel® Low Pin Controller (LPC) interface. Since no LPC 16550 UART is available commercially, an LPC Super I/O device (SIO) should be used to implement the module.

The LPC SIO used should have the following attributes:

- Its registers should be plug and play compatible
- All legacy controllers (including the 8042) and interfaces in the SIO should be hardware disabled following a PCI reset.

An I2C serial EEPROM is provided on the module to provide the BIOS with the information used to configure the COM port in the SIO. This information and method is detailed in the BIOS requirements section of the *Intel® LPC Debug Module Requirements Specification* (v1.0).

Using the serial EEPROM to specify the programming method allows any SIO that meets the above requirements to be used on the debug module. The serial EEPROM can be assigned the I2C addresses: 1010111xb – 1010100xb by the main board. Since only eight, I2C serial EEPROM devices can occupy one SMBUS segment, system designers should insure there is no conflict between the I2C address assigned to the debug module and other Serial EPROM devices in the system.

The serial EEPROM device should be capable of being written for field upgrade support. A jumper on the module for write-enable control is an acceptable way to implement this requirement.

The debug module is defined in such a way that it supports two operating environments:

- Operation with a legacy free OS
- Operation with a legacy OS

Operation with a legacy-free OS is the intended mode of operation of the Debug module.

Operation with a legacy OS may be required to support legacy-free early design validation and manufacturing test flows. Two connector sizes are therefore recommended for the module interface. The smaller connector only supports the debug port function. The larger connector supports the signals needed to have full 8042 controller support: RC#, A20GATE, and SERIRQ.

NOTE

Legacy operation should only be enabled for operation with a legacy OS. This means a BIOS setup option needs to be supported which turns legacy mode on and off. In legacy operation mode, a PS/2† Keyboard and mouse would need to be attached to the debug module since a legacy-free BIOS is not required to provide USB legacy keyboard emulation. In addition, when operating the module in legacy mode, the COM port should be programmed by the BIOS to operate as COM1.

A null modem cable is required to connect the debug module to the serial port on another PC. The debug module uses a DB9-male connector that is wired in the standard way for a PC serial COM port.

8.2.3 Header Design

8.2.3.1 Module to Mainboard Mechanical Interface

The only mechanical connection between the debug module and the main board is the LPC debug connector. No mechanical guides or retention hardware are required.

8.2.3.2 LPC Debug Connector

The LPC debug connector for desktop systems is a vertical 0.1 inches x 0.1 inches pin header with 16 or 20 pins. Pin 4 is voided to allow keying with the mating cable. The pins are 0.025-inch square posts or a round post with equivalent dimensioning as shown in Table 18 below.

Table 18. LPC Debug Connector Part Numbers

Connector	Header Parameter "A" (inches)	Number of Circuits
Debug	0.70	16
Legacy Extension	0.90	20

The LPC debug connector's physical dimensions are specified in Figure 23 below.

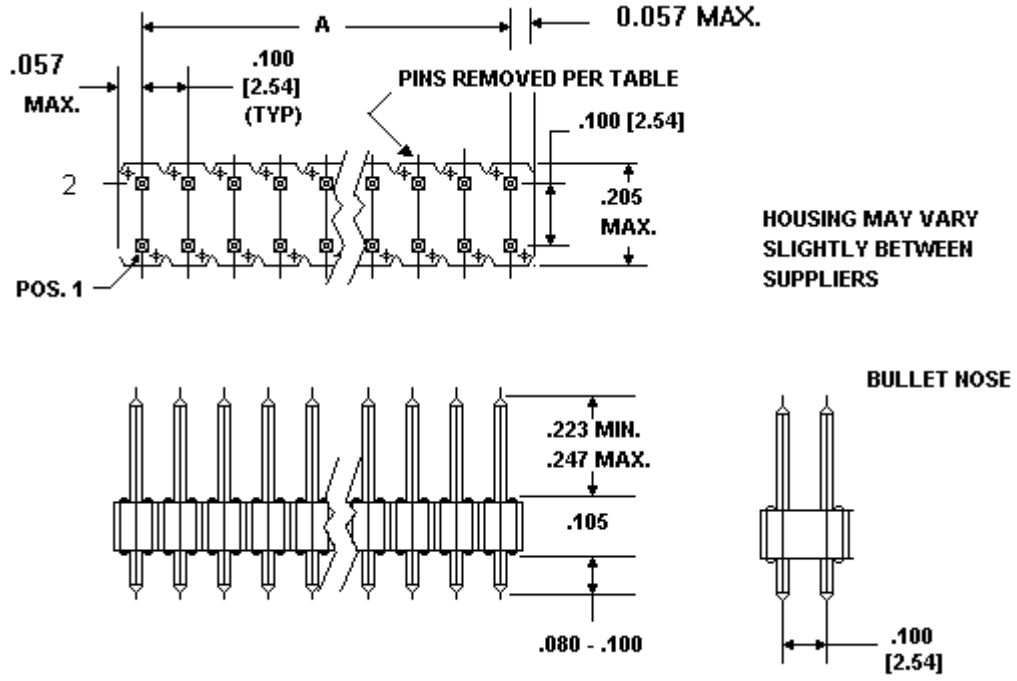


Figure 23. LPC Debug Connector Dimensions

The LPC debug connector's hole pattern is shown in Figure 24 below.

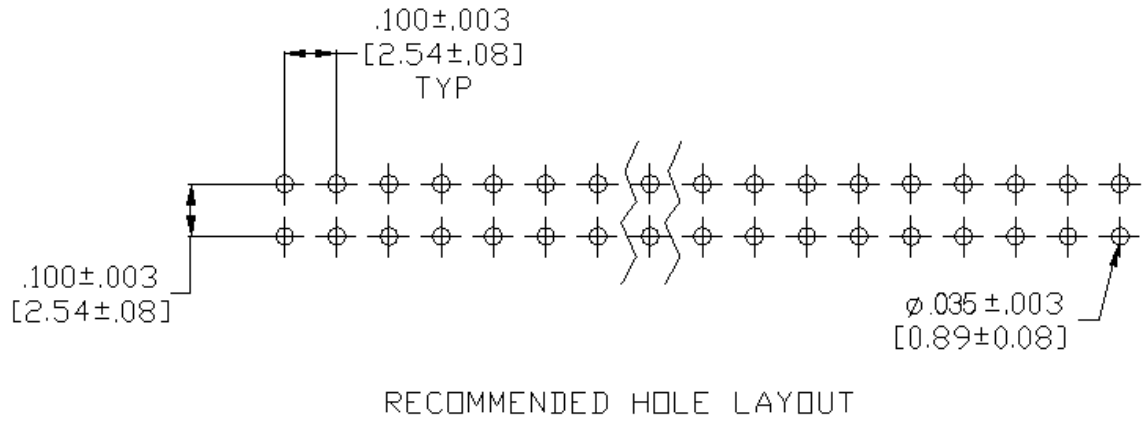


Figure 24. LPC Debug Connector Hole Layout

A physical keep-out around the LPC debug connector should be observed. The keep-out zone is 0.160 inches from the end of the connector hole pattern and 0.080 inches from the side of the connector, measured from the center of any pin. The keep-out is used to allow the cable connector to be attached without interference from adjacent components. The keep-out is shown in Figure 25.

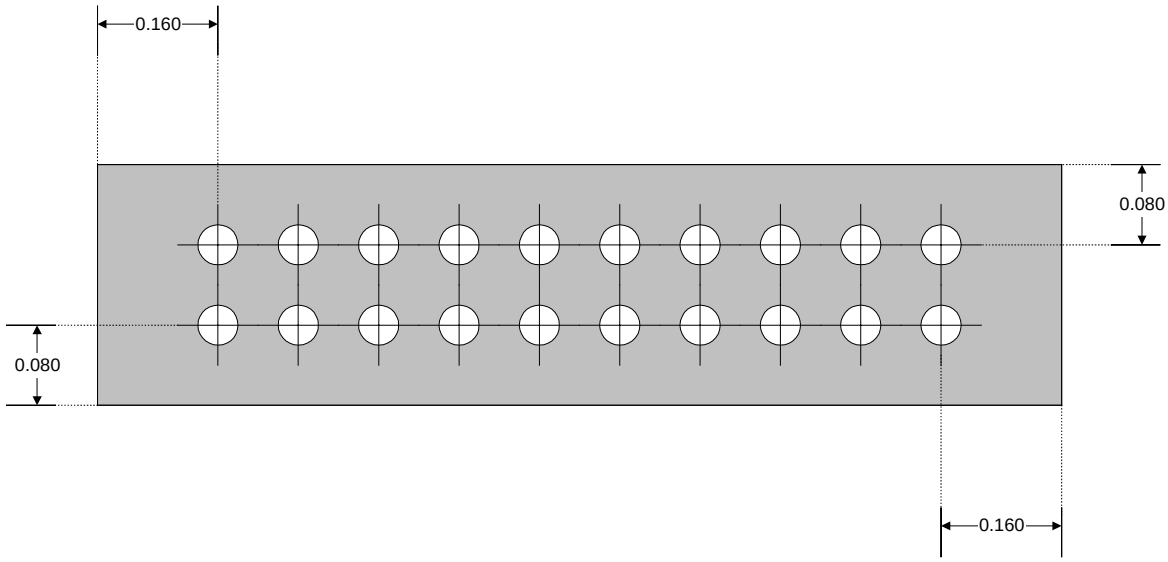


Figure 25. LPC Debug Connector Keep-Out Zone

8.2.4 Pin Assignments

The LPC debug connector's numbering scheme is specified in Figure 26 below.

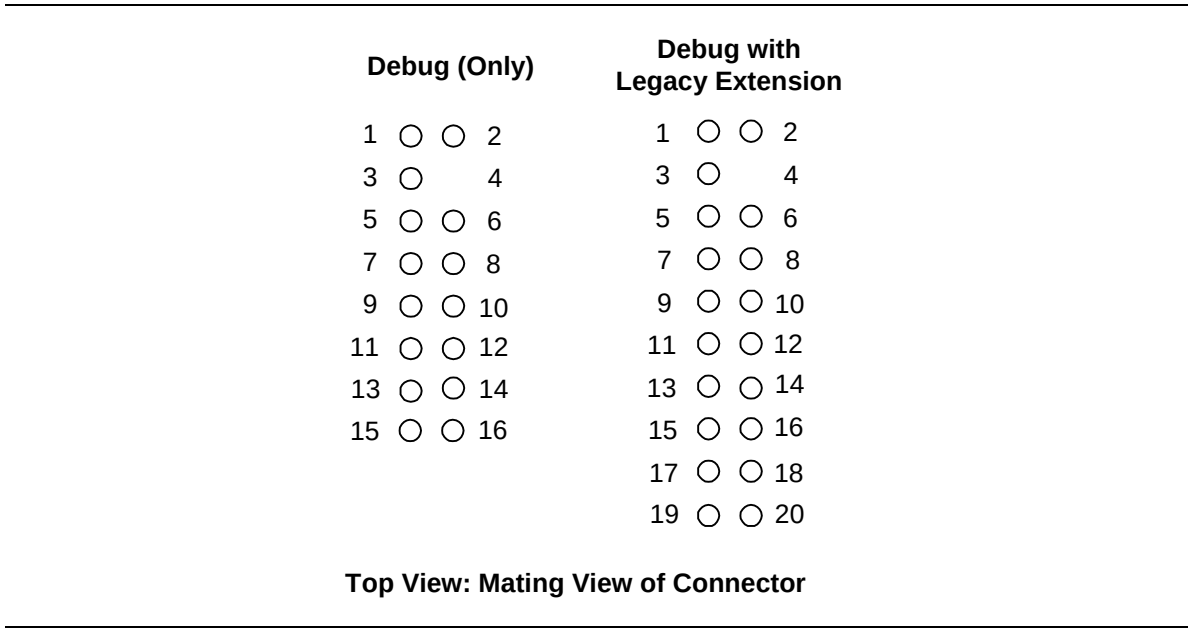


Figure 26. LPC Debug Connector Pin Numbering

8.2.5 LPC Debug Connector Pin Assignments

The pin assignments for the LPC debug connector, and LPC debug connector with legacy extension are shown in Table 19 below.

Table 19. LPC Debug Connector Pin Assignment

Pin	Signal	Pin	Signal	Notes
1	LCLK	2	VSS	Debug (Only)
3	LFRAME#	4	KEYWAY	
5	LRST#	6	VCC5	
7	LAD3#	8	LAD2#	
9	VCC3	10	LAD1#	
11	LAD0#	12	VSS	
13	SCL	14	SDA	
15	SPDA1	16	SPDA0	
17	VSS	18	SERIRQ	Legacy Extension
19	RC#	20	A20GATE	