CHAPTER 1 CODES AND CARRIER OPTIONS

REVISION STATUS

To ensure configuration control, revision status is maintained on each chapter. The following table provides a summary of the revision history.

Title	Revision Letter	Revision Date
Chapter 1 Codes and Carrier Options	B	06/09/04
Chapter 2 Package Design	B	06/09/04
Chapter 3 Board Assembly	A	03/01/03
Chapter 4 Package Materials	B	06/09/04
Chapter 5 Package Characterization	A	03/01/03
Chapter 6 Summary of Packing Quantities	B	06/09/04
Chapter 7 Trays	B	06/09/04
Chapter 8 Tape and Reel	A	08/21/03
Chapter 11 PIBS (Processor in Boxes)	B	06/09/04
Chapter 13 Packing Methods and Labels	B	06/09/04
Chapter 14 Chemical Content of Product carriers and Packing Materials	A	03/01/03

PRODUCT CARRIER OPTIONS

AMD offers several packing systems including package carrier and package carrier and packing container options, for its memory devices. The following table lists those systems that are used as a standard, as well as other options available upon request.

Product Carriers Per Package Type

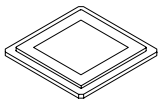
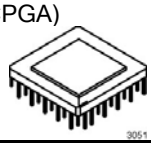
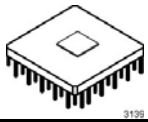
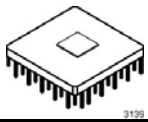
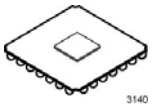
Package type	Ball/Pin Lead Count	Product Carrier	OPN Suffix Code[1]	Packing Container
Ceramic Column Grid Array (CCGA)	All configurations	Standard: Tray	N/A	Tray box
Ceramic Pin Grid Array (CPGA)	All pin counts	Standard: Tray	N/A	Tray box
Ceramic Micro Pin Grid Array (µCPGA)	All pin counts	Standard: Tray	N/A	Tray box
Organic Ball Grid Array (OBGA)	All Configurations	Standard: Tray	N/A	Dry pack & tray box
		Optional: 13" Tape & Reel	\T	Dry pack & reel box
Organic Pin Grid Array (OPGA)	All Configurations	Standard: Tray	N/A	Tray box
Organic Micro Pin Grid Array (µOPGA)	All Configurations	Standard: Tray	N/A	Tray box
Plastic Ball Grid Array (PBGA)	All Configurations Except low profile PBGA packages (Includes all ball counts of BGA, BGD, & BDT)	Standard: Tray (5 trays)	N/A	Dry pack & tray box
		Optional: Tray (1 tray)	\V	Dry pack & reel box
		Optional: 13 Tape & Reel	\T	Dry pack & reel box

Notes:
1. OPN suffix codes designate special pack options that are not AMD's standard method of packing that package and leadcount. (Standard pack methods do not require an OPN suffix, as denoted in the table by N/A.) Special pack option filled on a build-to-order basis only. OPNs for second-source products may or may not use this coding system depending on compatibility requirements with the proprietary source's OPN.

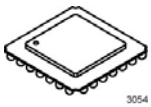
PACKAGE CODES

To utilize AMD's Packages and Packing Methodologies handbook more effectively, the user will need to know the internal package code that applies to the specific AMD processor product. The following two tables – "IC Package Codes" – provide cross-reference matrices between package family types, OPNs, and internal package codes.

AMD's IC Package Codes

Package Family	OPN Package Code[2]	AMD Internal Package Code	Description
Ceramic Column Grid Array Array (CCGA) 	JL	C2F	Flip-chip interconnected; solder column terminals; ceramic interposer; with lid over die
		CCF	Flip-chip interconnected, ceramic column interposer; solder column terminals
Ceramic Pin Grid Array (CPGA) 	HH	CCF	Flip-chip interconnected, square, large outline package; through-hole pins
Ceramic Micro Pin Grid Array (µCPGA) 		CGF	Flip-chip interconnected; through-hole pins
Organic Micro Pin Grid Array (OPGA) 		OGF	Flip-chip interconnected; through-hole pins
Organic Micro Pin Grid Array (µOPGA) 		UOG	Flip-chip interconnected; through-hole pins
Organic Ball Grid Array (OBGA) 	I	OBF	Flip-chip interconnected, organic ball grid array, without lid
	BL	OLF	Flip-chip interconnected, organic ball grid array, without lid

AMD's IC Package Codes (Continued)

Package Family	OPN Package Code[2]	AMD Internal Package Code	Description
Plastic Ball Grid Array (PBGA) 	A	BGA	Wire bonded, die-up package; solder ball terminals
	AA	BGD	Wire bonded, cavity-down package; thermally enhanced with a heat sink; solder ball terminals
	CC	BGT	Wire bonded, cavity-up, thin profile ball grid array package; solder ball terminals
	MB	LBA	Wire bondable rigid substrate, low profile ball grid array package; solder ball terminals; 1.7 mm maximum height, 1.0 mm pitch
	MC	LBB	Wire bondable rigid substrate, low profile ball grid array package; solder ball terminals; 1.7 mm maximum height, 1.0 mm pitch

Notes:

1. All package versions are within JEDEC metric standard unless otherwise noted.
2. These OPN (Ordering Part Number package designators apply to commercial, proprietary product only. OPNs for second-source products may not follow this coding depending on compatibility requirements with the proprietary source's OPN.
3. Mil size refers to the lead-tip-to-lead-tip width of the package when the leads are straightened for insertion into a board or socket. Standard mil sizes per package leadcount are: 8 through 20 lead = 300 mil; 22 lead = 400 mil; 24 through 48 lead = 600 mil; 50 through 64 lead = 900 mil.

AMD's Die and Wafer Package Codes

Device Format	OPN Package Code[1]	AMD Internal Package Code	Description
Die	XG	GDG	Die packed in gel pack
Die	XP	GDP	Die packed in waffle pack
Die	XT	GDT	Die packed in surf tape and reel
Wafer	DW	GDW	Wafer in gel-pack wafer tray

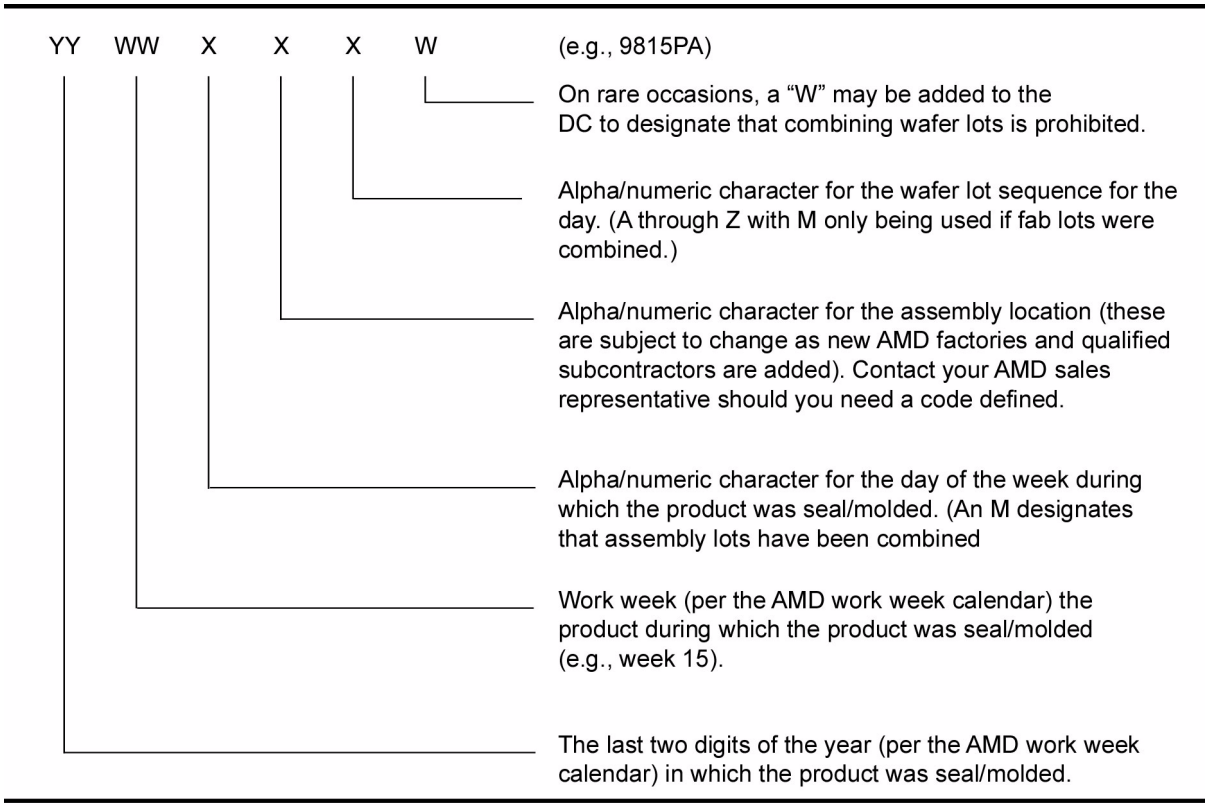
Notes:

1. These OPN (Ordering Part Number) package designators apply to commercial, proprietary product only. OPNs for second -source products may hnot follow this coding depending on compatibility requirements with the proprietary source's OPN.

PRODUCT DATE CODES

Every product AMD manufactures is assigned a product date code, which provides information that allows the product's manufacturing history to be traced. Consistent with the industry, AMD marks the seal date code, which reflects the day when the product was encapsulated (i.e., seal/molded) in an IC package body. The diagram below shows the construction of all product date codes.

Date Code Structure



Note: For some products, an alpha/numeric character may appear one space after the date code to identify the die revision level. Contact your AMD sales representative if you need this code deciphered.

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