CHAPTER 5 PACKAGE CHARACTERIZATION

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INTRODUCTION

With the increased density and complexity of CMOS VLSI semiconductor devices, the need to accurately evaluate the thermal properties of packaged integrated circuits (ICs) is fundamental to the understanding and prediction of device reliability and performance. Inseparably tied to the operating temperature of the device, failure rates increase exponentially as the temperature of the device junction rises. Thus controlling the junction temperature of each IC in the system is imperative in order to attain high reliability and long operating life. Likewise, understanding the thermal properties of each component in the system is important for addressing overall thermal concerns at the system level given the end-use application environment.

Thermal performance data, usually measured in the form of thermal resistance or thermal impedance characteristics ($R\theta_{JA}$, θ_{JA}), is used to estimate the junction temperature of a device operating in a given environment. A certain amount of caution should be exercised, however, when using thermal data to design or evaluate systems because many factors influence the thermal performance of the chip-package combination. These factors include such phenomenon as the ambient temperature, the power dissipation of the chip, the thermal conductivity of the printed circuit board (PCB), the proximity and power dissipation of neighboring devices, and the airflow through the system. Therefore, it is important to carefully evaluate and analyze the entire system and its environment before utilizing any standard thermal data. AMD reports data using the JEDEC JESD51 specification format so the end user can approximate the effect of the application environment.

The following sections detail the methodology and techniques used by AMD to evaluate the thermal performance of its devices, with an emphasis on fundamental heat flow properties. These methods comply with established standards, both government and commercial, and meet or exceed all military specifications for testing and reporting data. AMD's thermal data is collected for still air, moving air, and isothermal case temperature, using measurement techniques that are in conformance with MIL-SPEC-883D, Method 1012.1 specifications. AMD also adheres to the standards for thermal test method, environmental considerations, and mounting surface specification published by the Engineering Industries Association (EIA) and Joint Electronic Devices Engineering Council (JEDEC) as documented in the JESD51 [1] series. AMD is committed to providing current and relevant thermal information for every product it manufactures. In its state-of-the art thermal characterization facility, AMD can evaluate the thermal performance of any of its products. Customers interested in product-specific thermal data should contact an AMD sales representative.

TERMINOLOGY

The most common terminology used in the industry for specifying thermal performance is the θ_{JA} term and related forms. These are used to describe the thermal characteristics of semiconductor devices in various environments, such as natural or forced convection and are also used when simulating an infinite heat sink as in junction-to-case measurements. Recently, a new term was defined to meet the needs of end users of plastic surface-mount packages. Denoted as ψ_{JT} (EIA JEDEC JESD 51_2), this measurement allows a case temperature measurement during thermal test, which can then relate the case temperature in a free convection boundary condition to the junction temperature. The ψ_{JT} parameter also helps to validate junction temperature measurements and calculations during thermal characterization. The terminology commonly used to specify thermal performance is shown in the table *"Thermal Resistance Terminology" on page 5-3*, and mathematical constructs for calculating thermal resistance parameters are provided in *"Sample Calculations: Thermal Resistance" on page 5-5*.

Thermal Resistance Terminology

Term	Definition
θ_{JA}, $R\theta_{JA}$	Thermal resistance from junction to ambient: resistance from the operating portion of a semiconductor device to a natural convection (still air) environment; °C/W.
θ_{JMA}, $R\theta_{JA}$	Thermal resistance from junction to moving air: resistance from the operating portion of a semiconductor device to a forced convection (moving gas) environment surrounding the device; the gas is assumed to be air unless stated otherwise; °C/W.
θ_{JC}, $R\theta_{JC}$	Thermal resistance from junction to case: resistance from the operating portion of a semiconductor device to the outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across the surface; °C/W.
θ_{JR}, $R\theta_{JR}$	Thermal resistance from junction to reference point: resistance from the operating portion of a semiconductor device to a defined reference point within the specified environment surrounding the device; °C/W.
θ_{JX}, $R\theta_{JX}$	Thermal resistance from junction to environment: resistance from the operating portion of a semiconductor device to a defined non-standard environment surrounding the device; °C/W.
θ_{JL}, $R\theta_{JL}$	Thermal resistance from the operating portion of a semiconductor device to a liquid environment surrounding the device; °C/W.
θ_{CA}, $R\theta_{CA}$	Thermal resistance from specified reference location on the case of a semiconductor device to an ambient environment surrounding the device; °C/W.
Ψ_{JT}	Thermal characterization parameter from device junction to the top center of the package surface; °C/W.
T_J	Junction temperature; °C.
T_A	Ambient temperature; °C.
T_C	Case temperature; °C.
T_R	Reference temperature; °C, to standard environment.
T_X	Reference temperature; °C, to non-standard environment.
P_H	Device power dissipation, steady state; Watts.
I_{CC}	Device current supply; Amperes
V_{CC}	Device voltage supply; Volts.
PD	Device power dissipation in watts (V_{CC} x I_{CC}).
K_F	Kfactor; calibration constant for determining the $\Delta T/\Delta V$ relationship of the Thermally Sensitive Device (TSD); °C/mV.
TSD	Thermally sensitive device: usually a semiconductor junction which exhibits a linear relationship to temperature over a given temperature range with a constant current applied; °C/mV.

Note: θ_{JR} is an alternative symbol for $R\theta_{JR}$.

MEASUREMENT METHODS

AMD uses two primary test methods to evaluate the thermal resistance of packaged ICs: the live device method and the thermal test die method. In both methods, a heat source mounted within the package is utilized. For the live device method, the heat source is a thermal test chip.

The live device method provides weighted average values for thermal resistance, and can account for any hot spots or uneven temperature distributions on the die. The thermal test die method is preferred, however, because it enables the power dissipation and die size to be easily controlled. The following sections provide details on these two methods as well as on the calibration process that is required.

Calibration of the Thermally Sensitive Device . When utilizing either the live device method or the thermal test die method, the Thermally Sensitive Device (TSD) must first be calibrated to determine the $\Delta T/\Delta V$ characteristics (i.e., change in temperature over change in voltage). The calibration factor (KF) for the TSD is used to relate the forward voltage of the TSD to a temperature, thereby allowing thermal resistance to be computed using the algorithm (1) provided under *"Sample Calculations: Thermal Resistance" on page 5-5*. The devices under test are calibrated over the temperature range of interest in either a convection type oven or a temperature controlled fluid bath.

Live Device Method. When measuring the thermal characteristics of a live semiconductor device, the device must first be biased to provide the typical power dissipation for that device type and then a TSD must be located on the die to enable the junction temperature to be measured and monitored. The most commonly used TSD is either the substrate isolation diodes or an ESD input protection diode. Substrate diodes are preferred because they provide an array of the intrinsic parasitic diodes inherent in many semiconductor processes. Using input diodes for temperature sensing only gives the temperature information for a small region of the die.

To implement the electrical test method for a live device, the device must first be forward biased, as it is in normal operation, and allowed to dissipate power. Then it must be reverse biased and, at specified intervals (usually within 10 to 40 microseconds from the time power is removed), the TSD must be measured to determine the junction temperature. This is also referred to as the voltage-drop method or the pulse method. The parameter actually measured is the forward voltage drop of a semiconductor junction. The substrate isolation diodes are also electrically in parallel, so the junction temperature recorded is the weighted average of the hottest junction on the die, providing typical worst case values.

Due to the increasing complexity of the silicon, the live device method is less popular and not widely used for high pin-count products. Biasing the die with the correct vectors and signals while switching from the forward- to reverse-bias modes is becoming more difficult, and in some cases impossible.

Thermal Test Die Method. When using the thermal test die method, a specially designed thermal test die is assembled into the IC package. This test die contains a resistive element for power dissipation. Semiconductor junctions (i.e., diodes) are used as TSD to enable the temperatures at various locations on the die to be measured. This method is used primarily to evaluate the thermal resistances of packages, generically, given the range of die sizes appropriate for the module size of the thermal test die (usually 75 to 100 mils). These modules can be arrayed to produce larger die sizes in increments of the unit module (e.g., 100 mils^2, 200 mils^2 , etc.).

The thermal test die method is limited, however, in that it assumes evenly distributed power dissipation across the surface of the die. This typically produces a near-ideal heat source and lower thermal resistance results. Therefore, the die size and temperature distribution of the actual (production) device should be taken in to account when making these types of measurements. The temperature distribution of the production device can be determined by the use of non-contact thermometry methods such as liquid crystal thermography or infrared thermometry. The temperature distribution, assuming typical operating conditions, can then be computed based on evidence of hot spots and the resulting temperature distribution across the die. Based on this analysis, the thermal properties of the production device can be correlated with those obtained with the thermal test die.

Sample Calculations: Thermal Resistance

(Algorithm #)

For calibration of a Thermally Sensitive Device (TSD): (1)

$$K_F = \frac{T_{HI} - T_{LO}}{V_{LO} - V_{HI}}$$

where:

T_{HI} = High calibration temperature
T_{LO} = Low calibration temperature
V_{HI} = High TSD voltage
V_{LO} = Low TSD voltage

Note: This measurement is made at three or more temperatures to validate linearity of the TSD.

For calculating thermal resistance: (2)

$$\theta_{JR} = \frac{T_J - T_R}{P_H}$$

where:

θ_{JR} is the thermal resistance from junction to some specficed reference point for:

θ_{JA} = 2.54 mm below and 150 mm to the side of the device under test
θ_{JMA} = Directly upstream from the device under test
θ_{JC} = Side of the package directly adjacent to the backside of the die

For calculating the relationship between θ_{JA}, θ_{JC}, ***and*** θ_{CA}***:*** (3)

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

For calculating junction temperature: (4)

$$T_J = T_R + (\theta_{JR} \times P_D)$$

where:

T_R = Temperature at some specficed reference point
θ_{JR} = Thermal resistance to some specified reference point, R, °C/W

Thermal characterization parameter, ψ_{JT}***:*** (5)

$$\psi_{JT} = \frac{T_{JSS} - T_{ASS}}{P_H}$$

where:

ψ_{JT} = Thermal characterization parameter from junction to the top surface of package
T_{JSS} = Device junction temperature at steady-state power
T_{ASS} = Top surface of package, at steady-state power, measured by a thermocouple, infrared sensor, or fluoroptic sensor

Thermal characterization parameter, ψ_{TA}***:*** (6)

$$\psi_{TA} = \frac{T_{TSS} - T_{ASS}}{P_H}$$

where:

ψ_{TA} = Thermal characterization parameter from top surface of package to air
T_{TSS} = Temperature of top surface of package, at steady-state power
T_{ASS} = Ambient temperature, at steady-state power

For calculating the relationship between θ_{JA}, ***and*** ψ_{JT}***:*** (7)

$$\theta_{JA} = \psi_{JT} + \psi_{TA}$$

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MEASUREMENT ENVIRONMENTS

When using thermal performance data for semiconductor devices, the effects of the environment on the measured or modeled values must be considered. To simulate the environments that devices will encounter in end-use applications, thermal measurements are taken in still and moving air environments and at the case (or package body) environment.

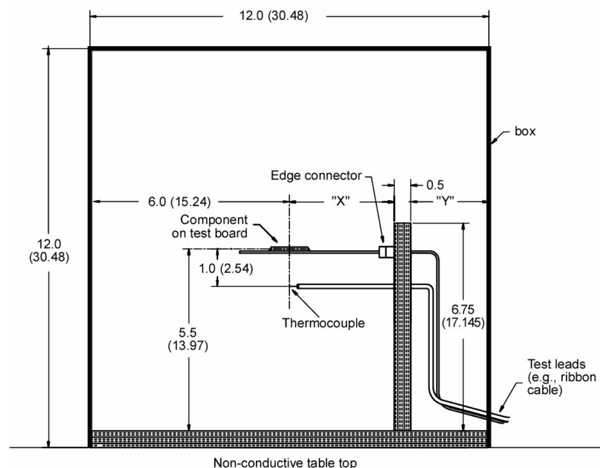


Figure 5.1 Side view of natural convection fixture used for still-air tests.

Natural Convection (Still-Air) Environment. Natural convection measurements (θ_{JA}) are performed in a chamber which encloses one cubic-foot volume of still air. A diagram of a still-air chamber is shown in *Figure 5.1* and *Figure 5.2*. The test board near the device under test is mounted horizontally (or vertically, if requested) in the chamber, and the reference temperatures both inside and outside the chamber are monitored. The device is allowed to come to a steady state thermal condition both before and after heating power is applied.

Forced Convection (Moving-Air) Environment. Forced convection (θ_{JMA}) measurements are performed in a laboratory wind tunnel, a diagram of which is shown in *Figure 5.3 on page 5-7*. The test boards can be mounted vertically or horizontally, depending on the requirement.

Air speeds of 100 to 1200 linear feet per minute (lfpm) are attainable in the tunnel. Air speed is monitored using a hot-wire anemometer, which is mounted on an XYZ stage near the device.

Case Environment. When taking case (θ_{JC}) measurements, a separate apparatus is required for hermetic versus plastic packages. For hermetic packages, a thermoelectric device or cold plate is used to keep the case temperature constant during the measurement process. The package is placed against the cold plate and held in position with an adjustable clamp. A thin layer of thermal grease is used to thermally contact the package to the test fixture. A thermocouple is mounted into the test fixture that comes in contact with the package body to allow case temperature measurements. Fixtures for junction-to-case measurements are customized for each package style.

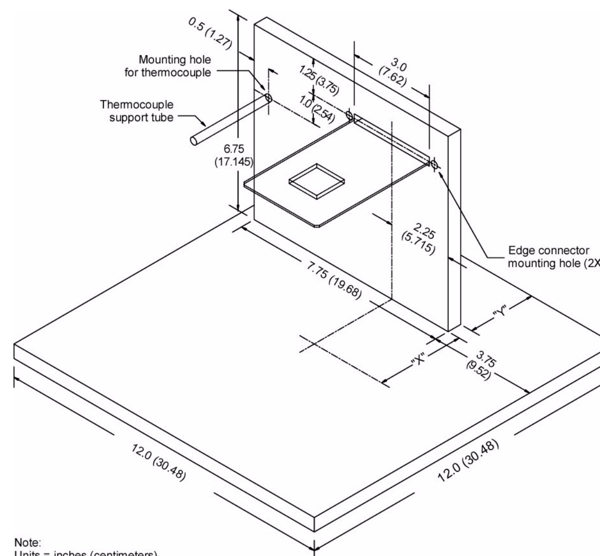


Figure 5.2 Isometric view of the natural convection fixture.

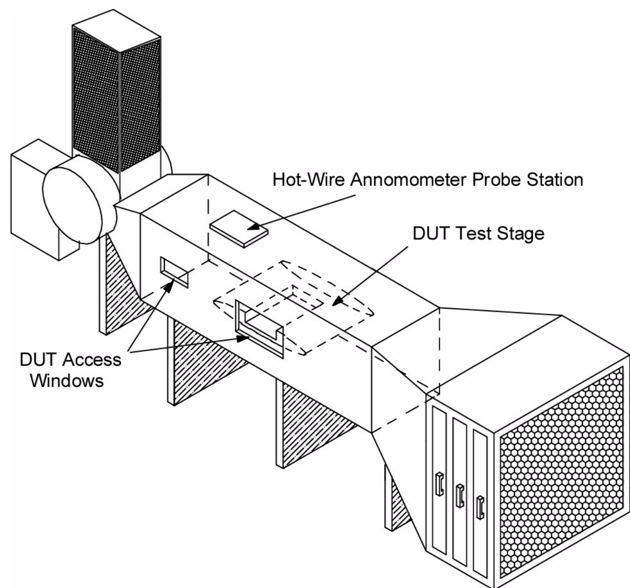


Figure 5.3 Forced convection chamber used to conduct moving-air tests.

For plastic packages, a temperature-controlled fluid bath containing deionized water is used. Fluid is forced onto the package body from both sides from nozzles as shown in *Figure 5.4*. Due to the high heat transfer capabilities of this method, it is assumed that the reference temperature is that of the liquid. This measurement is a relatively new technique that essentially provides the same boundary conditions as the cold plate method does for hermetic packages. But, caution should be used when attempting to calculate junction temperature from θ_{JC} values for plastic packages in end-use environments.

THERMAL CHARACTERIZATION PARAMETER (Ψ_{JT})

A new parameter has gained popularity due to the misconceptions arising from using the value of θ_{JC} to calculate junction temperatures for plastic packaged devices in end-use environments. This parameter is proportional to the temperature difference between the top center of the package and the junction temperature, relative to the power dissipation. It is a useful parameter for verifying device temperatures in an end-use environment. Refer to *"Sample Calculations: Thermal Resistance" on page 5-5* (algorithms 6 and 7) for examples of calculations using this new parameter.

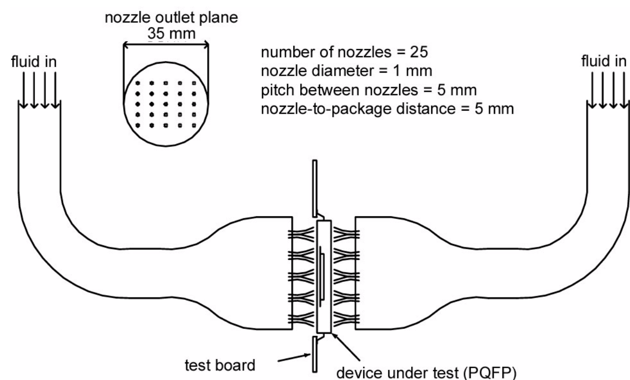


Figure 5.4 Jet nozzle impingement used for taking case measurements of a plastic package.

THERMAL TEST BOARDS

Before measuring the thermal characteristics of a semiconductor device, the component is assembled onto a test board using industry-standard techniques. The test boards AMD uses for this are standardized to conform with JEDEC specification JESD51_3. (Item 22 of the references list at the end of this chapter is a source for additional information on this specification.) Two types of test boards commonly used are low-effective or high-effective thermal conductivity test boards.

Low-Effective Thermal Conductivity Test Boards. Low-effective thermal conductivity test boards are designed to simulate worst-case board mounting. These boards have no internal planes and minimum trace routing.

High-Effective Thermal Conductivity Test Boards. High-effective thermal conductivity test boards are fabricated to have two evenly spaced internal planes. These boards more closely reflect applications in which ground or power planes are used in the PCB.

For both board types, FR4 is used as the board material, and small gauge wire is used to connect the device to the test interface. As shown in *Figure 5.5*, the board dimensions are 76.2 mm x 114.3 mm for packages having body sizes <28 mm and 101.6 mm x 114.3 mm for packages having body sizes ≥28 mm. By standardizing the board, the environment for testing is normalized to the board size, allowing comparisons between package families or package variations within a family. These PCB designs conform to JESD specifications.

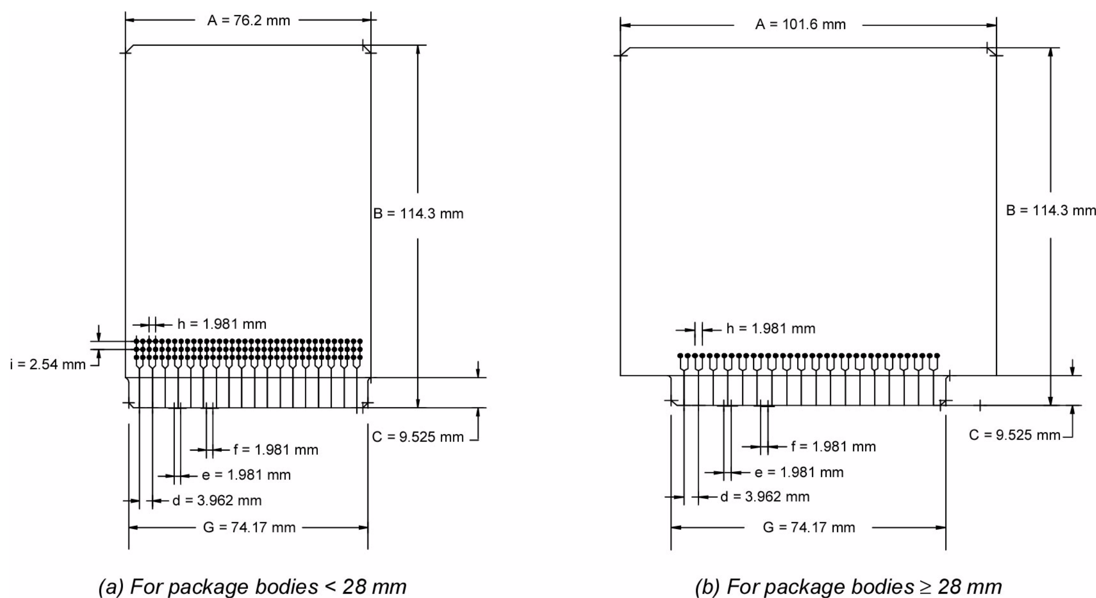


Figure 5.5 Thermal test board design for IC packages having body sizes (a) less than < 28 mm and (b) ≥ 28 mm.

THERMAL DATA REPORTS

Because thermal behavior is sensitive to the effects of the environment and PCB, a complete description of all aspects of the test environment is necessary. The primary information in AMD's thermal data reports are the thermal resistance values and a generic description of the test board. Still air (θ_{JA}), and moving air (θ_{JMA}) values are reported, as well as ψ_{JT} for plastic packages, or θ_{JC} for hermetic packages. These values are reported as raw data along with the average and standard deviation as shown in *"Sample of a Thermal Test Data Report" on page 5-9*. Along with each thermal data report, a complete description of the environmental chambers and the test setup is provided (as shown in *"Thermal Data Measurement Conditions" on page 5-10*). This information describes exactly the parameters used for the test, ensuring that the test method and environment are well understood.

Sample of a Thermal Test Data Report

θja, ψjt, θjc, θjma @ 200, 400, 600, & 800 lfpm

Requestor: Mail Stop:Internal Die No.PAETC 2x2Package:PGA 145

Ext: Prod Group:Ext Device Name:AMD Thermal Test DieLead Frame

Rec. Date: 8/1/96File No.96050Die Size:210 x 205Test Type

Comp Date: 8/8/96Operator:JPDie Attach:Ag/GlassPCB:Socket on 6 layer board

Initial Values							Final Values				Delta					
DUT No.	Amb Temp (°C)	V Diode (Volts)	Case Temp (°C)	Junct Temp (°C)	K Factor (°C/mV)	Wnd Spd (LFPM)	Amb Temp (°C)	V Diode (Volts)	Case Temp (°C)	Junct Temp (°C)	Junct Temp (°C)	V Heat (Volts)	I Heat (Amp)	Power (Watt)	θja **(°C/W)**	(Plastic) Ψjt (°C/W)
001	23.0	0.808	23.6	24.0	666	0	23.3	0.757	49.2	57.5	33.5	2.790	0.523	1.459	23.0	5.67
002	21.3	0.811	21.6	22.0	666	0	21.8	0.765	48.4	52.7	30.7	2.630	0.508	1.336	23.0	3.18
003	23.1	0.808	23.4	23.3	672	0	23.1	0.762	50.7	54.0	30.7	2.640	0.501	1.323	23.2	2.53
004	22.7	0.809	22.8	23.0	667	0	23.1	0.758	51.3	57.1	34.0	2.800	0.531	1.487	22.9	3.87
005	22.2	0.809	22.3	22.7	667	0	22.7	0.754	55.0	59.7	37.0	2.880	0.537	1.547	23.9	3.07
												Average:		1.430	23.2	
												Std. Dev.:		0.087	0.390	1.090
															θjma	
001	21.7	0.810	n/a	22.4	666	200	21.8	0.775	n/a	45.6	23.2	2.74	0.532	1.458	15.9	
002	22.0	0.810	n/a	22.5	666	200	22.3	0.776	n/a	45.1	22.6	2.71	0.532	1.442	15.7	
003	22.1	0.809	n/a	22.3	672	200	22.3	0.774	n/a	45.9	23.6	2.75	0.536	1.474	16	
004	22.3	0.810	n/a	22.5	667	200	22.2	0.775	n/a	45.9	23.4	2.74	0.538	1.474	15.9	
005	22.2	0.809	n/a	22.6	667	200	22.1	0.769	n/a	49.9	27.3	2.98	0.572	1.705	16	
												Average:		1.510	15.9	
												Std. Dev.:		0.098	0.116	
001	21.7	0.810	n/a	22.4	666	400	22.3	0.778	n/a	43.5	21.1	2.750	0.538	1.480	14.3	
002	22.0	0.810	n/a	22.5	666	400	22.2	0.779	n/a	43.1	20.6	2.730	0.540	1.474	14.0	
003	22.1	0.809	n/a	22.3	672	400	22.0	0.777	n/a	43.8	21.5	2.800	0.550	1.540	13.9	
004	22.3	0.810	n/a	22.5	667	400	22.0	0.779	n/a	43.3	20.8	2.730	0.541	1.477	14.1	
005	22.2	0.809	n/a	22.6	667	400	22.0	0.773	n/a	47	24.4	2.970	0.577	1.714	14.2	
												Average:		1.537	14.1	
												Std. Dev.:		0.092	0.122	
001	21.7	0.810	n/a	22.4	666	600	22.3	0.779	n/a	43.1	20.7	2.800	0.549	1.537	13.5	
002	22.0	0.810	n/a	22.5	666	600	22.1	0.781	n/a	41.8	19.3	2.750	0.546	1.502	12.9	
003	22.1	0.809	n/a	22.3	672	600	22.1	0.780	n/a	42.0	19.7	2.750	0.543	1.493	13.2	
004	22.3	0.810	n/a	22.5	667	600	22.1	0.780	n/a	42.0	19.5	2.740	0.544	1.491	13.1	
005	22.2	0.809	n/a	22.6	667	600	22.0	0.775	n/a	45.4	22.7	2.970	0.580	1.723	13.2	
												Average:		1.549	13.2	
												Std. Dev.:		0.088	0.186	
001	21.7	0.810	n/a	22.4	666	800	22.7	0.782	n/a	41.2	18.8	2.73	0.539	1.471	12.8	
002	22.0	0.810	n/a	22.5	666	800	22.2	0.783	n/a	40.7	18.2	2.7	0.539	1.455	12.5	
003	22.1	0.809	n/a	22.3	672	800	22.1	0.781	n/a	41.2	18.9	2.75	0.544	1.496	12.6	
004	22.3	0.810	n/a	22.5	667	800	22.0	0.782	n/a	40.8	18.3	2.73	0.546	1.491	12.3	
005	22.2	0.809	n/a	22.6	667	800	21.9	0.777	n/a	44.0	21.4	2.97	0.582	1.729	12.4	
												Average:		1.528	12.5	
												Std. Dev.:		0.101	0.184	

Ceramic Only		Initial Values					Final Values				Delta				
DUT No.	Amb Temp (°C)	V Diode (Volts)		Junct Temp (°C)	K Factor (°C/mV)	Wnd Spd (LFPM)	Amb Temp (°C)	V Diode (Volts)	Case Temp (°C)	Junct Temp (°C)	Junct Temp (°C)	V Heat (Volts)	I Heat (Amp)	Power (Watt)	θja **(°C/W)**
001	25.0	0.805	n/a	25.7	666	0	25.0	0.802	n/a	27.7	2.0	2.67	0.555	1.482	1.3
002	25.0	0.803	n/a	27.1	666	0	25.0	0.800	n/a	29.1	2.0	2.76	0.578	1.595	1.3
003	25.0	0.805	n/a	25.1	672	0	25.0	0.802	n/a	27.2	2.0	2.72	0.565	1.537	1.3
004	25.0	0.805	n/a	25.6	667	0	25.0	0.802	n/a	27.6	2.0	2.68	0.574	1.538	1.3
005	25.0	0.804	n/a	26.3	667	0	25.0	0.801	n/a	28.3	2.0	2.73	0.570	1.556	1.3
												Average:		1.542	1.3
												Std. Dev.:		0.037	0.031

Thermal Data Measurement Conditions

Measurement Area	Condition Parameters	Data Paremeters
Electrical Information	• V_H: Heating voltage (V)** • I_H: Heating current (mA)** • T_{HSS}: Steady-state heating time (900 s) • t_{MD}: Measurement time delay (20 µs from power off) • T_{SW}: Switching time (60µs) • K_F: Calibration factor, (°C/mV)*	• Δ_{VF} (V): delta forward voltage drop (diode) • Δ_{TJ} (°C): delta junction temperature • θ_{TR} (°C/W): thermal resistance • P_H (W): heating power
Environmental Information	• Test board orientation: θ_{JA} = Horizontal; θ_{JMA} = Vertical • θ_{JA} Chamber size = 1 ft^3 • T_{AO}: Ambient temperature at time zero (°C) (for θ_{JA}, θ_{JMA}, θ_{JC}, ΨJT)* • T_{ASS}: Ambient temperature at time zero (°C) (for θ_{JA}, θ_{JMA}, θ_{JC}, Ψ_{JT})**	• θ_{JA} (°C/W): junction-to-ambient thermal resistance** • θ_{JMA} (oC/W), junction-to-moving air thermal resistance** • θ_{JC} (°C/W), junction-to-case thermal resistance**
Package Surface Measurements	• T_{T0}, package temperature at time zero (°C) (for Ψ_{JT} and θ_{JC} only)* • TTSS, package temperature at steady state (°C) (Ψ_{JT} and θ_{JC} only)** • Temperature measurement method: Thermocouple: T-Type or K-Type • Thermocouple wire gauge # (AWG 40 g or 32 g) • Thermocouple attachment method (Scotch Kapton Film Tape tape #5413 32.9 m)	• Ψ_{JT} (°C/W)**
Thermal Test Card Criteria	• Board Dimensions (x, y, z), 3" x 4.5" x 0.0625" • Board Material (Fr4) • Non-nested design • Sense wire gauge, test system (20 g) • Sense wire gauge, test board (26 g) • Force wire gauge, test system (20 g) • Force wire gauge, test board (26 g)	

* Refer to "Initial Values" on test data sheet.

** Refer to "Final Values" on test data sheet.

ELECTRICAL CHARACTERIZATION

To meet the needs of today's complex, high-performance device designs, the electrical properties of microelectronics packaging systems must be characterized thoroughly and precisely. As clock speeds increase and rise times decrease, new performance demands are placed on the IC package. Electrical parasitics that were not considered critical to digital engineers in the past are now limiting device performance and require close attention. In addition, the IC package must be characterized at frequencies far above the system clock speed to accurately extract parasitics and determine bandwidth characteristics and performance criteria.

AMD engineers perform electrical characterizations in its engineering laboratory, which is fully equipped with traditional inductance, capacitance, and resistance measurement equipment. AMD's techniques and methodologies are continually refined to enable the properties of the package to be accurately measured and the fixture parasitics minimized. The commonly used measurement terminology is shown in *"Electrical Measurement Terminology" on page 5-12*.

Design engineers construct electrical models for use in time-domain simulations, which allow AMD to evaluate the effect of package structures on a device's electrical performance. AMD has the facilities to model package electrical interconnections based on geometric and material properties, and this capability extends to the creation of SPICE models that include the device simulation. Using these tools, AMD engineers are able to predict the electrical performance of a specific device and package combination. Moreover, these models can be extended to include the effects of the PCB interconnects, the backplanes, and the connectors in the end-use application, making system level modeling and simulation possible. By combining these measurement and modeling methodologies, AMD engineers are able to validate and verify the data through an iterative loop, further refining the model and SPICE libraries.

Electrical Measurement Terminology

Terminology used for electrical characterization measurements taken on IC package leads and interconnections:

Rxx = Series resistance

Cxx = Self (bulk) capacitance

Cxy = Mutual (pin-to-pin) capacitance

Lxx = Self inductance

Lloop = Loop inductance between two leads

From these measurements, the following parameters are calculated:

Mxy = Mutual Inductance =

C_{X0} = Capacitance to ground = Cbulk - C12 - C23 (example for lead 2, x = 2)

where:

xx = Represents the parasitic of the lead itself (e.g., self inductance, series resistance, or self capacitance)

xy = Represents a parasitic between $\geq$ 2 leads, traces, or bond wires (e.g., mutual capacitance or mutual inductance)

The following parameters represent bond-wire parasitics:

R_{BW} = Single bond-wire series resistance (# of parallel wires must be specified in the power distribution model)

L_{BW} = Single bond-wire series inductance (# of parallel wires must be specified in the power distribution model)

M_{BW} = Mutual inductance between two parallel wires. (Calculated from closed form expressions)

R_{BF} = Single bond finger, pin grid array, series resistance (# of parallel wires must be specified in power distribution model)

L_{BF} = Single bond finger, pin grid array, series inductance (# of parallel wires must be specified in power distribution model)

The following symbols represent pin parasitics (for pin grid array packages):

Lpin = Pin series inductance (# of parallel pins must be specified in the power distribution model)

Rpin = Pin series resistance (# of parallel pins must be specified in the power distribution model)

METHODOLOGY

The purpose of electrical measurements and models is to create a lumped model of the interconnections under test and incorporate it in the device models that are used in simulation software as a means of predicting the electrical operation of the device and package together. Fixtures have been designed for measuring PGA and BGA packages, as well as a variety of surface-mount packages, using one of the following tools:

- Impedance phase-gain analyzer (0.5 MHz to 15 MHz)
- Impedance analyzer (1 MHz to 1.8 GHz)
- Vector network analyzer (300 KHz to 3 GHz)
- High-bandwidth oscilloscope (TDR/TDT)

The generic test setup for a four-terminal pair, low-frequency measurement is shown in *Figure 5.6*. The setup for a one-port, high-frequency generic test is shown in *Figure 5.7*. From the measured data, lumped element models are generated for a single-lead, a power distribution network, and three peripheral leads (see *Figure 5.8 (a), (b), and (c)*, respectively). The following sections describe the common methods used to measure the various electrical parameters of IC packages.

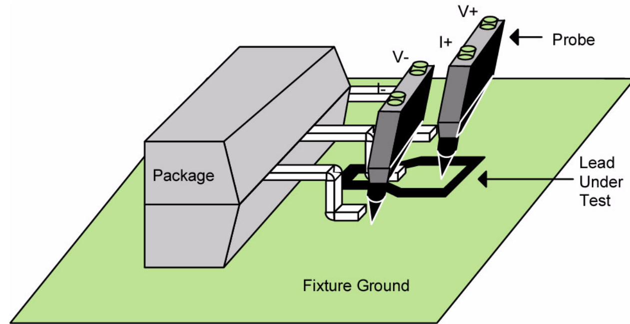


Figure 5.6 Typical four-terminal-pair measurement using v-probes and the fixture (both probes and fixture are connected to guard terminal).

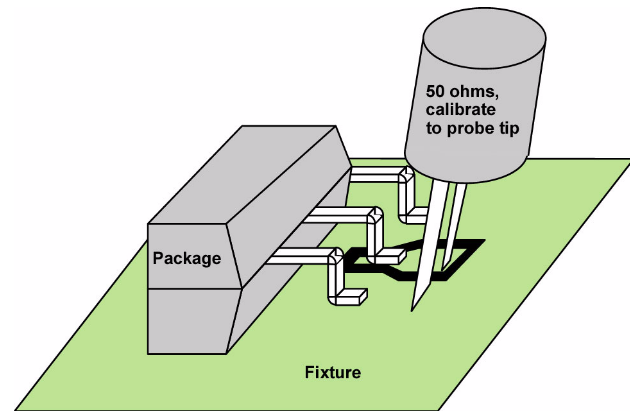
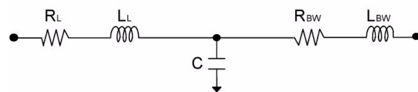
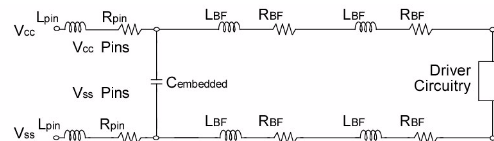


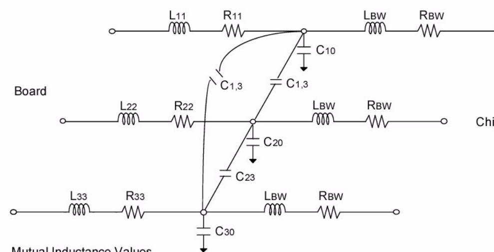
Figure 5.7 Setup for taking a generic, one-port impedance measurement using a 50-ohm controller impedance probe and test fixture.



(a) Typical Single Lead



(b) Power Distribution Network



(c) Three Peripheral Leads

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Figure 5.8 Lumped element models for (a) typical single lead, (b) power distribution netowrk, and (c) three peripheral leads.

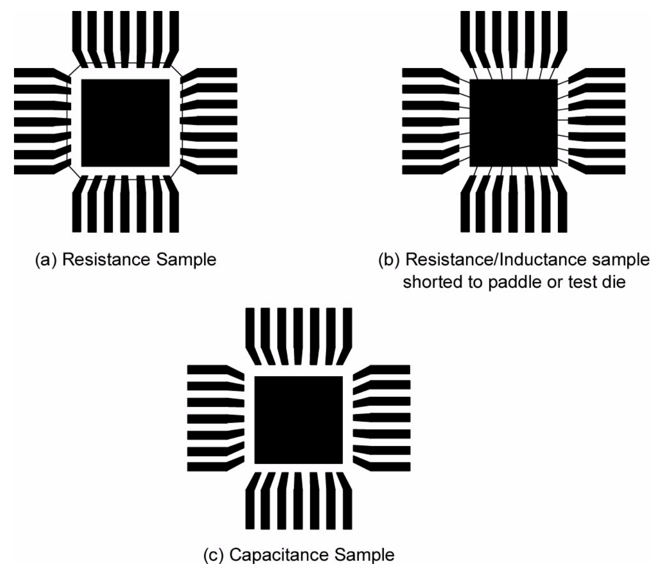

Figure 5.9 Stitch bond layouts for package samples being tested for resistance, inductance, and capacitance.

Series Resistance (Rxx). A DC micro-ohmmeter is used to make series resistance measurements. The samples are stitch-bonded from bond finger to bond finger to provide a defined path (see *Figure 5.9 (a)*). Two leads having similar geometric properties are selected, and a measurement is made that includes both leads. The value is divided by two to provide the typical DC resistance characteristics.

It is also possible to include bond-wire parasitics in resistance measurements. When necessary, bond wires of the appropriate length are bonded, as in *Figure 5.9 (b)*. Again, two leads having similar geometric properties are selected, and a measurement is made that includes both leads along with the two corresponding bond wires. The value is divided by two to provide the typical DC resistance characteristics. Series resistance can also be measured at frequency, using either an impedance analyzer or a vector network analyzer, to take into account the skin effect associated with high-speed applications.

Self Capacitance (Cxx). Self capacitance, also known as bulk capacitance or loading capacitance, represents the capacitance of the lead under test when compared to all the other leads and to the environment. Bulk capacitance measurements are performed while the sample is positioned on a test fixture that has a topside ground plane. The lead under test is isolated, and all other package leads are connected to a common potential (ground). Samples are left unbonded, as shown in *Figure 5.9 (c)*.

Self Inductance (Lxx). The self inductance of a conductor is dictated by the electrical current loop of the measurement. To measure accurately the inductance of a single lead, the total current loop must be taken into account. This is a primary concern when simulating the end-use application during the test. To accomplish this, special boards are designed with topside ground and isolation pads for the leads under test. The fact that the fixturing does not allow current to flow through those leads adjacent to the lead under test, eliminates the mutual inductance element from the measurement. High leadcount IC packages (e.g., PQFPs, PGAs, and BGAs) are assembled per the configuration in *Figure 5.9 (b)*. Note that the inductance measurement includes the inductance of a bond wire.

Mutual Capacitance (Cxy). Mutual capacitance is measured on adjacent leads using the sample assembly shown in *Figure 5.9 (c)* and a PCB that has a topside ground.

Mutual Inductance (Mxy). Mutual inductance is calculated from the self-inductance and a two-lead loop inductance. The self inductance measurement is performed as stated earlier. The loop inductance is measured by assembling samples like those shown in *Figure 5.9 (b)*. Two leads are isolated, and the inductance of the desired current loop is measured. This measurement is represented in the following equation:

$$Lloop = L11 + L22 - 2(M12)$$

where:

- M11 is the measured self inductance of the first lead.
- M22 is the measured self inductance of the second lead.
- M12 is the mutual inductance between the leads of interest.

M12 is calculated as:

$$M12 = \frac{(L11 + L22 - Lloop)}{2}$$

BOND WIRE SERIES INDUCTANCE AND RESISTANCE

Because bond wires have very small cross-sectional areas, the dominant parasitics associated with them are series inductance and resistance. Although the resistance of the wire is a factor, reducing inductance is often the package designer's primary goal. Therefore, in good package designs, efforts are made to keep the bond wire length at a minimum to avoid the voltage drop and noise associated with the well known V=Ldi/dt effect of inductance. The inductance of a bond wire is directly proportional to its length and diameter. Since bond wires are typically much smaller than the package interconnects, they have greater per unit length inductance.

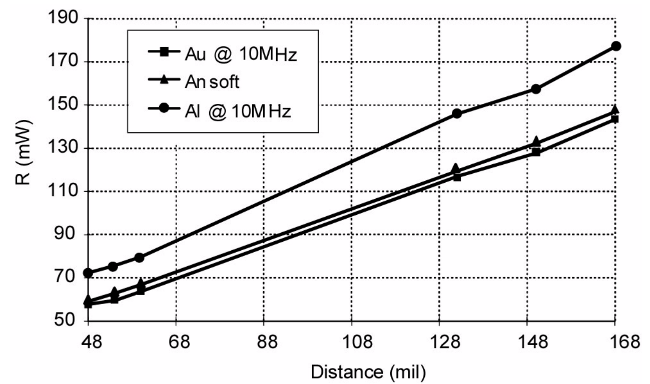

Figure 5.10 Bond-wire resistance (milliohms) vs. length (mils).

Figure 5.10 shows a plot of the wire resistance versus the separation between bond pads. In both charts, Au designates a 1.2-mil diameter gold wire, and Al designates a 1.0-mil diameter aluminum wire. AMD performed these simulations using a commercial finite element EM solver.

Figure 5.11 shows a plot of the bond wire inductance versus the separation between bond pads. The data was measured and modeled on a typical-height bond-wire loop. This chart is a useful guide for determining the relative self inductance of bond wires.

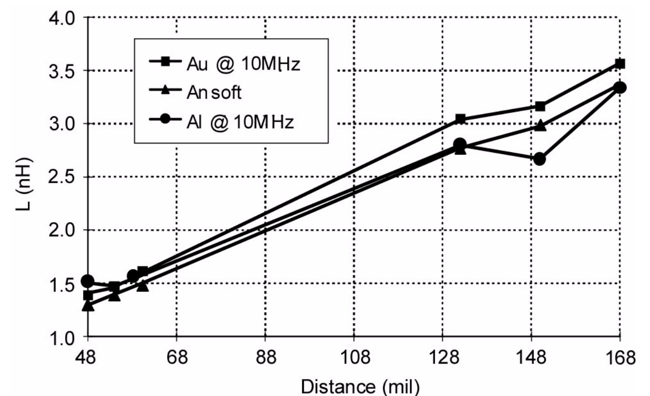

Figure 5.11 Bond-wire inductance (nanohenries) vs. length (mils).

PACKAGE ELECTRICAL VALUES

The following table lists the typical resistance, capacitance, and inductance values for select PLCC and PQFP packages. These values were generated using the electrical characterization methodologies explained herein.

Measured Electrical Values for Select PLCC and PQFP Packages

Pkg Type	Lead-count	Paddle and Body Size (mm x mm)	Maximum and Minimum Values					
			Lead Resistance Rxx, (mΩ)	Lead Inductance Lxx, (nH)	Mutual Inductance Mxy, (nH)	Mutual Capacitance Cxy, (pF)	Loaded Capacitance CLoaded, (pF)	Bond Wire Length (mm) & Inductance (NH)
PLCC	032	7.5 x 7.5 11.5 x 15.0	74-55	6.36-4.64	3.74-2.82	0.268-0.106	0.676-0.461	0.67-1.3 mm 1.1-1.3 nH
	044	5.7 x 5.7 17.5 x 17.5	69-65	8.38-7.68	5.19-4.66	0.410-0.326	1.02-0.699	1.2 mm 1.6 nH
TQFP	044	6.0 x 6.0 10.0 x 10.0	136-125	5.08-4.51	2.38-2.12	0.13-0.08	0.41-0.30	2.1 mm 2.0 nH
	080	7.0 x 7.0 12.0 x 12.0	180-164	5.16-4.58	2.32-2.12	0.23-0.18	0.48-0.42	2.45 mm 2.25 nH
LQFP	100	8.5 x 8.5 14.0 x 14.0	107-100	5.83-4.97	3.16-2.63	0.15-0.08	0.32-0.24	1.54 mm 1.70 nH
	144	8.5 x 8.5 20.0 x 20.0	105-94	7.18-5.72	3.52-2.72	0.39-0.28	0.82-0.67	2.4 mm 2.20 nH
	176	10.0 x 10.0 24.0 x 24.0	97-90	8.33-6.56	4.39-3.44	0.47-0.35	0.94-0.89	1.70 mm 1.75 nH
	208	11 x 11 28.0 x 28.0	102-95	9.97-7.85	5.42-4.20	0.62-0.42	1.22-1.04	2.0 mm 2.0 nH
PQFP	080	7.2 x 7.2 14 x 20	85-83	9.89-6.80	5.68-3.95	0.404-0.198	1.0-0.478	1.0 mm 1.4 nH
	100	7.5 x 7.5 28 x 28	94.8-80.9	8.88-8.13	4.95-4.58	0.399-0.368	1.061-0.498	1.2 mm 1.6 nH
	120	7.5 x 7.5 28 x 28	134-124	14.36-12.18	8.38-7.85	0.792-0.47	1.077-0.755	1.9 mm 1.9 nH
	144	8.7 x 10.2 28 x 28	130-116	9.9-9.6	4.86-3.89	0.587-0.479	2.68-1.768	2.0 mm 2.0 nH
	168	10.16 x 10.16 28 x 28	150-127	15.6-9.6	9.8-4.8	0.78-0.46	1.86-1.18	2.0 mm 2.0 nH
	208	0.40 x 0.40 28 x 28	135-128	13.96-11.24	8.94-7.10	0.678-0.450	1.33-1.064	1.9 mm 1.9 nH

ELECTRICAL MODELING

At AMD, the electrical measurements are validated with software modeling. Several tools are available, from simple numerical analysis to electromagnetic solvers and transmission-line characterization. A CAD interface is also supported to enable complex geometrical figures to be imported and considered in the electrical model.

The general format for package electrical models is SPICE, and many versions of SPICE models can be provided. The SPICE formats are HSPICE, Berkeley SPICE, and ContecSPICE. Models for prototype or proposed packages can also be generated from geometric and material properties.

For additional information about AMD's electrical characterization methods and data, contact a local AMD sales representative.

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