Proximity Communication

Robert J. Drost, Ph.D.
Sun Microsystems
Research Laboratories

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Open House

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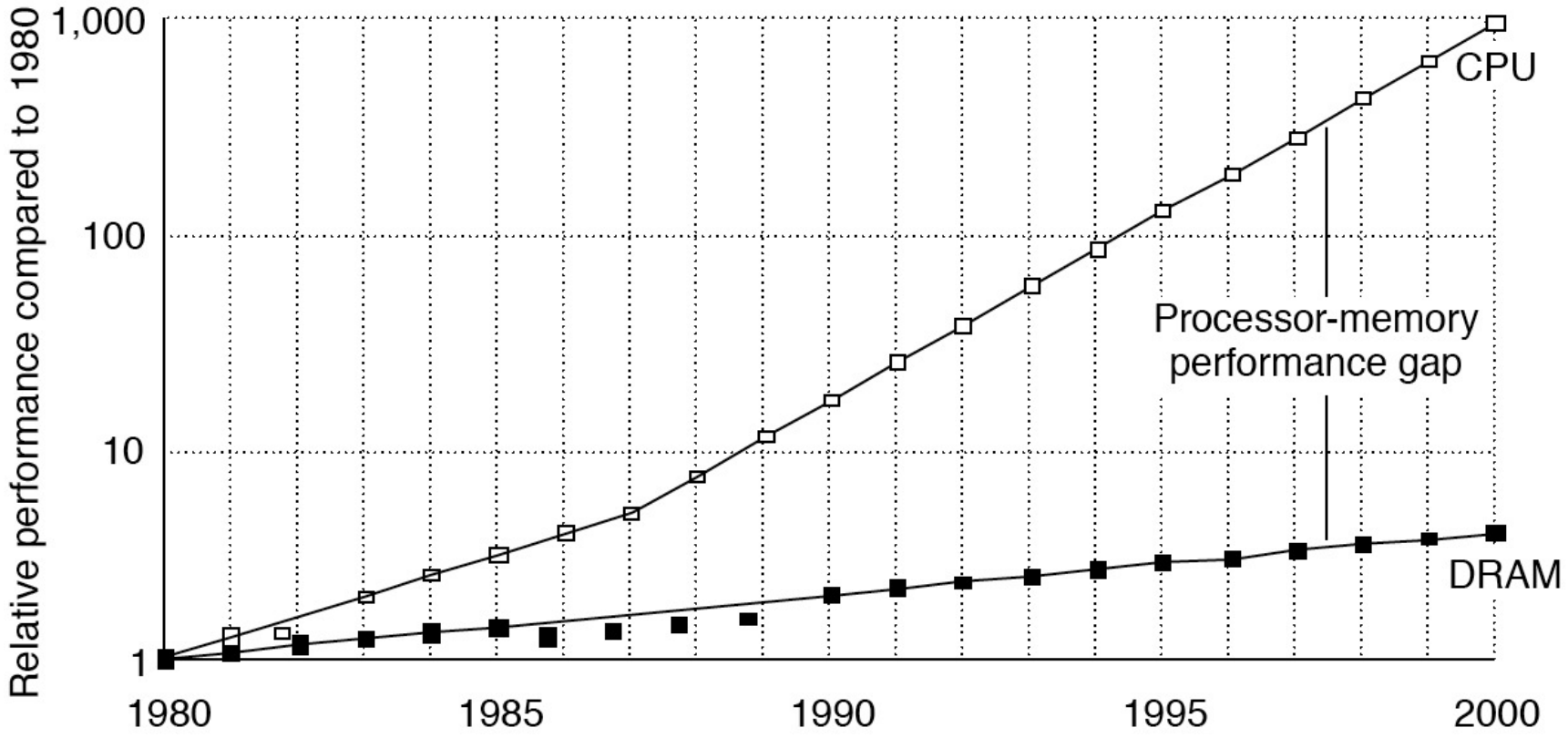
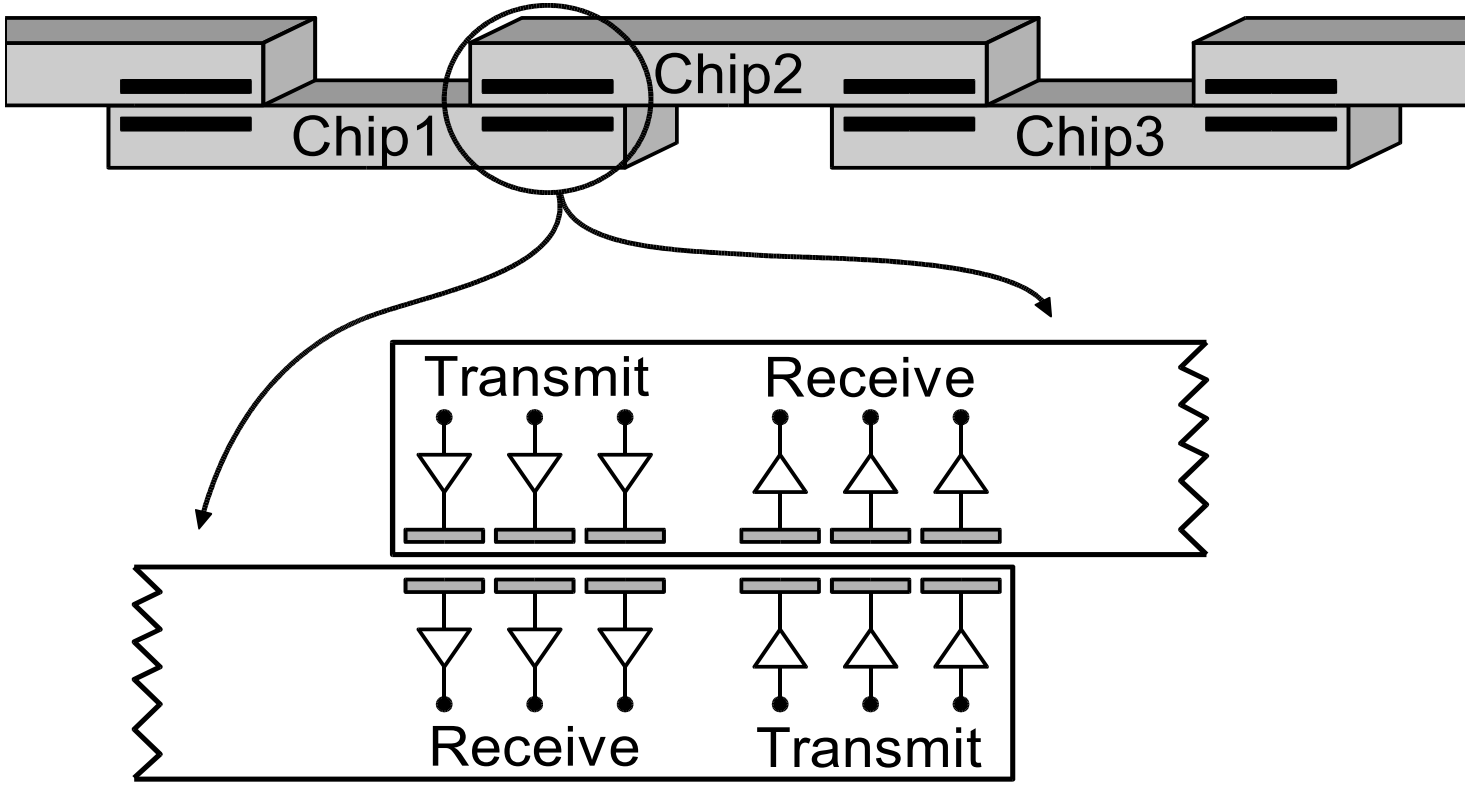
Motivation for Higher Bandwidth



J.L. Hennessy and D.A. Patterson, Computer Organization and Design, 2nd ed.

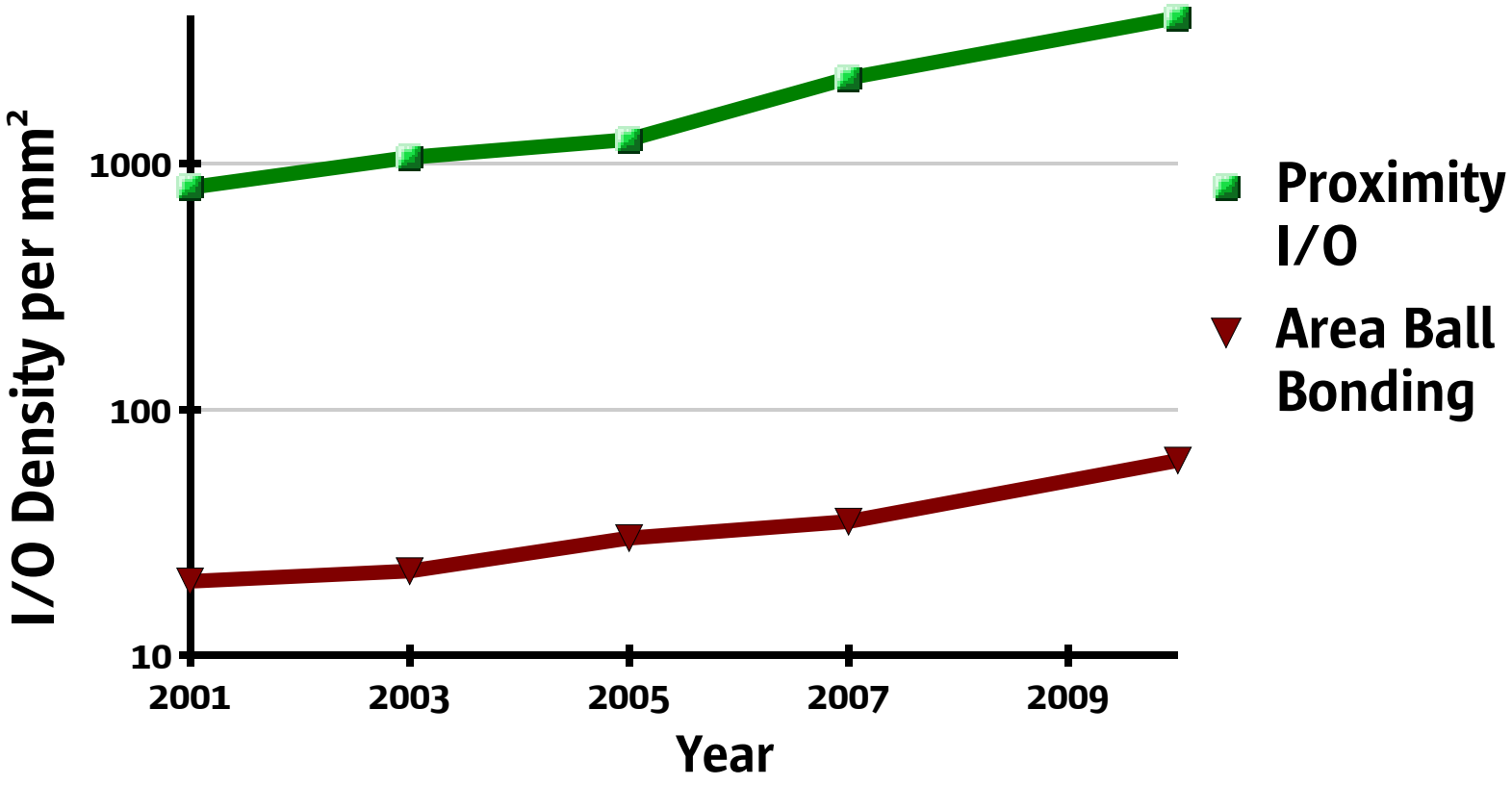
Proximity Communication



Proximity Communication Benefits

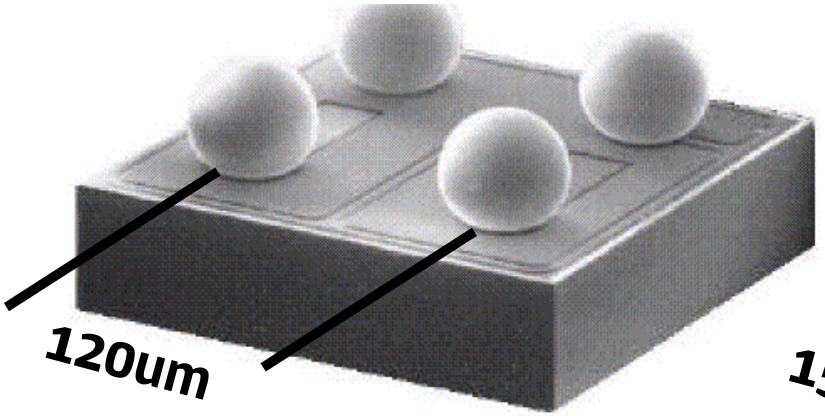
- Avoids Off-Chip Wires
- Increases Bandwidth/Area
- Makes Chips Replaceable..... ↑ System Yield
- Enhances Testing Capability..... ↑ System Yield
- Enables Smaller Chips..... ↑ Chip Yield
- Obviates ESD Protection..... Power ↓
- Shrinks Transmitter and Receiver.... Power ↓

I/O Density Comparison

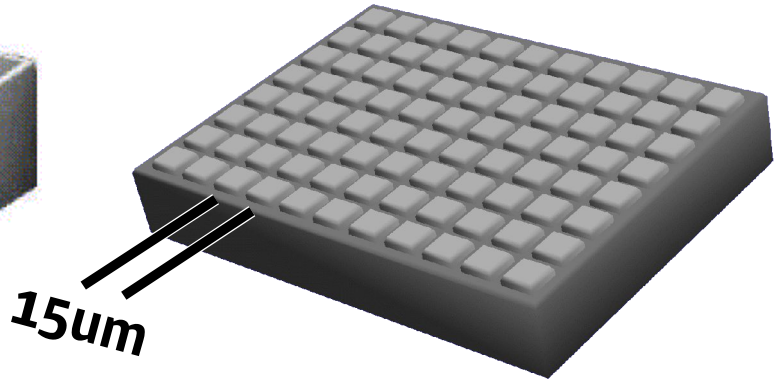


Comparison of Scale

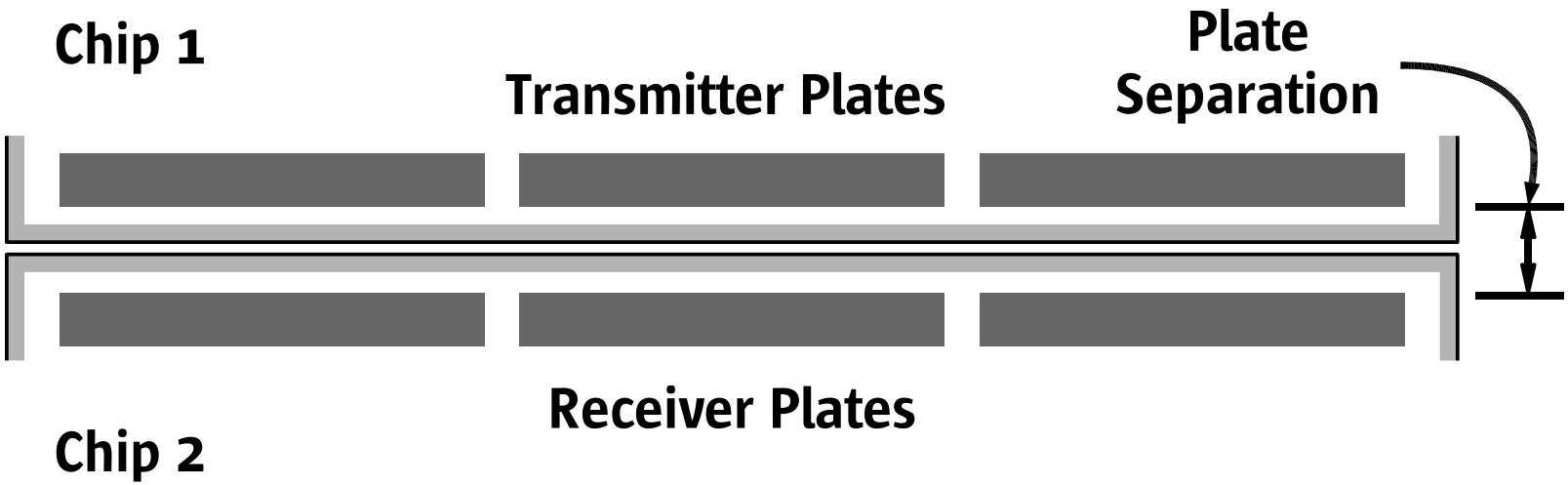
Area Ball Bonding



Proximity Communication

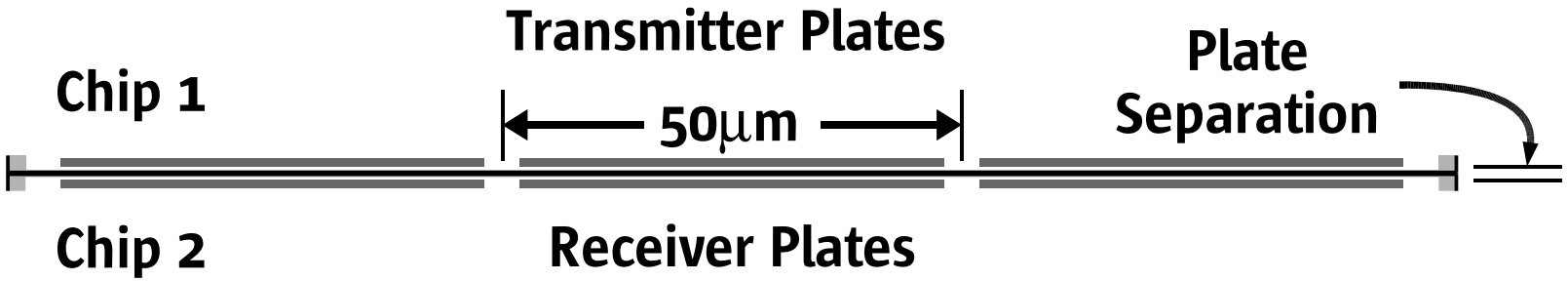


Pads Cross-Section

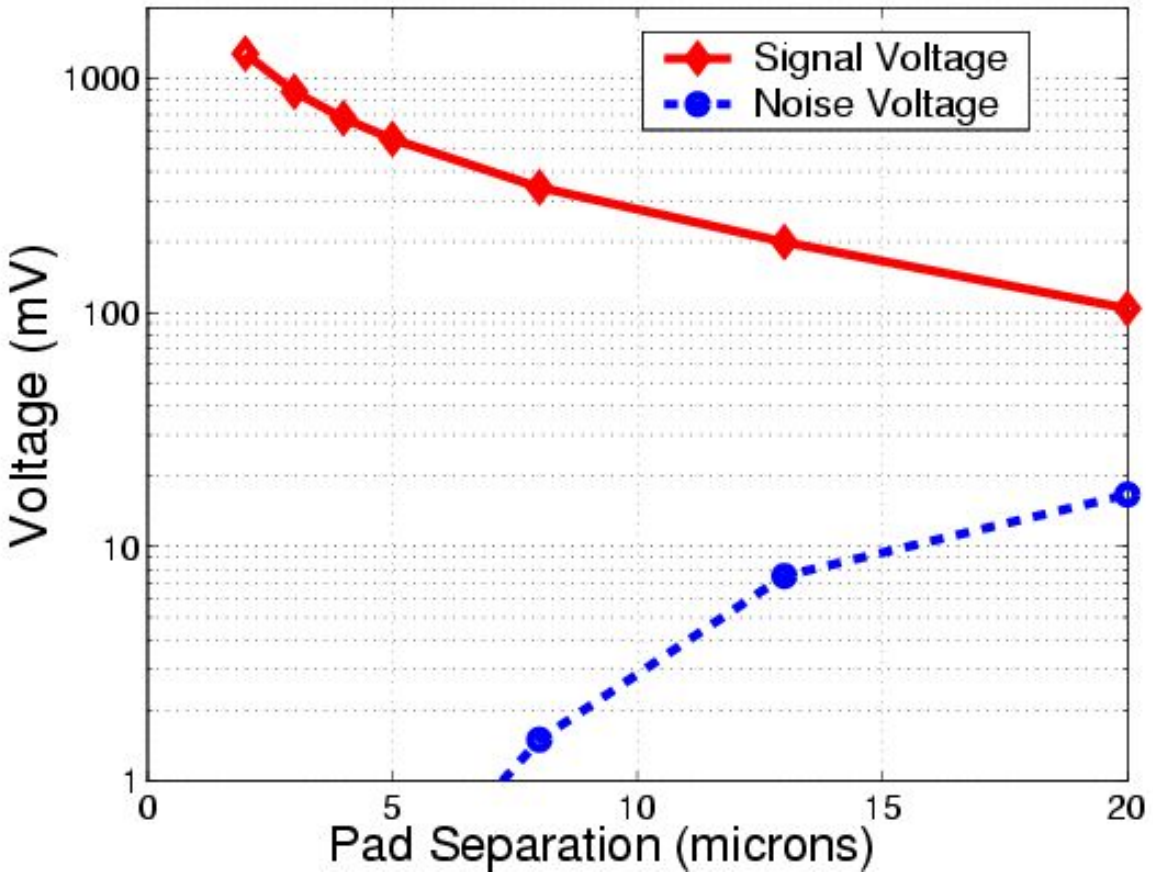


NOT to Scale!

Pads Cross-Section



Signal and Noise Simulated Coupling

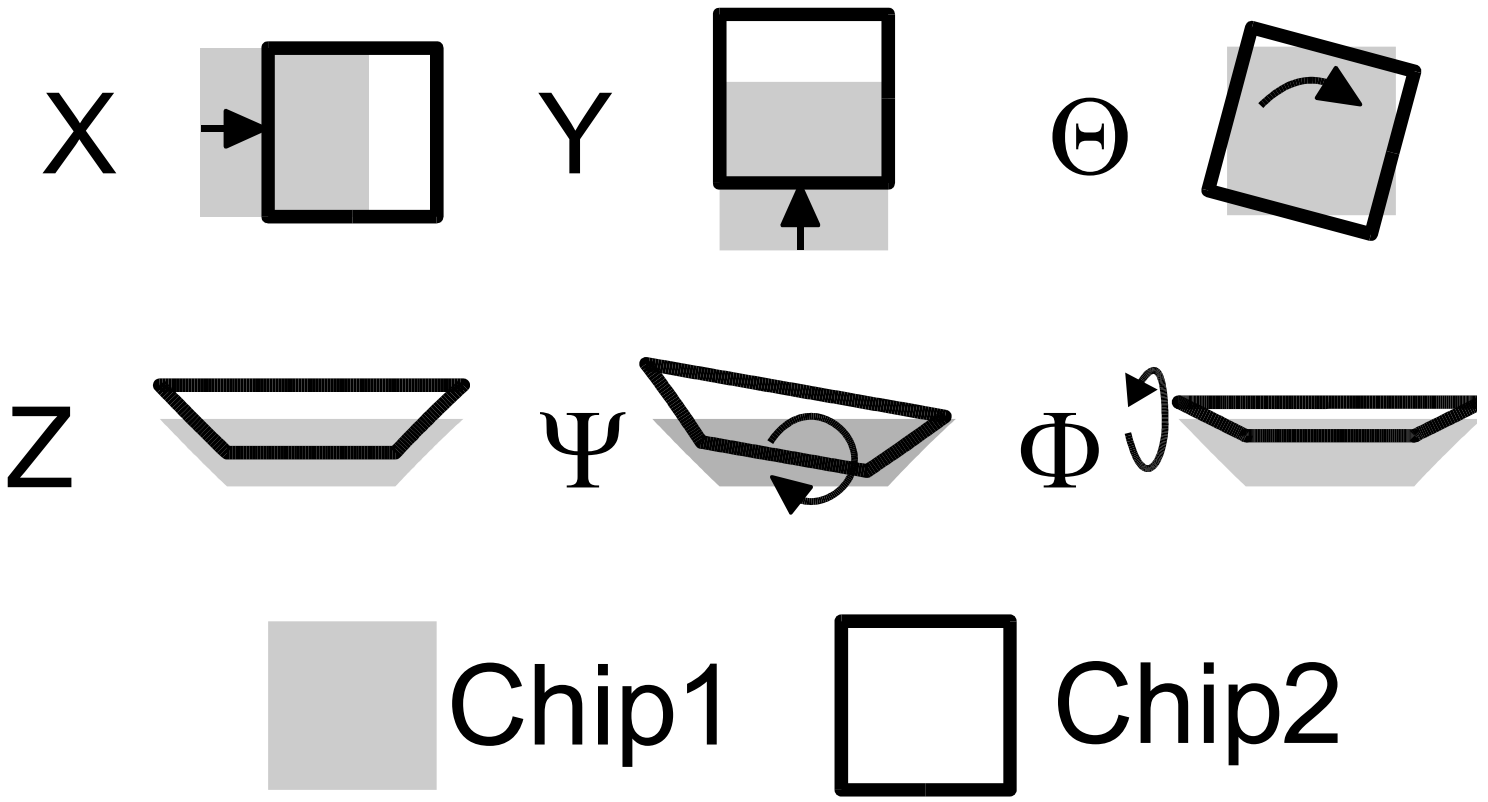


Mechanical Alignment Challenges

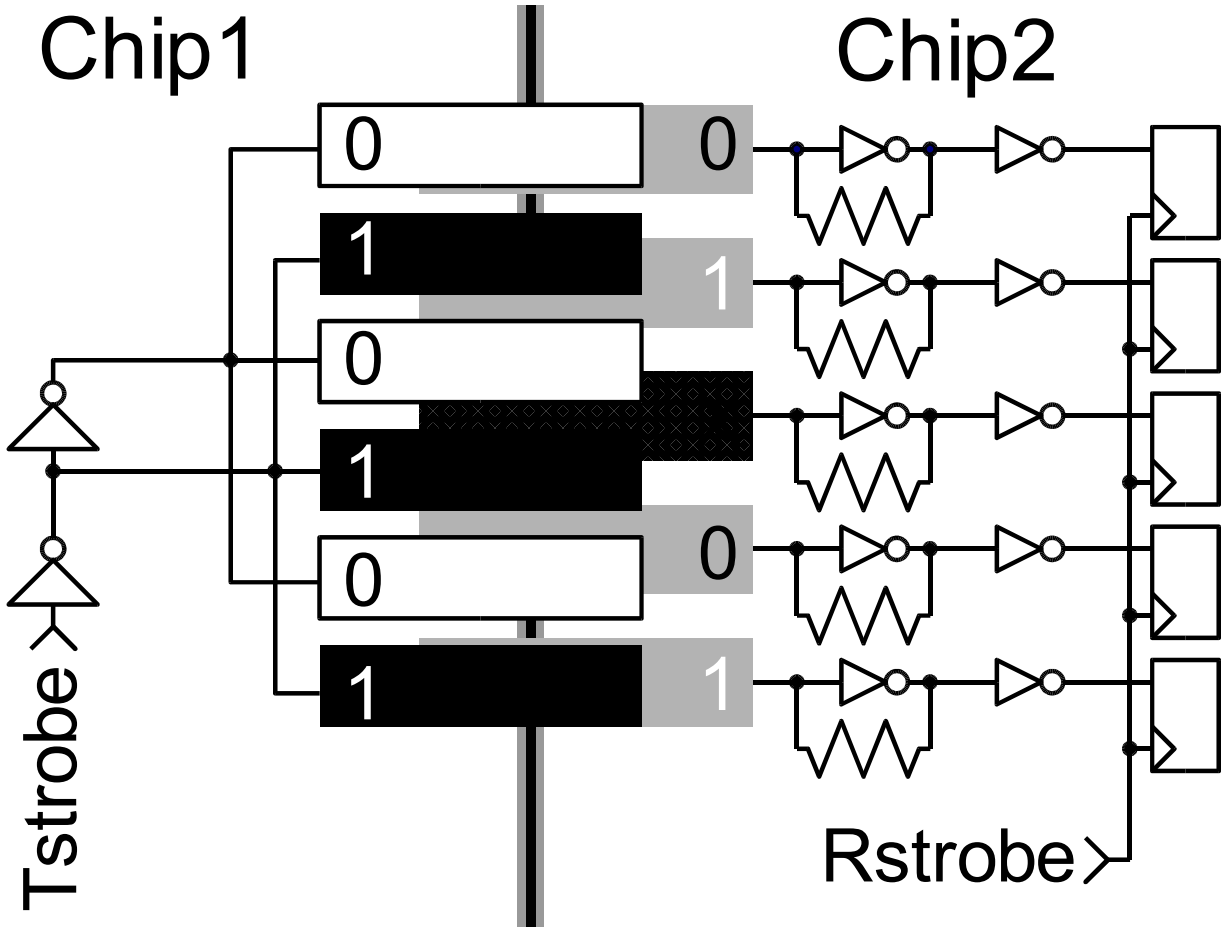
- Proximity Communication
  - Does not use permanent attach
  - Enhanced yield and utility, but is…

  sensitive to misalignment
  - Imperfect packaging
  - Thermal expansion causes misalignment
  - System vibration causes misalignment

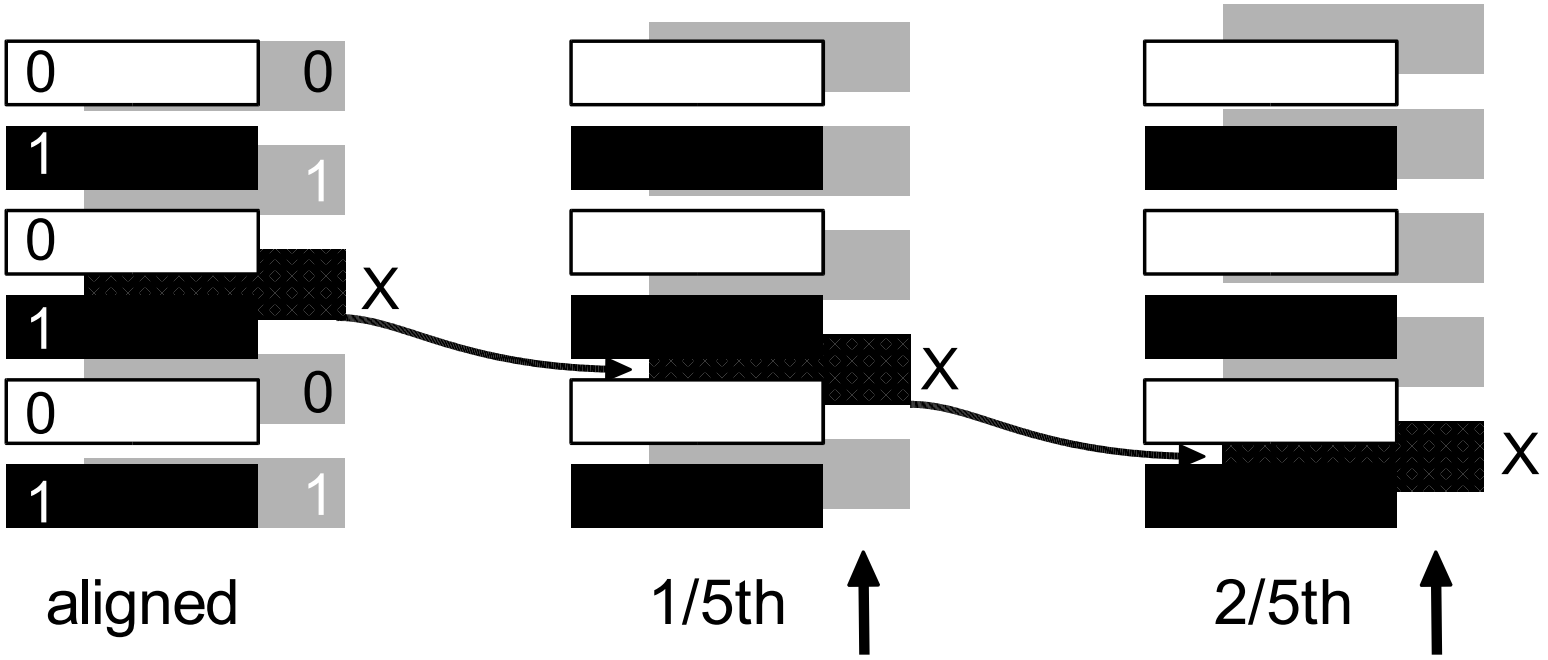
Six Degrees of Misalignment



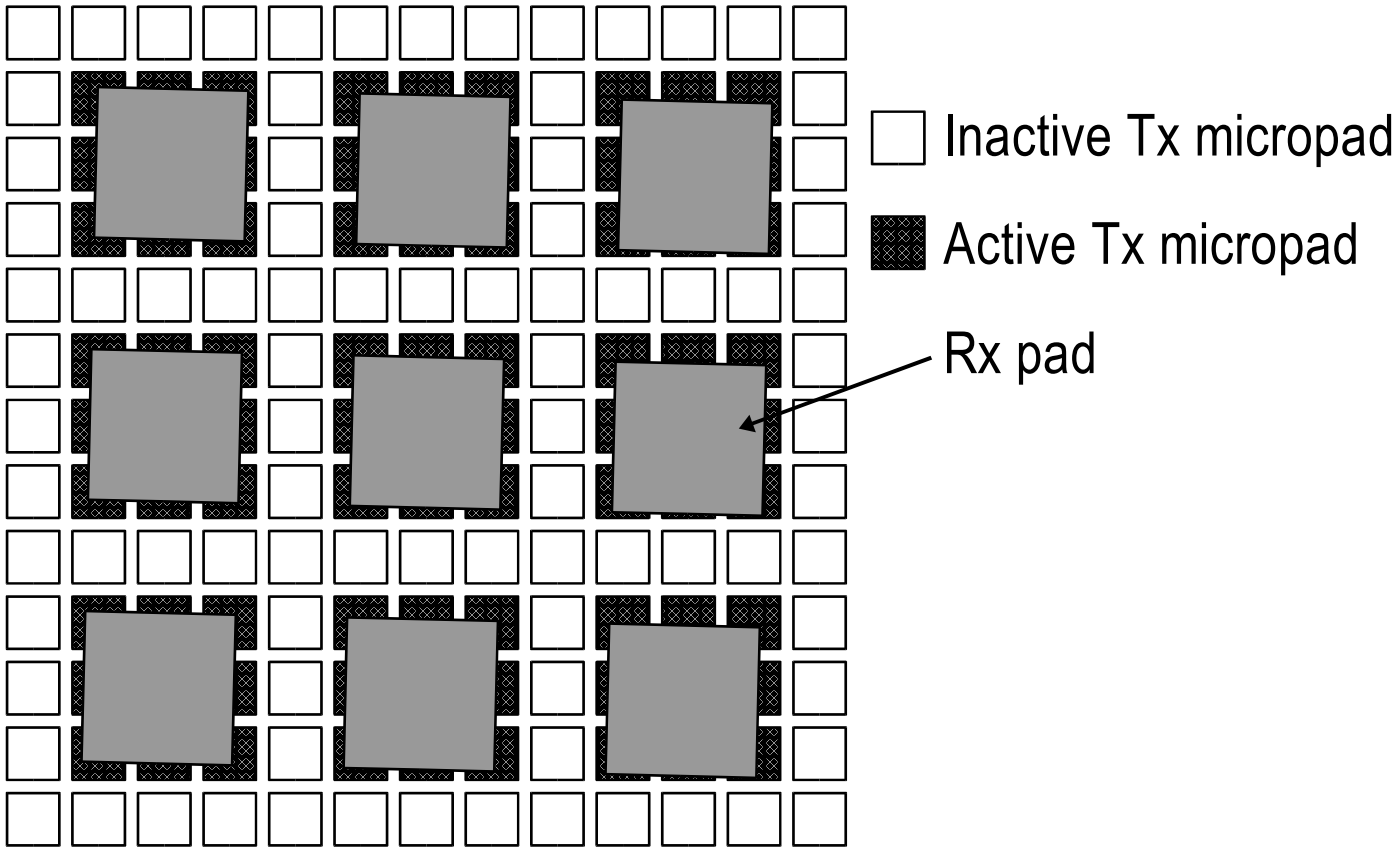
On-chip Alignment Measurement



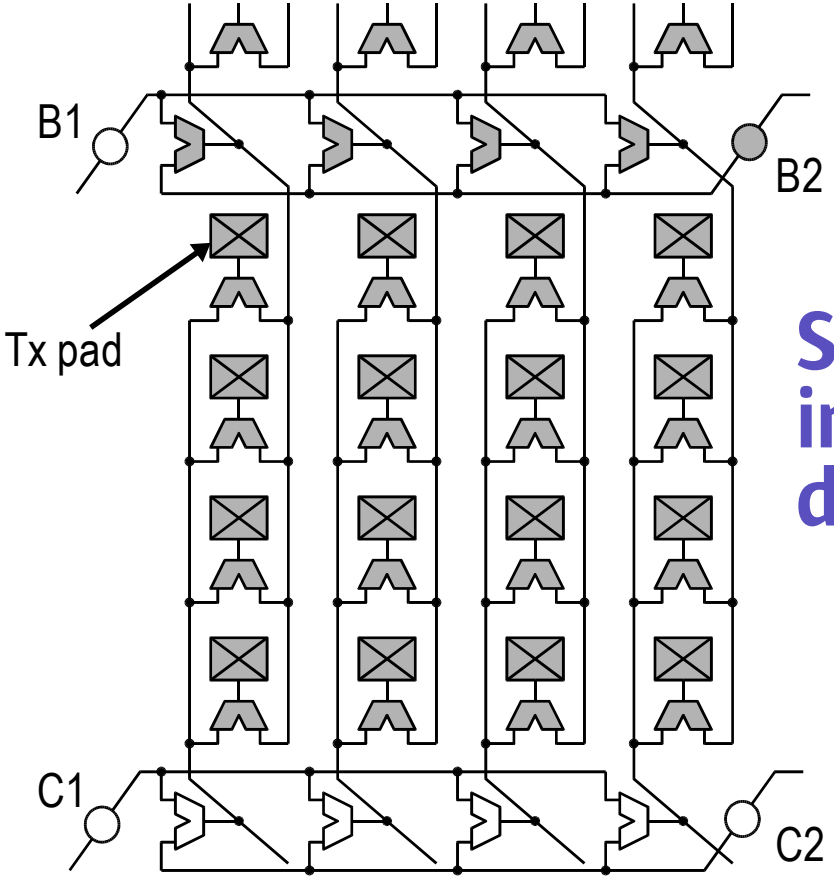
Vernier Under Misalignment



Electronic Alignment Top View

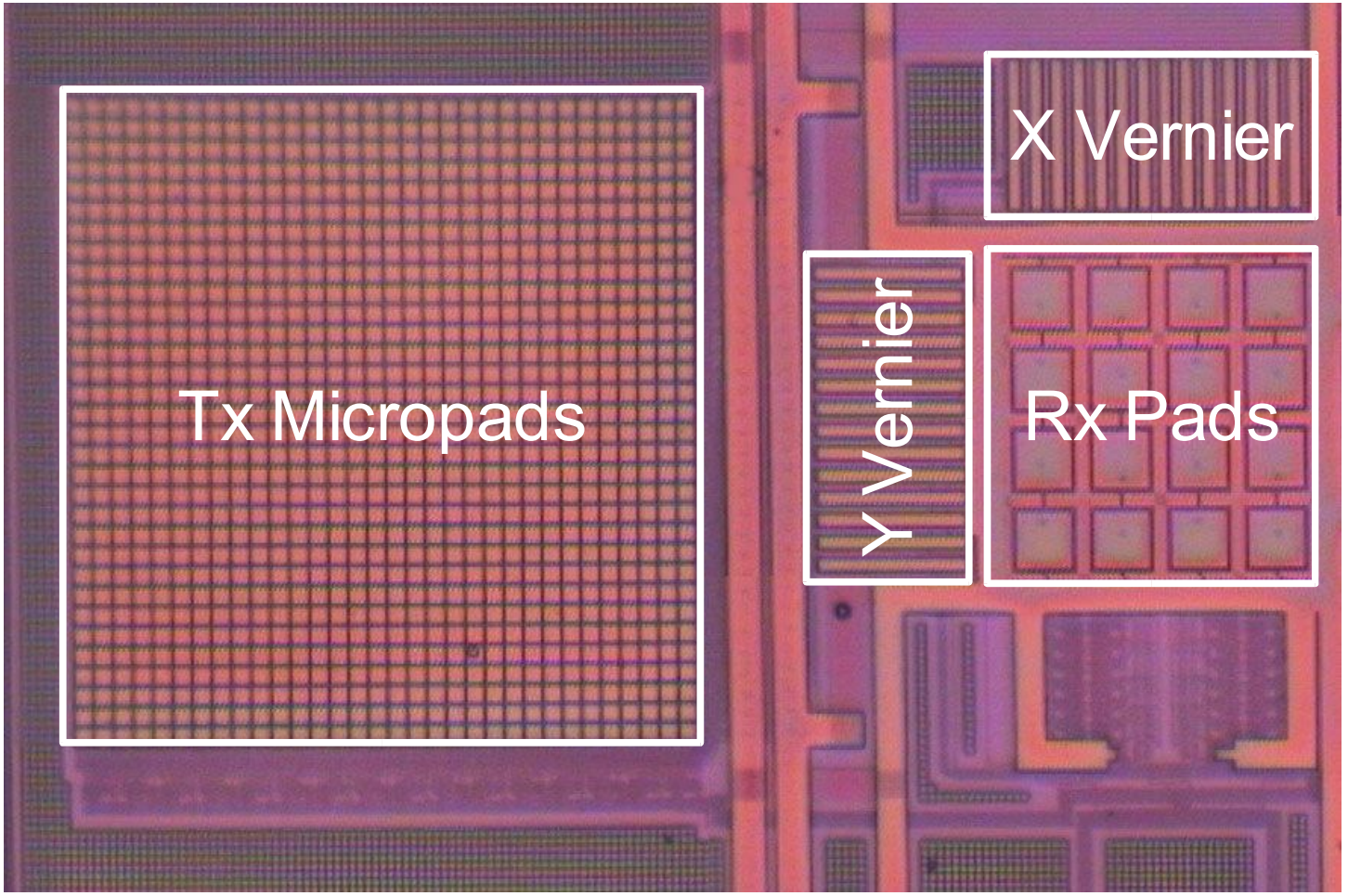


Steering Circuit One Receiver Pad Pitch

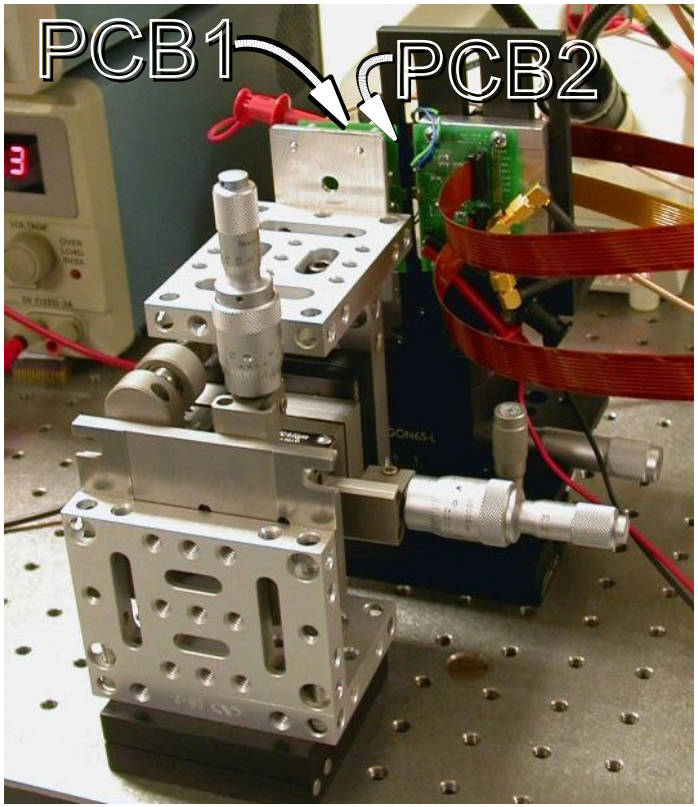


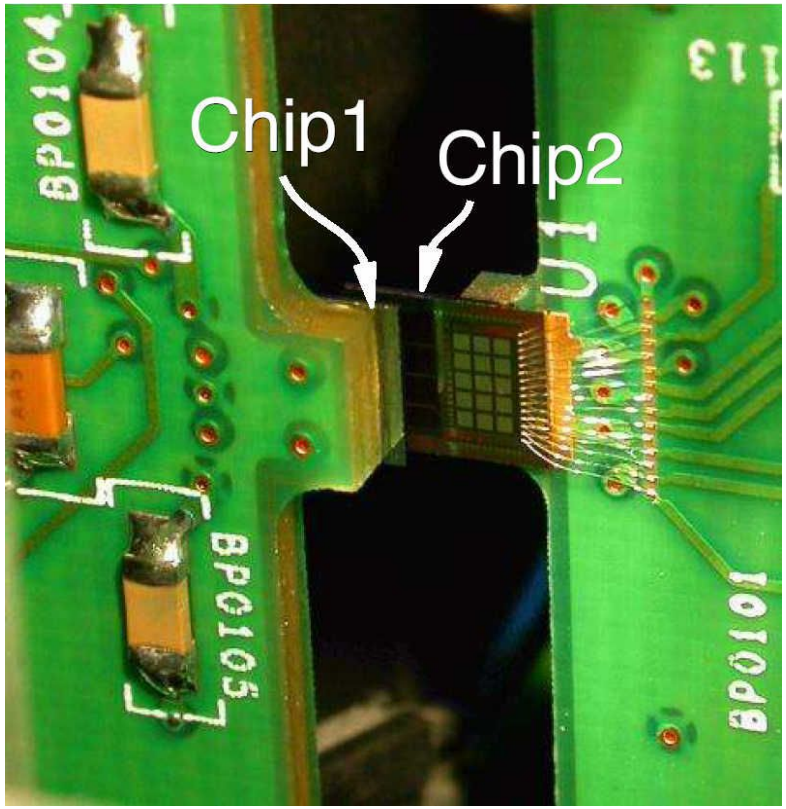
Steering in two dimensions

Chip Transceiver Photo



Experimental Setup

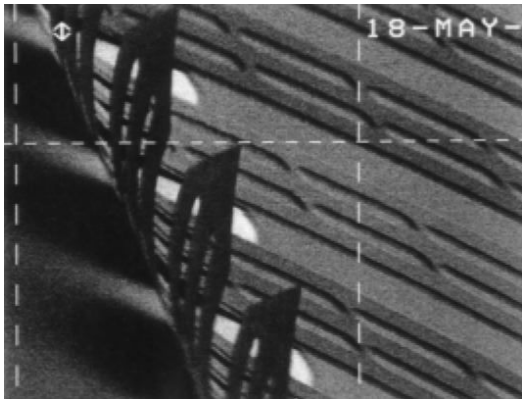




Power Connections

Microspring connectors

(Ref. 3,4)

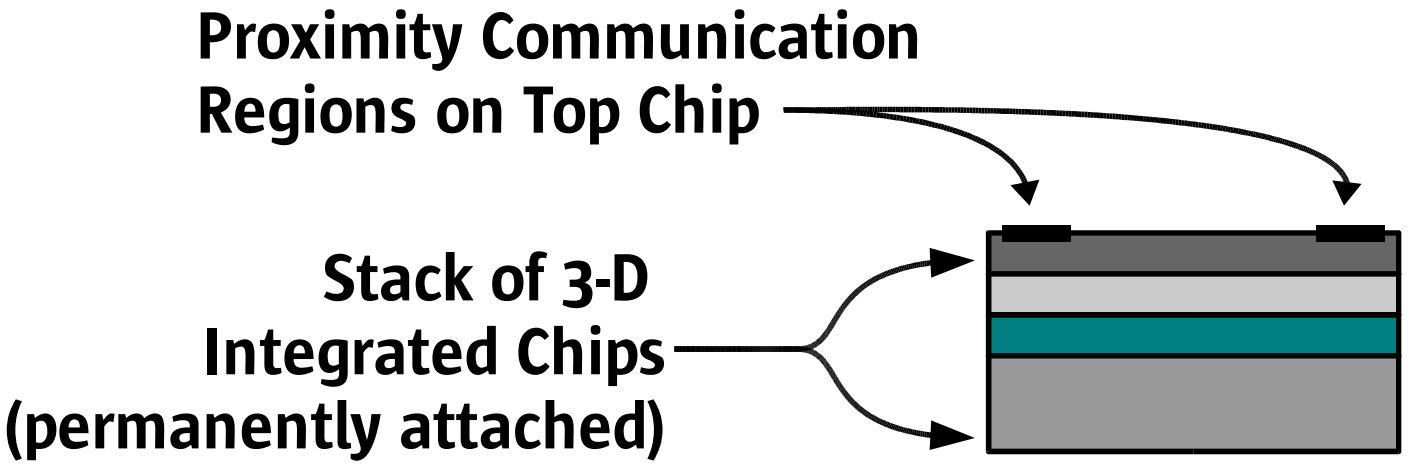


(Ref. 5)

(Ref. 3,4)

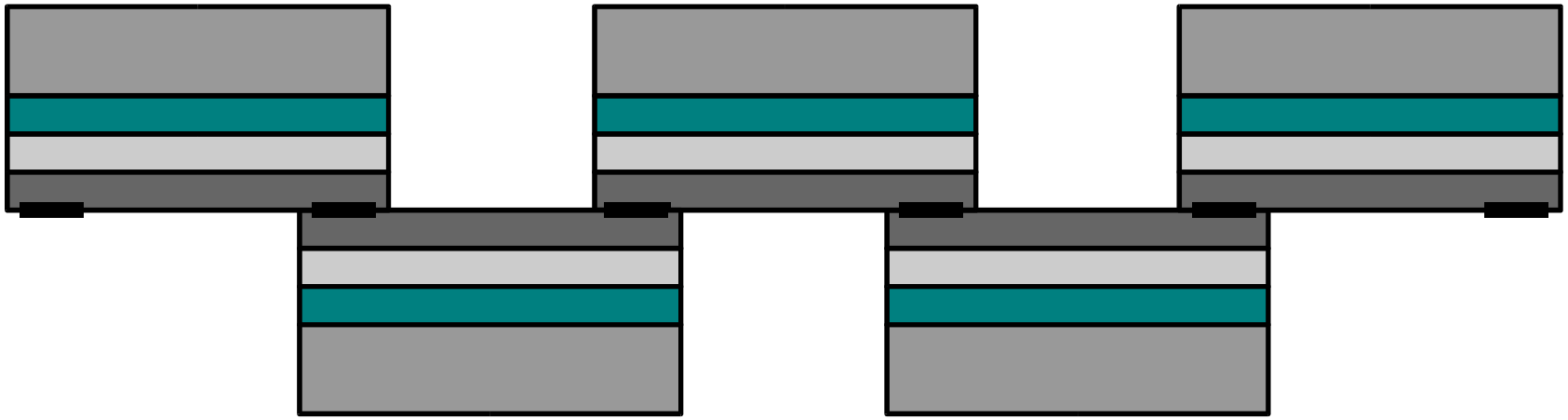
or…
Capacitive or Inductive Coupling

3-D Integration



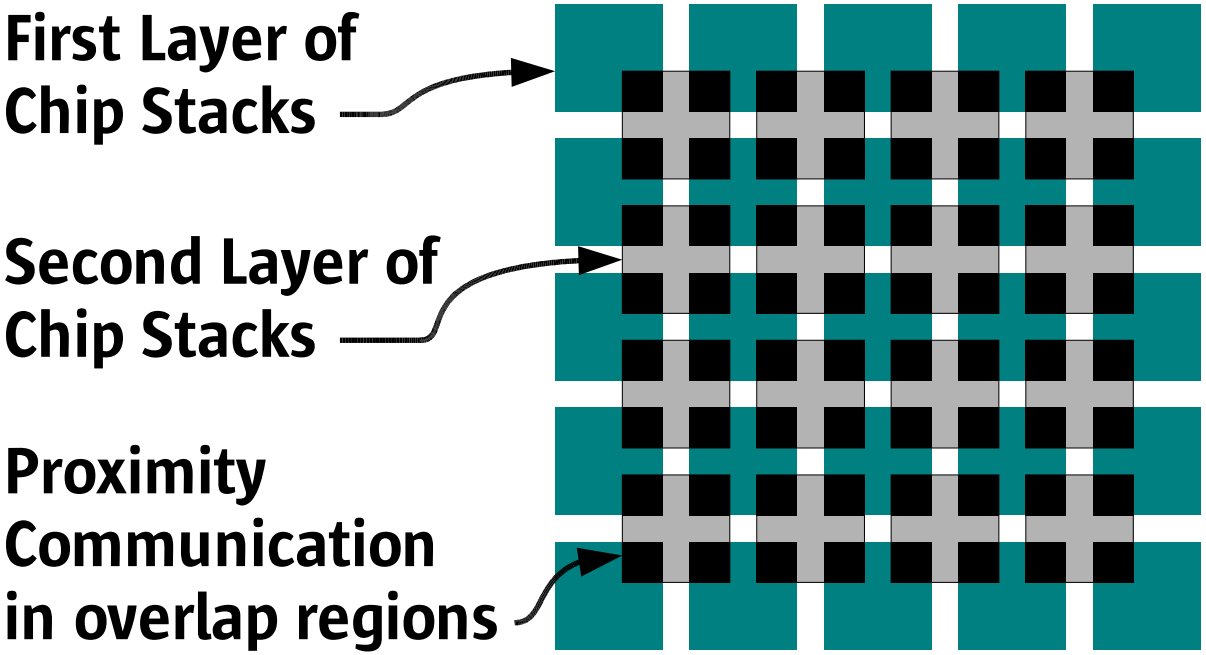
- Because of Known-Good-Die problem:
  - Limited number of chips in stack

3-D Integration



- 3-D integration provides chip stacks
- Proximity Comm. interconnects the stacks

Wafer Scale Interconnect



Summary

- Proximity Communication avoids off-chip wires
  - Increases available bandwidth per chip
  - Reduces I/O power
- Avoids permanent attachment
  - Makes chips replaceable, increases yield
  - Enhances testing capability
  - Enables wafer-scale integration

References

(1) R. Drost, R. Ho, R. D. Hopkins, I. Sutherland, "Electronic Alignment for Proximity Communication," *IEEE Int'l Solid-State Circuits Conference*, Feb. 2004.

(2) R. Drost, R. D. Hopkins, I. Sutherland, "Proximity Communications," *IEEE Custom Integrated Circuits Conference*, pp. 469-472, Sept. 2003.

(3) Microspring technology: www.formfactor.com

(4) N.L. Tracy, et al., "Array sockets and connectors using MicroSpring™ technology," *Electronics Manufacturing Technology Symposium IEEE*, pp. 129-140, Oct 2000.

(5) D. Smith and S. Alimonda, "A New Flip-Chip Technology for High-Density Packaging," *Proc. 46th Electronic Components and Technology Conf.*, May 1996.

(6) J.L. Hennessy and D.A. Patterson, Computer Organization and Design, 2nd ed., Morgan Kaufmann Publishers, San Francisco, 1997.

robert.drost@sun.com

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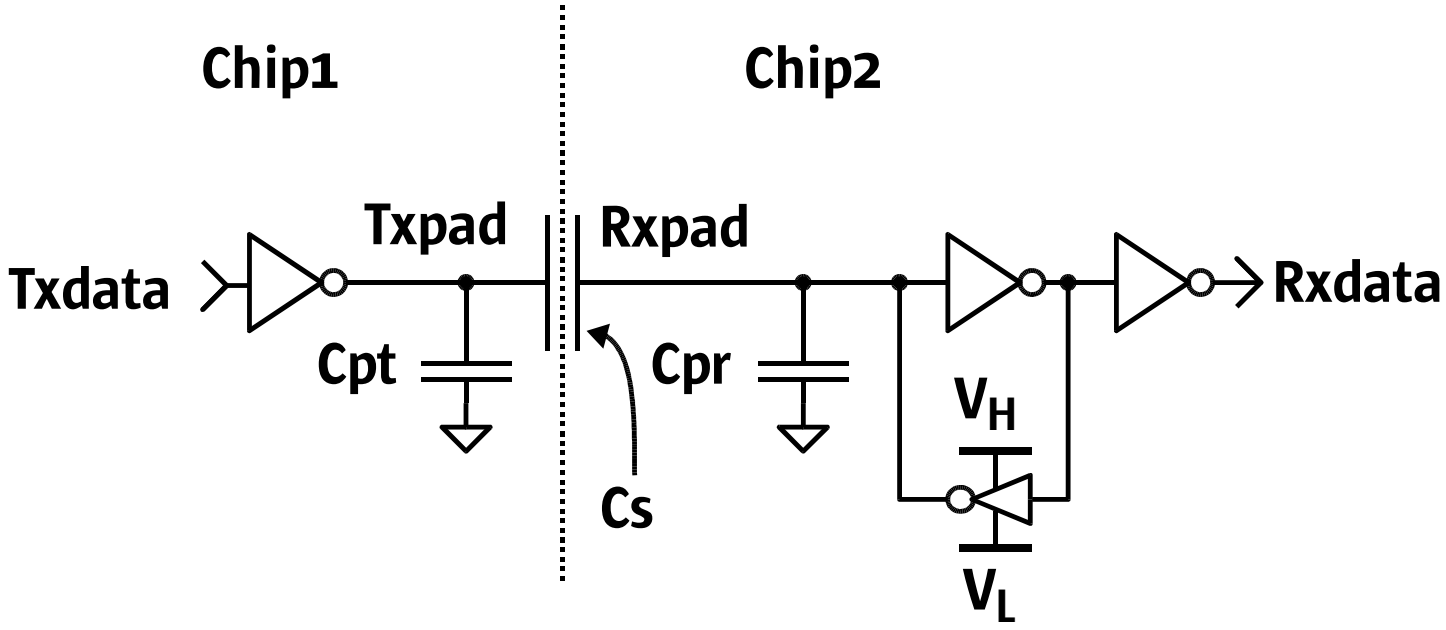
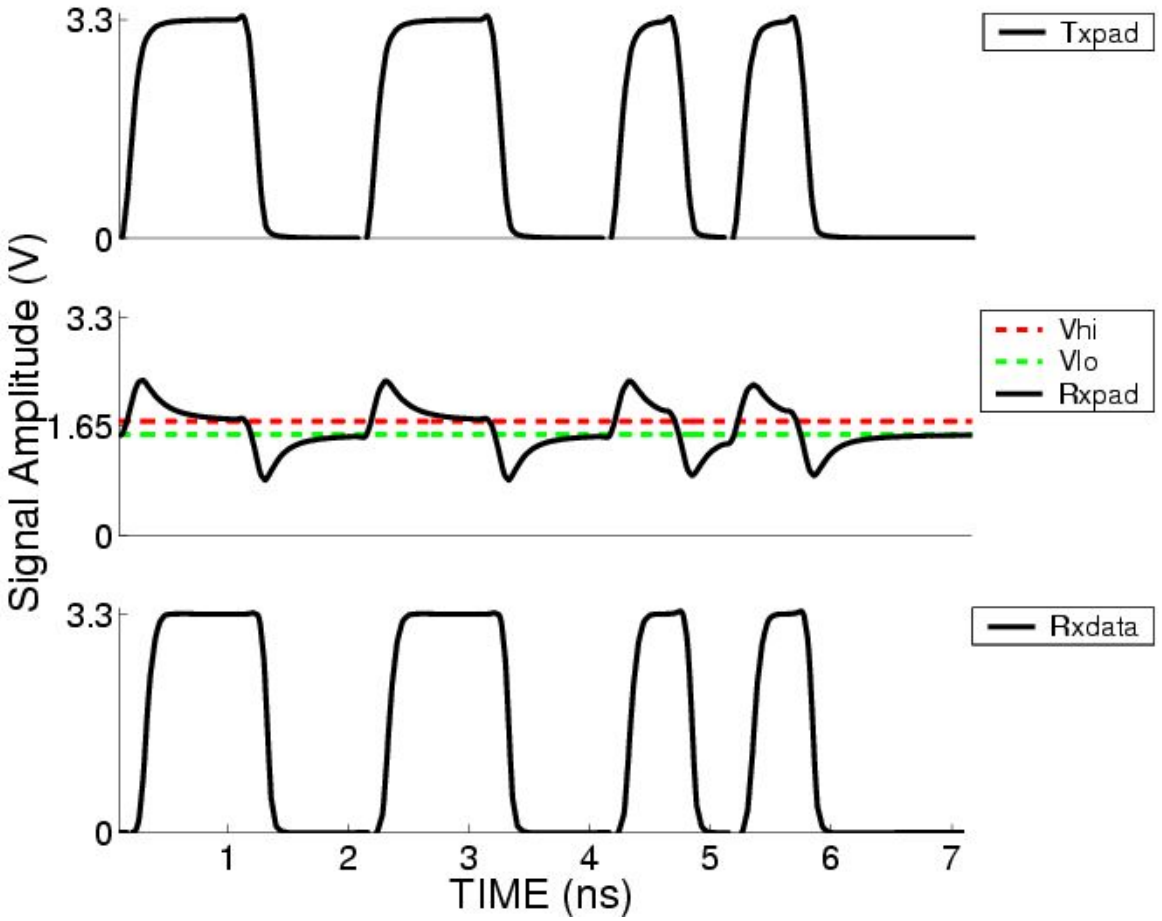
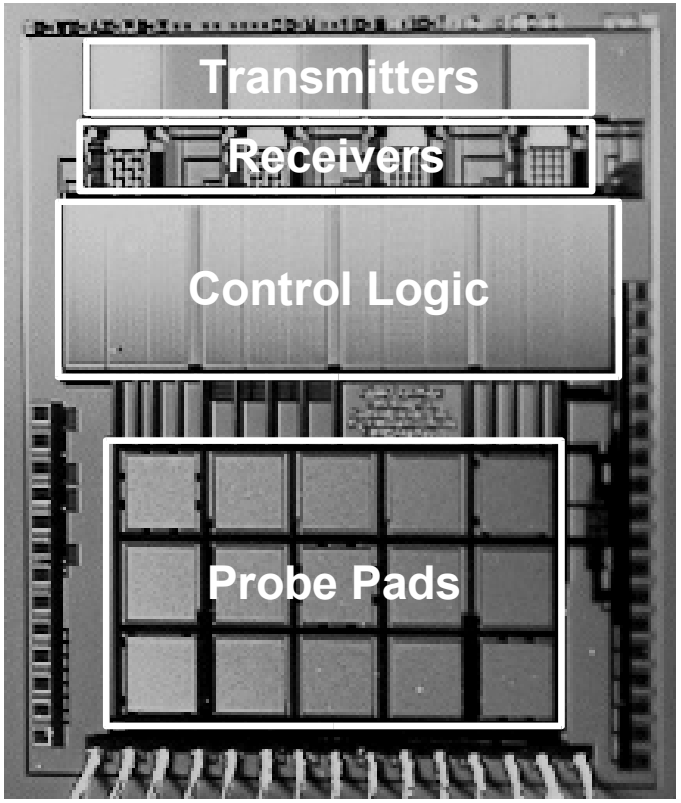
Transmit/Receive Circuits

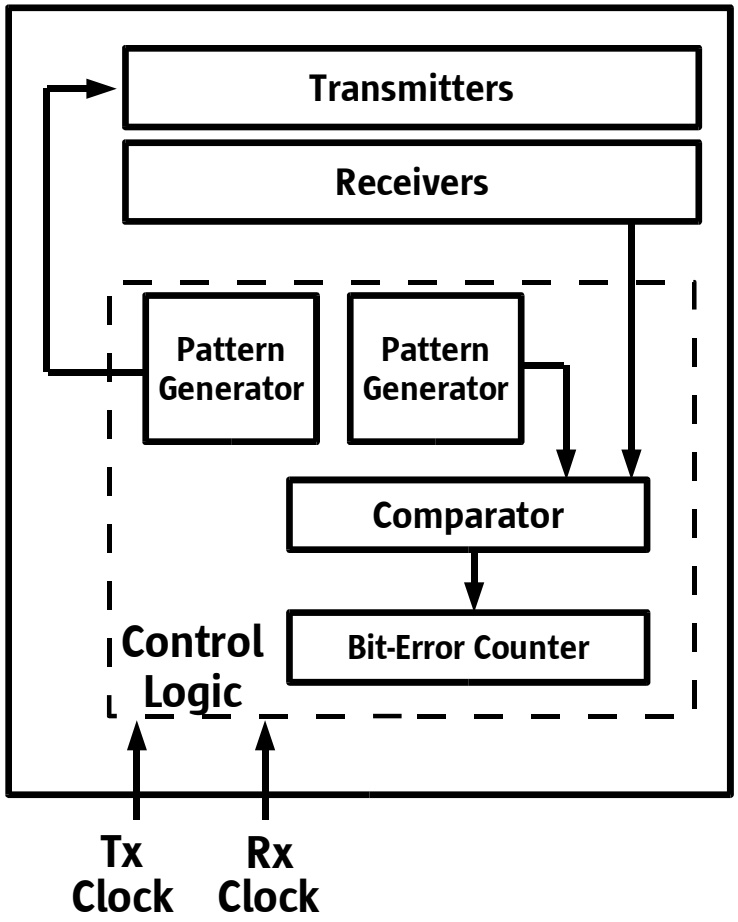


Transmit/Receive Simulated Waveforms



Test Chip


Transmitters
Receivers
Control Logic
Probe Pads


Transmitters
Receivers
Pattern Generator
Pattern Generator
Comparator
Bit-Error Counter
Control Logic
Tx Clock
Rx Clock

Test Chip Summary

Chip Size	3.6 x 4.1 mm
Chip Technology	0.35 um
Bit Pitch	50 um
Data rate for 16 simultaneously communicating channels	1.35 Gbps/channel
Bit error rate at 1 Gbps	$< 10^{-12}$
Static Power	3.6mW/channel
Dynamic Power	3.9 pJ/bit
Time margin for 16 simultaneously communicating channels at 1 Gbps	0.5 unit interval