Unusual Clock Dividers

Sometimes you need to divide a clock by odd or non-integer numbers – here are four circuits that are efficient and simple, plus they are cheaper and faster than any external PLL alternative.

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This article describes how to divide clocks by 1.5, 2.5, and by 3, and 5 with a 50% duty-cycle output. Dividing an incoming clock frequency by any integer number is trivial, and division by any even number always generates a 50% duty cycle output. However, sometimes it is necessary to generate a 50% duty cycle frequency that is not an even integer sub-multiple of the source clock.

These circuits are useful in XC4000-family and Spartan-family devices, where they are simple and efficient, and both cheaper and faster than any external phase-locked-loop alternative. Virtex devices do not need to use these tricks because they can implement these and many other functions in either of their four dedicated delay-locked-loop circuits, if the incoming clock rate is higher than 25 MHz.

How They Work

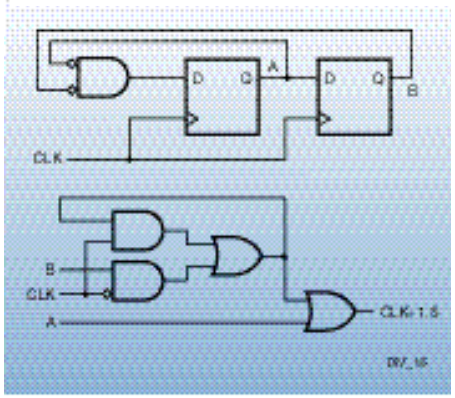
Each circuit assumes a 50/50 duty cycle of the incoming clock, otherwise the fractional divider output will jitter, and the integer divider will have unequal duty cycle. All four circuits use combinatorial feedback around a look-up table, which works perfectly and is glitch-free, but may cause your circuit simulator to fail.

These circuits have a look-up table input driven from the clock signal, with minimal skew between the A and B inputs. The chosen vertical clock line must, therefore, also have access to a LUT input. This is best achieved by coding the design as a Hard Macro.

Divide by 1.5 in One CLB.

This circuit divides the clock by 1.5, generating 60 MHz from a 90 MHz input for example (Figure1). The two flip-flops form a ÷3 circuit, and the G and H look-up tables together generate two output periods at the H output. The first output pulse is driven by the A flip-flop, the second output pulse is derived from the B flip-flop, but is delayed half an incoming clock cycle. The output stays Low while the clock is High, and stays High, after B has gone Low, until the clock goes Low again. It is this latch circuit that may cause simulator problems.

Divide by 1.5

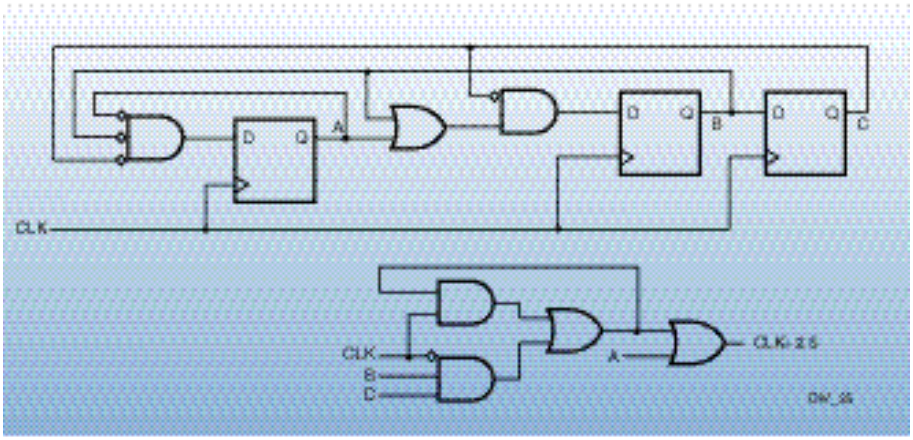


CLK	A	B	OUT
H	0	0	1
L	0	0	0
H	1	0	1
L	1	0	1
H	0	1	0
L	0	1	1

Figure 1

(Continued)

Divide by 2.5



CLK	A	B	C	OUT
H	0	0	0	0
L	0	0	0	0
H	1	0	0	1
L	1	0	0	1
H	0	1	0	0
L	0	1	0	0
H	0	1	1	0
L	0	1	1	1
H	0	0	1	1
L	0	0	1	0

Figure 2

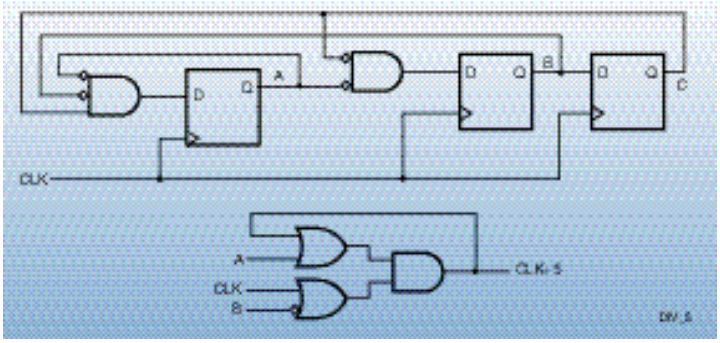
Divide by 2.5 in Two CLBs

This circuit divides the clock by 2.5, generating 40 MHz from a 100 MHz input for example (Figure 2). Three flip-flops form a ÷5 circuit, and the G and H look-up tables together generate two output periods at the H output. The first output pulse is driven by the A flip-flop, the second output pulse is derived from the B AND C signal, but is delayed half an incoming clock cycle. The output stays Low while the clock is High, and stays High after B has gone Low, until the clock goes Low again. It is this latch circuit that may cause simulator problems.

Divide by 5 with 50% Output Duty Cycle

This two-CLB circuit divides the clock by five and maintains a 50/50 output duty cycle (Figure 3). Three flip-flops form a ÷5 circuit, and the G look-up tables generate the divided output. The first output pulse is started by the A flip-flop and terminated by the B flip-flop, when the clock is Low. It is this latch circuit that may cause simulator problems.

Divide by 5



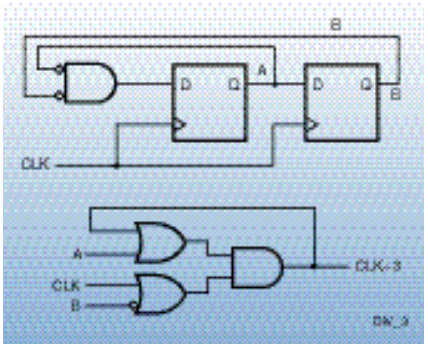
CLK	A	B	C	OUT
H	0	0	0	1
L	0	0	0	1
H	0	1	0	1
L	0	1	0	0
H	0	1	1	0
L	0	1	1	0
H	0	0	1	0
L	0	0	1	0
H	1	0	0	1
L	1	0	0	1

Figure 3

Divide by 3 with 50% Output Duty Cycle

This one-CLB circuit divides the clock by three, and maintains a 50/50 output duty cycle (Figure 4). The two flip-flops form a ÷3 circuit, and the G look-up tables generate the divided output. The first output pulse is started by the A flip-flop and terminated by B flip-flop, when the clock is Low. It is this latch circuit that may cause simulator problems.

Divide by 3



CLK	A	B	OUT
H	0	0	0
L	0	0	0
H	1	0	1
L	1	0	1
H	0	1	1
L	0	1	0

Figure 4