

# Lead Free Solder Joint Reliability Estimation by Finite Element Modelling Advantages, Challenges and Limitations

Bart Vandeveld, Mario Gonzalez, Paresh Limaye,  
Petar Ratchev, Jan Vanfleteren, Eric Beyne  
IMEC  
Leuven, Belgium

## Abstract

Finite element modelling (FEM) has been widely used for the estimation of the lifetime of solder joints subjected to temperature cycling. Thanks to the expertise of decades, a significant number of companies, universities and research institutes were able to have a relatively accurate estimation of life time for SnPb solder. For the leadfree solder materials, first attempts for correlation models show up but there are several problems. First of all, there is a wide range of alloys and alloy compositions, which have a different material behaviour (E-modulus, CTE) but also a different resistance to thermal fatigue. Second, it is shown in several papers that leadfree solders have different failure modes compared to SnPb. In particular at low temperatures (-40°C, -55°C), some leadfree materials show brittle behaviour and this is not covered by the current simulation models based on creep fatigue at high temperature. Experiments show that the trends in leadfree solder joint reliability are cycling-condition and package dependent. For long dwell times and stiff packages, leadfree assembled component show an inferior reliability compared to SnPb. In this paper, the simulation results for a wide range of packages and cycling conditions are presented and compared to experimental cycling test results. In general, the paper shows the advantages, the challenges and the limitations of FEM for leadfree solder joint simulation.

## Introduction

Increasing global concern about the environment is bringing regulatory (European directives) and consumer ("green products") pressure on the electronics industry in Europe and Japan to reduce or completely eliminate the use of lead (Pb) in products. An important date is July 2006 when Europe forbids the use of lead in electronics.

The transition from a technology using SnPb for electronic interconnections (with more than 50 years of experience) to a new lead-free technology is a challenging and demanding task for the companies. It has an impact on material supply, process equipment and conditions but also the reliability will change. Components have to withstand higher soldering temperatures (typically 20-35°C higher) and the solder joints should have at least the same life time (expressed in number of thermal cycles).

## Advantages, limitations and challenges of FEM for leadfree solder joint simulation

The **advantages** of using Finite Element modelling for estimation of life time of SnPb has been applied for decades and showed its usefulness for SnPb soldered packages. As solder joint fatigue is one of the main failure modes in electronic systems, structural design optimisation by FEM has improved the reliability of electronic systems significantly and avoided multiple prototyping and extensive experimental testing ("first time right" design).

Simulation of SnPb solder joint reliability is quite well developed and applied. The main reason of its success is that SnPb is a simple material, with a clear failure mode (cycling creep deformation, resulting in mechanical fatigue). Several issues are showing up which are typically for leadfree solder joints and makes simulation and also reliability testing much more complicated:

- How does leadfree solder materials behave at low temperature? It is known that Ag makes the solder materials more brittle (higher brittleness transition temperature). Even when creep will be lower at the higher temperatures for leadfree solder materials, the lower temperatures could be the crack initiator. Dag Andersson et al. [1] found that cracks start to grow even in the first cycles, but only in the case where temperature went down to -55°C.
- Formation of new intermetallic systems, which may result in early brittle fractures. A nice example is a SnPb solder joint on a NiAu finish of PCB. The samples failed at 1/3<sup>rd</sup> of the intrinsic fatigue life of the joint itself. Can we expect similar problems with the leadfree solder materials? Or in general, can we have unexpected failures (there is no long term reliability data available for leadfree solder materials).
- Data for all type of leadfree solder materials in all kind of compositions. SnPb will be not replaced by a single leadfree solder material. Both material data (E-modulus, CTE, creep behaviour) and correlation

models (e.g. relation between creep strain and life time) must be measured for all these new materials.

- How are the acceleration factors for leadfree solder materials. W. Engelmaier already mentioned possible appearing problems with leadfree solder joint reliability: “Leadfree solders have creep rates up to 100 times slower than the creep rates of standard Sn/Pb solders. The implication is that meaningful reliability tests cannot be very much accelerated; and that while the use of LF-solder for consumer goods like cell phones is OK, it clearly cannot as yet be recommended for high-reliability applications” [2].

The solution of all these problems will be the challenges for the simulation people.

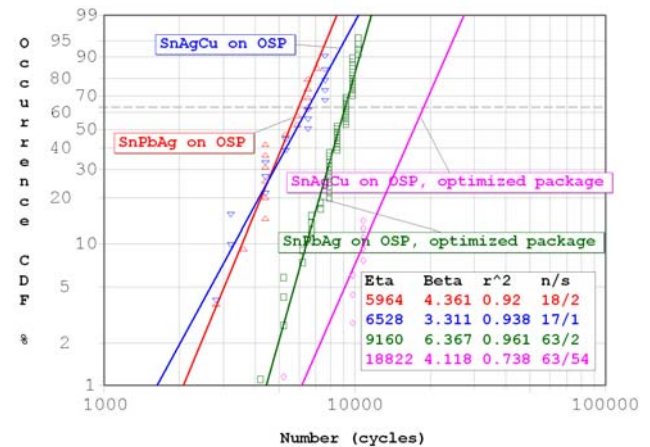
### Experimental study: different failure mode for SnAgCu solder joints

In literature, first results in thermal cycling tests for leadfree-assembled components are published [2-4]. These results depict that there is no general conclusion about the trend in life time from SnPb to SnAgCu. The main conclusion is probably that the trend is very dependent on the package type but also on the applied loading conditions ( $T_{min}$ ,  $T_{max}$ , dwell and ramp-up time). Leadfree solder materials are more creep resistant at high temperatures resulting in higher life time under similar stress conditions for the solder joint. However, the leadfree solder materials have a higher elastic modulus, which can result for certain packages in much higher stress conditions. Moreover, in some packages, the solder joints are subjected to deformations instead of forces (e.g. underfilled flip chip joints), which is often worse for the leadfree solders.

Own experiments with the Polymer Stud Grid Array (PSGA) package [5] have shown that the trend is dependent on the package (**Figure 1**):

- For the original PSGA package, the reliability of the leadfree assemblies was even lower than for SnPb (SnPb: 6528 cycles; SnAgCu: 5964 cycles).
- For the optimised PSGA package, the reliability of the leadfree assemblies is almost doubled (SnPb: 9160; SnAgCu: 18826). The optimised package differs in the overmould material, which provides a coefficient of thermal expansion (CTE) closer to the one of the package polymer body resulting in lower forces onto the solder joints.

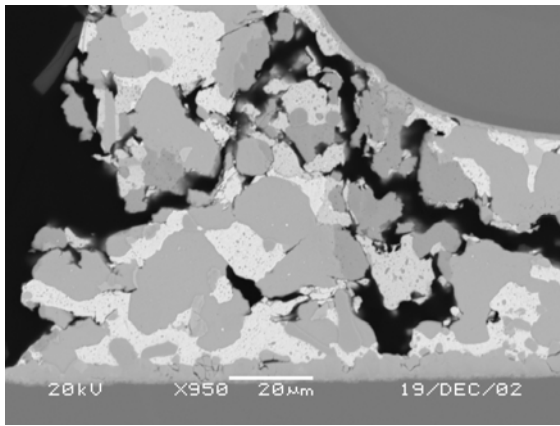
This comparison clearly shows that the trends are dependent on the type of package.



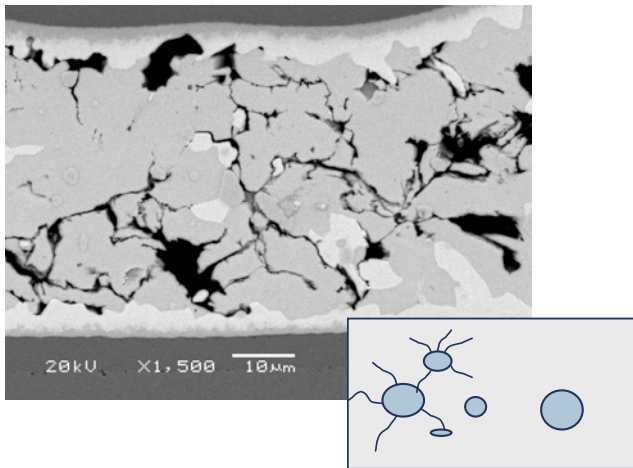
**Figure 1: PSGA thermal cycling results (-40 to 125°C, 1 hour cycle time) of original and optimised packages mounted on FR4 board.**

A different failure mode is also found for the SnAgCu solder joints [6].

- **SnPbAg:** typical solder fatigue failure is found with the crack propagating along the Sn and Pb grain interfaces (**Figure 2**).
- **SnAgCu:** also fatigue failure is observed (**Figure 3**), but the crack propagation is different from the one observed in SnPbAg. The crack propagates through the bulk of the solder in a web-like fashion linking the brittle particles in the solder volume. They are mainly (Au,Ni)Sn<sub>4</sub> particles, if Ni/Au surface finish is used or Cu<sub>6</sub>Sn<sub>5</sub> particles, formed with OSP surface finish. The softer Ag<sub>3</sub>Sn particles, typical for this solder, do not play a significant role in this process. This failure mode was not observed until now. It is also not clear if the presence of these brittle body particles are positive to the reliability or not. They can initiate cracks but they can also function as crack stoppers or crack deviators. As the tested life time is very high and as we have seen cracks stopping at the particles, we assume that these particles function as crack stoppers/deviators.

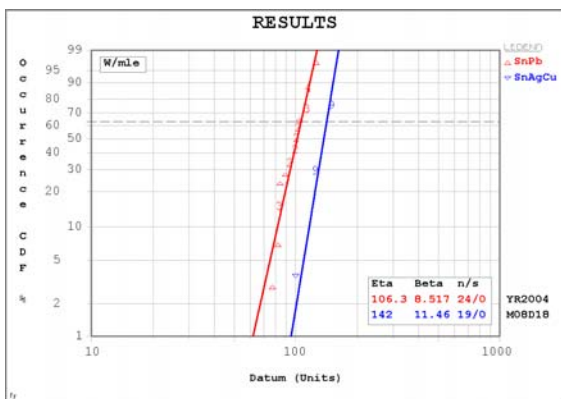


**Figure 2: Low magnification SEM picture of a corner SnPbAg solder connection.**



**Figure 3: Low magnification SEM picture of a corner SnAgCu solder connection.**

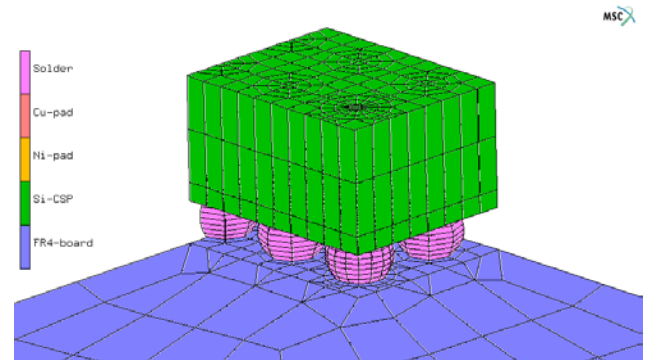
Similar work has been done for the CSP 16x6 package. Although the reliability test showed a better reliability for the leadfree assemblies, it gives no information about long term life time.



**Figure 4: Thermal cycling reliability test data for 16x6 area array CSP**

### Simulation study: thermal cycling of different packages using SnAgCu solder material

The finite element model for the 5x4 CSP package is shown in **Figure 5**. A uniform temperature cycling load is subjected to the structure and the results of the simulation are the induced deformation and stresses/strains. For this CSP, the main deformation mode of the solder joint is shear between the stiff silicon chip (2.6 ppm/°C, 169 GPa, 0.68 mm thickness) and the FR4 board (16 ppm/°C, 25 GPa, 1 mm thickness). With this model, the one-to-one comparison is simulated for the two solder materials. The simulation is also performed for two loading conditions (**Table 1**). It is expected that the trends can be dependent on the loading conditions.

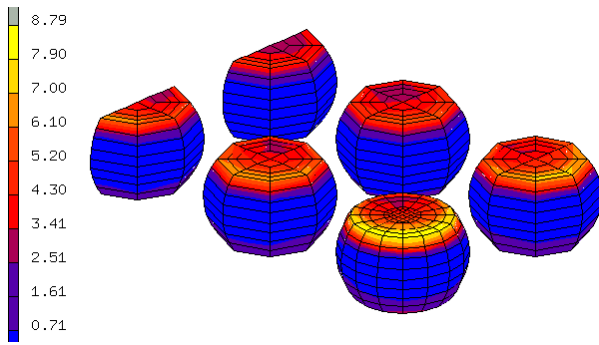


**Figure 5: Three dimensional FEM for the 5x4 CSP mounted on a 1 mm thick FR4 board.**

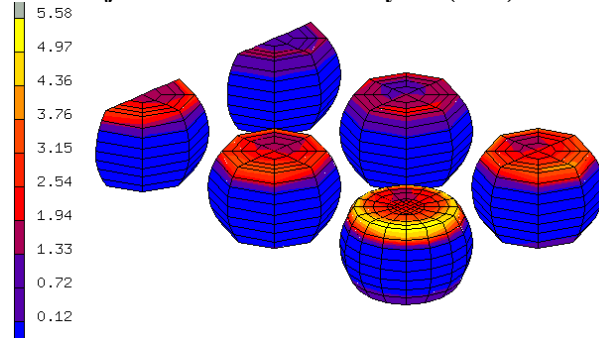
**Table 1: Three loading conditions for FEM analysis**

ID	Range	Cycle time	Ramp-up	Dwell
LC1	0 to 100°C	30 min.	5 min	10 min
LC2	-40 to 125°C	1 hour	15 min.	15 min.

As the thermal mismatch between the chip and FR4 board is linearly dependent on the DNP (distance to neutral point), the highest strains are found in corner joints. **Figure 6** and **Figure 7** compares the accumulated inelastic strain after two temperature cycles (LC2). The highest strains are in both cases in the corner solder joint and at the chip side. There is no essential difference in strain distribution between the two solders, only the size differs.



**Figure 6: Accumulated inelastic strain in SnPb solder joint after two thermal cycles (LC2).**



**Figure 7: Accumulated inelastic strain in SnAgCu solder joint after two thermal cycles (LC2).**

A method of comparing the strain values and to avoid the effects of singularity effects, is to average the strain over a limited number of elements belonging to a damage volume (selected in the area of highest strain). The results of the simulations are shown in **Table 2**. Following trends are found:

- The strains for SnAgCu are significant higher (2.72x for LC1, 1.66x for LC2). The main reason is the lower creep strain rate for SnAgCu allowing higher stresses before creep occurs.
- The acceleration factor (from LC1 to LC2) is higher for SnAgCu. This includes that more extreme thermal ranges will have more effect on SnAgCu solders (strain increase with factor 2.91 when evolving from LC1 to LC2).

**Table 2: Inelastic strain per cycle, averaged over damage volume, per thermal cycle for 5x4 CSP package.**

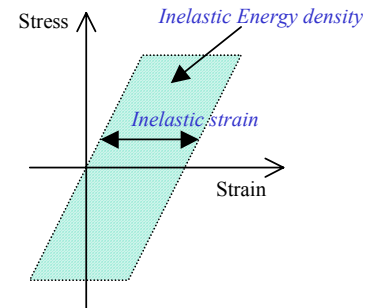
Solder	0 to 100°C	-40 to 125°C	Accel. factor
SnPb	1.17 %	2.08 %	$AF = 1.78$
SnAgCu	0.43 %	1.25 %	$AF = 2.91$
Pb / Pb-free	2.72	1.66	

Instead of relating the inelastic strain per cycle to expectation of life time, it is also possible to use the induced inelastic energy dissipation. **Table 3** shows the results and the conclusion is different from **Table 2**:

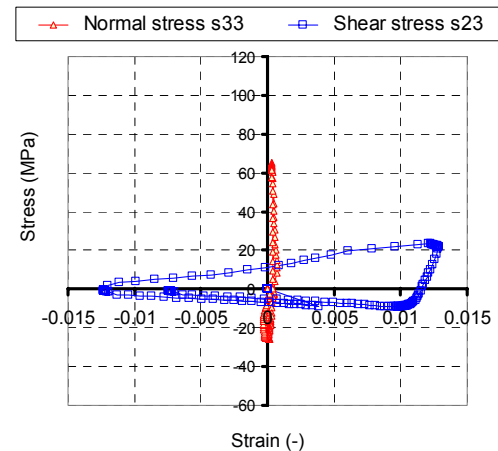
- For LC1, SnPb still scores better than SnAgCu. For LC2, the opposite trend is found. The reason for the different trend in **Table 2** vs. **Table 3** can be explained as follows. As depicted in **Figure 8**, the inelastic strain is the width of the stress-strain hysteresis loop achieved in each thermal cycle. The inelastic energy is the area of this hysteresis loop. For SnAgCu, the stresses reach much higher values during the temperature cycling, resulting in higher hysteresis loops. Although the inelastic strain for SnAgCu during LC2 is smaller (= width of the loop), the dissipated energy per cycle (= area in the loop) is higher due to the higher stresses. **Figure 9** and **Figure 10** shows the hysteresis loops for one normal and one shear stress/strain component and proves the upper statement.

**Table 3: Inelastic energy density per cycle, averaged over damage volume, per induced cycle for 5x4 CSP package.**

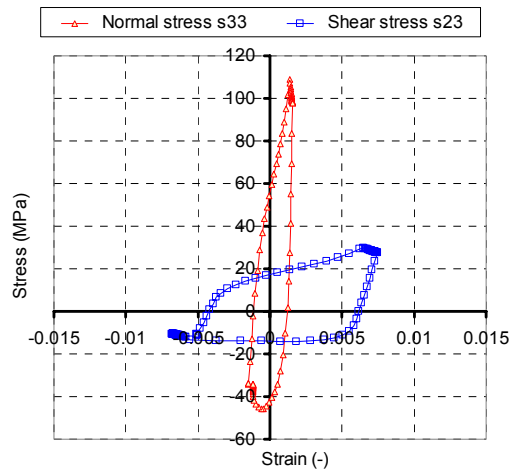
Solder	0 to 100°C	-40 to 125°C	Accel. factor
SnPb	0.263 MJ/m <sup>3</sup>	0.446 MJ/m <sup>3</sup>	$AF = 1.70$
SnAgCu	0.177 MJ/m <sup>3</sup>	0.536 MJ/m <sup>3</sup>	$AF = 3.02$
Pb / Pb-free	1.49	0.83 !!!	



**Figure 8: Schematic drawing explaining the difference between inelastic strain and inelastic strain energy density.**



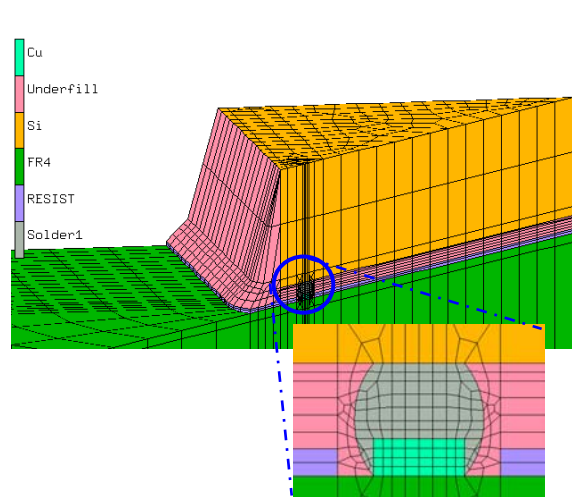
**Figure 9: Hysteresis loop for one normal and one shear component for SnPb case**



**Figure 10: Hysteresis loop for one normal and one shear stress for SnAgCu case.**

**Figure 11** shows the FEM for an underfilled  $5 \times 5 \times 0.68 \text{ mm}^3$  flip chip on a 1.6 mm thick FR4 board. An optimised underfill material is used ( $25 \text{ ppm}/^\circ\text{C}$ , 10 GPa). The deformation mode for flip chip is significantly different from the CSP. The main load is the out-of-plane thermal mismatch with the underfill [11] instead of shear for the CSP.

**Table 4** and **Table 5** shows the inelastic strain respectively inelastic energy density for this flip chip assembly. Similar trends as for CSP are found for this structure. In literature, inferior reliability was found for underfilled SnAgCu flip chip, which could be an indication that it is better to look to energy density instead of strain [4].



**Figure 11: FEM for the underfilled  $5 \times 5 \text{ mm}^2$  flip chip assembly mounted on a 1 mm thick FR4 board.**

**Table 4: Inelastic strain, averaged over damage volume, per thermal cycle for underfilled flip chip assembly**

Solder	0 to 100°C	-40 to 125°C	Accel. factor
SnPb	1.41%	2.51%	$AF = 1.78$
SnAgCu	0.73%	1.59%	$AF = 2.17$
Pb / Pb-free	1.92	1.58	

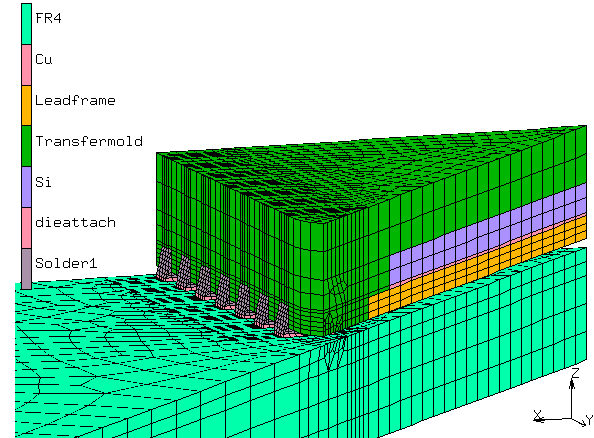
**Table 5: Inelastic energy density, averaged over damage volume, per induced cycle for underfilled flip chip assembly.**

Solder	0 to 100°C	-40 to 125°C	Accel. factor
SnPb	0.340 MJ/m <sup>3</sup>	0.510 MJ/m <sup>3</sup>	$AF = 1.50$
SnAgCu	0.311 MJ/m <sup>3</sup>	0.700 MJ/m <sup>3</sup>	$AF = 2.25$
Pb / Pb-free	1.09	0.73 !!!	

The third package that is investigated in this study is the Quad Flat Non leaded (QFN) package, which is nowadays very popular as it is a thermally enhanced package, in particular when the lead-frame is also soldered to the FR4 board.

In this FEM, there is no solder applied in the area between the lead-frame and the PCB. The results are shown in

**Table 6.** When applying SnAgCu, almost no inelastic strains were induced in the solder. The same conclusion is true when analysing the energy density. The main reason is that SnAgCu can support much higher stresses before creep occurs, and it seems that these higher stresses are sufficient to compensate the thermal mismatch between the package and board. For this package, it seems that the lead-free SnAgCu gives a much higher solder reliability than its SnPb alternative.



**Figure 12: FEM for the 56 pins QFN package assembled to an FR4 board.**



**Table 6: Inelastic strain, averaged over damage volume, per thermal cycle for 56 pins QFN package**

Solder	0 to 100°C	-40 to 125°C	Accel. factor
SnPb	0.44	0.88	$AF = 2.00$
SnAgCu	0.07	0.19	$AF = 2.71$
Pb / Pb-free	6.29	4.63	

#### Acknowledgments

This work has been supported by the EC-Growth GRD1-2001-40712 project with acronym IMECAT ([www.imec.be/IMECAT](http://www.imec.be/IMECAT)).

The authors also would like to thank the people from the ACOSTE and MSR group within IMEC for their support to this paper.

#### References

- [1] C. Andersson, D. Andersson, P-E Tegehall, Johan Liu, Effect of different temperature cycle profiles on the crack propagation and microstructural evolution of real lead free solder joints of different electronic components, Eurosime04 conference, May 9-12, 2004, Brussels, Belgium.
- [2] W. Engelmaier, Reliability of leadfree solder joints revisited, Global SMT & Packaging, Nove 2003.
- [3] Bartelo, J., Cain, S. R., Caletka, D., Darbha, K., Gosselin, T., Henderson, D. W., King, D., Knadle, K., Sarkhel, A., Thiel, G. and Woychik, C., "Thermomechanical fatigue behavior of selected lead-free solders", Proceedings, IPC SMTA Council APEX 2001.
- [4] P. Chalco and E. Blackshear, Reliability issues of BGA packages attached with lead-free solder, Proceedings InterPack01, The Pacific Rim / ASME International Electronic Packaging Technical Conference, July 8-13, 2001, Kauai, Hawaii.
- [5] A. Schubert, R. Dudek, E. Auerswald, A. Gollhardt, B. Michel, H. Reichl, Fatigue Life Models for SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulation, pp 603-610, ECTC 2003, New Orleans, US.
- [6] P. Ratchev, B. Vandevelde and I. De Wolf, Reliability and Failure analysis of SnAgCu solder interconnections for PSGA packages on Ni/Au surface finish, IEEE Transactions on Device and Materials Reliability, Vol. 4, no.1, March 2004.
- [7] S. Wiese, E. Meusel, K.J. Wolter, Microstructural Dependence of Constitutive Properties of Eutectic SnAg and SnAgCu Solders, proceedings of the 53rd Electronic Components and Technology Conference, 2003, Page(s): 197-206.