R2880
Data Sheet - BGA
FAST ETHERNET RISC PROCESSOR

RDC ***RISC DSP Communication***

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1. Overview

The R2880 is a high performance and high integration network processor. It includes RDC's proprietary RISC processor core, DMA controller, Timer/Watch dog, INT controller, 16 byte FIFO UART, SDRAM controller, Flash/SRAM controller, GPIO, 10/100M MAC, PCI & Cardbus interface … etc. The running frequency for R2880 is up to 100MHz and it is in LFBGA 225-package.

2. Features

- **CPU Core**

- RDC's proprietary RISC architecture.
- Five-Stage Pipeline Architecture.
- Speed up to 100 MHz
- Supports an 8K-byte Uniform cache

- **ROM/RAM/SDRAM Controller and Addressing**

- Supports 16-bit Data Bus Width
- Flash ROM/SRAM control interface
- SDRAM control interface
- 16M Addressing
- 64K byte I/O space

- **Two Independent DMA Controllers**

- **Interrupt Controller**

- Provides 8 maskable external interrupt channels

- **Counter/Timers**

- Three independent 16-bit timers
- Timer 1 can be programmed as a watchdog timer

- **High Performance UART Ports**

- Supports 2 High Performance UARTs with Send/Receive 16-byte FIFO
- Programmable Baud Rate Generator
- The data rates are programmable from 50 to 460.8K baud (Max to 1Mbps)
- The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd or no parity, 5~8 Data bit

- **RDC Debug Tool Support**

- RDC debug tool with JTAG-like interface

- **General Programmable I/O**

- 48 programmable I/O ports.
- Pins individually configurable to input or output.

- **Two 10/100M Fast Ethernet MAC ports**

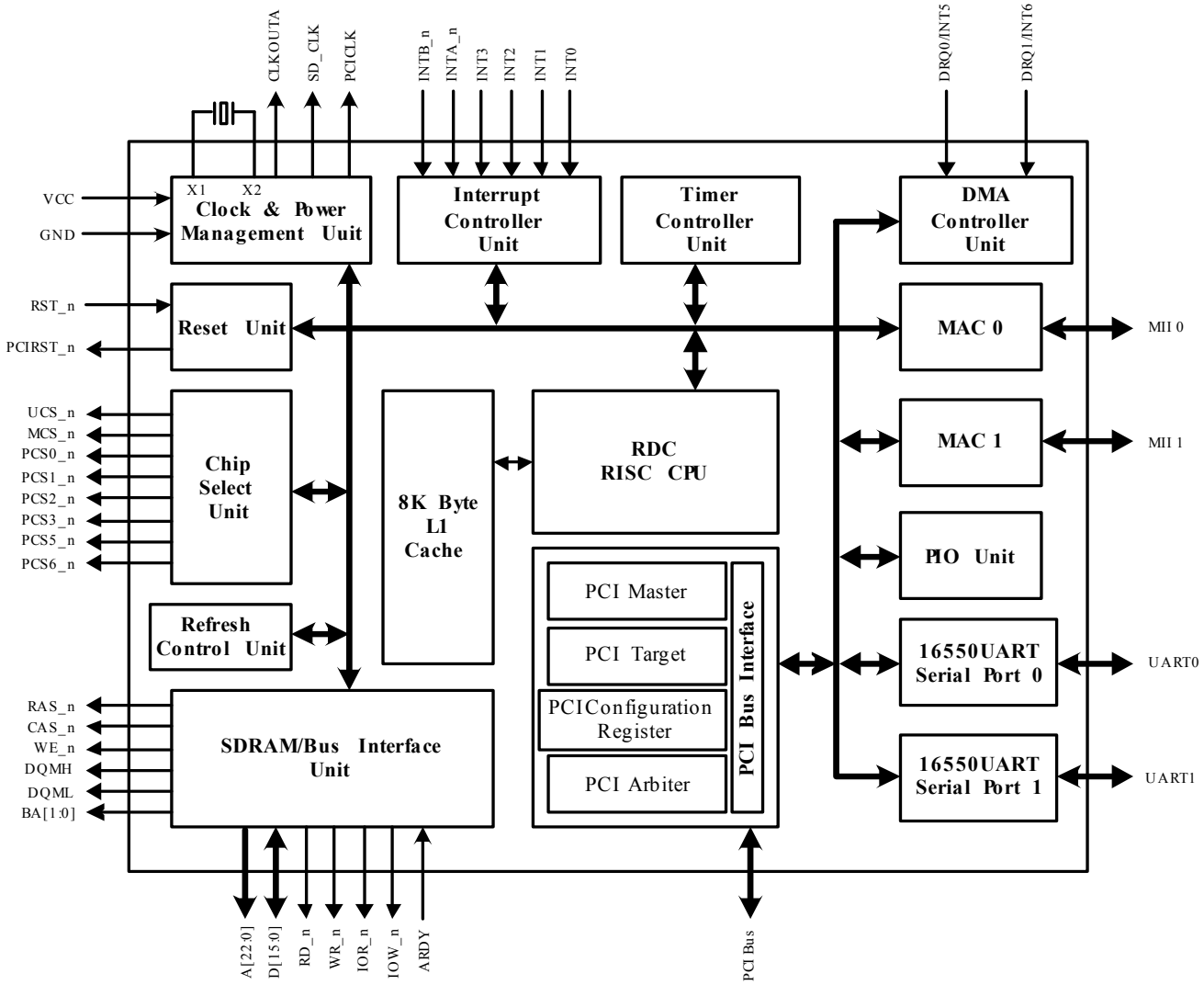
- IEEE 802.3u MII interface
- IEEE 802.3x flow control in full-duplex mode
- Internal Loop-back self test circuit support
- Descriptor architecture for packet Tx/Rx

- **PCI Control Interface Support**

- Supports up to 5 PCI Master
- Speed up to 33 MHz

- **Two Card Bus Interface Support**

3. Block Diagram



4. Pin Description

4.1 PINout Table

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
A1	PAD31	D13	TXD1_3	H10	GND_IO	M7	D1
A2	PAD27	D14	TXD1_0	H11	VDD_IO	M8	D5
A3	PAD24	D15	TXC1	H12	TXD0_1/PIO41	M9	D14
A4	PAD23	E1	UCS_n	H13	TXD0_0/PIO40	M10	D11
A5	PAD20	E2	PCS2_n/PREQ2_n/PIO18	H14	TXD0_3/PIO43	M11	DQMH
A6	PAD17	E3	PCS1_n/CFRAME1_n	H15	RXC0	M12	A0/MA0
A7	IRDY_n	E4	PCS0_n/CFRAME0_n	J1	DTR1_n/SAD9/PIO31	M13	RAS_n
A8	DEVSEL_n	E5	PCS5_n/PREQ3_n/PIO20	J2	DCD1_n/SAD12/PIO34	M14	A10/MA10/BSEL
A9	C/BE1_n	E6	VDD_CORE	J3	DSR1_n/SAD11/PIO33	M15	RST_n
A10	PAD12	E7	VDD_IO	J4	CTS1_n/SAD10/PIO32	N1	SA4/PIO4
A11	PAD8	E8	VDD_IO	J5	VDD_IO	N2	SA2/PIO2
A12	PAD7	E9	VDD_IO	J6	GND_IO	N3	SA0/PIO0
A13	PCICLK	E10	VDD_CORE	J7	GND_IO	N4	A21/SA17
A14	PAD3	E11	VDD_CORE	J8	GND_CORE	N5	A17/SAD5
A15	TXD1_2	E12	RXD1_3	J9	GND_CORE	N6	A15/SAD3
B1	DRQ1/INT6/PGNT4_n	E13	RXD1_1	J10	GND_IO	N7	D0
B2	PGNT0_n	E14	RXD1_2	J11	VDD_IO	N8	D4
B3	PAD29	E15	RXDV1	J12	RXD0_3/PIO47	N9	D15
B4	PAD26	F1	SA15/PIO15	J13	RXD0_0/PIO44	N10	D10
B5	C/BE3_n	F2	MCS_n/PIO22	J14	RXD0_1/PIO45	N11	A11/MA11/JTAGEN
B6	PAD18	F3	INTB_n	J15	RXD0_2/PIO46	N12	A5/MA5/BYPASS
B7	C/BE2_n	F4	INTA_n	K1	RI1_n/SAD13/PIO35	N13	CAS_n
B8	PAR	F5	VDD_CORE	K2	SIN1/SAD14/PIO26	N14	BA0
B9	PAD13	F6	GND_CORE	K3	INT3/PIO25	N15	A2/MA2
B10	PAD11	F7	GND_IO	K4	SOUT1/SAD15/PIO27	P1	SA3/PIO3
B11	C/BE0_n	F8	GND_IO	K5	VDD_CORE	P2	A22/SA18/ALE
B12	PAD0	F9	GND_CORE	K6	GND_CORE	P3	A18/SAD6
B13	PCIRST_n	F10	GND_IO	K7	GND_CORE	P4	RD_n
B14	COL1	F11	VDD_IO	K8	GND_IO	P5	A19/SAD7
B15	TXD1_1	F12	MDC	K9	GND_IO	P6	A13/SAD1
C1	DRQ0/INT5/PREQ4_n	F13	RXD1_0	K10	GND_CORE	P7	IOW_n/PIO17
C2	PREQ0_n	F14	MDIO	K11	VDD_CORE	P8	D3
C3	PGNT1_n	F15	CLKOUTA	K12	SOUT0	P9	DQML
C4	PAD30	G1	SA13/PIO13	K13	DSR0_n/TCK/PIO38	P10	D12
C5	PAD25	G2	SA14/PIO14	K14	SIN0	P11	D8
C6	PAD21	G3	SA12/PIO12	K15	RXDV0	P12	A9/MA9
C7	PAD16	G4	SA11/PIO11	L1	INT2/PIO24	P13	A6/MA6/PCKD0
C8	TRDY_n	G5	VDD_IO	L2	INT1/PIO23	P14	WE_n
C9	PAD14	G6	GND_CORE	L3	SA6/PIO6	P15	BA1
C10	PAD9	G7	GND_CORE	L4	SA7/PIO7	R1	WR_n

Ball No.	Function	Ball No.	Function	Ball No.	Function	Ball No.	Function
C11	PAD4	G8	GND_IO	L5	VDD_PLL	R2	X1
C12	PAD1	G9	GND_CORE	L6	GND_PLL	R3	X2
C13	PAD5	G10	GND_CORE	L7	VDD_IO	R4	A14/SAD2
C14	TXEN1	G11	VDD_IO	L8	VDD_IO	R5	A12/SAD0
C15	RXC1	G12	TXEN0	L9	VDD_IO	R6	IOR_n/PIO16
D1	PCS3_n/PGNT2_n/PIO19	G13	COL0	L10	VDD_CORE	R7	D2
D2	PCS6_n/PGNT3_n/PIO21	G14	TXD0_2/PIO42	L11	A1/MA1	R8	D6
D3	PREQ1_n	G15	TXC0	L12	CTS0_n/TMS/PIO37	R9	D7
D4	PAD28	H1	SA8/PIO8	L13	RTS0_n/TDO/PIO36	R10	D13
D5	PAD22	H2	RTS1_n/SAD8/PIO30	L14	A3/MA3/DIVID	R11	D9
D6	PAD19	H3	SA9/PIO9	L15	DCD0_n/TDI/PIO39	R12	SD_CLK
D7	FRAME_n	H4	SA10/PIO10	M1	INT0/BHE_n/PIO29	R13	A8/MA8/CLKSEL
D8	STOP_n	H5	VDD_IO	M2	SA5/PIO5	R14	A7/MA7/PCKD1
D9	PAD15	H6	GND_IO	M3	SA1/PIO1	R15	A4/MA4
D10	PAD10	H7	GND_CORE	M4	A20/SA16		
D11	PAD6	H8	GND_IO	M5	A16/SAD4		
D12	PAD2	H9	GND_IO	M6	ARDY/PIO28		

4.2 Functional Description

I = Input;

O = Output;

PU = Pull up 75KΩ;

PD = Pull down 75KΩ;

PU* = Pull up 75KΩ when the PIOn pin is used;

PD* = Pull down 75KΩ when the PIOn pin is used;

● CPU Core (4 PINs)

Ball No.	Symbol	Type	Description
M15	RST_n	I/PU	Reset input with Schmitt trigger. When RST_n is asserted, the CPU immediately terminates all operations, clears the internal registers & logic, and changes the address to the reset address FFFF00h.
R2	X1	I	25MHz frequency input, within 100 ppm tolerance, to the amplifier (oscillator).
R3	X2	O	Frequency output from the inverting amplifier (oscillator).
F15	CLKOUTA	O	The CLKOUTA output frequency is the same as the X1 input frequency. When CLKSEL = 1, the frequency of CLKOUTA is equal to that of PCICLK. When CLKSEL = 0, the frequency of CLKOUTA is equal to that of X1.

● Bus Interface (42 PINs)

Ball No.	Symbol	Type	Description
P4	RD_n	O	Read Strobe. One active low signal indicates that the micro-controller is performing a memory or I/O read cycle. RD_n floats during a bus hold or reset.
R1	WR_n	O	Write strobe. This pin indicates that the data on the bus is to be written into a memory or an I/O device. WR_n is active during T2, T3, and Tw of any write cycle, floating during a bus hold or reset.
M12 L11 N15	A0/MA0 A1/MA1 A2/MA2	O	A[2:0]: Address bus 2 to 0. Non-multiplexed memory or I/O addresses. The address bus is one-half of a SD_CLK period earlier than the D bus. The address bus is in a high-impedance state during a bus hold or reset. MA[2:0]: The SDRAM raw and column address output.

L14 P13	A3/MA3/DIVID A6/MA6/PCKD0	O/I/PU	A[7:3]: Address bus 7 to 3. Non-multiplexed memory or I/O addresses. The address bus is one-half of a SD_CLK period earlier than the D bus. The address bus is in a high-impedance state during a bus hold or reset. MA[7:3]: The SDRAM raw and column address output. DIVID: PLL Clock out Frequency Selection 0: x3 1: x4
R15 N12 R14	A4/MA4 A5/MA5/BYPASS A7/MA7/PCKD1	O/I/PD	BYPASS: PLL Clock out Bypass 0: Normal operation 1: Bypass Mode PCKD[1:0]: PCI Clock Selection 00: /2 01: /3 10: /4 11: /5 *Note: A4/MA4 must be pulled down for normal operation.*
R13 P12 M14 N11	A8/MA8/CLKSEL A9/MA9 A10/MA10/BSEL A11/MA11/JTAGEN	O/I/PD	A[11:8]: Address bus. Non-multiplexed memory or I/O addresses. The address bus is one-half of a SD_CLK period earlier than the D bus. The address bus is in a high-impedance state during a bus hold or reset. MA [11:8]: The SDRAM raw and column address output. CLKSEL: CLOCKOUTA Output Frequency Selection. 0: CLKOUTA = 25MHz 1: CLKOUTA = PCICLK (33MHz) BSEL: Boot ROM Bus Width Selection. 0: 8 bit 1: 16 bit JTAGEN: JTAG function enable. Default is pulled low and disabled. *Note: A9/MA9 must be pulled down for normal operation.*
R5 P6 R4 N6 M5 N5 P3 P5	A12/SAD0 A13/SAD1 A14/SAD2 A15/SAD3 A16/SAD4 A17/SAD5 A18/SAD6 A19/SAD7	I/O	A[19:12]: Address bus. Non-multiplexed memory or I/O addresses. The address bus is one-half of a SD_CLK period earlier than the D bus. The address bus is in a high-impedance state during a bus hold or reset. SAD [7:0]: The combination pins with addresses and data. They are designed for slower peripheral bus.
M4	A20/SA16	O	A[22:20]: Address bus. Non-multiplexed memory or I/O

N4 P2	A21/SA17 A22/SA18/ALE		addresses. The address bus is one-half of a SD_CLK period earlier than the D bus. The address bus is in a high-impedance state during a bus hold or reset. SA[18:16]: The slow bus address 16, 17 and 18. ALE: Address latch enable. Active high. This pin indicates an address output on the D bus. Address is guaranteed to be valid on the trailing edge of ALE.
N7 M7 R7 P8 N8 M8 R8 R9 P11 R11 N10 M10 P10 R10 M9 N9	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	I/O	Data bus for memory or I/O access. The D bus is in a floating state during a bus hold or reset condition and this bus can also be used to load system configuration information (with pull-up or pull-low resistor) into the RESCON register when RST_n goes from low to high and the Watchdog timeout is reset.
E1	UCS_n	O	Upper memory chip select. UCS_n is active low when the system accesses the defined portion of the upper 8M bytes (800000-FFFFFF) memory block. UCS_n default active address region is from FF0000h to FFFFFFh after power-on reset. The address range for UCS_n is programmed by software. This pin incorporates a weak pull-up resistor.

● SDRAM Interface (8 PINs)

Ball No.	Symbol	Type	Description
R12	SD_CLK	O	SDRAM clock output. This clock output is from internal De-skew PLL. It can be three to six multiple of input clock X1.
P14	WE_n	O	SDRAM/EDO write enable.
N13	CAS_n	O	SDRAM column address selector.
M13	RAS_n	O	SDRAM raw address selector.
P15, N14	BA[1: 0]	O	SDRAM bank address 1 & 0.
P9	DQML	O	Input/Output mask.
M11	DQMH	O	Input/Output mask.

● MII Interface (28 PINs)

Ball No.	Symbol	Type	Description
H13 H12 G14 H14	TXD0_0/PIO40 TXD0_1/PIO41 TXD0_2/PIO42 TXD0_3/PIO43	I/O/PU*	Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal. PIO: General purpose PIN.
G15	TXC0	I/PU	Supports the transmit clock supplied by the external PMD device. This clock should always be active.
H15	RXC0	I/PU	Supports the receive clock supplied by the external PMD device. This clock should always be active.
K15	RXDV0	I/PD	Data valid is asserted by an external PHY when the received data is present on the RXD [3:0] lines and is de-asserted at the end of the packet. This signal should be synchronized with the RXC signal.
J13 J14 J15 J12	RXD0_0/PIO44 RXD0_1/PIO45 RXD0_2/PIO46 RXD0_3/PIO47	I/O/PU*	Four parallel receiving data lines. This data is driven by an external PHY attached to the media and should be synchronized with the RXC signal. PIO: General purpose PIN.
G13	COL0	I/PD	This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
G12	TXEN0	O	This pin functions as transmit enable. It indicates that a transmission to an external PHY device is active on the MII port.
D14 B15 A15 D13	TXD1_0 TXD1_1 TXD1_2 TXD1_3	O	Four parallel transmit data lines. This data is synchronized to the assertion of the TXC signal and is latched by the external PHY on the rising edge of the TXC signal.
C14	TXEN1	O	This pin functions as transmit enable. It indicates that a transmission is active on the MII port to an external PHY device.
D15	TXC1	I	Supports the transmit clock supplied by the external PMD device. This clock should always be active.
C15	RXC1	I	Supports the receive clock supplied by the external PMD device. This clock should always be active.
F13 E13 E14 E12	RXD1_0 RXD1_1 RXD1_2 RXD1_3	I/PD	Four parallel receive data lines. This data is driven by an external PHY that the media is attached and should be synchronized with the RXC signal.
E15	RXDV1	I/PD	Data valid is asserted by an external PHY when the received data is present on the RXD1 [3:0] lines and is de-asserted at the end of the packet.
B14	COL1	I/PD	This pin functions as the collision detection. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin.
F12	MDC	O	MII management data clock is sourced by the R2880 to the external PHY devices as a timing reference for the transfer of information on the MDIO signal.
F14	MDIO	I/O/PD	MII management data input/output transfers control information and status between the external PHY and the R2880.

● Peripheral Bus (40 Pins)

Ball No.	Symbol	Type	Description
N3 M3 N2 P1 N1 M2 L3 L4 H1 H3 H4 G4 G3 G1 G2 F1	SA0/PIO0 SA1/PIO1 SA2/PIO2 SA3/PIO3 SA4/PIO4 SA5/PIO5 SA6/PIO6 SA7/PIO7 SA8/PIO8 SA9/PIO9 SA10/PIO10 SA11/PIO11 SA12/PIO12 SA13/PIO13 SA14/PIO14 SA15/PIO15	I/O/PU*	SA[15:0]: Slow bus address 15 to 0. PIO: General purpose PIN.
R6	IOR_n/PIO16	I/O/PU*	When register EAh bit is set, this pin is IOR_n. IOR_n is set for PCMCIA bus. PIO: General purpose PIN.
P7	IOW_n/PIO17	I/O/PU*	When register EAh bit is set, this pin is IOW_n. IOW_n is set for PCMCIA bus. PIO: General purpose PIN.
E4 E3	PCS0_n/CFRAME0_n PCS1_n/CFRAME1_n	I/O/PU*	PCS1_n & PCS0_n: Peripheral chip selects. These pins are active low when the micro-controller accesses the defined peripheral memory block (I/O or memory address). For I/O access, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address access, the base address can be located in the 16M-Byte memory address region. These pins are asserted with the multiplexed D address bus and not floating during bus holds. CFRAME[1:0]_n: Cardbus Frame Pin 1 & 0. These pins are used to support two extra Cardbus devices to cooperate with PCI interface. The functions are the same as those for the FRAME_n pins or the PCI interface.
E2 D1	PCS2_n/PREQ2_n/PIO18 PCS3_n/PGNT2_n/PIO19	I/O/PU*	PCS2_n & PCS3_n: Peripheral chip selects. These pins are active low when the micro controller accesses the defined peripheral memory block (I/O or memory address). For I/O access, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address access, the base address can be located in the 16M-Byte memory address region. These pins are asserted with the multiplexed D address bus and not floating during bus holds. PREQ2_n: PCI Bus Request 2. This signal is the PCI bus request signal used as inputs by the internal PCI arbiter. This pin must be pulled up when PIO pin is used or PQ2 (please refer to bit 9 in FCh register on page 34) enabled. PGNT2_n: PCI Grant 2. This signal is the PCI bus grant output signal generated by the internal PCI arbiter. This pin must be pulled up when PIO pin is used or PQ2 (please refer to bit 9 in

			FCh register on page 34) enabled. PIO: General purpose PIN.
E5 D2	PCS5_n/PREQ3_n/PIO20 PCS6_n/PGNT3_n/PIO21	I/O/PU*	PCS5_n & PCS6_n: Peripheral chip selects/latched address bit. For PCS_n feature, these pins are active low when the micro-controller accesses the fifth or sixth region of the peripheral memory (I/O or memory space). The base address of PCS_n is programmable. These pins are asserted with the multiplexed D address bus and not floating during bus hold conditions. PREQ3_n: PCI Bus Request 3. This signal is the PCI bus request signal used as inputs by the internal PCI arbiter. This pin must be pulled up when PIO pin is used or PQ3 (please refer to bit 10 in FCh register on page 34) enabled. PGNT3_n: PCI Grant 3. This signal is the PCI bus grant output signal generated by the internal PCI arbiter. This pin must be pulled up when PIO pin is used or PQ3 (please refer to bit 10 in FCh register on page 34) enabled. PIO: General purpose PIN.
F2	MCS_n/PIO22	I/O/PU*	MCS_n: Midrange Memory Chip Select. For MCS_n feature, this pin is active low when the micro-controller accesses the defined portion of memory region. At this moment, MCS_n can be mapped to I/O. PIO: General purpose PIN.
M1 L2 L1 K3	INT0/BHE_n/PIO29 INT1/PIO23 INT2/PIO24 INT3/PIO25	I/O/PU*	INT[3:0]: Maskable Interrupt Request 3 to 0. They are active high. The interrupt inputs can be configured as either edge-triggered or level-triggered. The requesting device must hold INT0, INT1, INT2, or INT3 until the request is acknowledged to guarantee interrupt recognition. BHE_n: Bus High Enable. (Please refer to page 38 for the detailed information.) PIO: General purpose PIN.
B1 C1	DRQ1/INT6/PGNT4_n DRQ0/INT5/PREQ4_n	I/O/PU*	DRQ[1:0]: DMA request 1 & 0. These pins are asserted high by an external device when the device is ready for DMA channel 1 or channel 0 to perform a transfer. These pins are level-triggered and internally synchronized. The DRQ signals are not latched and must remain active until serviced. For INT6/INT5: When the DMA function is not used, the INT6 and INT5 can be used as an additional external interrupt request. And they share the corresponding interrupt type and register control bits. The INT6/5 are level-triggered only. PGNT4_n: PCI Grant 3. This signal is the PCI bus grant output signal generated by the internal PCI arbiter. This pin must be pulled up when PIO pin is used or PQ4 (please refer to bit 11 in FCh register on page 34) enabled.

			PREQ4_n: PCI Bus Request 3. This signal is the PCI bus request signal used as inputs by the internal PCI arbiter. This pin must be pulled up when PIO pin is used or PQ4 (please refer to bit 11 in FCh register on page 34) enabled.
M6	ARDY/PIO28	I/O/PU	Asynchronous ready. This pin indicates to the micro-controller that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge of input that is asynchronous to SD_CLK and is active high. However, the falling edge of ARDY must be synchronized to SD_CLK. Tie ARDY high, so the micro-controller is always asserted in the ready condition. To guarantee the wait states inserted, ARDY must be pulled low before to phase 2 of T2 or phase 1 of T3. Please note that the ARDY signal is internally pulled high. PIO: General purpose PIN.
H2 J1 J4 J3 J2 K1	RTS1_n/SAD8/PIO30 DTR1_n/SAD9/PIO31 CTS1_n/SAD10/PIO32 DSR1_n/SAD11/PIO33 DCD1_n/SAD12/PIO34 RI1_n/SAD13 /PIO35	I/O/PU*	RTS1_n: Request To Send. DTR1_n: Data Terminal Ready. CTS1_n: Clear To Send. DSR1_n: Data Set Ready. DCD1_n: Carry Sense Detection. RI1_n: Ring Input. SAD[13:8]: The combination pins with addresses and data. They are designed for slower peripheral bus. PIO: General purpose PIN.
K2 K4	SIN1/SAD14/PIO26 SOUT1/SAD15/PIO27	I/O/PU	SIN1: Serial Data Input. SOUT1: Serial Data Output. SAD[13:8]: The combination pins with addresses and data. They are designed for slower peripheral bus. PIO: General purpose PIN.

● PCI Bus (50PINs)

Ball No.	Symbol	Type	Description
A13	PCICLK	O	33 MHz PCI Clock input. This clock is used by all of the R2880 logic that is in the PCI clock domain.
B13	PCIRST_n	O	PCI Reset. This pin is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.
A1, C4, B3, D4, A2, B4, C5, A3, A4, D5, C6, A5, D6, B6, A6, C7, D9, C9, B9, A10,B10, D10,C10,A11, A12,D11,C13, C11,A14,D12,	PAD[31:0]	I/O	PAD[31:0]: PCI AD bus. These pins perform address when the bus state is address phase and perform data when the bus state is data phase.

C12, B12			
B5, B7, A9, B11	C/BE[3:0]_n	I/O	Bus Command and Byte Enables. During the address phase, C/BE[3:0]_n define the Bus Command. During the data phase, C/BE[3:0]_n define the Byte Enables.
D7	FRAME_n	I/O/PU	PCI Frame. This pin is driven by a PCI master to indicate the beginning and duration of a PCI transaction. This pin must be pulled up.
A7	IRDY_n	I/O/PU	PCI Initiator Ready. This pin is asserted low by the master to indicate that it is able to transfer the current data transfer. A data was transferred if both IRDY_n and TRDY_n are asserted low during the rising edge of the PCI clock. This pin must be pulled up.
C8	TRDY_n	I/O/PU	PCI Target Ready. This pin is asserted low by the target to indicate that it is able to receive the current data transfer. A data was transferred if both IRDY_n and TRDY_n are asserted low during the PCI clock rising edge. This pin must be pulled up.
D8	STOP_n	I/O/PU	PCI Stop. This pin is asserted low by the target to indicate that it is unable to receive the current data transfer. This pin must be pulled up.
A8	DEVSEL_n	I/O/PU	Device Select. This pin is driven by the devices, which have decoded the addresses belonging to them. This pin must be pulled up.
B8	PAR	I/O	PCI Parity. This pin is driven to even parity by PCI master over the PAD[31:0] and C/BE[3:0]_n bus during address and write data phases. This should be pulled high through a weak external pull-up resistor. The target drives parity during data read.
F4 F3	INTA_n INTB_n	I/PU	INTA_n: PCI Interrupt Input A. PCI INTA_n must be connected when normal modes of PCI Interrupts are supported. INTB_n: PCI interrupt input B. PCI INTB_n must be connected when normal modes of PCI Interrupts are supported.
D3, C2	PREQ[1:0]_n	I/PU*	PCI Bus Request. These signals are the PCI bus request signals used as inputs by the internal PCI arbiter. These pins must be pulled up.
C3, B2	PGNT[1:0]_n	O/PU*	PCI Grant. These signals are the PCI bus grant output signals generated by the internal PCI arbiter. These pins must be pulled up.

- **16550 UART (6 PINs)**

Ball No.	Symbol	Type	Description
K14	SIN0	I/PU	SIN0: Serial Input. Serial Data Input from the communications link.
K12	SOUT0	O	SOUT0: Serial Output. Composite serial data output to the communications link.
L13	RTS0_n/TDO/PIO36	I/O/PU*	RTS0_n: Request To Send. When low, this indicates to MODEM or data set that URAT is ready to exchange data. TDO: JTAG Test Data Output pin. PIO: General purpose PIN.
L12	CTS0_n/TMS/PIO37	I/O/PU*	CTS0_n: Clear To Send. When low, this indicates to UART that MODEM or data set is ready to exchange data. TMS: JTAG Test Mode Select pin. PIO: General purpose PIN.
K13	DSR0_n/TCK/PIO38	I/O/PU*	DSR0_n: Data Set Ready. When low, this indicates that MODEM

			or data set is ready to establish the communication link with UART. TCK: JTAG Test Clock input pin. PIO: General purpose PIN.
L15	DCD0_n/TDI/PIO39	I/O/PU*	DCD0_n: Data Carry Detection. When low, it indicates that the data carrier has been detected by the MODEM or data set. TDI: JTAG Test Data Input pin. PIO: General purpose PIN.

- **Power (47 PINs)**

Ball No.	Symbol	Type	Description
J5, H5, G5, E7, E8, E9, F11,G11,H11, J11,L9,L8,L7	VDD_IO	I	I/O power pins, pure 3.3V.
L10,K11,E11, E10, E6, F5, K5	VDD_CORE	I	Core power pins, pure 2.5V.
H9,J10,H10, F10,J7, K9, H8, K8, J6, H6, F7, F8, G8	GND_IO	I	I/O ground pins.
F6, F9, G6, G7, G9, G10, H7, J8, J9, K6, K7, K10,	GND_CORE	I	Core ground pins.
L5	VDD_PLL	I	De-skew PLL power pin, pure 2.5V.
L6	GND_PLL	I	Multiple PLL power pin, pure 2.5V.

Notes:

1. When the PIO Mode register and PIO Direction register are configured as PIO modes, the 48 MUX definition pins can be used as PIO pins. For example, IOR_n/PIO16 can be used as PIO16.
2. The PIO status during Power-On reset:

   (1) PIO18~PIO27 and PIO36~PIO47 are normal operations.

   (2) Other PIOs are inputs with pull-up.
3. In Slow Bus Mode (Bus Mode 0):

   I/O bus is mapped to SAD [15:0] or SAD [7:0]. It depends on the software setting of SBWSEL in the Bus Control Register to select 16-bit or 8-bit mode. Memory bus is mapped to A [11:0]/D [15:0].
4. In Normal Bus Mode (Bus Mode 1):

   I/O bus and Memory bus are all mapped to A [22:0] and D [15:0]. The SAD [15:0] bus is inactive in this mode.
5. Change Bus Mode 0 and Bus Mode 1 by means of setting the internal Bus Control Register. This action must

be initialized by software.

6. As all/partial Slow Bus Address, SA[18:0], on multiplexed pins are required, Bus Control Register should be enabled, then the default settings are disabled.
7. All the PCI I/Os are 5V tolerance.

4.3 PIN Capacitance Description

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance		2.8		pF
C_{OUT}	3.3V Output Capacitance	2.7		4.9	pF
C_{BID}	3.3V Bi-directional Capacitance	2.7		4.9	pF

4.4 PIN Pull-up/Pull-down Description

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
RST_n	I	--	1	0	1	Y	--	
X1	I	--	0	0	0	Note 1	--	Note 1: 2.5V
X2	O		--	--	--	Note 1	--	
CLKOUTA	O	16mA	--	--	--	N	F	
RD_n	O	12mA	--	--	--	Y	S	
WR_n	O	12mA	--	--	--	Y	S	
A0/MA0	O	16mA	--	--	--	N	F	
A1/MA1	O	16mA	--	--	--	N	F	
A2/MA2	O	16mA	--	--	--	N	F	
A3/MA3/DIVID	O/I	16mA	1	0	0	N	F	Ext. pull-up/down to select CPU & SDRAM frequency.
A4/MA4	O/I	16mA	0	1	0	N	F	Ext. pull-down for normal operation.
A5/MA5/BYPASS	O/I	16mA	0	1	0	N	F	Ext. pull-up to into bypass mode.
A6/MA6/PCKD0	O/I	16mA	1	0	0	N	F	Ext. pull-up/down to select PCI frequency
A7/MA7/PCKD1	O/I	16mA	0	1	0	N	F	Ext. pull-up/down to select PCI frequency
A8/MA8/CLKSEL	O/I	16mA	0	1	0	N	F	Ext. pull-up/down to select CLKOUTA clock to be 25MHz PHYCLOCK or 33MHz PCICLOCK.
A9/MA9	O/I	16mA	0	1	0	N	F	Ext.pull-down for normal operation.
A10/MA10/BSEL	O/I	16mA	0	1	0	N	F	Ext. pull-up/down to select 8bit/16bit.
A11/MA11/JTAGEN	O/I	16mA	0	1	0	N	F	Ext. pull-up to turn on JTAG function.
A[19:12]/SAD[7:0]	I/O	16mA	0	0	0	Y	F	

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
A20/SA16	O	16mA	--	--	--	N	F	
A21/SA17	O	16mA	--	--	--	N	F	
A22/SA18/ALE	O	16mA	--	--	--	N	F	
D[15:0]	I/O	16mA	0	0	0	Y	F	
UCS_n	O	12mA	--	--	--	N	S	
SD_CLK	O	16mA	--	--	--	N	F	
WE_n CAS_n RAS_n BA[1:0] DQML DQMH	O	12mA	--	--	--	N	F	
TXC0 RXC0	I	--	1	0	1	Y	--	
TXD0_[3:0]/ PIO[43:40]	I/O	16mA	Note2	0	0	Y	S	Note 2: Programmed by PIO mode & dir. Register.
RXD0_[3:0]/PIO[47:44]	I/O	16mA	Note2	0	0	Y	S	
TXEN0	O	16mA	--	--	--	Y	S	
RXDV0	I	--	0	1	0	Y	--	
COL0	I	--	0	1	0	Y	--	
TXC1 RXC1	I	--	0	0	1	Y	--	
TXD1_[3:0]	O	16mA	--	--	--	Y	S	
RXD1_[3:0]	I	--	0	1	0	Y	--	
TXEN1	O	16mA	--	--	--	Y	S	
RXDV1	I	--	0	1	0	Y	--	
COL1	I	--	0	1	0	Y	--	
MDC	O	8mA	--	--	--	Y	S	
MDIO	I/O	8mA	0	1	0	Y	S	
SA[15:0]/PIO[15:0]	I/O	16mA	Note2	0	0	Y	F	
IOR_n/PIO16	I/O	12mA	Note2	0	0	Y	S	
IOW_n/PIO17	I/O	12mA	Note2	0	0	Y	S	
PCS0_n/CFRAME0_n	I/O	Note5	1	0	0	Y	F	
PCS1_n/CFRAME1_n	I/O	Note5	1	0	0	Y	F	
PCS2_n/PREQ2_n/PIO18	I/O	Note5	Note3	0	0	Y	S	Note 3: Programmed by PIO mode, dir. & PQ2 enabled register.
PCS3_n/PGNT2_n/PIO19	I/O	Note5	Note3	0	0	Y	S	
PCS5_n/PREQ3_n/PIO20	I/O	Note5	Note4	0	0	Y	F	Note 4: Programmed by PIO mode, dir. & PQ3 enabled register.
PCS6_n/PGNT3_n/PIO21	I/O	Note5	Note4	0	0	Y	F	
MCS_n/PIO22	I/O	12mA	Note2	0	0	Y	S	
INT0/BHE_n/PIO29	I/O	16mA	Note2	0	0	Y	F	
INT1/PIO23	I/O	16mA	Note2	0	0	Y	F	
INT2/PIO24	I/O	Note5	Note2	0	0	Y	F	

PIN Name	Type	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Description
INT3/PIO25	I/O	Note5	Note2	0	0	Y	F	
DRQ0/INT5/PREQ4_n	I	--	Note6	0	--	Y	--	Note6: PQ4 enabled register.
DRQ1/INT6/PGNT4_n	I/O	Note5	Note6	0	0	Y	F	
ARDY/PIO28	I/O	8mA	1	0	0	Y	S	
RTS1_n/SAD8/PIO30	I/O	16mA	Note2	0	0	Y	F	
DTR1_n/SAD9/PIO31	I/O	16Ma	Note2	0	0	Y	F	
CTS1_n/SAD10/PIO32	I/O	16mA	Note2	0	0	Y	F	
DSR1_n/SAD11/PIO33	I/O	16mA	Note2	0	0	Y	F	
DCD1_n/SAD12/PIO34	I/O	16mA	Note2	0	0	Y	F	
RI1_n/SAD13/PIO35	I/O	16mA	Note2	0	0	Y	F	
SIN1/SAD14/PIO26	I/O	16mA	Note2	0	0	Y	F	
SOUT1/SAD15/PIO27	I/O	16mA	Note2	0	0	Y	F	
PCICLK	O	Note5	--	--	--	Y	F	Note5: PCI type IO pad.
PCIRST_n	O	Note5	--	--	--	Y	F	
PAD[31:0]	I/O	Note5	0	0	0	Y	F	
C/BE[3:0]_n	I/O	Note5	0	0	0	Y	F	
FRAME_n IRDY_n TRDY_n STOP_n DEVSEL_n	I/O	Note5	1	0	0	Y	F	
PAR	I/O	Note5	0	0	0	Y	F	
INTA_n INTB_n	I(OD)	--	1	0	--	Y	--	
PREQ[1:0]_n	I	--	1	0	--	Y	--	
PGNT[1:0]_n	O	Note5	--	--	--	Y	F	
SIN0	I	--	1	0	0	Y	--	
SOUT0	O	8mA	--	--	--	Y	S	
RTS0_n/TDO/PIO36	I/O	16mA	Note2	0	0	Y	S	
CTS0_n/TMS/PIO37	I/O	8mA	Note2	0	0	Y	S	
DSR0_n/TCK/PIO38	I/O	8mA	Note2	0	0	Y	S	
DCD0_n/TDI/PIO39	I/O	8mA	Note2	0	0	Y	S	

Note 1: The pins never in the driving current, pull-up, pull-down, schimitt trigger, I/O pad, and slew rate status are not shown in the above table.

Note 2: Programmed by PIO mode & dir. Register.

Note 3: Programmed by PIO mode, dir. & PQ2 enabled register.

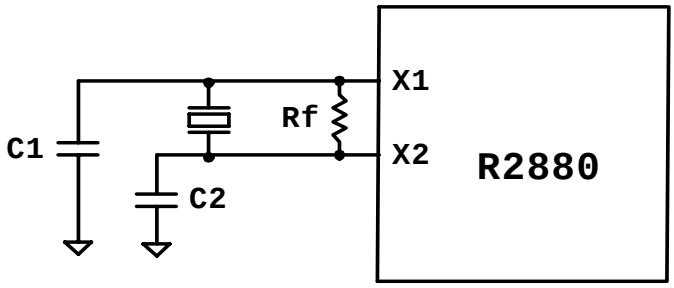
Note 4: Programmed by PIO mode, dir. & PQ3 enabled register.

Note5: PCI type IO pad.

Note6: PQ4 enabled register.

5. Crystal Characteristics

5.1 Fundamental Mode



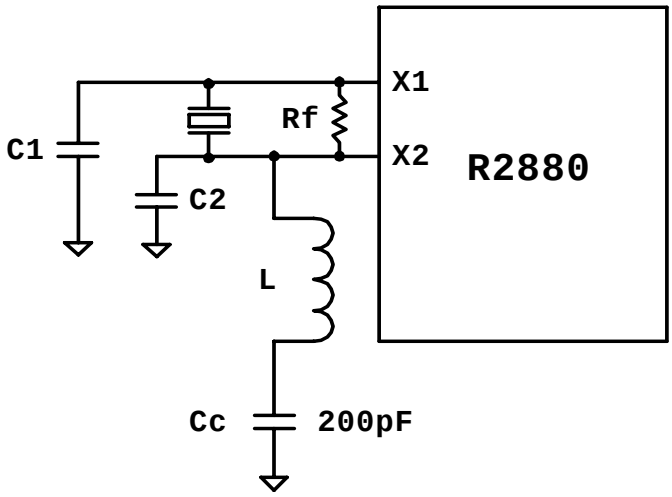
C1 ---------- 20pF ± 20%

C2 ---------- 20pF ± 20%

Rf ---------- 1 mega-ohm

5.2 Third-Overtone Mode

Normally, high frequency use for third overtone mode can get price advantage, but additional L and Cc are needed.



Typical value suggestions are as follows:

C1 ---------- 20pF ± 20%

C2 ---------- 20pF ± 20%

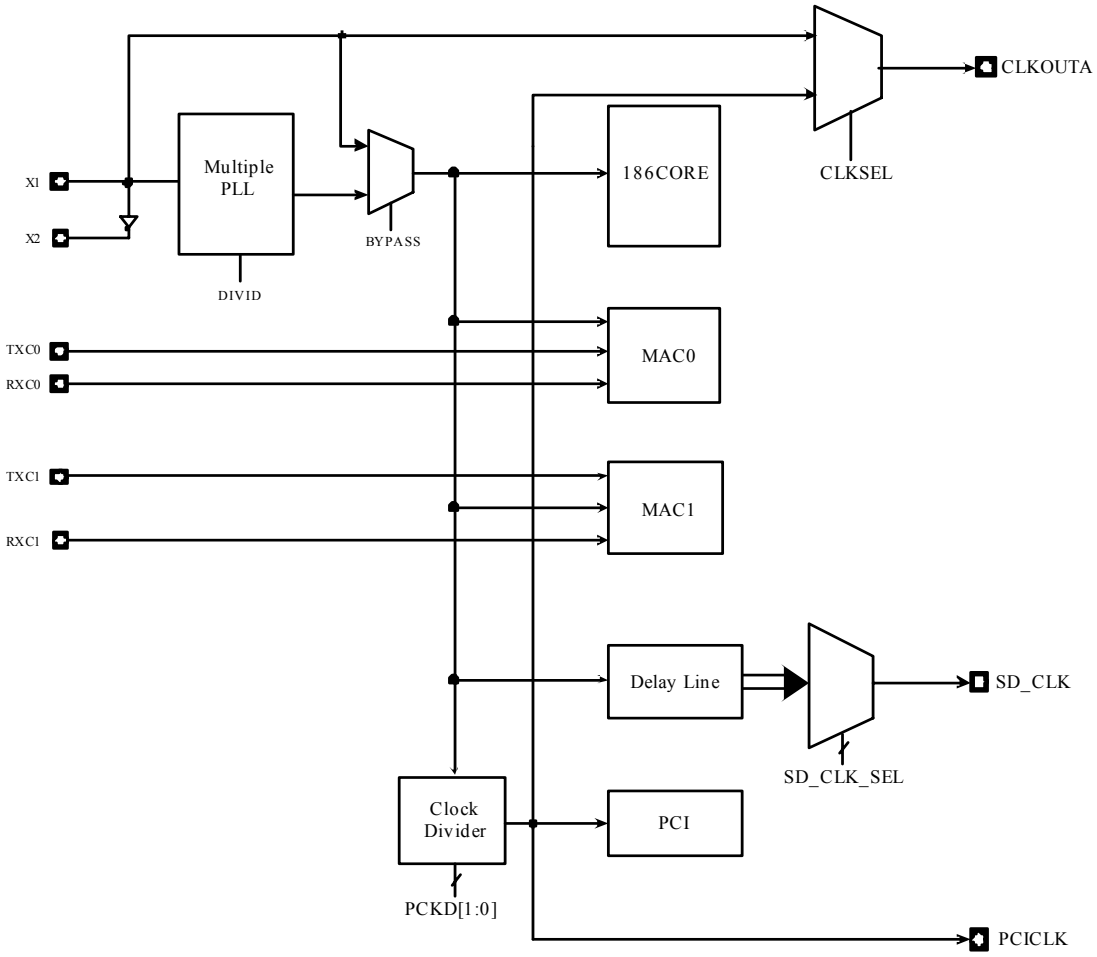
Cc ---------- 200pF± 20%

Rf ---------- 1 Mega-Ohm

L ---------- 4.7uH, 6.8uH, 8.2uH, 10uH (25MHz)

Note: X1 input clock must be within + - 100ppm tolerance.

6. Clock Unit



PLL Configuration Table:

Input Clock Range (Mhz)	DIVID	Multiple	Output Clock (Mhz)
25	0	3	75
	1	4	100

PCI Clock Divider Configuration Table:

Input Clock Range (Mhz)	PCKD[1:0]		Multiple	Output Clock (Mhz)
75	0	0	1/2	37.5
	0	1	1/3	25
	1	0	1/4	18.75
	1	1	1/5	15
100	0	0	1/2	Reserved
	0	1	1/3	33.3
	1	0	1/4	25
	1	1	1/5	20

7. Execution UNIT

7.1 General Registers

The R2880 has eight 16-bit general registers. And the AX, BX, CX, and DX can be subdivided into two 8-bit registers (AH, AL, BH, BL, CH, CL, DH and DL). The functions of these registers are described as follows:

AX: Word Divide, Word Multiply, Word I/O operation.

AH: Byte Divide, Byte Multiply, Byte I/O, Decimal Arithmetic, Translate operation.

AL: Byte Divide, Byte Multiply operation.

BX: Translate operation.

CX: Loops, String operation

CL: Variable Shift and Rotate operation.

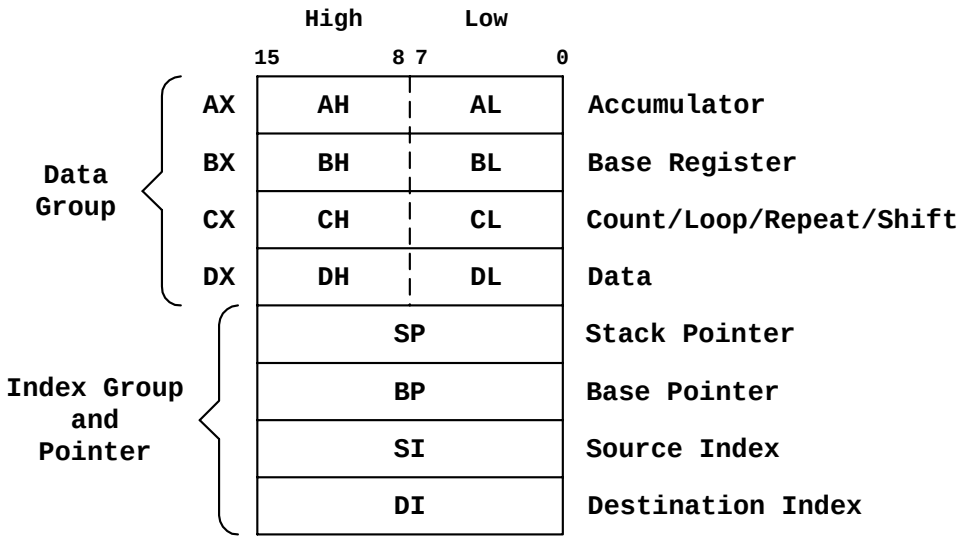
DX: Word Divide, Word Multiply, Indirect I/O operation

SP: Stack operations (POP, POPA, POPF, PUSH, PUSHA, PUSHF)

BP: General-purpose registers which can be used to determine offset address of operands in Memory.

SI: String operations

DI: String operations



GENERAL REGISTERS

7.2 Segment Registers

R2880 has four 16-bit segment registers: CS, DS, SS and ES. The segment registers contain the base addresses (starting location) of these memory segments, and they are immediately addressable for code (CS), data (DS & ES), and stack (SS) memory.

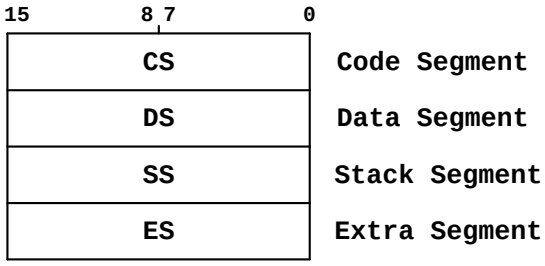
CS (Code Segment): The CS register points to the current code segment, which contains instruction to be fetched. The default location memory space for all instructions is 64K. The initial value of CS register is 0FFFFh.

DS (Data Segment): The DS register points to the current data segment, which generally contains program

variables. The DS register is initialized to 0000H.

SS (Stack Segment): The SS register points to the current stack segment, which is for all stack operations, such as pushes and pops. The stack segment is used for temporary space. The SS register is initialized to 0000H.

ES (Extra Segment): The ES register points to the current extra segment, which is typically for data storage, such as large string operations and large data structures. The ES register is initialized to 0000H.



SEGMENT REGISTERS

7.3 Instruction Pointer and Status Flags Registers

IP (Instruction Pointer): The IP is a 16-bit register and it contains the offset of the next instruction to be fetched. The IP register cannot be directly accessed by software. This register is update by the bus interface unit. It can be changed, saved or restored as a result of program execution. The IP register is initialized to 0000H and the starting execution address for CS:IP is at 0FFFF00H.

Register Name: Processor Status Flags Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				OF	DF	IF	TF	SF	ZF	Rsvd	AF	Rsvd	PF	Rsvd	CF

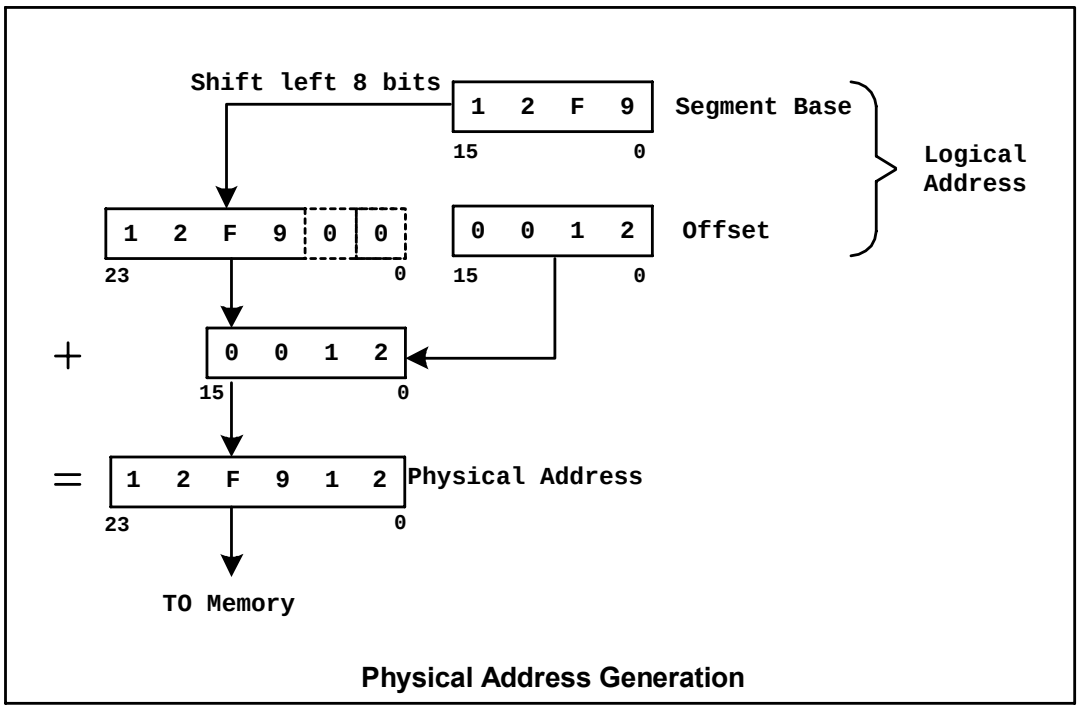
These flags reflect the status after the Execution Unit is executed.

Bit	Name	Description
15-12	Rsvd	Reserved.
11	OF	Overflow Flag. If an arithmetic overflow occurs, this flag will be set.
10	DF	Direction Flag. If this flag is set, the string instructions are in the process of incrementing address. If DF is cleared, the string instructions are in the process of decrementing address. Refer to the STD and CLD instructions for how to set and clear the DF flag.
9	IF	Interrupt-Enable Flag. Refer to the STI and CLI instructions for how to set and clear the IF flag. Set to 1: The CPU enables the mask able interrupt request. Set to 0: The CPU disables the mask able interrupt request.
8	TF	Trace Flag. Set to enable single-step mode for debugging; Clear to disable the single-step mode. If an application program sets the TF flag with POPF or IRET instruction, a debug exception is

		generated after the instruction (The CPU automatically generates an interrupt after each instruction) that follows the POPF or IRET instruction.
7	SF	Sign Flag. If this flag is set, the high-order bit of the result of an operation will be 1, indicating the state of being negative.
6	ZF	Zero Flag. If this flag is set, the result of operation will be zero.
5	Rsvd	Reserved
4	AF	Auxiliary Flag. If this flag is set, there will be a carry from the low nibble to the high one or a borrow from the high nibble to the low nibble of the AL general-purpose register. It is used in BCD operation.
3	Rsvd	Reserved
2	PF	This flag will be set if the result of the low-order 8-bit operation has even parity.
1	Rsvd	Reserved
0	CF	Carry Flag. If CF is set, there will be a carry out or a borrow into the high-order bit of the instruction result.

7.4 Address Generation

The Execution Unit generates a 24-bit physical address to Bus Interface Unit by the Address Generation. Memory is organized in sets of segments. Each segment contains a 16-bit value. Memory is addressed with a two-component address that consists of a 16-bit segment and 16-bit offset. The Physical Address Generation figure describes how the logical address is transferred to the physical address.



Physical Address Generation

8. Peripheral Register List

The Peripheral Control Block can be mapped into either Memory or I/O space by programming the Peripheral Control Block Relocation Register (FEh). After reset, the default Legacy Peripheral Control Block offset is located at FF00h in I/O space, the SDRAM Control Register, EDO, Cache and Low speed clock is located at FE00h in I/O space, and Ethernet Control Register is located at FD00h and FE00h in I/O space.

The following table lists are all the definitions of the Peripheral Control Block Registers, and the detailed descriptions will be arranged on the related Block Unit.

8.1 Legacy Peripheral Registers (Base Address FF00h)

Offset (HEX)	Register Name	Page	Offset (HEX)	Register Name	Page
FE	Peripheral Control Block Relocation Register	33	6A	PIO Mode 2 Register	110
FC	PAD Function Select Control Register	34	66	Timer 2 Mode/Control Register	81
F8	Processor Extended ID Register	34	62	Timer 2 Maxcount Compare A Register	82
F6	Reset Configuration Register	36	60	Timer 2 Count Register	81
F4	Processor Release Level Register	33	5E	Timer 1 Mode/Control Register	79
F2	Auxiliary configuration Register	40	5C	Timer 1 Maxcount Compare B Register	80
F0	Auxiliary Processor Release Level Register	34	5A	Timer 1 Maxcount Compare A Register	80
EA	Bus Control Register	37	58	Timer 1 Count Register	80
E6	Watchdog Timer Control Register	82	56	Timer 0 Mode/Control Register	77
E4	Enable RCU Register	53	54	Timer 0 Maxcount Compare B Register	79
E2	Clock Pre-scaler Register	53	52	Timer 0 Maxcount Compare A Register	79
DA	DMA1 Control Register	72	50	Timer 0 Count Register	78
D8	DMA1 Transfer Count Register	73	4A	PCI INTB Control Register	56
D6	DMA1 Destination Address High Register	73	48	PCI INTA Control Register	56
D4	DMA1 Destination Address Low Register	73	44	Serial Port 0 Interrupt Control Register	57
D2	DMA1 Source Address High Register	74	42	Serial Port 1 Interrupt Control Register	58
D0	DMA1 Source Address Low Register	74	40	MAC Interrupt Control Register	58
CA	DMA0 Control Register	69	3E	INT3 Control Register	59
C8	DMA0 Transfer Count Register	71	3C	INT2 Control Register	59
C6	DMA0 Destination Address High Register	71	3A	INT1 Control Register	60
C4	DMA0 Destination Address Low Register	71	38	INT0 Control Register	61
C2	DMA0 Source Address High Register	72	36	DMA1/INT6 Interrupt Control Register	61
C0	DMA0 Source Address Low Register	72	34	DMA0/INT5 Interrupt Control Register	62
AE	Chip Select Recovery Time Configuration Register	47	32	Timer Interrupt Control Register	62
AC	MCS_n Extended Register	47	30	Interrupt Status Register	63
AA	Chip Size Multiplier Register	46	2E	Interrupt Request Register	63
A8	PCS_n and MCS_n Auxiliary Register	45	2C	Interrupt In-service Register	64
A6	Midrange Chip Select Register	44	2A	Priority Mask Register	65
A4	Peripheral Chip Select Register 0	43	28	Interrupt Mask Register	65
A2	Low Memory Chip Select Register	42	26	Poll Status Register	66

A0	Upper Memory Chip Select Register	41	24	Poll Register	66
88	(See 7.2)	29	22	End-of-Interrupt Register	67
86	(See 7.2)	29	18	(See 7.2)	29
84	(See 7.2)	29	16	(See 7.2)	29
82	(See 7.2)	29	14	(See 7.2)	29
80	(See 7.2)	29	12	(See 7.2)	29
7A	PIO Data 1 Register	107	10	(See 7.2)	29
78	PIO Direction 1 Register	108	0F-0C	Configuration Data Register	52
76	PIO Mode 1 Register	108	0A	PCI Configuration Address – High Word Register	51
74	PIO Data 0 Register	108	08	PCI Configuration Address – Low Word Register	51
72	PIO Direction 0 Register	109	06	Double Word Access Data – High Word Register	50
70	PIO Mode 0 Register	109	04	Double Word Access Data – Low Word Register	49
6E	PIO Data 2 Register	109	02	Double Word Access Address – High Word Register	49
6C	PIO Direction 2 Register	110	00	Double Word Access Address – Low Word Register	49

8.2 16550 UART Register Definitions (Base Address FF00h)

Offset (HEX)	Register Name	Mnemonic	Page
80h	UART0 Receiver Buffer Register (when DLAB=0 & Read)	**RBR0**	93
	UART0 Transmitter Holding Register (when DLAB=0 & Write)	**THR0**	94
	UART0 Divisor Latch [Low Byte] (when DLAB=1)	**DLL0**	94
82h	UART0 Interrupt Enable Register (when DLAB=0)	**IER0**	95
	UART0 Divisor Latch [High Byte] (when DLAB=1)	**DLH0**	94
84h	UART0 Interrupt Identification Register (when Read)	**IIR0**	96
	UART0 FIFO Control Register (when Write)	**FCR0**	97
86h	UART0 Line Control Register	**LCR0**	98
88h	UART0 MODEM Control Register	**MCR0**	99
8Ah	UART0 Line Status Register	**LSR0**	100
8Ch	UART0 MODEM Status Register	**MSR0**	102
8Eh	UART0 Scratch Register	**SCR0**	103
10h	UART1 Receiver Buffer Register (when DLAB=0 & Read)	**RBR1**	93
	UART1 Transmitter Holding Register (when DLAB=0 & Write)	**THR1**	94
	UART1 Divisor Latch [Low Byte] (when DLAB=1)	**DLL1**	94
12h	UART1 Interrupt Enable Register (when DLAB=0)	**IER1**	95
	UART1 Divisor Latch [High Byte] (when DLAB=1)	**DLH1**	94
14h	UART1 Interrupt Identification Register (when Read)	**IIR1**	96
	UART1 FIFO Control Register (when Write)	**FCR1**	97
16h	UART1 Line Control Register	**LCR1**	98
18h	UART1 MODEM Control Register	**MCR1**	99
1Ah	UART1 Line Status Register	**LSR1**	100
1Ch	UART1 MODEM Status Register	**MSR1**	102
1Eh	UART1 Scratch Register	**SCR1**	103

8.3 Cache Control Register (Base Address FEC0h)

Offset (HEX)	Register Name	Mnemonic	Page
C0h	Cache Control Register	**CCR**	111
C4h	Non-Cache Region0 Starts Address High Register	**NCR0SH**	112
C2h	Non-Cache Region0 Starts Address Low Register	**NCR0SL**	111
C8h	Non-Cache Region0 End Address High Register	**NCR0EH**	112
C6h	Non-Cache Region0 End Address Low Register	**NCR0EL**	112
CCh	Non-Cache Region1 Starts Address High Register	**NCR1SH**	113
CAh	Non-Cache Region1 Starts Address Low Register	**NCR1SL**	113
D0h	Non-Cache Region1 End Address High Register	**NCR1EH**	114
CEh	Non-Cache Region1 End Address Low Register	**NCR1EL**	113
D4h	Non-Cache Region2 Starts Address High Register	**NCR2SH**	114
D2h	Non-Cache Region2 Starts Address Low Register	**NCR2SL**	114
D8h	Non-Cache Region2 End Address High Register	**NCR2EH**	115
D6h	Non-Cache Region2 End Address Low Register	**NCR2EL**	115
DCh	Non-Cache Region3 Starts Address High Register	**NCR3SH**	116
DAh	Non-Cache Region3 Starts Address Low Register	**NCR3SL**	115
E0h	Non-Cache Region3 End Address High Register	**NCR3EH**	116
DEh	Non-Cache Region3 End Address Low Register	**NCR3EL**	116
E4h	Write-Invalid Region Starts Address High Register	**WIRSH**	117
E2h	Write-Invalid Region Starts Address Low Register	**WIRSL**	117
E8h	Write-Invalid Region End Address High Register	**WIREH**	118
E6h	Write-Invalid Region End Address Low Register	**WIREL**	117

8.4 SDRAM Control Registers (Base Address FE00h)

Offset (HEX)	Register Name	Mnemonic	Page
F2h	SDRAM Mode Set Register	**SDRAMMSR**	119
F4h	SDRAM Control Register	**SDRAMCR**	119
F6h	SDRAM Timing Parameter Register	**SDRAMTPR**	120

8.5 Fast Ethernet MAC Control Registers (Base Address: MAC0/FD00h & MAC1/FE00h)

Offset (HEX)	Register Name	Mnemonic	Page
00h	MAC Control Register 0	**MCR0**	126
04h	MAC Control Register 1	**MCR1**	127
08h	MAC Bus Control Register	**MBCR**	128
0Ch	TX Interrupt Control Register	**MTICR**	129
10h	RX Interrupt Control Register	**MRICR**	129
14h	TX Poll Command Register	**MTPR**	130
18h	RX Buffer Size Register	**MRBSR**	130
1Ah	RX Descriptor Control Register	**MRDCR**	131
1Ch	MAC Last Status Register	**MLSR**	131
20h	MAC MDIO Control Register	**MMDIO**	132
24h	MAC MDIO Read Data Register	**MMRD**	133

28h	MAC MDIO Write Data Register	**MMWD**	133
2Ch	MAC TX Descriptor Start Address 0 Register	**MTDSA0**	134
30h	MAC TX Descriptor Start Address 1 Register	**MTDSA1**	134
34h	MAC RX Descriptor Start Address 0 Register	**MRDSA0**	135
38h	MAC RX Descriptor Start Address 1 Register	**MRDSA1**	135
3Ch	MAC INT Status Register	**MISR**	136
40h	MAC INT Enable Register	**MIER**	136
44h	MAC Event Counter INT Status Register	**MECISR**	137
48h	MAC Event Counter INT Enable Register	**MECIER**	138
50h	MAC Successfully Received Packet Counter	**MRCNT**	138
52h	MAC Event Counter 0 Register	**MECNT0**	139
54h	MAC Event Counter 1 Register	**MECNT1**	139
56h	MAC Event Counter 2 Register	**MECNT2**	139
58h	MAC Event Counter 3 Register	**MECNT3**	140
5Ah	MAC Successfully Transmit Packet Counter Register	**MTCNT**	140
5Ch	MAC Event Counter 4 Register	**MECNT4**	141
5Eh	MAC Pause Frame Counter Register	**MPCNT**	141
60h	MAC Hash Table Word 0	**MAR0**	141
62h	MAC Hash Table Word 1	**MAR1**	142
64h	MAC Hash Table Word 2	**MAR2**	142
66h	MAC Hash Table Word 3	**MAR3**	142
68h	MAC Multicast Address first two bytes Register	**MID0L**	143
6Ah	MAC Multicast Address second two bytes Register	**MID0M**	143
6Ch	MAC Multicast Address last two bytes Register	**MID0H**	143
70h	MAC Multicast Address first two bytes Register	**MID1L**	144
72h	MAC Multicast Address second two bytes Register	**MID1M**	144
74h	MAC Multicast Address last two bytes Register	**MID1H**	144
78h	MAC Multicast Address first two bytes Register	**MID2L**	145
7Ah	MAC Multicast Address second two bytes Register	**MID2M**	145
7Ch	MAC Multicast Address last two bytes Register	**MID2H**	145
80h	MAC Multicast Address first two bytes Register	**MID3L**	146
82h	MAC Multicast Address second two bytes Register	**MID3M**	146
84h	MAC Multicast Address last two bytes Register	**MID3H**	146

8.6 PCI Compliant Configuration Registers

Offset (HEX)	Register Name	Page
01h – 00h	Vendor ID Register	84
03h – 02h	Device ID Register	84
05h – 04h	Command Register	84
07h – 06h	Status Register	85
08h	Revision ID Register	85
0Bh – 09h	Class Code Register	86
0Ch	BIST, Header Type, Latency Timer, Cache Line Size Register	86
3Fh – 10h	PCI Standard Register (Reserved)	86
43h – 40h	PCI Devices Memory Space Base Address Register	87
47h – 44h	PCI Devices Memory Space Base Address Mask Register	87
4Bh – 48h	PCI Devices I/O Space Base Address Register	87
4Fh – 4Ch	PCI Devices I/O Space Base Address Mask Register	88

8.7 Bridge & CardBus Specific Registers in the PCI Configuration Registers

9. Peripheral Control Block Registers

The peripheral control block can be mapped into either memory or I/O space by programming the Peripheral Control Block Registers (FEh Registers). It starts at FF00h in I/O space after reset.

Register Offset: FEh
Register Name: Peripheral Control Block Relocation Register
Reset Value : 20FFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			M/IO_n	Base											

The Peripheral Control Block (PCB) is mapped into either memory or I/O space by programming this register. When the other chip selects (PCSx_n) are programmed to zero wait state and the external ready is ignored, PCSx_n can overlap the control block.

Bit	Name	Attribute	Description
15-13	Rsvd	RO	Reserved.
12	M/IO_n	R/W	Memory/IO space. As reset, this bit is set to 0 and the PCB map starts at FF00h in I/O space. Set 1: The PCB is located in memory space. Set 0: The PCB is located in I/O space (Default).
11-0	Base	R/W	PCB Relocation Base Address In I/O space, defaults for the lower eight bits of the address are 00h. When PCB is mapped to I/O space, Base[11:0] are mapped to Address[19:8] and Base[11:8] must be programmed as 00h. In memory space, Base[11:0] are mapped to Address[23:12] and defaults for Address[11:0] are 00h.

Register Offset: F4h
Register Name: Processor Release Level Register
Reset Value : 1AD9h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	0	1	1	0	1	1	0	0	1

The read only registers specify the processor release version and RDC identification number.

Bit	Name	Attribute	Description
15-12	PRL	RO	4'b0001
11-8	PV	RO	Processor version.
7-0	ID	RO	RDC identification number 8'hD9 for 16M-byte case.

Register Offset: F0h
Register Name: Auxiliary Processor Release Level Register
Reset Value : 2800h

Register Offset: F8h
Register Name: Processor Extended ID Register
Reset Value : 1610h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEID															

Bit	Name	Attribute	Description
15-0	PEID	RO	This read only register specifies the RDC identification extended number.

Register Offset: FCh
Register Name: PAD Function Select Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		CB1E	CB0E	PQ4E	PQ3E	PQ2E	Reserved								

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
13	CB1E	R/W	Cardbus device 1 Enabled. Default disabled.
12	CB0E	R/W	Cardbus device 0 Enabled. Default disabled.
11	PQ4E	R/W	PCI request 4 Enabled. Default disabled.
10	PQ3E	R/W	PCI request 3 Enabled. Default disabled.
9	PQ2E	R/W	PCI request 2 Enabled. Default disabled.
8-0	Rsvd	RO	Reserved.

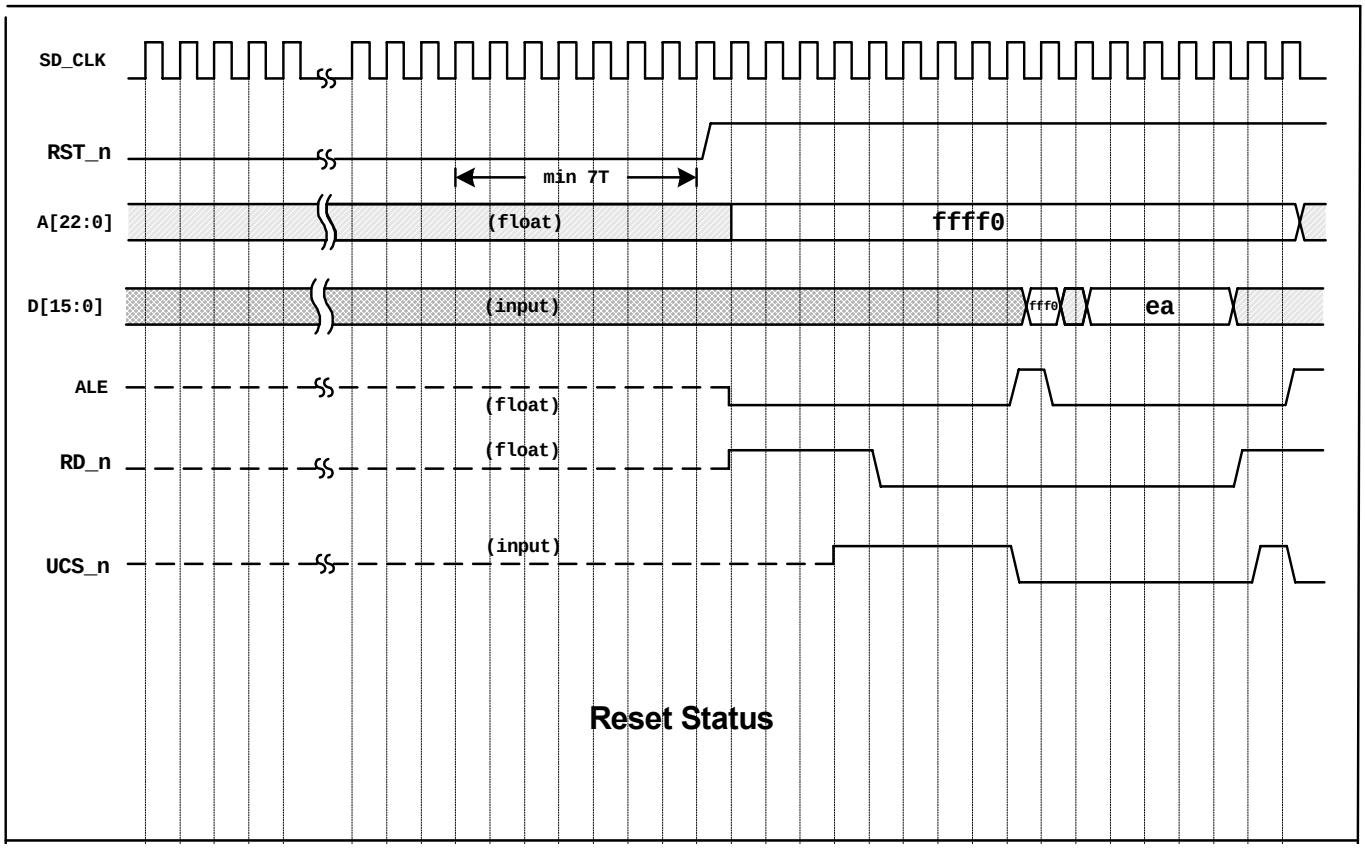
---

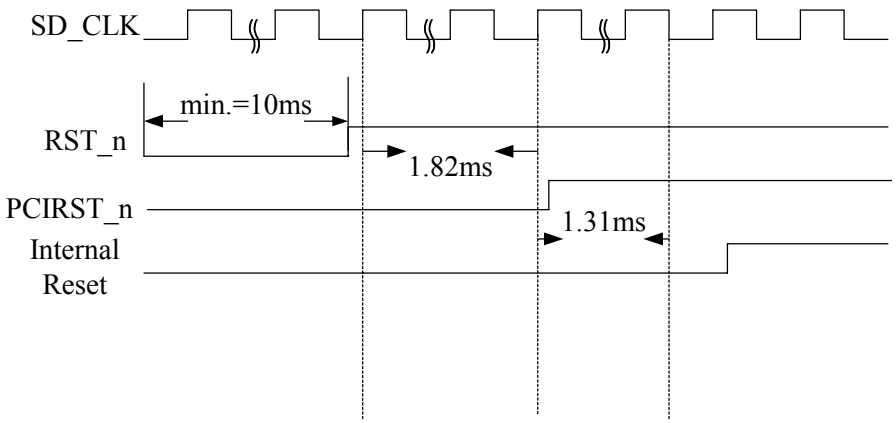
10. Reset Unit

Processor initialization is accomplished with activation of the RST_n pin. To reset the processor, this pin should be held low for at least seven oscillator periods. The Reset Status Figure shows the status of the RST_n pin and the other related pins.

When RST_n goes from low to high, the state of input pins (with weak pull-up or pull-down resistors) will be latched, and each pin will perform the individual function.

10.1 Power-up Reset





Power-up Reset Timing

Register Offset: F6h
Register Name: Reset Configuration Register
Reset Value : D[15:0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RC															

Bit	Name	Attribute	Description
15-0	RC	RO	Reset Configuration D[15:0]. The D[15:0] must be with weakly pulled-up or pulled-down resistors to correspond to the contents when they are latched into this register as the RST_n signal goes from low to high. The value of the reset configuration register provides the system information when this register is read by software. This register is read only and the contents remain valid until next processor reset.

11. Bus Interface UNIT

11.1 Slow Bus

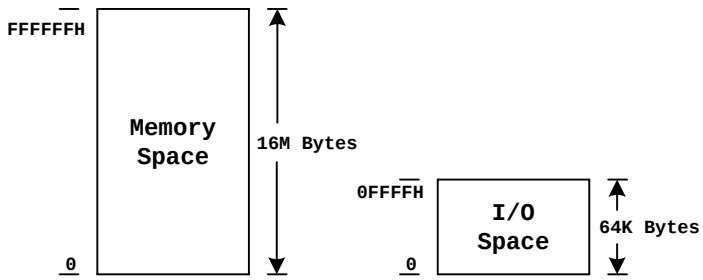
Register Offset: EAh
Register Name: Bus Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BMOD	SBWSEL	Reserved						BHE	Reserved				SLAEn	Reserved	

Bit	Name	Attribute	Description
15	BMOD	R/W	Bus Mode Select bit. Set 0: Slow bus mode. When the PCS/MCS regions are accessed, the bus cycle is mapped to SAD [15:0] or SAD [7:0]. Set 1: Normal bus mode. When the PCS/MCS regions are accessed, the bus cycle is mapped to A [19:0] and D [15:0]. The SAD bus is inactive in this mode.
14	SBWSEL	R/W	Slow bus width select Set 1: as 8-bit mode. Set 0: as 16-bit mode.
13-8	Rsvd	RO	Reserved.
7	BHE	R/W	Write high byte enable. When Pin 41 (INT0/BHE_n/PIO29) is set as PIO mode, don't care this bit. When Pin 41 is set as normal function mode, Set 1: Pin 41 is used as BHE_n. Set 0: Pin 41 is used as INT0.
6-3	Rsvd	RO	Reserved.
2	SLAEn	R/W	Slow Bus Latch Address Enable. Set 1: SA18 is enabled and ALE disabled.
1-0	Rsvd	RO	Reserved

11.2 Memory and I/O Interface

The memory space consists of 16M bytes (8M 16-bit port) and the I/O space consists of 64k bytes (32k 16-bit port). Memory devices exchange information with the CPU during memory read, memory write and instruction fetch bus cycles. I/O read and I/O write bus cycles use a separate I/O address space. Only IN/OUT instruction can access I/O address space, and information must be transferred between the peripheral devices and the AX register. The first 256 bytes of I/O space can be accessed directly by the I/O instructions. The entire 64k bytes I/O address space can be accessed indirectly, through the DX register. I/O instructions always force address A[22:16] to low level.



Memory and I/O Space

11.3 Data Bus

The memory address space data bus is physically implemented by dividing the address space into two banks of up to 8M bytes. One bank connects to the lower half of the data bus and contains the even-addressed bytes (A0=0); the other bank connects to the upper half of the data bus and contains odd-addressed bytes (A0=1). WHB_n and WLB_n determine whether one bank or both banks participate in the data transfer.

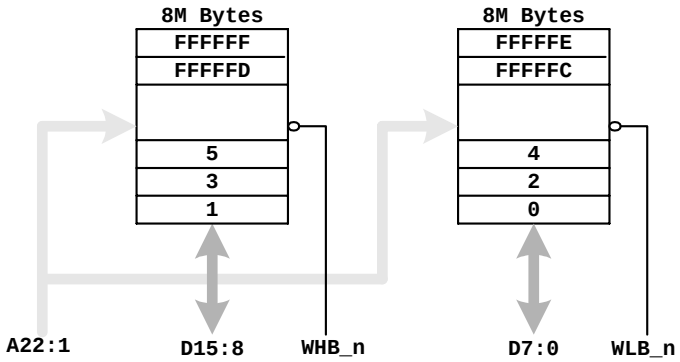
Functionality of WHB_n and WLB_n can be implemented by BHE_n, A0 and WR_n. The BHE_n and A0 pins are encoded as below.

BHE_n	A0	Bus Cycle
0	0	Word Transfer
0	1	High Byte Transfer
1	0	Low Byte Transfer
1	1	Reserved

Therefore, WHB_n and WLB_n can be considered as:

WHB_n = BHE_n logic or WR_n

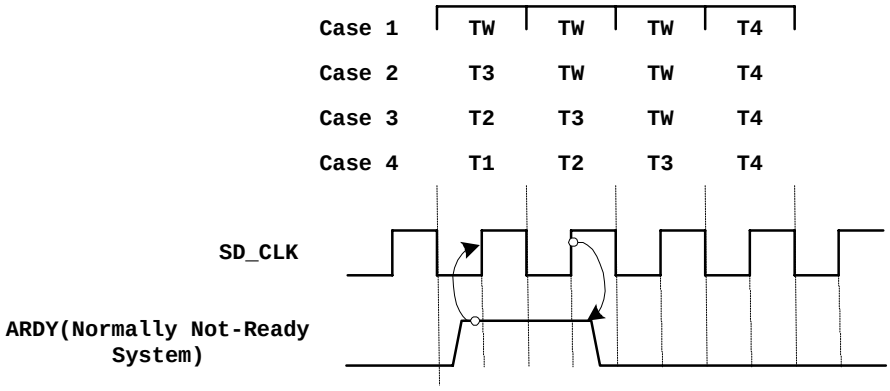
WLB_n = A0 logic or WR_n



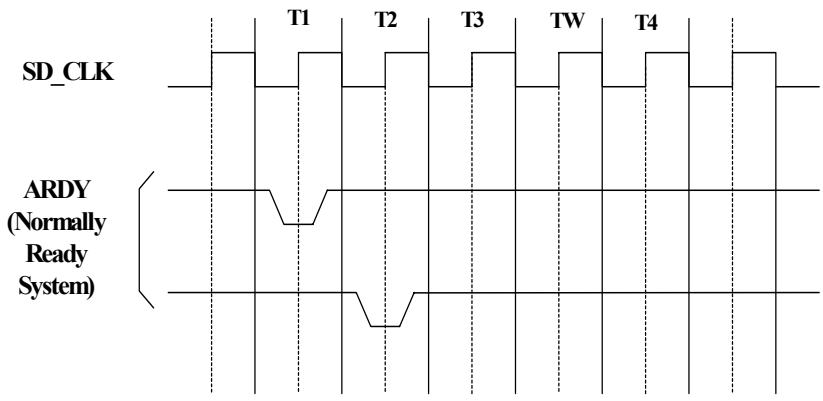
Physical Data Bus Models

11.4 Wait States

Wait states extend the data phase of the bus cycle. The ARDY input with low level will be inserted wait states in. To avoid wait states, ARDY must be high within a specified setup time prior to phase 2 of T1 and keep to phase 2 of T2. To insert wait states, ARDY must be driven low within a specified setup time prior to phase 2 of T1 or phase 2 of T2. When the SDRAMEN bit in the SDRAM Control Register (FEF4h) is set to 1, the external ready ARDY and internal wait states are ignored while accessing the SDRAMs.



Asynchronous Ready Waveforms



Asynchronous Ready Waveforms

11.5 Bus Width

Default for the R2880 is 16-bit bus access and the bus can be programmed as 8-bit or 16-bit access during memory or I/O access is located in the PCSx_n address space. The UCS_n code- fetched selection can be 8-bit or 16-bit bus width, which is decided by the BWSEL pin input status when the RST_n pin goes from low to high. When the BWSEL pin is with a pull-low resistor, the bus width for the code-fetched selection is 8 bits. The SDRAM bus width is unchangeable 16 bits. If the R2880 has been set as 16-bit mode, it cannot be changed to 8-bit mode.

Register Offset: F2h
Register Name: Auxiliary Configuration Register
Reset Value : 0080h

15	14	13	12	11	10 9 8	7	6	5	4	3	2	1	0
PCS6	PCS5	PCS3	PCS2	PCS1	Reserved	USIZ	0	0	0	0	0	MSIZ	PCS0

Bit	Name	Attribute	Description
15	PCS6	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
14	PCS5	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
13	PCS3	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
12	PCS2	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
11	PCS1	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.
10-8	Rsvd	RO	Reserved
7	USIZ	RO	Boot code bus width. This bit reflects the BWSEL pin input status when the RST_n pin goes from low to high. Set 0: 16-bit bus width booting when the BWSEL pin is **without a pull-low** resistor. (Default: It is an internal pull-high resistor.) Set 1: 8-bit bus width booting when the BWSEL pin is with a 4.7k ohm external pull-low resistor.
6-2	Rsvd	RO	Reserved
1	MSIZ	R/W	Midrange Data Bus Size selection. This bit determines the width of the data bus for all MCS and PCS space accesses (if mapped to memory space). 1: 8-bit data bus access. 0: 16-bit data bus access.
0	PCS0	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. 1: 8-bit data bus access. 0: 16-bit data bus access.

12. Chip Select UNIT

The Chip Select Unit provides 9 programmable chip select pins to access a specific memory or peripheral device. The chip selects are programmed through five peripheral control registers (A0h, A2h, A4h, A6h and A8h) and all the chip selects can be inserted wait states in by programming the peripheral control registers.

12.1 UCS_n

The UCS_n default is active on reset for Code access. The active memory range is upper 8M (800000h – FFFFFFh), which is programmable. And the default memory active range of UCS_n is 64k (FF0000h – FFFFFFh). UCS_n will drive low within four SD_CLK cycles when active if no wait state is inserted. There are fifteen wait states inserted into UCS_n active cycle on reset.

Register Offset: A0h
Register Name: Upper Memory Chip Select Register
Reset Value : F03Bh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	LB[2:0]			0	0	0	0	0	0	1	1	R3	R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14-12	LB[2:0]	R/W	**LB[2:0]**, Memory block size selection for UCS_n chip select pin. The active region of the UCS_n chip select pin can be configured by LB[2:0]. The default memory block size is from 800000h to FFFFFFh. Please refer to the following **Upper Memory Block Size** table for register FFAAh bit 5-3.
11-4	Rsvd	RO	Reserved
3	R3	R/W	See Bit[1:0].
2	R2	R/W	Ready Mode. This bit is used to configure the ready mode for the UCS_n chip select. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit3, Bit 1-0: R3, R1-R0**, Wait-State value. R2880 can insert wait states for an access to the UCS_n memory cycle. The reset value for (R3, R1, R0) is (1, 1, 1). **R3, R1, R0 -- Wait States** 0, 0, 0 -- 0 0, 0, 1 -- 1 0, 1, 0 -- 2 0, 1, 1 -- 3 1, 0, 0 -- 5

			1, 0, 1 -- 7 1, 1, 0 -- 9 1, 1, 1 -- 15

Upper Memory Block Size table:

FFAAh bit 5-3 \ LB[2:0]	000	100	110	111
000	512K	256K	128k	64k
001	1M	512K	256K	128k
010	2M	1M	512K	256K
011	4M	2M	1M	512K
100	8M	4M	2M	1M

12.2 LCS_n

LCS_n means the lower memory region chip selects. The active memory range is lower 8M (000000h – 7FFFFFh), which is programmable. It can be expanded to 8M bytes by FFAAh b2:0.

Register Offset: A2h
Register Name: Low Memory Chip Select Register
Reset Value : ——

15	14 13 12	11	10	9	8	7	6	5	4	3	2	1	0
0	LB[2:0]	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14-12	LB[2:0]	R/W	**LB[2:0]**, Memory block size selection for SDRAM memory region. The active region of SDRAM memory can be configured by LB[2:0]. The SDRAM memory region is not active on reset, but any read or write access to the Low Memory Chip Select Register (A2h) activates this region. Please refer to the following **Low Memory Block Size** table for register FFAAh bit 2-0.
11-0	Rsvd	RO	Reserved

Low Memory Block Size Table:

FFAAh bit2-0 \ LB[2:0]	000	001	011	111
000	64K	128K	256K	512K
001	128K	256K	512K	1M
010	256K	512K	1M	2M
011	512K	1M	2M	4M
100	1M	2M	4M	8M

12.3 PCSx_n

In order to define these pins, the peripheral or memory chip selects are programmed through A4h and A8h registers. The base address memory block can be located anywhere within the 1M-byte memory space, exclusive of the areas associated with SDRAM memory region and UCS_n. If the chip selects are mapped to I/O space, the access range is 64k bytes. PCS6_n – PCS5_n can be configured from (0 to 31wait states) + (1 to 225 wait states). PCS3_n – PCS0_n can be configured from (1 to 31 wait states) + (1 to 225 wait states). The PCSx_n pins are not active on reset. The PCSx_n pins are activated as chip selects by writing to the peripheral chip select register.

Register Offset: A4h
Register Name: Peripheral Chip Select Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA[19:12]								BA23	BA22	BA21	BA20	R3	R2	R1	R0

Bit	Name	Attribute	Description
15-8	BA[19:12]	R/W	Base Address. BA[23:12] corresponds to Bit [23:12] of the 16M-Byte(24-bits) programmable base address of the PCS_n chip select block. When the PCS_n chip selects are mapped to I/O space, BA[23:16] must be written to 0000b because the I/O address bus is only 64K bytes (16-bits) wide. Please refer to the following **Peripheral Chip Size** table for register FFAAh bit 8-6.
7-4	BA[23:20]	R/W	
3	R3	R/W	See Bit[1:0].
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the ready mode for the PCS3_n – PCS0_n chip selects. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit 3, Bit 1-0: R3, R1, R0**, Wait-State Values. PR4 (refer to Bit 5 in the A8h register), R3, R1, and R0 determine the number of wait states inserted into T3 of the PCS3_n – PCS0_n access. **PR4, R3, R1, R0 -- Wait States** 0, 0, 0, 0 -- 1 0, 0, 0, 1 -- 3 0, 0, 1, 0 -- 5 0, 0, 1, 1 -- 7 0, 1, 0, 0 -- 9 0, 1, 0, 1 -- 15 0, 1, 1, 0 -- 25 0, 1, 1, 1 -- 40 1, 0, 0, 0 -- 60 1, 0, 0, 1 -- 80 1, 0, 1, 0 -- 100 1, 0, 1, 1 -- 125 1, 1, 0, 0 -- 150

			1, 1, 0, 1 -- 180 1, 1, 1, 0 -- 210 1, 1, 1, 1 -- 255

Peripheral Chip Size table:

FFAAh bit8-6	PCS0	PCS1	PCS2	PCS3	PCS5	PCS6
000	BASE	BASE+256	BASE+512	BASE+768	BASE+1280	BASE+1536
001	BASE	BASE+512	BASE+1024	BASE+1536	BASE+2560	BASE+3072
010	BASE	BASE+1024	BASE+2048	BASE+3072	BASE+5120	BASE+6144
011	BASE	BASE+2048	BASE+4096	BASE+6144	BASE+10240	BASE+12288
100	BASE	BASE+4096	BASE+8192	BASE+12288	BASE+20480	BASE+24576

12.4 MCS_n

Register Offset: A6h
Register Name: Midrange Chip Select Register
Reset Value : 0100h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA[19:13]							Rsvd	BA23	BA22	BA21	BA20	R3	R2	R1	R0

The base address can be set to any integer multiple of the size of the memory block size selected in this Midrange Chip Select Register. For example, if the midrange block is 16Kbytes, the block could be located at 100000h, 104000h, or 108000h, but not at 102000h.

Bit	Name	Attribute	Description
15-9	BA[19:13]	R/W	Base Address. BA[23:13] corresponds to Bit [7:4] and Bit [15:9] of the 16M-Byte (24-bits) programmable base address of the MCS chip select block. Bit 8 is Reserved and always 1.
8	Rsvd	RO	
7-4	BA[23:20]	R/W	
3	R3	R/W	See Bit[1:0].
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the ready mode for the MCS chip selects. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit 3, Bit 1-0: R3, R1, R0**, Wait-State Values. R3, R1, and R0 determine the number of wait states inserted into T3 of the MCS_n access. With regard to the values of R4, please refer to bit 4 in the FFACh register. **R4, R3, R1, R0 -- Wait States** 0, 0, 0, 0 -- 1 0, 0, 0, 1 -- 3 0, 0, 1, 0 -- 5 0, 0, 1, 1 -- 7 0, 1, 0, 0 -- 9 0, 1, 0, 1 -- 15

			0,	1,	1,	0	--	25
			0,	1,	1,	1	--	40
			1,	0,	0,	0	--	60
			1,	0,	0,	1	--	80
			1,	0,	1,	0	--	100
			1,	0,	1,	1	--	125
			1,	1,	0,	0	--	150
			1,	1,	0,	1	--	180
			1,	1,	1,	0	--	210
			1,	1,	1,	1	--	255

Register Offset: A8h

Register Name: PCS_n and MCS_n Auxiliary Register

Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	M[6:0]							MCS MS	MS	PR4	R4	R3	R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14-8	M[6:0]	R/W	MCS_n Block Size (M[6:0]). Please refer to the following **Midrange Memory Block Size** table for register FFAAh bit 11-9.
7	MCSMS	R/W	MCS map selector Set 1: for memory space. Set 0: for I/O space. Default value 1: as memory space. If MCS is mapped to I/O space and conflicts with PCB region, then MCS won't be activated. For example, if MCS is configured as 64K and mapped to I/O space, MCS_n won't be activated while I/O accesses EAh. However, MCS_n will be activated while 0000h is accessed.
6	MS	R/W	Memory or IO space selector. This bit determines whether the PCS_n pins are active during memory bus cycle or IO bus cycle. Set 1: PCS_n is active for memory cycle. Set 0: PCS_n is active for IO cycle.
5	PR4	R/W	See bit[1:0] in the A4h register.
4-3	R[4:3]	R/W	See bit[1:0]
2	R2	R/W	Ready Mode. This bit only applies to the PCS6_n – PCS5_n chip selects. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit 4-3 and Bit 1-0: R4, R3, R1, R0**, Wait-State Values. R4, R3, R1, and R0 determine the number of wait states inserted into T3 of the PCS5_n – PCS6_n access. **R4, R3, R1, R0 -- Wait States** 0, 0, 0, 0 -- 1 0, 0, 0, 1 -- 3

			0, 0, 1, 0 -- 5 0, 0, 1, 1 -- 7 0, 1, 0, 0 -- 9 0, 1, 0, 1 -- 15 0, 1, 1, 0 -- 25 0, 1, 1, 1 -- 40 1, 0, 0, 0 -- 60 1, 0, 0, 1 -- 80 1, 0, 1, 0 -- 100 1, 0, 1, 1 -- 125 1, 1, 0, 0 -- 150 1, 1, 0, 1 -- 180 1, 1, 1, 0 -- 210 1, 1, 1, 1 -- 255

Midrange Memory Block Size table:

FFAAh bit[11:9]					
Total Block Size 000	Total Block Size 001	Total Block Size 010	Total Block Size 011	Total Block Size 100	M[6:0]
8K	16K	32K	64K	128K	0000001b
16K	32K	64K	128K	256K	0000010b
32K	64K	128K	256K	512K	0000100b
64K	128K	256K	512K	1M	0001000b
128K	256K	512K	1M	2M	0010000b
256K	512K	1K	2M	4M	0100000b
512K	1M	2M	4M	8M	1000000b

Register Offset: AAh
Register Name: Chip Size Multiplier Register
Reset Value : 0000h

15	14 13 12	11 10 9	8 7 6	5 4 3	2 1 0
Rsvd	W[2:0]	M[2:0]	P[2:0]	U[2:0]	L[2:0]

Bit	Name	Attribute	Description
15	Rsvd	R	Reserved
14-12	W[2:0]	R/W	Wait-State Value. W[2:0] determine the number of wait states inserted into T1 of PCS6_n, PCS5_n and the PCS3_n – PCS0_n access. **W2, W1, W0 -- Wait States** 0, 0, 0 -- 0 0, 0, 1 -- 1 0, 1, 0 -- 3 0, 1, 1 -- 7 1, 0, 0 -- 11 1, 0, 1 -- 15

			1, 1, 0 -- 20 1, 1, 1 -- 31
11-9	M[2:0]	R/W	MCS chip select size multiplier
8-6	P[2:0]	R/W	PCS chip select size multiplier
5-3	U[2:0]	R/W	UCS chip select size multiplier
2-0	L[2:0]	R/W	LCS chip select size multiplier

Register Offset: ACh
Register Name: MCS_n Extended Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	R4	0	W2	W1	W0

Bit	Name	Attribute	Description
15-5	Rsvd	R/O	Defaults: 0.
4	R4	R/W	Default: 0. Please see the description for bit 1-0 in the A6h register.
3	Rsvd	RO	Default: 0
2-0	W[2:0]	R/W	T1 Wait-State Value. Defaults: 0. **W2, W1, W0 -- Wait States** 0, 0, 0 -- 0 0, 0, 1 -- 1 0, 1, 0 -- 3 0, 1, 1 -- 7 1, 0, 0 -- 11 1, 0, 1 -- 15 1, 1, 0 -- 20 1, 1, 1 -- 31

Register Offset: AEh
Register Name: Chip Select Recovery Time Configuration Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				UCSRTC				MCSRTC				PCSRTC			

Bit	Name	Attribute	Description
15-12	Rsvd	R/O	Defaults: 0.
11-8	UCSRTC	R/W	UCS recovery time configuration.
7-4	MCSRTC	R/W	MCS recovery time configuration.
3-0	PCSRTC	R/W	PCS recovery time configuration.

Configuration	Recovery Time (clock cycle)
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

13. Double-Word Access Unit

Register Offset: 00h
Register Name: Double Word Access Address – Low Word Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LADDR														Reserved	

Bit	Name	Attribute	Description
15-2	LADDR	R/W	Double word access Address [15:2].
1-0	Rsvd	RO	Reserved.

Register Offset: 02h
Register Name: Double Word Access Address – High Word Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIO	Reserved							HADDR							

Bit	Name	Attribute	Description
15	MIO	R/W	Memory / IO space: Set 1: Indicate memory space. Set 0: Indicate IO space.
14-8	Rsvd	RO	Reserved. These bits always return ’0’s.
7-0	HADDR	R/W	Double word access Address [23:16].

Register Offset: 04h
Register Name: Double Word Access Data – Low Word Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LDATA															

Bit	Name	Attribute	Description
15-0	LDATA	R/W	Double word access Data [15:0].

Register Offset: 06h
Register Name: Double Word Access Data – High Word Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HDATA															

Bit	Name	Attribute	Description
15-0	HDATA	R/W	Double word access Data [31:16].

14. PCI Configuration Space Access Unit

Register Offset: 08h (Word Access)
Register Name: PCI Configuration Address – Low Word Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVN					FUNN			REGN							

Bit	Name	Attribute	Description
15-11	DEVN	R/W	**Device Number.** This field selects one agent on the PCI bus. During a Type 1 configuration cycle, this field is mapped to PAD[15:11]. During a Type 0 configuration cycle, this field is decoded and one of PAD[31:11] is driven to 1. The R2880 is always Device number 0.
10-8	FUNN	R/W	**Function Number.** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The R2880 North Bridge only responds to configuration cycle with a function number of 000b.
7-0	REGN	R/W	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. *Note: Bit 1-0 are write only. When read, they are always returned as '0s'.*

Register Offset: 0Ah (Word Access)
Register Name: PCI Configuration Address – High Word Register
Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CE	Reserved							BUSN							

Bit	Name	Attribute	Description
15	CE	R/W	**Configuration Enable.** When this bit is set to 1, accesses to PCI configuration space are enabled. If this bit is reset to 0, accesses to PCI configuration space are disabled.
14-8	Rsvd	RO	**Reserved.**
7-0	BUSN	R/W	**Bus Number.** When the bus number is programmed to 00h, the target of the configuration cycle is either the R2880 or the PCI Device that is connected to the R2880. If the bus number is programmed to 00h and the R2880 is not the target, a Type 0 configuration cycle is generated on PCI Bus. If the bus number is non-zero, a Type 1 configuration cycle is generated on PCI bus with the bus number mapped to PAD[23:16] during the address phase.

Register Offset: 0Fh – 0Ch (Dword Access – Word, Byte Access are option)
Register Name: Configuration Data Register
Reset Value: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDR																															

Configuration Data Register is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by Configuration Data Register is determined by the contents of Configuration Address Register.

Bit	Name	Attribute	Description
31-0	CDR	R/W	If bit 15 of PCI Configuration Address – High Word Register is 1, any I/O reference that falls in the PCI Configuration Data Register space is mapped to configuration space with the contents of PCI Configuration Address Register.

15. Refresh Control UNIT

The Refresh Control Unit (RCU) automatically generates refresh bus cycle. After a period of time, the RCU generates a memory read request to the bus interface unit.

A user guide to program SDRAM:

(1) Configure Lower Memory Chip Select Register (A2h) and Chip Size Multiplier Register (AAh) to set SDRAM space.

(2) Set Clock Pre-scaler Register (E2h) and enable RCU Register (E4h) to enable SDRAM refresh

Register Offset: E2h
Register Name: Clock Pre-scaler Register
Reset Value : 0080h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RC[14:0]														

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14-0	RC[14:0]	RW	Refresh Counter Reload Value. It contains the value of the desired clock count interval between refresh cycles. The counter value should not be set to less than 12h, otherwise there would never be sufficient bus cycle available for the processor to execute code. For Example: SDRAM specification specifies to refresh 1 time every 15.6 u sec and system clock is 25Mhz. The Refresh Counter Reload Value = 15.6us*25Mhz = 15.6us / 40ns = 390.

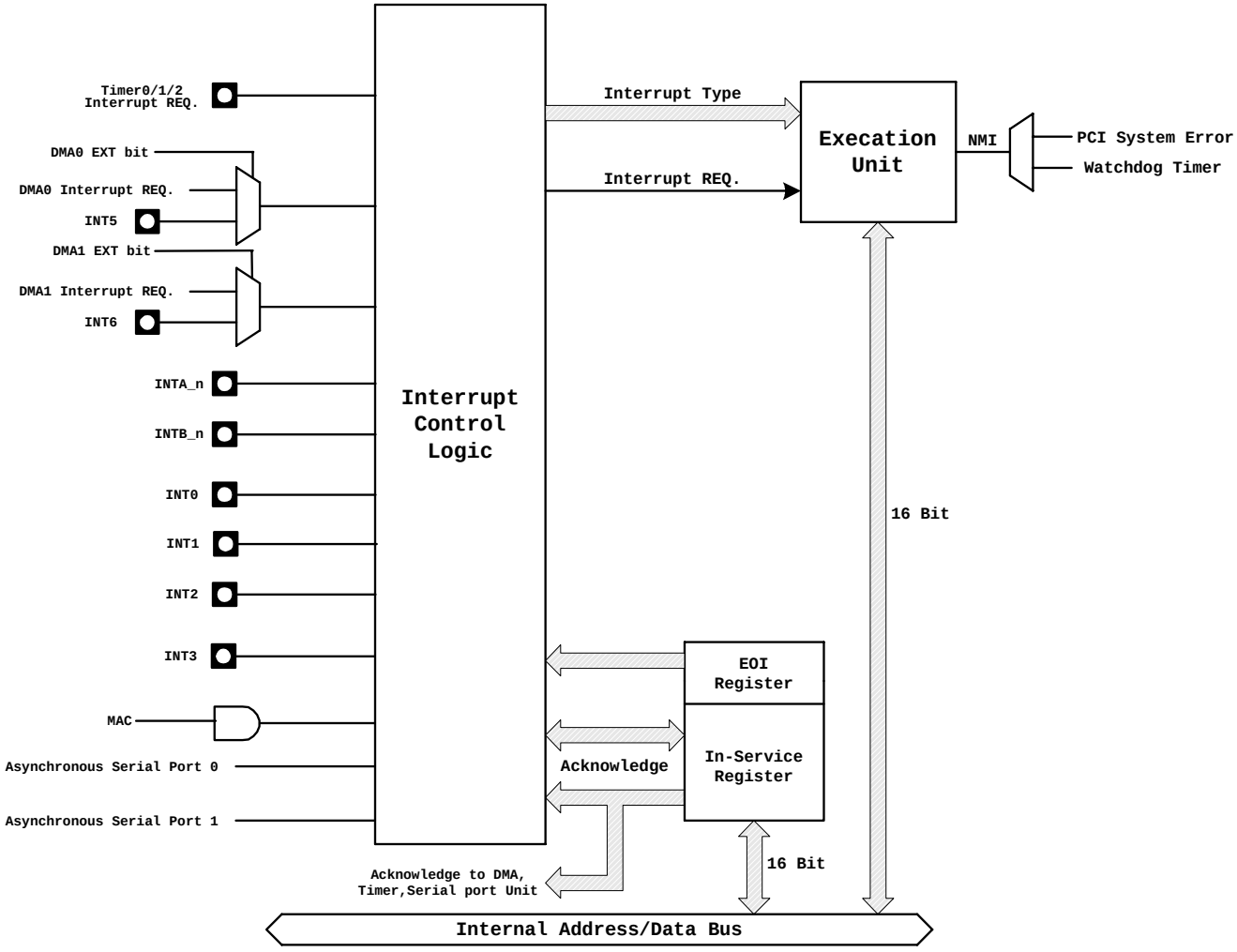
Register Offset: E4h
Register Name: Enable RCU Register
Reset Value : 8000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	T[14:0]														

Bit	Name	Attribute	Description
15	E	RW	Enable RCU Set 1: Enable the refresh counter unit. Set 0: Clear the refresh counter and stop refresh requests, but will not reset the refresh address.
14-0	T[14:0]	RO	Refresh Count. This read-only field contains the present value of the down counter which triggers refresh requests.

16. Interrupt Controller UNIT

There are 18 interrupt request sources connected to the controller: 6 maskable interrupt pins (INT[3:0], INT5 and INT6); 2 dedicated Interrupt pins for PCI interface (INTA_n and INTB_n); 1 non-maskable interrupt (WDT); 9 internal unit request sources (Timer 0, 1 and 2; DMA 0 and 1; MAC 0 and1; Asynchronous Serial Port 0 and 1).



Interrupt Control Unit Block Diagram

16.1 Interrupt Vector, Type and Priority

The following table shows the interrupt vector address, type and the priority. Programming the priority registers will change the maskable interrupt priority. The vector address for each interrupt is fixed.

Interrupt source	Interrupt Type	Vector Address	EOI Type	Priority	Note
Divide Error Exception	00h	00h		1	
Trace interrupt	01h	04h		1-1	*
NMI	02h	08h		1-2	*
Breakpoint Interrupt	03h	0Ch		1	
INTO Detected Over Flow Exception	04h	10h		1	
Array Bounds Exception	05h	14h		1	
Undefined Op code Exception	06h	18h		1	
ESC Op code Exception	07h	1Ch		1	
Timer 0	08h	20h	08h	2-1	*
Reserved	09h				
DMA 0/INT5	0Ah	28h	0Ah	3	
DMA 1/INT6	0Bh	2Ch	0Bh	4	
INT0	0Ch	30h	0Ch	5	
INT1	0Dh	34h	0Dh	6	
INT2	0Eh	38h	0Eh	7	
INT3	0Fh	3Ch	0Fh	8	
MAC	10h	40h	10h	9	
Asynchronous Serial port 1	11h	44h	11h	9	
Timer 1	12h	48h	08h	2-2	*
Timer 2	13h	4Ch	08h	2-3	*
Asynchronous Serial port 0	14h	50h	14h	9	
PCI INTA	15h	54h	15h	A	
PCI INTB	16h	58h	16h	A	
Reserved					

Note *: When the interrupt occurs in the same time, the priority is (1-1 > 1-2); (2-1> 2-2 > 2-3)

16.2 Interrupt Requests

When an interrupt is requested, the internal interrupt controller verifies that the interrupt is enabled (the IF flag is enabled and the MSK bit is not set) and there are no higher priority interrupt requests being serviced or pending. If the interrupt is granted, the interrupt controller uses the interrupt type to access a vector from the interrupt vector table.

If the external INT is active (level-triggered) to request the interrupt controller service, the INT pins must be held till the micro controller enters the interrupt service routine. There is no interrupt-acknowledge output when running in fully nested mode, so the PIO pins should be used to simulate the interrupt-acknowledge pin if necessary.

16.3 Programming the Registers

Software is programmed through the registers (4Ah, 48h, 44h, 42h, 40h, 3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 26h, 24h and 22h) to define the interrupt controller operation.

Register Offset: 4Ah
Register Name: PCI INTB Control Register
Reset Value : 003Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Rsvd	ELS	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by an edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	Rsvd	RO	Reserved
5	ELS	R/W	Edge/Level Select Set 1 = Falling edge/Low-level trigger. Set 0 = Rising edge/High-level trigger.
4	LTM	R/W	Level-Triggered Mode. Set 1: An interrupt is triggered by a level. Set 0: An interrupt is triggered by the edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INTB. Set 0: Enable the INTB interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit 2-0 in the 44h register.

Register Offset: 48h
Register Name: PCI INTA Control Register
Reset Value : 003Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Rsvd	ELS	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by an edge going from low to high. The low to high edge will be latched

			(one level) till this interrupt is serviced.
6	Rsvd	RO	Reserved
5	ELS	R/W	Edge/Level Select Set 1: Falling edge/Low-level trigger. Set 0: Rising edge/High-level trigger.
4	LTM	R/W	Level-Triggered Mode. Set 1: An interrupt is triggered by a level. Set 0: An interrupt is triggered by the edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INTA. Set 0: Enable the INTA interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit 2-0 in the 44h register.

Register Offset: 44h
Register Name: Serial Port 0 Interrupt Control Register
Reset Value : 001Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the asynchronous serial port 0. Set 0: Enable the serial port 0 interrupt.
2-0	PR[2:0]	R/W	Priority. These bits determine the priorities of the serial ports relative to the other interrupt signals. **The priority selection:** **PR2**, **PR1**, **PR0** -- **Priority** 0 , 0 , 0 -- 0 (High) 0 , 0 , 1 -- 1 0 , 1 , 0 -- 2 0 , 1 , 1 -- 3 1 , 0 , 0 -- 4 1 , 0 , 1 -- 5 1 , 1 , 0 -- 6 1 , 1 , 1 -- 7 (Low)

Register Offset: 42h
Register Name: Serial Port 1 Interrupt Control Register
Reset Value : 001Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the asynchronous serial port 1. Set 0: Enable the serial port 1 interrupt.
2-0	PR[2:0]	R/W	Priority. These bits determine the priorities of the serial ports relative to the other interrupt signals. **The priority selection:** **PR2**, **PR1**, **PR0** -- **Priority** 0 , 0 , 0 -- 0 (High) 0 , 0 , 1 -- 1 0 , 1 , 0 -- 2 0 , 1 , 1 -- 3 1 , 0 , 0 -- 4 1 , 0 , 1 -- 5 1 , 1 , 0 -- 6 1 , 1 , 1 -- 7 (Low)

Register Offset: 40h
Register Name: MAC Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set to 1 and bit 4 is cleared to 0, an interrupt is triggered by an edge from MAC0 or MAC1, which goes from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved
4	LTM	R/W	Level-Triggered Mode. Set 1: An interrupt is triggered by a level. Set 0: An interrupt is triggered by the edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of MAC.

			Set 0: Enable the MAC interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit 2-0 in the 44h register.

Register Offset: 3Eh
Register Name: INT3 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Rsvd	ELS	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by an edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	Rsvd	RO	Reserved
5	ELS	R/W	Edge/Level Select Set 1 = Falling edge/Low-level trigger. Set 0 = Rising edge/High-level trigger.
4	LTM	R/W	Level-Triggered Mode. Set 1: An interrupt is triggered by a level. Set 0: An interrupt is triggered by the edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT3. Set 0: Enable the INT3 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit 2-0 in the 44h register.

Register Offset: 3Ch
Register Name: INT2 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Rsvd	ELS	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is cleared to 0, an interrupt is

			triggered by an edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	Rsvd	RO	Reserved
5	ELS	R/W	Edge/Level Select Set 1 = Falling edge/Low-level trigger. Set 0 = Rising edge/High-level trigger.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by a level. Set 0: An interrupt is triggered by the edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT2. Set 0: Enable the INT2 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit 2-0 in the 44h register.

Register Offset: 3Ah
Register Name: INT1 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	ELS	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by an edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT1
5	ELS	R/W	Edge/Level Select Set 1: falling edge /Low-level trigger Set 0: rising edge /High-level trigger
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by a level. Set 0: An interrupt is triggered by the edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT1. Set 0: Enable the INT1 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit 2-0 in the 44h register.

Register Offset: 38h
Register Name: INT0 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	ELS	LTM	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge trigger mode enable. When this bit is set and bit 4 is cleared to 0, an interrupt is triggered by an edge going from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT0
5	ELS	R/W	Edge/Level Select. Set 1: Falling edge/Low-level trigger. Set 0: Rising edge/High-level trigger.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by a level. Set 0: An interrupt is triggered by the edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of INT0. Set 0: Enable the INT0 interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit 2-0 in the 44h register.

Register Offset: 36h
Register Name: DMA1/INT6 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	LS	0	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved
5	LS	R/W	Level Select. Set 1: Low-level trigger. Set 0: High-level trigger.
4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA1 controller. Set 0: Enable the DMA1 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit 2-0 in the 44h register.

Register Offset: 34h
Register Name: DMA0/INT5 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	LS	0	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved
5	LS	R/W	Level Select Set 1 = Low-level trigger. Set 0 = High-level trigger.
4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the DMA0 controller. Set 0: Enable the DMA0 controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit 2-0 in the 44h register.

Register Offset: 32h
Register Name: Timer Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source of the timer controller. Set 0: Enable the timer controller interrupt.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those for bit 2-0 in the 44h register.

Register Offset: 30h
Register Name: Interrupt Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DHLT	Reserved									MAC1	MAC0	Rsvd	TMR2	TMR1	TMR0

The **reset value** is not defined.

Bit	Name	Attribute	Description
15	DHLT	RO	DMA Halt. Set 1: Halt any DMA activity when non-mask able interrupts occur. Set 0: When an IRET instruction is executed.
14-6	Rsvd	RO	Reserved
5-4	MAC[1:0]	R/W	Indicate that the corresponding MAC controller has an interrupt request while set to 1.
3	Rsvd	RO	Reserved
2-0	TMR[2:0]	R/W	Indicate that the corresponding timer has an interrupt request pending while set to 1.

Register Offset: 2Eh
Register Name: Interrupt Request Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			PIB	PIA	SP0	SP1	MAC	I3	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR

The Interrupt Request register is a read-only register. For internal interrupts (SP0, SP1, D1/I6, D0/I5, MAC, and TMR), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge. For INT[3:0], INTA_n and INTB_n external interrupts, the corresponding bits (I[3:0], PIA and PIB) reflect the current values of the external signals.

Bit	Name	Attribute	Description
15-13	Rsvd	RO	Reserved
12	PIB	RO	PCI Interrupt Requests. Set 1: The corresponding INTB pin has an interrupt pending.
11	PIA	RO	PCI Interrupt Requests. Set 1: The corresponding INTA pin has an interrupt pending.
10	SP0	RO	Serial Port 0 Interrupt Request. Indicates the interrupt status of the serial port 0.
9	SP1	RO	Serial Port 1 Interrupt Request. Indicates the interrupt status of the serial port 1.
8	MAC	RO	MAC Interrupt Request. Indicates the interrupt status of the MAC1 **or** MAC0.

7-4	I[3:0]	RO	Interrupt Requests. Set 1: The corresponding INT pin has an interrupt pending.
3-2	D1/I6 – D0/I5	RO	DMA Channel or INT Interrupt Request. Set 1: The corresponding DMA channel or INT has an interrupt pending.
1	Rsvd	RO	Reserved
0	TMR	RO	Timer Interrupt Request. Set 1: The timer control unit has an interrupt pending.

Register Offset: 2Ch
Register Name: Interrupt In-Service Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			PIB	PIA	SP0	SP1	MAC	I3	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR

In this Register, bits are set by the interrupt controller when the interrupt is taken and each bit is cleared by writing the corresponding interrupt type to the EOI register.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
12	PIB	R/W	PCI Interrupt B In-Service. Set 1: the corresponding INTB interrupt is currently being serviced.
11	PIA	R/W	PCI Interrupt A In-Service. Set 1: the corresponding INTA interrupt is currently being serviced.
10	SP0	R/W	Serial Port 0 Interrupt In-Service. Set 1: the serial port 0 interrupt is currently being serviced.
9	SP1	R/W	Serial Port 1 Interrupt In-Service. Set 1: the serial port 1 interrupt is currently being serviced.
8	MAC	R/W	MAC In-Service. Indicates the MAC1 **OR** MAC0 interrupt is currently being serviced.
7-4	I[3:0]	R/W	Interrupt In-Service. Set 1: the corresponding INT interrupt is currently being serviced.
3-2	D1/I6 – D0/I5	R/W	DMA Channel or INT Interrupt In-Service. Set 1: the corresponding DMA channel or INT interrupt is currently being serviced.
1	Rsvd	RO	Reserved
0	TMR	R/W	Timer Interrupt In-Service. Set 1: the timer interrupt is currently being serviced.

Register Offset: 2Ah
Register Name: Priority Mask Register
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

It determines the minimum priority level at which mask able interrupts can generate interrupts.

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved
2-0	PRM[2:0]	R/W	Priority Field Mask, determining the minimum priority that is required in order for a mask able interrupt source to generate an interrupt. **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

Register Offset: 28h
Register Name: Interrupt Mask Register
Reset Value : FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			PIB	PIA	SP0	SP1	MAC	I3	I2	I1	I0	D1/I6	D0/I5	Rsvd	TMR

Bit	Name	Attribute	Description
15-13	Rsvd	RO	Reserved
12	PIB	R/W	PCI Interrupt B Mask. When set 1, this bit indicates that the INTB_n is masked.
11	PIA	R/W	PCI Interrupt A Mask. When set 1, this bit indicates that the INTA_n is masked.
10	SP0	R/W	Serial Port 0 Interrupt Mask. When set 1, this bit indicates that the asynchronous serial port 0 interrupt is masked.
9	SP1	R/W	Serial Port 1 Interrupt Mask. When set 1, this bit indicates that the asynchronous serial port 1 interrupt is masked.
8	MAC	R/W	MAC Interrupt Mask. When set 1, this bit indicates that the MAC[1:0] interrupts are masked.
7-4	I[3:0]	R/W	External Interrupt Mask. When set 1, I[3:0] bits indicate that the corresponding interrupts are masked.
3-2	D1/I6 –	R/W	DMA Channel or INT Interrupt Masks.

	D0/I5		When set 1, these bits indicate that the corresponding interrupts are masked.
1	Rsvd	RO	Reserved
0	TMR	R/W	Timer Interrupt Mask. When set 1, this bit indicates that the Timer controller interrupt is masked.

Register Offset: 26h
Register Name: Poll Status Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

The Poll Status (POLLST) register mirrors the current state of the Poll register. The POLLST register can be read without affecting the current interrupt requests.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S4-S0 field contains valid data.
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

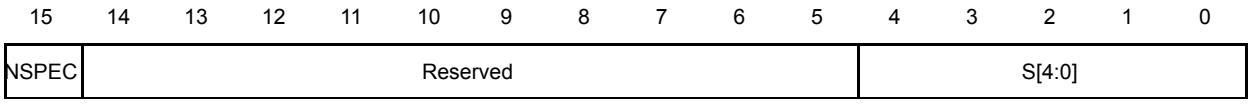
Register Offset: 24h
Register Name: Poll Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

When the Poll register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Poll register.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S[4:0] field contains valid data.
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

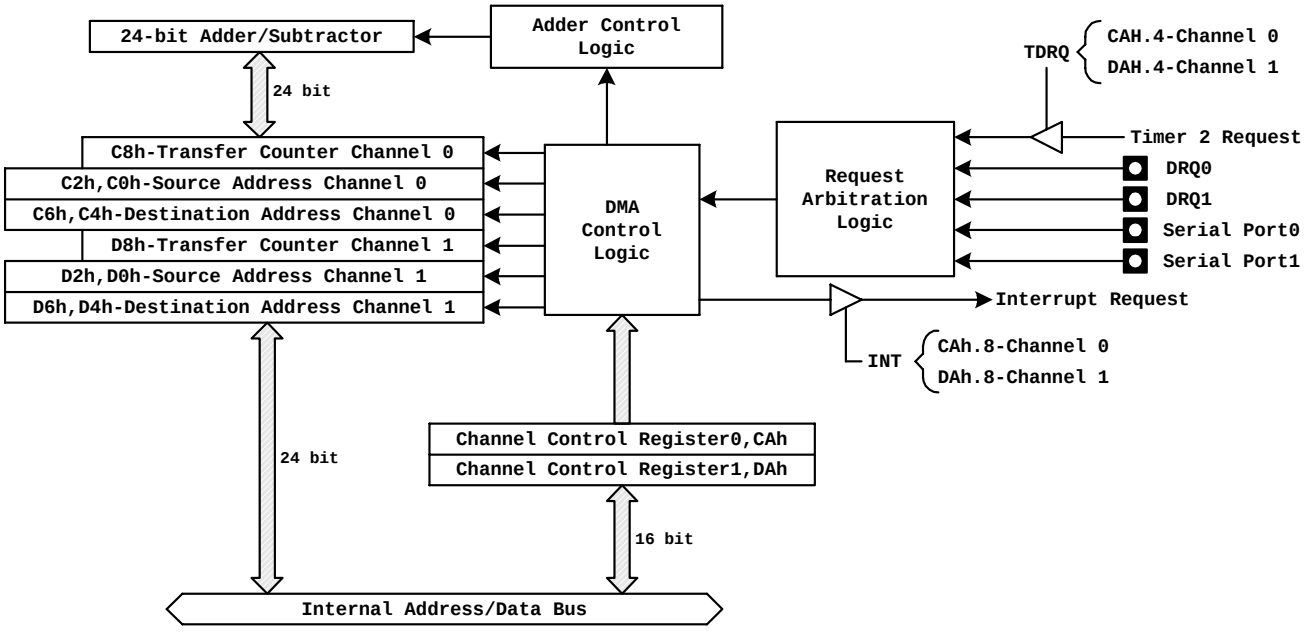
Register Offset: 22h
Register Name: End - Of - Interrupt
Reset Value : Write Only



Bit	Name	Attribute	Description
15	NSPEC	R/W	Non-Specific EOI. Set 1: indicates non-specific EOI. Set 0: indicates the specific EOI interrupt type in S[4:0].
14-5	Rsvd	RO	Reserved
4-0	S[4:0]	WO	Source EOI Type. It specifies the EOI type of the interrupt that is currently being processed.

17. DMA UNIT

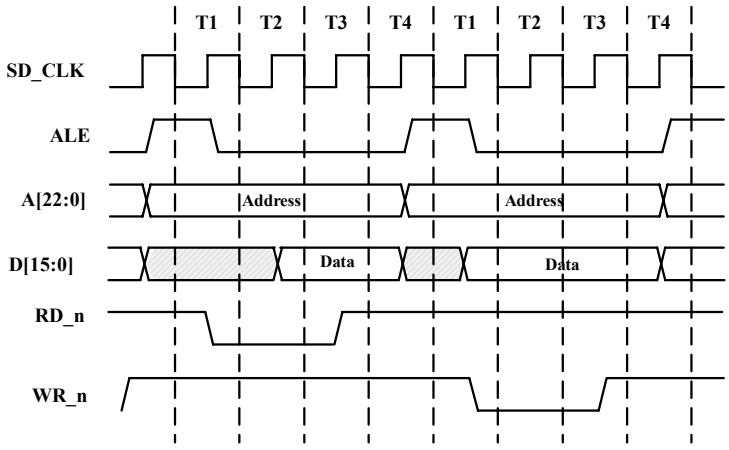
The DMA controller provides the data transfer between the memory and peripherals without the intervention of the CPU. There are two DMA channels in the DMA unit. Each channel can accept DMA requests from one of three sources: external pins (DRQ0 for channel 0 or DRQ1 for channel 1), serial ports (port 0 or port 1), or Timer 2 overflow. The data transfer from sources to destinations can be memory to memory, memory to I/O, I/O to I/O, or I/O to memory. Either bytes or words can be transferred to or from even or odd addresses and two bus cycles are necessary (read from sources and write to destinations) for each data transfer.



DMA Unit Block

17.1 DMA Operation

Every DMA transfer consists of two bus cycles (see figure of Typical DMA Transfer) and the two bus cycles cannot be separated by a bus hold request, a refresh request, or another DMA request. The registers (CAh, C8h, C6h, C4h, C2h, C0h, DAh, D8h, D6h, D4h, D2h, and D0h) are used to configure and operate the two DMA channels.



Typical DMA Transfer

Register Offset: CAh (DMA0)
Register Name: DMA0 Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO_n	DDEC	DINC	SM/IO_n	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	B_n/W

Bit	Name	Attribute	Description
15	DM/IO_n	R/W	Destination Address Space Select. Set 1: The destination address is in memory space. Set 0: The destination address is in I/O space.
14	DDEC	R/W	Destination Decrement. Set 1: The destination address is automatically decremented after each transfer. The B_n/W (bit 0) bit determines the decrement value, which is by 1 or 2 when both DDEC and DINC bits are set to 1 or 0. The address remains constant. Set 0: Disable the decrement function.
13	DINC	R/W	Destination Increment. Set 1: The destination address is automatically incremented after each transfer. The B_n/W (bit 0) bit determines the incremented value is by 1 or 2. Set 0: Disable the increment function.
12	SM/IO_n	R/W	Source Address Space Select. Set 1: The Source address is in memory space. Set 0: The Source address is in I/O space.
11	SDEC	R/W	Source Decrement. Set 1: The Source address is automatically decremented after each transfer. The B_n/W (bit 0) bit determines the decremented value is by 1 or 2 when both SDEC and SINC bits are set to 1 or 0. The address remains constant. Set 0: Disable the decrement function.
10	SINC	R/W	Source Increment. Set 1: The Source address is automatically incremented after each transfer. The

			B_n/W (bit 0) bit determines the incremented value is by 1 or 2. Set 0: Disable the increment function.
9	TC	R/W	Terminal Count. Set 1: The synchronized DMA transfer is terminated when the DMA Transfer Count Register reaches 0. Set 0: The synchronized DMA transfer is not terminated when the DMA Transfer Count Register reaches 0. Unsynchronized DMA transfer is always terminated when the DMA transfer count register reaches 0, regardless of the setting of this bit.
8	INT	R/W	Interrupt. Set 1: DMA unit generates an interrupt request when the transfer count is completed. The TC bit must be set to 1 to generate an interrupt.
7-6	SYN[1:0]	R/W	Synchronization Type Selection. **SYN1 , SYN0 -- Synchronization Type** 0 , 0 -- Unsynchronized 0 , 1 -- Source synchronized 1 , 0 -- Destination synchronized 1 , 1 -- Reserved
5	P	R/W	Priority. Set 1: It selects high priority for this channel when both DMA 0 and DMA 1 are transferred in the same time.
4	TDRQ	R/W	Timer Enable/Disable Request. Set 1: Enable the DMA requests from timer 2. Set 0: Disable the DMA requests from timer 2.
3	EXT	R/W	This bit enables the external interrupt functionality of the corresponding DRQ pin. Set 1: the external pin is an INT pin and requests on the pin are passed to the interrupt controller. Set 0: The pin functions as a DRQ pin.
2	CHG	R/W	Changed Start Bit. This bit must be set to 1 when the ST bit is modified.
1	ST	R/W	Start/Stop DMA channel. Set 1: Start the DMA channel Set 0: Stop the DMA channel
0	B_n/W	R/W	Byte/Word Select. Set 1: The address is incremented or decremented by 2 after each transfer. Set 0:The address is incremented or decremented by 1 after each transfer. Only byte transfer is supported if either source or destination bus width is 8 bit.

Register Offset: C8h (DMA0)
Register Name: DMA0 Transfer Count Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA 0 transfer Count. The value of this register will be decremented by 1 after each transfer.

Register Offset: C6h (DMA0)
Register Name: DMA0 Destination Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DDA[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DDA[23:16]	R/W	High DMA 0 Destination Address. These bits are mapped to A[23:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

Register Offset: C4h (DMA0)
Register Name: DMA0 Destination Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA[15:0]															

Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA 0 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [23:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: C2h (DMA0)
Register Name: DMA0 Source Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DSA[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DSA[23:16]	R/W	High DMA 0 Source Address. These bits are mapped to A[23:16] during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

Register Offset: C0h (DMA0)
Register Name: DMA0 Source Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA[15:0]															

Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA 0 Source Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA [23:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: DAh (DMA1)
Register Name: DMA1 Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO_n	DDEC	DINC	SM/IO_n	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	B_n/W

The definitions of Bit [15:0] for DMA0 are the same as those of Bit [15:0] of Register DAh for DMA1.

Register Offset: D8h (DMA1)
Register Name: DMA1 Transfer Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA 1 transfer Count. The value of this register will be decremented by 1 after each transfer.

Register Offset: D6h (DMA1)
Register Name: DMA1 Destination Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DDA[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DDA[23:16]	R/W	High DMA 1 Destination Address. These bits are mapped to A[23:16] during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

Register Offset: D4h (DMA1)
Register Name: DMA1 Destination Address Low Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA[15:0]															

Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA 1 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [23:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: D2h (DMA1)
Register Name: DMA1 Source Address High Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DSA[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	DSA[23:16]	R/W	High DMA 1 Source Address. These bits are mapped to A[23:16] during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 00000000b.

Register Offset: D0h (DMA1)
Register Name: DMA1 Source Address Low Register
Reset Value : ——

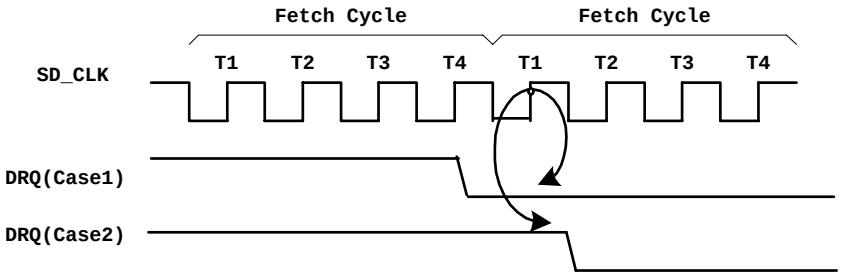
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA[15:0]															

Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA 1 Source Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA[23:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

17.2 External Requests

External DMA requests are asserted on the DRQ pins. The DRQ pins are sampled on the rising edge of SD_CLK. It takes a minimum of four clocks before the DMA cycle is initiated by the Bus Interface. The DMA request is cleared four clocks before the end of the DMA cycle. And no DMA acknowledge is provided, since the chip-selects (PCSx_n) can be programmed to be active for a given block of memory or I/O space, and the DMA source and destination address registers can be programmed to point to the same given block.

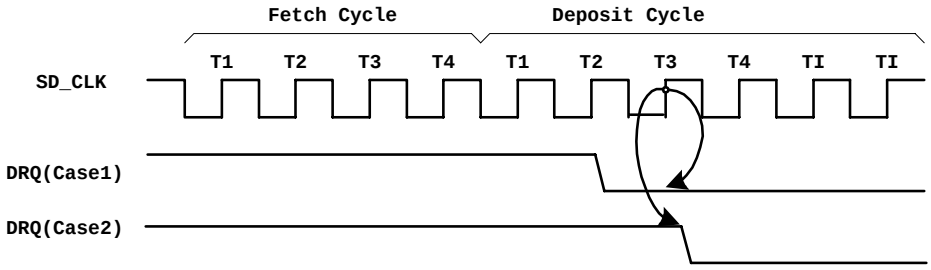
DMA transfer can be either source- or destination-synchronized, and it can also be unsynchronized. The Source-Synchronized Transfer figure shows the typical source-synchronized transfer, which provides the source device at least three clock cycles from the time. It is acknowledged to de-assert its DRQ line.



NOTES:
Case1 : Current source synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current source synchronized transfer will be immediately followed by antoher DMA transfer.

Source-Synchronized Transfers

The Destination-Synchronized Transfer figure shows the typical destination-synchronized transfer, which differs from a source-synchronized transfer in which two idle states are added to the end of the deposit cycle. The two idle states extend the DMA cycle to allow the destination device to de-assert its DRQ pin four clocks before the end of the cycle. If the two idle states were not inserted, the destination device would not have time to de-assert its DRQ signal.



NOTES:
Case1 : Current destination synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current destination synchronized transfer will be immediately followed by another DMA transfer.

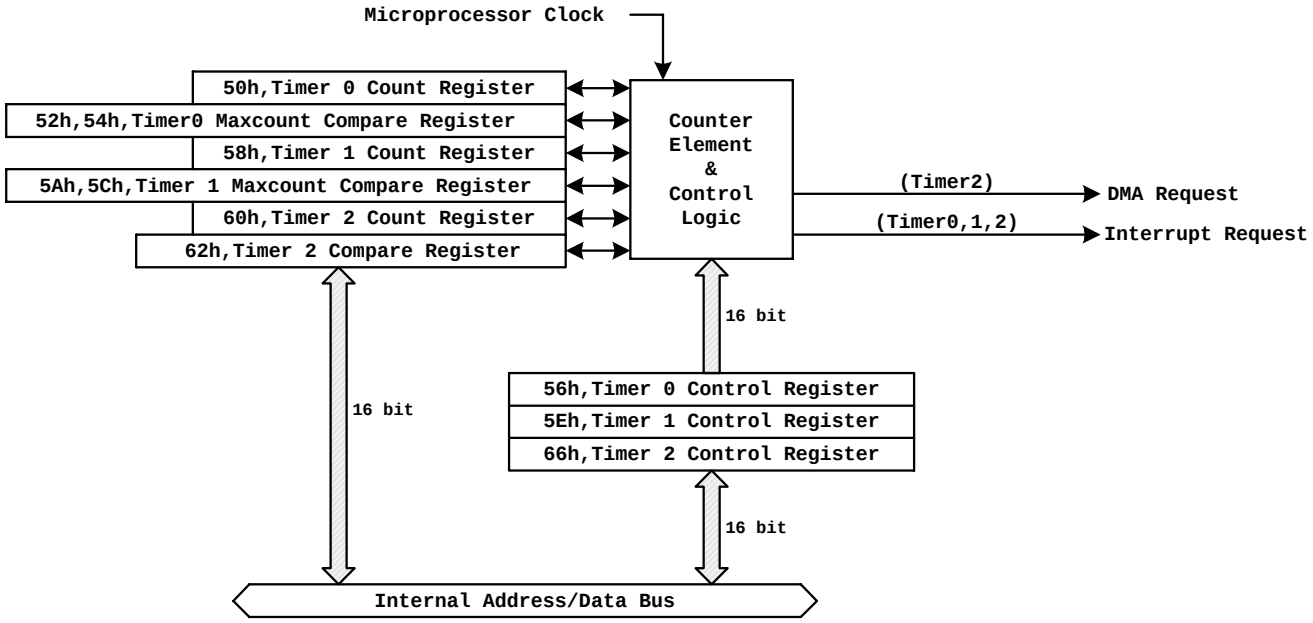
Destination-Synchronized Transfers

17.3 Serial Port/DMA Transfer

The serial port data can be DMA transfer to or from memory or I/O space. And the B_n/W bit of the DMA Control Register must be set to 0 for byte transfer. The map address of the Transmit Data Register is written to the DMA Destination Address Register and the memory or I/O address is written to the DMA Source Address Register, when the data are transmitted. The map address of the Receive Data Register is written to the DMA Source Address Register and the memory or I/O address is written to the DMA Destination Address Register, when the data are received.

The software is programmed through the Serial Port Control Register to perform the serial port/ DMA transfer. When a DMA channel is in use by a serial port, the corresponding external DMA request signal is deactivated. For DMA to the serial port, the DMA channel should be configured as being destination-synchronized. For DMA from the serial port, the DMA channel should be configured as being source-synchronized.

18. Timer Control UNIT



Timer / Counter Unit Block

There are three 16-bit programmable timers in the R2880. The timer operation is independent of the CPU. These three timers can be programmed as a timer element. Timer 2 can be used as a pre-scaler to Timer 0 and Timer 1 or as a DMA request source.

Register Offset: 56h
Register Name: Timer 0 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	RIU	0	0	0	0	0	0	MC	Rsvd	P	Rsvd	ALT	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable Bit. Set 1: The timer 0 is enabled. Set 0: The timer 0 is inhibited from counting. The INH_n bit must be set to 1 during writing the EN bit, and the INH_n bit and EN bit must be in the same write.
14	INH_n	R/W	Inhibit Bit. This bit allows selective updating the EN bit. The INH_n bit must be set to 1 during writing the EN bit, and both the INH_n bit and EN bit must be in the same write. This bit is not stored and is always read as 0.

13	INT	R/W	Interrupt Bit. Set 1: An interrupt request is generated when the count register equals a maximum count. If the timer is configured in dual max-count mode, an interrupt is generated each time the count reaches Max-Count A or Max-Count B. Set 0: Timer 0 will not issue interrupt requests.
12	RIU	R/W	Register in Use Bit. Set 1: The Maxcount Compare B Register of timer 0 is being used. Set 0: The Maxcount Compare A Register of timer 0 is being used.
11-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. In dual maxcount mode, this bit is set as each time either Maxcount Compare A or Maxcount Compare B register is reached. This bit is set regardless of the INT bit (offset 56h [15]).
4	Rsvd	RO	Reserved.
3	P	R/W	Pre-scaler Bit. This bit defines the timer 0 clock source. Set 0: Timer 0 Count Register is incremented by one every 8 internal processor clocks. Set 1: Timer 0 Count Register is incremented by one which is pre-scaled by Timer 2.
2	Rsvd	RO	Reserved.
1	ALT	R/W	Alternate Compare Bit. This bit controls whether the timer runs in single or dual maximum count mode. Set 1: Specify dual maximum count mode. In this mode, the timer counts to Maxcount Compare A, then resets the count register to 0. The timer counts to Maxcount Compare B, then resets the count register to 0 again, and starts over with Maxcount Compare A. Set 0: Specify single maximum count mode. In this mode, the timer counts to the value contained in Maxcount Compare A and reset to 0, and then the timer counts to Maxcount Compare A again. Maxcount Compare B is not used in this mode.
0	CONT	R/W	Continuous Mode Bit. Set 1: The timer runs continuously. Set 0: The timer will halt after each counting to the maximum count and EN bit will be cleared.

Register Offset: 50h

Register Name: Timer 0 Count Register

Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Count Value. This register contains the current count of Timer 0. The count is incremented by one every **8** internal processor clocks, or pre-scaled by Timer 2.

Register Offset: 52h
Register Name: Timer 0 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare A Value.

Register Offset: 54h
Register Name: Timer 0 Maxcount Compare B Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare B Value.

Register Offset: 5Eh
Register Name: Timer 1 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	RIU	0	0	0	0	0	0	MC	Rsvd	P	Rsvd	ALT	CONT

These definitions for timer 1 are the same as those of register 56h for timer 0.

Register Offset: 58h
Register Name: Timer 1 Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Count Value. This register contains the current count of timer 1. The count is incremented by one every 8 internal processor clocks, pre-scaled by Timer 2.

Register Offset: 5Ah
Register Name: Timer 1 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare A Value.

Register Offset: 5Ch
Register Name: Timer 1 Maxcount Compare B Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare B Value.

Register Offset: 66h
Register Name: Timer 2 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	0	0	0	0	0	0	0	MC	0	0	0	0	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable Bit. Set 1: Timer 2 is enabled. Set 0: Timer 2 is inhibited from counting. The INH_n bit must be set to 1 during writing the EN bit, and the INH_n and EN bit must be in the same write.
14	INH_n	R/W	Inhibit Bit. This bit allows selective updating the EN bit. The INH_n bit must be set to 1 during writing the EN bit, and both the INH_n and EN bit must be in the same write. This bit is not stored and is always read as 0.
13	INT	R/W	Interrupt Bit. Set 1: An interrupt request is generated when the count register equals a maximum count. Set 0: Timer 2 will not issue interrupt request.
12-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. This bit is set regardless of the INT bit (66h.13).
4-1	Rsvd	RO	Reserved
0	CONT	R/W	Continuous Mode Bit. Set 1: The timer is continuously running when it reaches the maximum count. Set 0: The EN bit (66h [15]) is cleared and the timer is held after each timer count reaches the maximum count.

Register Offset: 60h
Register Name: Timer 2 Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Count Value. This register contains the current count of Timer 2. The count is incremented by one every 8 internal processor clocks.

Register Offset: 62h
Register Name: Timer 2 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Compare A Value.

18.1 Watchdog Timer

The R2880 has one independent watchdog timer, which is programmable. **The watchdog timer is active after reset** and the timeout count with a maximum count value. The keyed sequence (3333h, CCCCh) must be written to the register (E6h) first, then the new configuration to the Watchdog Timer Control Register. It is a single write, so every writing to the Watchdog Timer Control Register will follow this rule.

When the watchdog timer activates, an internal counter is counting. If this internal count is over the watchdog timer duration, the watchdog timeout happens. The keyed sequence (AAAAh, 5555h) must be written to the register (E6h) to reset the internal count and prevent the watchdog timeout. The internal count should be reset before the Watchdog Timer timeout period is modified to ensure that an immediate timeout will not occur.

Register Offset: E6h
Register Name: Watchdog Timer Control Register
Reset Value : C080h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA	WRST	RSTFLAG	NMIFLAG	Rsvd				COUNT							

Bit	Name	Attribute	Description
15	ENA	R/W	Enable Watchdog Timer. Set 1: Enable Watchdog Timer. Set 0: Disable Watchdog Timer.
14	WRST	R/W	Watchdog Reset. Set 1: WDT generates a system reset when WDT timeout count is reached. Set 0: WDT generates an NMI interrupt when WDT timeout count is reached if the NMIFLAG bit is 0. If the NMIFLAG bit is 1, the WDT will generate a system reset when timeout.
13	RSTFLAG	R/W	Reset Flag. When watchdog timer reset event has occurred, hardware will set this bit to 1. This bit will be cleared by any keyed sequence write to this register or external reset. This bit is 0 after an external reset or 1 after a watchdog timer reset.

<table>
<tr><td>12</td><td>NMIFLAG</td><td>R/W</td><td>NMI Flag.
After WDT generates an NMI interrupt, this bit will be set to 1 by H/W. This bit will be cleared by any keyed sequence written to this register.</td></tr>
<tr><td>11-8</td><td>Rsvd</td><td>RO</td><td>Reserved</td></tr>
<tr><td>7-0</td><td>COUNT</td><td>R/W</td><td>Timeout Count. The COUNT setting determines the duration of the watchdog timer timeout interval.
a. The duration equation: Duration =(2^{Exponent}) / (Frequency/2)
b. The Exponent of the COUNT setting:
(Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, Bit 0) = (Exponent)
(0 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (N/A)
(x , x , x , x, x , x , x , 1) = (10)
(x , x , x , x, x , x , 1 , 0) = (20)
(x , x , x , x, x , 1 , 0 , 0) = (21)
(x , x , x , x, 1 , 0 , 0 , 0) = (22)
(x , x , x , 1, 0 , 0 , 0 , 0) = (23)
(x , x , 1 , 0, 0 , 0 , 0 , 0) = (24)
(x , 1 , 0 , 0, 0 , 0 , 0 , 0) = (25)
(1 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (26)
c. Watchdog timer Duration reference table:
For example: System clock =100Mhz and frequency exponent=10, then
Duration = 2^{10} / (100Mhz / 2) = 2048 / 100Mhz = 20.48 us
<table>
<tr><th>Frequency\ Exponent</th><th>10</th><th>20</th><th>21</th><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th></tr>
<tr><td>75 MHz</td><td>27.3 us</td><td>28 ms</td><td>55.9 ms</td><td>111.8 ms</td><td>223.7 ms</td><td>447.4 ms</td><td>894.8 ms</td><td>1.79 s</td></tr>
<tr><td>100 MHz</td><td>20.5 us</td><td>21 ms</td><td>41.9 ms</td><td>83.9 ms</td><td>167.8 ms</td><td>335.5 ms</td><td>671 ms</td><td>1.34 s</td></tr>
</table>
</td></tr>
</table>

19. PCI Configuration Registers

Register Offset: 01**h** – 00**h**
Register Name: Vendor ID Register
Reset Value: 17F3**h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VID															

Bit	Name	Attribute	Description
15-0	VID	RO	This register contains a 16-bit value which is assigned to RDC Semiconductor Co., Ltd.

Register Offset: 03**h** – 02**h**
Register Name: Device ID Register
Reset Value: 2880**h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DID															

Bit	Name	Attribute	Description
15-0	DID	RO	This register contains a 16-bit value assigned to R2880 device.

Register Offset: 05**h** – 04**h**
Register Name: Command Register
Reset Value: 0006**h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							SEEN	Reserved			MWIC	SCOC	MDC	MAC	IOAC

Bit	Name	Attribute	Description
15-9	Rsvd	RO	Reserved
8	SEEN	RW	SERR_n Enable 0: Disable 1: Enable
7-5	Rsvd	RO	Reserved
4	MWIC	RO	Memory Write and Invalid Command.
3	SCOC	RO	Special Cycle operations control.

2	MDC	RO	PCI Bus Master Device Control. This bit always returns ‘1’
1	MAC	RO	Memory Space Accesses Control. It controls a device’s response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. Always set to “1” at R2880
0	IOAC	RO	I/O Space Accesses Control.

Register Offset: 07**h –** 06**h**
Register Name: Status Register
Reset Value: 0200**h**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPE	SS	RMAS	RTAS	STAS	DT		Reserved								

Bit	Name	Attribute	Description
15	DPE	R/W	Detected Parity Error. This bit must be set whenever the device detects a parity error. This is a read only bit and is cleared by writing '1' to it.
14	SS	R/W	SERR_n status. This bit must be set whenever the device asserts SERR_n. This is a read only bit and is cleared by writing '1' to it.
13	RMAS	R/W	Receive Master Abort Status when R2880 acts as a master. This bit is set to '1' when the R2880 generates a transaction (Except for Special Cycle), and is terminated with master-abort. This is a read only bit and is cleared by writing '1' to it.
12	RTAS	R/W	Receive Target Abort Status when R2880 acts as a master. This bit is set to '1' when the R2880 encounters a target abort condition. This is a read only bit and is cleared by writing a '1' to it.
11	STAS	RO	Signal Target Abort Status when R2880 acts as a slave. The R2880 as a slave never generates a Target abort. This bit is always 0.
10-9	DT	RO	DEVSEL_n Timing.
8-0	Rsvd	RO	Reserved. These bits always return ’0’s.

Register Offset: 08**h**
Register Name: Revision ID Register
Reset Value: 00**h**

7	6	5	4	3	2	1	0
RID							

Bit	Name	Attribute	Description
7-0	RID	RO	Version number of the R2880.

Register Offset: 0B**h –** 09**h**
Register Name: Class Code Register
Reset Value: 0600_00**h**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC																							

Bit	Name	Attribute	Description
23-0	CC	RO	Class Code of the R2880.

Register Offset: 0C**h**
Register Name: BIST, Header Type, Latency Timer, Cache Line Size Register
Reset Value: 0000_0000**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST								HTR								LTR								CLSR							

Bit	Name	Attribute	Description
31-24	BISTR	RO	This register identifies the control and status of BIST. Since the R2880 does not implement the BIST function, this byte should be read as 00h.
23-16	HTR	RO	This register identifies the type of predefined header in the configuration space. Since the R2880 is a single function device (bit7='0') and not a PCI-to-PCI bridge, this byte should be read as 00h.
15-8	LTR	RO	This register identifies the value of the Latency Timer for Bus Master in units of PCI Clocks. Since the R2880 does not check this item, this byte should be read as 00h.
7-0	CLSR	RO	This register identifies the system cache line size in units of DWORDs. Since the R2880 does not implement Memory Write and Invalidate command, this byte should be read as 00h.

Register Offset: 3F**h** - 10**h**
Register Name: PCI Standard Register (Not Used in R2880, Reserved)
Reset Value: all zero for default setting

Register Offset: 43**h** – 40**h**
Register Name: PCI Devices Memory Space Base Address
Reset Value: 0000_0000**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								MBA																Reserved							ME

Bit	Name	Attribute	Description
31-24	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
23-8	MBA	R/W	PCI Devices Memory Base Address [23:8].
7-1	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
0	ME	R/W	PCI Devices Memory Space Enable.

Register Offset: 47**h** – 44**h**
Register Name: PCI Devices Memory Space Base Address Mask
Reset Value: 00FF_FF00**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								MBAM																Reserved							

Bit	Name	Attribute	Description
31-24	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
23-8	MBAM	R/W	PCI Devices Memory Base Address Mask Bit [23:8].
7-0	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.

Register Offset: 4B**h** - 48**h**
Register Name: PCI Devices I/O Space Base Address
Reset Value: 0000_0000**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																IBA								Reserved							IE

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
15-8	IBA	R/W	PCI Devices I/O Base Address [15:8].

7-1	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
0	IE	R/W	PCI Devices I/O Space Enable.

Register Offset: 4F**h** – 4C**h**
Register Name: PCI Devices I/O Space Base Address Mask
Reset Value: 0000_FF00**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																IBAM								Reserved							

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
15-8	IBAM	R/W	PCI Devices I/O Base Address Mask bits [15:8].
7-0	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.

Register Offset: 53**h – 50h**
Register Name: CardBus Device-0 Memory Space Base Address
Reset Value: 0000_0000**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								MBA																Reserved							ME

Bit	Name	Attribute	Description
31-24	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
23-8	CMBA	R/W	CardBus Device-0 Memory Base Address[23:8].
7-1	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
0	CME	R/W	CardBus Device-0 Memory Space Enable.

Register Offset: 57**h** – 54**h**
Register Name: CardBus Device-0 Memory Space Base Address Mask
Reset Value: 00FF_FF00**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								MBAM																Reserved							

Bit	Name	Attribute	Description
31-24	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
23-8	MBAM	R/W	CardBus Device-0 Memory Base Address Mask Bit[23:8].
7-0	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.

Register Offset: 5B**h** - 58**h**
Register Name: CardBus Device-0 I/O Space Base Address
Reset Value: 0000_0000**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																IBA								Reserved							IE

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
15-8	CIBA	R/W	CardBus Device-0 I/O Base Address [15:8].
7-1	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
0	IE	R/W	CardBus Device-0 I/O Space Enable.

Register Offset: 5F**h** – 5C**h**
Register Name: CardBus Device-0 I/O Space Base Address Mask
Reset Value: 0000_FF00**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																IBAM								Reserved							

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
15-8	IBAM	R/W	CardBus Device-0 I/O Base Address Mask bits [15:8].
7-0	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.

Register Offset: 63**h** – 60**h**
Register Name: CardBus Device-1 Memory Space Base Address
Reset Value: 0000_0000**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								MBA																Reserved							ME

Bit	Name	Attribute	Description
31-24	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
23-8	CMBA	R/W	CardBus Device-1 Memory Base Address [23:8].
7-1	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
0	CME	R/W	CardBus Device-1 Memory Space Enable.

Register Offset: 67**h** – 64**h**
Register Name: CardBus Device-1 Memory Space Base Address Mask
Reset Value: 00FF_FF00**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								MBAM																Reserved							

Bit	Name	Attribute	Description
31-24	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
23-8	MBAM	R/W	CardBus Device-1 Memory Base Address Mask Bit[23:8].
7-0	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.

Register Offset: 6B**h** - 68**h**
Register Name: CardBus Device-1 I/O Space Base Address
Reset Value: 0000_0000**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																IBA								Reserved							IE

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
15-8	CIBA	R/W	CardBus Device-1 I/O Base Address [15:8].

7-1	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
0	IE	R/W	CardBus Device-1 I/O Space Enable.

Register Offset: 6F**h** – 6C**h**
Register Name: CardBus Device-1 I/O Space Base Address Mask
Reset Value: 0000_FF00**h**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																IBAM								Reserved							

Bit	Name	Attribute	Description
31-16	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.
15-8	IBAM	R/W	CardBus Device-1 I/O Base Address Mask bits [15:8].
7-0	Rsvd	RO	Reserved. All are ‘0’s. To write any value to these bits causes no effect.

Register Offset: 7F**h** – 70**h** (Reserved)

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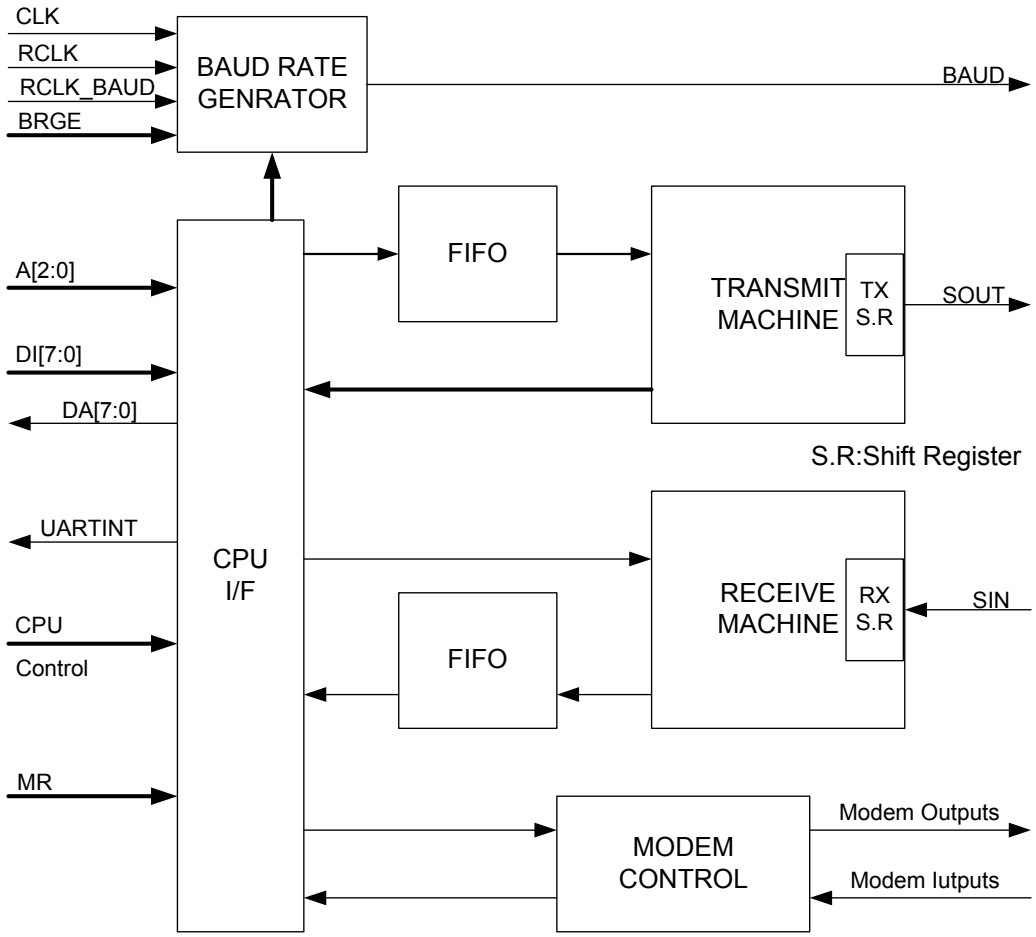
20. 16550 UART Serial Port

The system programmer may access any of the UART registers summarized in the following Table via the CPU. These registers control the UART operation in which the transmission and reception of data and status are included, and each register bit in the Table has its own name.

Register Address	Register Name	Mnem.	Bit No.									Note.
			15-8	7	6	5	4	3	2	1	0	
80h/10h	Receiver Buffer Register	**RBR**	0	RBR[7]	RBR[6]	RBR[5]	RBR[4]	RBR[3]	RBR[2]	RBR[1]	RBR[0]	DLAB=0 & read only
	Transmitter Holding Register	**THR**	0	THR[7]	THR[6]	THR[5]	THR[4]	THR[3]	THR[2]	THR[1]	THR[0]	DLAB=0 & write only
	Divisor Latch(LS)	**DLL**	0	DL[7]	DL[6]	DL[4]	DL[4]	DL[3]	DL[2]	DL[1]	DL[0]	DLAB=1
82h/12h	Interrupt Enable Register	**IER**	0	0	0	0	0	EMSI	ERLSI	ETHREI	ERDAI	DLAB=0
	Divisor Latch(MS)	**DLM**	0	DL[15]	DL[14]	DL[13]	DL[12]	DL[11]	DL[10]	DL[9]	DL[8]	DLAB=1
84h/14h	Interrupt Identified Register	**IIR**	0	FIFO Enabled (Note)	FIFO Enabled (Note)	0	0	IID[2]	IID[1]	IID[0]	IP	Read Only
	FIFO Control Register	**FCR**	DMAC TL2-0	RCVR Trigger Level (MSB)	RCVR Trigger Level (LSB)	Reserved	Reserved	DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enabled	Write Only
86h/16h	Line Control Register	**LCR**	0	DLAB	SB	SP	EPS	PEN	STB	WLS[1]	WLS[0]	
88h/18h	MODEM Control Register	**MCR**	0	0	0	ACE	Loop	LDCD	LRI	RTS	DTR	
8Ah/1Ah	Line Status Register	**LSR**	0	Error in RCVR FIFO (Note)	TEMT	THRE	BI	FE	PE	OE	DR	
8Ch/1Ch	MODEM Status Register	**MSR**	0	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS	
8Eh/1Eh	Scratch Register	**SCR**	0	SCR[7]	SCR[6]	SCR[5]	SCR[4]	SCR[3]	SCR[2]	SCR[1]	SCR[0]	

Note: These bits are always 0 in the 16450 mode.



UART Block Diagram

20.1 Receiver Buffer Register and Transmitter Holding Register

Register Offset: 80h
Register Name: UART0 Receiver Buffer Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								RBR [7:0]							

This register is Receiver Buffer Register when DLAB=0 and the read function is operated.

Register Offset: 80h
Register Name: UART0 Transmitter Holding Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								THR [7:0]							

This register is Transmitter Holding Register when DLAB=0 and the write function is operated.

20.2 Divisor Latch LS and MS Register

The divisor value, DLL[15:0], is the host clock / 16 / Baud Rate.

For example:

Host Clock=75Mhz, and Baud Rate=57600, then

Divisor=75Mhz/16/57600=81.3 ➔ 81

Register Offset: 80h
Register Name: UART0 Divisor Latch (LS) Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLL [7:0]							

This register is Divisor Latch (LS) Register when DLAB=1.

Register Offset: 82h
Register Name: UART0 Divisor Latch (MS) Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLL [15:8]							

This register is Divisor Latch (MS) Register when DLAB=1.

20.3 Interrupt Enable Register

This Interrupt Enable Register (IER) enables the four types of UART interrupts. Each interrupt can individually activate the interrupt output signal (UARTINT). It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, setting the relative bit of the IER register to 1 will enable the selected interrupt(s). Disabling an interrupt prevents it from being indicated as being active in the IIR and from activating the UARTINT output signal. All other system functions operate in their normal manners, including the setting of the Line Status and MODEM Status Registers. The details of each bit of the IER are described as below:

Register Offset: 82h
Register Name: UART0 Interrupt Enable Register
Reset Value : XX00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	0	0	BMSI	ERLSI	ETHREI	ERDAI

Bit	Name	Attribute	Description
7-4	Rsvd	RO	Reserved and always 0.
3	EMSI	R/W	The MODEM Status Interrupt bit. Set to 1 to enable the MODEM Status Interrupt.
2	ERLSI	R/W	The Enable Receiver Line Status Interrupt bit. Set to 1 to enable the Receiver Line Status Interrupt.
1	ETHREI	R/W	The Enable Transmitter Holding Register Empty Interrupt bit. Set to 1 to enable the Transmitter Holding Register Empty Interrupt.
0	ERDAI	R/W	The Enable Received Data Interrupt bit. Set to 1 to enable the Received Data Available Interrupt (and timeout interrupts in the FIFO mode).

20.4 Interrupt Identification Register

This is a read only register. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register (IIR). The four levels of interrupt conditions in priority order are Receiver Line Status, Received Data Ready, Transmitter Holding Register Empty, and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. The details of each bit of Interrupt Identification Register are described as below.

Register Offset: 84h
Register Name: UART0 Interrupt Identification Register (Read Only)
Reset Value : XX01h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								FIFOs Enabled	FIFOs Enabled	0	0	IID2	IID1	IID0	IP

Bit	Name	Attribute	Description
7-6	FIFOs Enabled	R/W	These two bits are set when FCR [0]=1.
5-4	Rsvd	RO	Reserved and always 0.
3	IID2	R/W	The Interrupt ID indicator. In the NS16450 Mode, this bit is 0. In the FIFO mode, this bit is set along with bit 2 when a timeout interrupt is pending.
2-1	IID[1:0]	R/W	The Interrupt ID indicator. These two bits are used to identify the highest priority interrupt pending as indicated in the following table:
0	IP	R/W	The Interrupt Pending indicator. This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending or not. Set 1: Indicate that no interrupt is pending. Set 0: Indicate that an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.

Interrupt Control Function:

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Rest Control
0	0	0	1	—	None	none	—
0	1	1	0	Highest	Receiver Line Status	overrun error, parity error, framing error, or break interrupt	reading the line status register
0	1	0	0	Second	Received Data Available	received data available or trigger level reached	reading the receiver buffer register or the FIFO dropping below the trigger level
1	1	0	0	Second	Character Timeout Indication	no character has been removed from or input to the RCVR FIFO during the last 4 characters times and there is at least 1 character in it during this time	reading the receiver buffer register
0	0	1	0	Third	Transmitter Holding Register Empty	transmitter holding register empty	reading the IIR register (if the source of interrupt is available) or writing into the transmitter holding register
0	0	0	0	Fourth	MODEM Status	clear to send, data set ready, ring indicator, or data carrier detect	reading the modem status register

20.5 FIFO Control Register

The FIFO Control Register (write only) is at the same location as the Interrupt Identification Register (read only). This register is used to enable the FIFO, clear the FIFO, set the RCVR FIFO trigger level, and select the type of DMA signaling.

Register Offset: 84h
Register Name: UART0 FIFO Control Register (Write Only)
Reset Value : X000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					DMACTL[2:0]			RCVR Trigger (MSB)	RCVR Trigger (LSB)	Rsvd		DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enabled

Bit	Name	Attribute	Description
10-8	DMACTL [2:0]	R/W	With the DMA transfers listed as follows, users can configure these bits for the UART Port. ***DMACTL [2:0]*** — ***Receive*** — ***Transmit*** 000 — No DMA — No DMA 001 — DMA0 — DMA1 010 — DMA1 — DMA0 011 — Reserved — Reserved 100 — DMA0 — No DMA 101 — DMA1 — No DMA 110 — No DMA — DMA0 111 — No DMA — DMA1
7-6	RCVRTL [1:0]	R/W	RCVR Trigger. These two bits are used to set the trigger level for the RCVR FIFO interrupt. **RCVRTL[1:0] – RCVR FIFO Trigger Level (Bytes)** 0 0 -- 01 Bytes 0 1 -- 04 Bytes 1 0 -- 08 Bytes 1 1 -- 14 Bytes
5-4	Rsvd	RO	Reserved
3	DMA Mode Select	R/W	DMA Mode Select. Setting FCR0[3]=1 will cause the UART to change from mode 0 to mode 1 if FCR0[0]=0.
2	XMIT FIFO Reset	R/W	XMIT FIFO Reset. Writing a 1 to FCR0[2] clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.
1	RCVR FIFO Reset	R/W	RCVR FIFO Reset. Writing a 1 to FCR0[1] clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.
0	FIFO Enabled	R/W	FIFO Enable. Writing a 1 to FCR0 enables both the XMIT and RCVR FIFO. Resetting FCR0[0] will clear all bytes in both FIFO. When changing from FIFO Mode to NS16450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when written to other FCR bits or they will not be programmed.

20.6 Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The detailed contents of each bit of LCR register is as follows:

Register Offset: 86h
Register Name: UART0 Line Control Register
Reset Value : XX00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DLAB	Set Break	Stick Parity	EPS	PEN	STB	WSL1	WSL0

Bit	Name	Attribute	Description
7	DLAB	RW	Divisor Latch Access bit. Set 1: To access the Divisor Latches of the Baud Generator during a Read or Write operation. Set 0: To access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register
6	SB	R/W	Break Control bit. It causes a break condition to be transmitted to the receiving UART. Set 1: the serial output (SOUT) is forced to the Spacing (logic 0) state. Set 0: the Break is disabled. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. ***Note:*** *This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.* *1.Load an all Os, pad character, in response to THRE.* *2.Set break after the next THRE.* *3.Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.* *During the break, the Transmitter can be used as a character timer to accurately establish the break duration.*
5	SP	R/W	Stick Parity bit. Set Bit 5=1, Bit 4=1, & Bit 3=1, the Parity bit is transmitted and checked as logic 0. Set Bit 5=1, Bit 4=0, & Bit 3=1, the Parity bit is transmitted and checked as logic 1. Set Bit 5=0, Stick Parity is disabled.
4	EPS	R/W	Even Parity Select bit. Set Bit 4=0 & Bit 3=1, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. Set Bit 4=1 & Bit 3=1, an even number of logic 1s is transmitted or checked.
3	PEN	R/W	Parity Enable bit. Set 1: A Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

2	STB	R/W	Stop bit. This bit specifies the number of Stop bits transmitted and received in each serial character. Set 0: One Stop bit is generated in the transmitted data. Set 1: One and a half stop bits are generated for a 5-bit word length characters. Two stop bits are generated for 6-, 7-, or 8-bit word length characters. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.
1-0	WLS[1:0]	R/W	These two specify the number of bits in each transmitted or received serial character. **WLS[1:0] -- Character Length** 0 0 -- 5-bit character 0 1 -- 6-bit character 1 0 -- 7-bit character 1 1 -- 8-bit character

20.7 Modem Control Register

This Modem Control Register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The details are described as below:

Register Offset: 88h
Register Name: UART0 MODEM Control Register
Reset Value : XX00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	ACE	Loop	LDCD	LRI	RTS	DTR

Bit	Name	Attribute	Description
7-6	Rsvd	RO	Reserved and always 0.
5	ACE	R/W	Autoflow Control is Enabled when set. ACE can be configured by MCR bits 1and 5 as shown in the following table. MCR bit5(AFE) / MCR bit1(RTS): 1 / 1 — Auto-RTS and auto-CTS enabled 1 / 0 — Auto-CTS enabled 0 / X — AFE disabled
4	Loop	R/W	This bit provides a local loop back feature for diagnostic testing of the UART. Set to 1, the following occur: The transmitter Serial Output (SOUT) is set to the Marking (logic 1) state. The receiver Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is “looped back” into the Receiver Shift Register input. The four MODEM Control inputs (CTS_n, DSR_n, RI_n, and DCD_n) are disconnected, and the 2 MODEM Control outputs (DTR_n and RTS_n) are internally connected to the two MODEM Control inputs (DSR_n, CTS_n), and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted are immediately received. This feature allows the processor to verify the transmitted and received data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the sources of the interrupts are now the lower four bits of the MODEM Control Register instead of the four

			MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
3, 2	LDCD, LRI	R/W	Bit3: The bit controls DCD_n signal internal if loop back mode is enabled. Bit2: The bit controls RI_n signal internal if loop back mode is enabled.
1	RTS	R/W	The Request To Send bit. This bit controls the Request To Send (RTS_n) output. Set 1: the RTS_n output is forced to logic 0. Set 0: the RTS_n output is forced to logic 1.
0	DTR	R/W	The Data Terminal Ready indicator. This bit controls the Data Terminal Ready (DTR_n) output. Set 1: the DTR_n output is forced to logic 0. Set 0: the DTR_n output is forced to logic 1. ***Note:*** *The DTR_n output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.*

20.8 Line Status Register

This register provides status information to the part of the CPU processing data transfer. The contents of each Bit of the Line Status Register are described as below.

Register Offset: 8Ah
Register Name: UART0 Line Status Register
Reset Value : XX60h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								Error in RCVR (Note 2)	TEMT	THRE	BI	FE	PE	OE	DR

Bit	Name	Attribute	Description
7	Error in RCVR (Note 2)	R/W	Error in Receive FIFO. In the NS16450 Mode, this is a 0. In the FIFO mode, LSR [7] is set to 1 when there is at least one parity error, framing error or break indication in the FIFO. LSR [7] is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO. ***Note:*** *The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.*
6	TEMT	R/W	The Transmitter Empty indicator. Set 1: This bit is set to 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. Set 0: This bit is reset to 0 whenever either the Transmitter Holding Register or the Transmitter Shift Register contains a data character. In the FIFO mode, this bit is set to one whenever the transmitter FIFO and shift register are both empty.
5	THRE	R/W	The Transmitter Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt Enable is set high. Set 1: This bit will be set to 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. Set 0: This bit is reset to 0 upon the CPU loading character to the Transmitter Holding Register. In the FIFO mode, this bit is set when the XMIT FIFO is empty; it is cleared when at

			least 1 byte is written to the XMIT FIFO.
4	BI	R/W	Break Interrupt indicator. Set 1: This bit will be set to 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + Data Bits + Parity Bit + Stop Bit). Set 0: This bit will be reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit. ***Note:*** *Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.*
3	FE	R/W	Framing Error indicator. This bit indicates that the received characters don't have a valid Stop Bit. Set 1: This bit will be set to 1 whenever the Stop Bit follows the last data bit or Parity bit is detected as a logic 0 bit (Spacing level). Set 0: Automatic set to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error occurs. To do this, it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data".
2	PE	R/W	Parity Error indicator. This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity select bit. Set 1: This bit will be set upon detection of a parity error. Set 0: Automatic set to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.
1	OE	R/W	Overrun Error indicator. This bit indicates that the data in the Receiver Buffer Register were not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. Set 1: Indicate OE indicator is set to logic 1 upon detection of an overrun condition. Set 0: Automatic reset to 0 whenever the CPU reads the contents of the Line Status Register. If the data in the FIFO mode continue to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.
0	DR	R/W	Data Ready indicator. Set 1: Indicate whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Set 0: Automatic set to 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

20.9 Modem Status Register

This Modem Status Register (MSR) provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to logic 1 whenever a control input from the MODEM changes its state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register. The contents of the MSR register are described as below.

Register Offset: 8C
Register Name: UART0 MODEM Status Register
Reset Value : XXX0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

Bit	Name	Attribute	Description
7	DCD	R/W	Data Carrier Detect. This bit is the complement of the Data Carrier Detect (DCD_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to OUT2 in the MCR.
6	RI	R/W	Ring Indicator. This bit is the complement of the Ring Indicator (RI_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to OUT1 in the MCR.
5	DSR	R/W	Data Set Ready. This bit is the complement of the Data Set Ready (DSR_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to DTR in the MCR.
4	CTS	R/W	Clear To Send. This bit is the complement of the Clear to Send (CTS_n) input. If bit 4 (Loop Bit) of the MCR is set to 1, this bit is equivalent to RTS in the MCR.
3	DDCD	R/W	Delta Data Carrier Detect. This bit indicates that the DCD_n input has changed the state. ***Note:*** *Whenever bit 0, 1, 2 or 3 is set to logic 1, a MODEM Status Interrupt is generated.*
2	TERI	R/W	Trailing Edge Ring Indicator. This bit indicates that the RI_n input has changed from a low to a high state.
1	DDSR	R/W	Delta Data Set Ready. This bit indicates that the DSR_n input has changed the state since the last time it was read by the CPU.
0	DCTS	R/W	Delta Clear To Send. This bit indicates that the CTS_n input has changed the state since the last time it was read by the CPU.

20.10 Scratchpad Register

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Register Offset: 8E
Register Name: UART0 Scratch Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								SCR[7:0]							

20.11 Programmable Baud Generator

The UART contains a programmable Baud Generator that is divided by any divisor from 2 to 2^{16}-1.. The output frequency of the Baud Generator is 16 times the Baud [divisor # = (CPU frequency)/(baud rate*16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Baud Rates	CPUCLK=75MHz				CPUCLK=100MHz			
	DLM	DLL	Baud	Dev.(%)	DLM	DLL	Baud	Dev.(%)
1200	0Fh	42h	1200	0	14h	58h	1200	0
2400	07h	A1h	2400	0	0Ah	2Ch	2400	0
4800	03h	D1h	4798	0.04	05h	16h	4800	0
9600	01h	E8h	9606	0.06	02h	8Bh	9601	0
19200	0h	F4h	19211	0.06	01h	46h	19171	0.15
38400	0h	7Ah	38422	0.06	0h	A3h	38344	0.15
57600	0h	51h	57870	0.5	0h	6Dh	57339	0.45
115200	0h	29h	114329	0.76	0h	36h	115741	0.47
230400	0h	14h	234375	1.73	0h	1Bh	231481	0.47
460860	0h	0Ah	468750	1.71	0h	0Eh	446428	3.13

20.12 FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR [0]=1, IER [0]=1), RCVR interrupt will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the

interrupt, it is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR=06), as before, has higher priority than the received data available (IIR=04) interrupt.

D. The data ready bit (LSR [0]) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:

—at least one character is in the FIFO.

—the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).

—the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 ms at 300 BAUD with a 12-bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

C. When a timeout interrupt has occurred: It is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred: The timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR [0]=1, IER [1]=1), XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE=1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

20.13 FIFO Polled Mode Operation

With FCR [0]=1, resetting IER [0], IER [1], IER [2], IER [3] or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR [0] will be set as long as there is one byte in the RCVR FIFO.

LSR [1] to LSR [4] will specify which error(s) has occurred.

Character error status is handled the same way as in the interrupt mode, the IIR is not affected since IER2=0.

LSR [5] will indicate when the XMIT FIFO is empty.

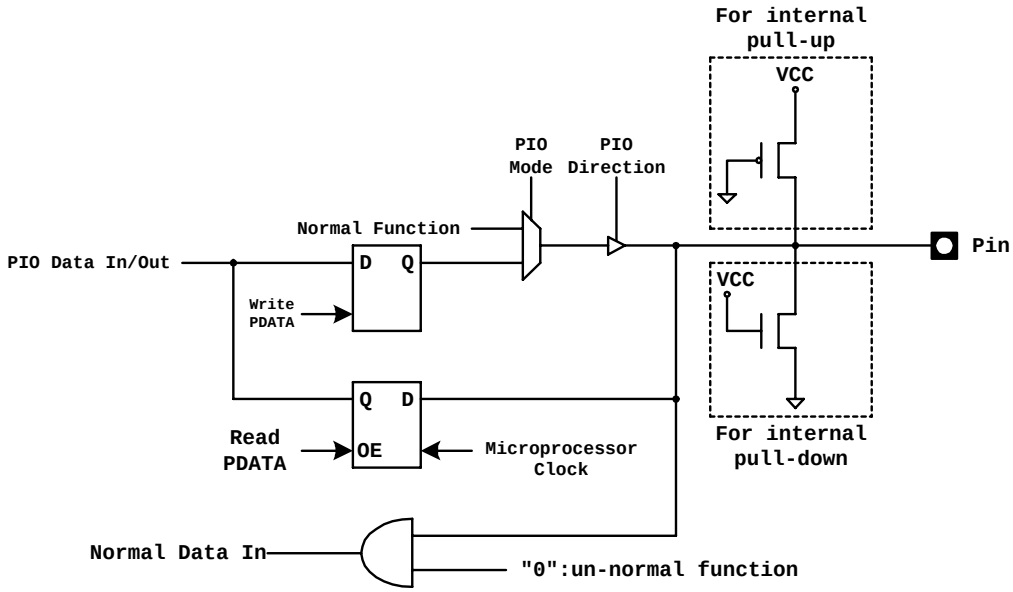
LSR [6] will indicate that both the XMIT FIFO and Shift Register are empty.

LSR [7] will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

21. PIO UNIT

The R2880 provides 48 programmable I/O signals, which are multi-functional pins with other signals of normal functions. Software is used to program the registers (7Ah, 78h, 76h, 74h, 72h, 70h, 6Eh, 6Ch and 6Ah) to configure these multi-functional pins for PIO or normal functions.



PIO pin Operation Diagram

21.1 PIO Multi-Function Pin List Table

PIO No.	Ball No.	Multi Function	Reset status/PIO internal resister
0	N3	SA0	PIO/ Input with 75K pull-up
1	M3	SA1	PIO/ Input with 75K pull-up
2	N2	SA2	PIO/ Input with 75K pull-up
3	P1	SA3	PIO/ Input with 75K pull-up
4	N1	SA4	PIO/ Input with 75K pull-up
5	M2	SA5	PIO/ Input with 75K pull-up
6	L3	SA6	PIO/ Input with 75K pull-up
7	L4	SA7	PIO/ Input with 75K pull-up
8	H1	SA8	PIO/ Input with 75K pull-up
9	H3	SA9	PIO/ Input with 75K pull-up
10	H4	SA10	PIO/ Input with 75K pull-up
11	G4	SA11	PIO/ Input with 75K pull-up
12	G3	SA12	PIO/ Input with 75K pull-up
13	G1	SA13	PIO/ Input with 75K pull-up
14	G2	SA14	PIO/ Input with 75K pull-up
15	F1	SA15	PIO/ Input with 75K pull-up
16	R6	IOR_n	PIO/ Input with 75K pull-up
17	P7	IOW_n	PIO/ Input with 75K pull-up
18	E2	PCS2_n/PREQ2_n	Normal operation

19	D1	PCS3_n/PGNT2_n	Normal operation
20	E5	PCS5_n/PREQ3_n	Normal operation
21	D2	PCS6_n/PGNT3_n	Normal operation
22	F2	MCS_n	Normal operation
23	L2	INT1	Normal operation
24	L1	INT2	Normal operation
25	K3	INT3	Normal operation
26	K2	SIN1/SAD14	Normal operation
27	K4	SOUT1/SAD15	Normal operation
28	M6	ARDY	PIO/ Input with 75K pull-up
29	M1	INT0/BHE_n	PIO/ Input with 75K pull-up
30	H2	RTS1_n/SAD8	PIO/ Input with 75K pull-up
31	J1	DTR1_n/SAD9	PIO/ Input with 75K pull-up
32	J4	CTS1_n/SAD10	PIO/ Input with 75K pull-up
33	J3	DSR1_n/SAD11	PIO/ Input with 75K pull-up
34	J2	DCD1_n/SAD12	PIO/ Input with 75K pull-up
35	K1	RI1_n/SAD13	PIO/ Input with 75K pull-up
36	L13	RTS0_n/TDO	Normal operation
37	L12	CTS0_n/TMS	Normal operation
38	K13	DSR0_n/TCK	Normal operation
39	L15	DCD0_n/TDI	Normal operation
40	H13	TXD0_0	Normal operation
41	H12	TXD0_1	Normal operation
42	G14	TXD0_2	Normal operation
43	H14	TXD0_3	Normal operation
44	J13	RXD0_0	Normal operation
45	J14	RXD0_1	Normal operation
46	J15	RXD0_2	Normal operation
47	J12	RXD0_3	Normal operation

PIO Mode	PIO Direction	Pin Function
0	0	Normal Operation
0	1	PIO input with pull-up/pull-down
1	0	PIO output
1	1	PIO input without pull-up/pull-down

Register Offset: 7Ah

Register Name: PIO Data 1 Register

Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA[31:16]															

Bit	Name	Attribute	Description
15-0	PDATA [31:16]	R/W	PIO Data Bits. These bits PDATA[31:16] are mapped to the PIO[31:16] that indicate the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 78h
Register Name: PIO Direction 1 Register
Reset Value : F003h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR[31:16]															

Bit	Name	Attribute	Description
15-0	PDIR [31:16]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input pin. Set 0: Configure the PIO pin as an output or as a pin of normal function.

Register Offset: 76h
Register Name: PIO Mode 1 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE[31:16]															

Bit	Name	Attribute	Description
15-0	PMODE [31:16]	R/W	PIO Mode Bits. The definitions of PIO pins are configured by the combination of PIO Mode and PIO Direction. The PIO pins are programmed individually. The definitions (PIO Mode, PIO Direction) for the functions of PIO pins: (0 , 0) – Normal operation , (0 , 1) – PIO input with pull-up/pull-down (1 , 0) – PIO output , (1 , 1) -- PIO input without pull-up/pull-down

---

Register Offset: 74h
Register Name: PIO Data 0 Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA[15:0]															

Bit	Name	Attribute	Description
15-0	PDATA [15:0]	R/W	PIO Data Bits. These bits PDATA[15:0] are mapped to the PIO[15:0] that indicate the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 72h
Register Name: PIO Direction 0 Register
Reset Value : FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR[15:0]															

Bit	Name	Attribute	Description
15-0	PDIR [15:0]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input pin. Set 0: Configure the PIO pin as an output or as a pin of normal function.

Register Offset: 70h
Register Name: PIO Mode 0 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE[15:0]															

Bit	Name	Attribute	Description
15-0	PMODE [15:0]	R/W	PIO Mode Bits.

Register Offset: 6Eh
Register Name: PIO Data 2 Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA[47:32]															

Bit	Name	Attribute	Description
15-0	PDATA [47:32]	R/W	PIO Data Bits. These bits PDATA[47:32] are mapped to the PIO[47:32] that indicate the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 6Ch
Register Name: PIO Direction 2 Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR[47:32]															

Bit	Name	Attribute	Description
15-0	PDIR [47:32]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input pin. Set 0: Configure the PIO pin as an output or as a pin of normal function.

Register Offset: 6Ah
Register Name: PIO Mode 2 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE[47:32]															

Bit	Name	Attribute	Description
15-0	PMODE [47:32]	R/W	PIO Mode Bit. The definitions of PIO pins are configured by the combination of PIO Mode and PIO Direction. The PIO pins are programmed individually. The definitions (PIO Mode, PIO Direction) for the functions of PIO pins: (0 , 0) – Normal operation , (0 , 1) – PIO input with pull-up/pull-down (1 , 0) – PIO output , (1 , 1) -- PIO input without pull-up/pull-down

22. CACHE Control Unit

22.1 Cache Control Register

Register Offset: FEC0h
Register Name: Cache Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICE	DCE	Rsvd	NCFE	NCR3	NCR2	NCR1	NCR0	WIR	Reserved						

Bit	Name	Attribute	Description
15	ICE	R/W	Instruction Cache Is enabled when set
14	DCE	R/W	Data Cache is enabled when set
13	Rsvd	RO	Reserved
12	NCFE	R/W	Non-Cache Read FIFO is enabled.
11	NCR3	R/W	Non-Cache region3 is enabled when set
10	NCR2	R/W	Non-Cache region2 is enabled when set
9	NCR1	R/W	Non-Cache region1 is enabled when set
8	NCR0	R/W	Non-Cache region0 is enabled when set
7	WIR	R/W	Write Invalid region is enabled when set
6-0	Rsvd	RO	Reserved

22.2 Non-Cache Region Register

Register Offset: FEC2h
Register Name: Non-Cache Region0 Start Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

Register Offset: FEC4h
Register Name: Non-Cache Region0 Start Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

Register Offset: FEC6h
Register Name: Non-Cache Region0 End Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRE[15:3]													reserved		

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

Register Offset: FEC8h
Register Name: Non-Cache Region0 End Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

Register Offset: FECAh
Register Name: Non-Cache Region1 Start Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

Register Offset: FECCh
Register Name: Non-Cache Region1 Start Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

Register Offset: FECEh
Register Name: Non-Cache Region1 End Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRE[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

Register Offset: FED0h
Register Name: Non-Cache Region1 End Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

Register Offset: FED2h
Register Name: Non-Cache Region2 Start Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

Register Offset: FED4h
Register Name: Non-Cache Region2 Start Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

Register Offset: FED6h
Register Name: Non-Cache Region2 End Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRE[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

Register Offset: FED8h
Register Name: Non-Cache Region2 End Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

Register Offset: FEDAh
Register Name: Non-Cache Region3 Start Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRS	R/W	Non-Cache Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region start address [2:0]

Register Offset: FEDCh
Register Name: Non-Cache Region3 Start Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRS	R/W	Non-Cache Region start address [23:16]

Register Offset: FEDEh
Register Name: Non-Cache Region3 End Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCRE[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	NCRE	R/W	Non-Cache Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Non-Cache Region end address [2:0]

Register Offset: FEE0h
Register Name: Non-Cache Region3 End Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								NCRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	NCRE	R/W	Non-Cache Region end address [23:16]

22.3 Write Invalid Region Register

Register Offset: FEE2h
Register Name: Write Invalid Region Start Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIRS[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	WIRS	R/W	Write Invalid Region start address [15:3]
2-0	0	RO	Must be 000b mapped to Write Invalid Region start address [2:0]

Register Offset: FEE4h
Register Name: Write Invalid Region Start Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								WIRS[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	WIRS	R/W	Write Invalid Region start address [23:16]

Register Offset: FEE6h
Register Name: Write Invalid Region End Address Low Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WIRE[15:3]													Reserved		

Bit	Name	Attribute	Description
15-3	WIRE	R/W	Write Invalid Region end address [15:3]
2-0	0	RO	Must be 000b mapped to Write Invalid Region start address [2:0]

Register Offset: FEE8h
Register Name: Write Invalid Region End Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								WIRE[23:16]							

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7-0	WIRE	R/W	Write Invalid Region end address [23:16]

23. SDRAM Control Unit

23.1 SDRAM Mode Set Register

Register Offset: F2h
Register Name: SDRAM Mode Set Register
Reset Value : 0020h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									LAT[2:0]			Reserved			

Bit	Name	Attribute	Description
15-7	Rsvd	RO	Reserved
6-4	LAT[2:0]	R/W	CAS_n Latency Select. Refer to the following list: **LAT [2:0]** — **CAS_n Latency** 0 0 0 — Reserved 0 0 1 — Reserved 0 1 0 — 2 (Default) 0 1 1 — 3 1 0 0 — Reserved 1 0 1 — Reserved 1 1 0 — Reserved
3-0	Rsvd	RO	1'b0.

23.2 SDRAM Control Register

Register Offset: F4h
Register Name: SDRAM Control Register
Reset Value : 0001h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										APCHG	SSSEL1	SSSEL0	SREF	Rsvd	SDRAM EN

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved
5	APCHG	R/W	Auto Pre-Charge Set 1: Auto Precharge Enable Set 0: Auto Precharge Disable (default)
4-3	SSSEL[1:0]	R/W	The SDRAM Size Select bit. (Default is 2'b0) **SSEL1-0 -------- SDRAM Size Select**

			0 0 -------- 1Mx16 bits 0 1 -------- 4Mx16 bits 1 0 -------- Reserved 1 1 -------- Reserved
2	SREF	R/W	Self-Refresh Enable. Set 1: Enable Self-Refreshed when SDRAM is in power mode. Set 0: Disable Self-Refreshed. (Default)
1	Rsvd	RO	Reserved
0	SDRAMEN	R/W	SDRAM Enable. Set 1: Enable SDRAM. (Default) Set 0: Disable SDRAM.

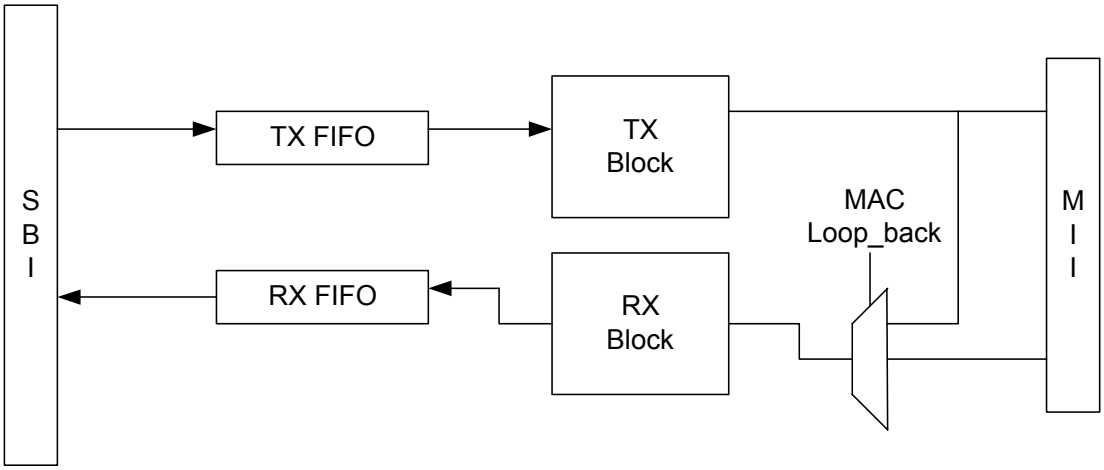
23.3 SDRAM Timing Parameter Register

Register Offset: F6h
Register Name: SDRAM Timing Parameter Register
Reset Value : F933h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SREXT[2:0]			TWR	MRC[3:0]				MPR[3:0]				RCD[3:0]			

Bit	Name	Attribute	Description
15-13	SREXT[2:0]	R/W	Self-Refresh Exit Time (t_{SREX}). The Self-Refresh Exit Time can be programmed from 0 to 7 Clocks.
12	TWR	R/W	Write Recovery Time. 1: 2 Clocks cycle. 0: 1 Clock cycle.
11-8	MRC[3:0]	R/W	Min Row Cycle Time (t_{RC}). It can be programmed from 0 to 15 Clocks.
7-4	MPR[3:0]	R/W	Min Pre-charge Time (t_{RP}). It can be programmed from 0 to 15 Clocks.
3-0	RCD[3:0]	R/W	Row to Column Delay time (t_{RCD}). It can be programmed from 0 to 15 Clocks.

24. Fast Ethernet Control Unit



SBI : System Bus Interface

MAC Block Diagram

24.1 RX Descriptor Format

15	3	2	1	0
DRST				
DRLEN				
DRBP			0	0
DRBP [23:16]				
DRNX			0	0
DRNX [23:16]				
HIDX[5:0]				
Reserve2				
Reserve3				

1. DRST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O	RXOK	Reserved		PHY ERR	DRI BBLE	OBL	LONG	RUNT	CRC ERR	BROAD CAST	MULTI CAST	MCH	MIDH	MID	

The RX circuit will stop receiving packet if Owner Bit=0.

DRST [14:0]: RX Status. The MAC will update the RX status field after frame receiving is complete.

Bit	Name	Description
15	O	Owner Bit. Set1: MAC. Set0: CPU.

14	RXOK	RX successful. This bit indicates that the packet was received successfully without error. It includes: (1) RX_ER = 0 (MII interface). (2) Ignore DRIBBLE status. (3) No over buffer length. (4) Without CRC error. (5) Not a LONG packet. (6) Not a RUNT packet. (7) No FIFO Full.
13-12	Rsvd	Reserved.
11	PHYERR	PHY RX Error packet. Read 1 means that an error occurred in receiving packets on MII interface.
10	DRIBBLE	Dribble packet. Read 1 means the received packet is a dribble packet.
9	OBL	Over Buffer Length. Read 1 means the received packet length > buffer maximum length.
8	LONG	Long packet. Read 1 means the received packet length > maximum packet length.
7	RUNT	Runt packet. Read 1 means the received packet length < 64 Bytes.
6	CRCERR	CRC Error packet. Read 1 means receiving a packet with CRC errors.
5	BROADCAST	It indicates that the received packet is a broadcast packet.
4	MULTICAST	It indicates that the received packet is a multicast packet.
3	MCH	Multicast Hit. It indicates that the received packet hits one of the hash-table bits.
2	MIDH	MID table is hit.
1-0	MID	Index of matched MIDx. These two bits indicate that the received packet hits one of the MID groups.

2. DRLEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					DRLEN										

Bit	Name	Description
15-11	Rsvd	Reserved.
10-0	DRLEN	The size of the received frame.

3. DRBP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DRBP																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DRBP	RX Data Buffer Pointer. This is a 24-bit address pointer and DRBP [1:0] is always 2'b00.

4. DRNX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DRNX																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DRNX	RX Next Frame Descriptor Pointer. This is a 24-bit descriptor address pointer and DRNX [1:0] is always 2'b00. This field must be pointed to next descriptor start address or its start address.

5. HIDX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										HIDX					

Bit	Name	Description
15-6	Rsvd	Reserved.
5-0	HIDX	HIDX[5:0] is a hash index. If MCR1[14] is set to 1, the hash index number will be written into RX description.

6. Reserve2

7. Reserve3

Note:

1. RX Descriptor start address and Data Buffer start address must be Double-Word alignment.
2. The RX packet will be filtered out if its length is less than 6. (Not complete DA information.)

24.2 TX Descriptor Format

15	3	2	1	0
DTST				
DTLEN				
DTBP			0	0
DTBP [23:16]				
DTNP			0	0
DTNP [23:16]				

1. DTST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
O	TXOK	DIS CRC	Reserved						TXFUR	LATEC	EXCEE DC	COLCNT			

The TX circuit will stop transmitting packet if the Owner Bit=0

DTST [14:0]: TX Status and packet control. The MAC will update the TX status field after frame transmission is completed. The control bit is for each packet usage.

Bit	Name	Description
15	O	Owner Bit. Set1: MAC. Set0: CPU.
14	TXOK	TX packet successful. This bit indicates that the packet was transmitted successfully without error. It includes: (1) No late collision. (2) No excessive collision. (3) No TX FIFO under-run. (4) No lost carrier.
13	DISCRC	Disable append CRC field. This is a control bit. =1: disable CRC append. =0: enable CRC append on TX packet. When the status is updated, this bit will keep in previous setting.
12-7	Rsvd	Reserved
6	TXFUR	FIFO Under-Run.
5	LATEC	Late Collision.
4	EXCEEDC	Exceed Collision.
3-0	COLCNT	Collision Counts.

2. DTLEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					DTLEN										

Bit	Name	Description
15-11	Rsvd	Reserved.
10-0	DTLEN	The length of the transmitted packet.

3. DTBP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DTBP																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DTBP	TX Buffer Pointer. This is a 24-bit address pointer.

4. DTNP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								DTNP																							

Bit	Name	Description
31-24	Rsvd	Reserved
23-0	DTNP	TX Next Descriptor Pointer. This is a 24-bit descriptor address pointer and DTNP [1:0] is always 2'b00. This field must be pointed to next descriptor start address or its start address.

Note:

1. TX Descriptor start address must be Double-Word alignment.
2. TX Data Buffer start address can be any byte alignment address.
3. Take care that the transmitted data are less than 60 bytes when drivers are run.

24.3 MCR0: MAC Control Register 0 (00h)

Register Offset: 00h
Register Name: MCR0: MAC Control Register 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FULLD	TXEIE	Rsvd	XMTEN	Reserved		FCEN	AMCP	RXEIE	FBCP	PROM	ADRB	ALONG	ARUNT	RCV EN	ACRCER

Bit	Name	Attribute	Description
15	FULLD	R/W	Full Duplex. Set 1: Full duplex. Set 0: Half duplex. (Default)
14	TXEIE	R/W	TX Early Interrupts Enable. Set 1: MAC will generate one TX early interrupt when the data are transmitted over early interrupt threshold (see MCR1 [7:6]). Set 0: TX early interrupt will be disabled.
13	Rsvd	RO	Reserved
12	XMTEN	R/W	Transmission Enable
11-10	Rsvd	RO	Reserved
9	FCEN	R/W	Flow Control Function Enable. Set 1: will enable flow control. Set 0: will disable flow control.
8	AMCP	R/W	Accept Multicast Packet. Set 1: will enable hash table function. Set 0: will disable hash table function.
7	RXEIE	R/W	RX Early Interrupts Enable. Set to 1, MAC will generate one RX early interrupt when the data are received over early interrupt threshold (see MCR1 [7:6]). Set 0: RX early interrupt will be disabled.
6	FBCP	R/W	Filter Broadcast Packet. Set 1: to filter broadcast packet. Set 0: to accept broadcast packet.
5	PROM	R/W	Promiscuous Mode. Set 1: MAC will receive all packets without checking the MAC address. Set 0: MAC will only receive the packet that hits the MAC address.
4	ADRB	R/W	Accept DRIBBLE packet. Set 1: Enable to accept dribble packets. Set 0: Disable.
3	ALONG	R/W	Accept Long packet. Set 1: Enable to accept long packets. Set 0: Disable.
2	ARUNT	R/W	Accept RUNT packet. Set 1: Enable to accept runt packets. The packets which length > 6 and < 64 will be accepted, but the packets which length >0 and < 6 will be rejected. Set 0: Disable to accept runt packets.
1	RCVEN	R/W	Receive Enable. Set 1: Enable to receive packets. Set 0: Disable packet receive.
0	ACRCER	R/W	Accept CRC Error packet. Set 1: Enable. Set 0: Disable.

24.4 MCR1: MAC Control Register 1 (04h)

Register Offset: 04h
Register Name: MCR1: MAC Control Register 1
Reset Value : 0010h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUCP	WIDX	Reserved				TPF	ECR	EITH [1:0]		MAXLEN [1:0]		0	0	LBM	MRST

Bit	Name	Attribute	Description
15	AUCP	R/W	Filter uni-cast packet by hash-table. Set 1: Enable. Set 0: Disable.
14	WIDX	R/W	Write the hash index number that was hit by hash-table. Set 1: Enable to write the HIDX [5:0] into Rx descriptor. Set 0: Disable this function.
13-10	Rsvd	RO	Reserved
9	TPF	RO	Trigger Pause Frame to be transmitted. If flow control (FCEN bit in MCR0 [9]) is enabled, this bit will be set automatically when received descriptor unavailable happens. TPF refers to XMTEN bit (MCR0 [12]). When XMTEN bit is set, the pause frame can be sent.
8	ECR	R/W	Excessive Collision Retransmit times. 0: 16 times. (Default) 1: 32 times.
7-6	EITH [1:0]	R/W	Early Interrupt Threshold. 00: 1129 bytes. (Default) 01: 1257 bytes. 10: 1385 bytes. 11: 1513 bytes.
5-4	MAXLEN [1:0]	R/W	Maximum Packet Length Selector. Define the length of long packets. 01: 1518 bytes. (Default) 10: 1522 bytes. 11: 1534 bytes. 00: 1537 bytes.
3-2	Rsvd	R/O	Reserved
1	LBM	R/W	Loop-Back mode. 0: Normal Mode. (Default) 1: MAC Loop-Back.
0	MRST	R/W	MAC Reset. Set 1 to reset MAC. After reset, this bit will be cleared to 0.

24.5 MBCR: MAC Bus Control Register (08h)

Register Offset: 08h
Register Name: MBCR: MAC Bus Control Register
Reset Value : 1F1Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			RHPT [4:0]					Reserved		RXFTH [1:0]		TXFTH [1:0]		FIFOTL [1:0]	

PS. Update this register only when RCVEN=0

Bit	Name	Attribute	Description
15-13	Rsvd	RO	Reserved
12-8	RHPT [4:0]	R/W	SDRAM Bus Request High Priority Timer. When MAC issues a bus request to SDRAM arbiter, this timer will start to count down. After this timer is timeout, if SDRAM arbiter is still not granted to MAC, the SDRAM bus request will become high priority. Wait time = 0 ~15 host clocks. (Default=15 host clocks)
7-6	Rsvd	RO	Reserved
5-4	RXFTH [1:0]	R/W	RX FIFO Data Threshold. MAC receive machine starts to move the received data into host memory when receiving data over the RX FIFO threshold. 00: 8 bytes. 01: 16 bytes. (Default) 10: 32 bytes. 11: 64 bytes.
3-2	TXFTH [1:0]	R/W	TX FIFO Data Threshold. MAC transmit machine starts to send out packets to PHY when transmitting data into TX FIFO over the threshold. 00: 16 bytes. 01: 32 bytes. 10: 64 bytes. (Default) 11: 96 bytes.
1-0	FIFOTL [1:0]	R/W	FIFO Transfer Length. The every transfer data length between MAC FIFO and SDRAM. 00: 4 bytes. 01: 8 bytes. 10: 16 bytes. (Default) 11: 32 bytes.

24.6 MTICR: TX Interrupt Control Register (0Ch)

Register Offset: 0Ch
Register Name: MTICR: TX Interrupt Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TXINTC [3:0]				Reserved		TXTIMER [5:0]					

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-8	TXINTC [3:0]	R/W	TX Interrupt Control. 0: Turn off this function. N: Generate an interrupt after sending N packets (1~15 packets).
7-6	Rsvd	RO	Reserved
5-0	TXTIMER [5:0]	R/W	Wait TX Timer. When timeout, it automatically generates an interrupt. Timer waiting time: (63 + TXTIMER * 64) TX clock

24.7 MRICR: RX Interrupt Control Register (10h)

Register Offset: 10h
Register Name: MRICR: RX Interrupt Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RXINTC [3:0]				Reserved		RXTIMER [5:0]					

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved
11-8	RXINTC [3:0]	R/W	RX Interrupt Control. 0: Turn off this function. N: Generate an interrupt after N packets (1~15 packets) are received.
7-6	Rsvd	RO	Reserved
5-0	RXTIMER [5:0]	R/W	Wait RX Timer. When timeout, it automatically generates an interrupt. Timer waiting time: (63 + RXTIMER * 64) RX clock

24.8 MTPR: TX Poll Command Register (14h)

Register Offset: 14h
Register Name: MTPR: TX Poll Command Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															TM2TX

Bit	Name	Attribute	Description
15-1	Rsvd	RO	Reserved
0	TM2TX	R/W	Trigger MAC to Transmit. When Write: Trigger MAC to check TX description owner bit. If owner bit=0, MAC will standby until the owner bit=1 to start transmission. When Read: TM2TX is current transmission status. When TM2TX= 1, it means MAC is in transmitting. When TM2TX= 0, it means transmission was completed.

24.9 MRBSR: RX Buffer Size Register (18h)

Register Offset: 18h
Register Name: MRBSR: RX Buffer Size Register
Reset Value : 0600h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					RBSZ [10:0]									RBSZ[1:0]	

PS. Update this register only when RCVEN=0

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved
10-2	RBSZ [10:2]	R/W	RX Buffer Size Bit10~Bit2 for all RX frame data buffer of Descriptors.
1-0	RBSZ [1:0]	R/W	RX Buffer Size Bit1:0 must be 00.

24.10 MRDCR: RX Descriptor Control Register (1Ah)

Register Offset: 1Ah
Register Name: MRDCR: RX Descriptor Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXPT [7:0]								RXDESPAN [7:0]							

Bit	Name	Attribute	Description
15-8	RXPT [7:0]	R/W	RX Descriptor Threshold value. MAC controller will send TX Pause Frame when available RX Descriptor reaches this threshold value.
7-0	RXDESPAN [7:0]	R/W	RX Descriptor Available Number for flow-control. When MAC finishes one descriptor data transfer into RX buffer, the RX descriptor available number will decrease 1 automatically. Use “IN” instruction to read this register and “OUT” instruction to increase the register value. When RCVEN=0, use “OUT” instruction to setup RX descriptor available number. When RCVEN=1, use “OUT” instruction to increase RX descriptor available number. This register must be initialized before RCVEN = 1.

24.11 MLSR: MAC Last Status Register(1Ch)

Register Offset: 1Ch
Register Name: MLSR: MAC Last Status Register
Reset Value : 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXFOR	LATEC	EXCEEDC	Reserved		RXDESPUA	TXFUR	Rsvd	PHYEER	DRIBBLE	OBL	LONG	RUNT	CRCERR	BROADCAST	MULTICAST

PS. The MAC last time status. It is updated by next packet coming.

Bit	Name	Attribute	Description
15	RXFOR	RO	RX FIFO Over-Run
14	LATEC	RO	Transmit Late Collision.
13	EXCEEDC	RO	Transmit Exceed Collision.
12-11	Rsvd	RO	Reserved
10	RXDESPUA	RO	RX Descriptor Unavailable.

9	TXFUR	RO	TX FIFO Under-Run.
8	Rsvd	RO	Reserved
7	PHYERR	RO	PHY RX Error.
6	DRIBBLE	RO	Dribble Packet.
5	OBL	RO	Received Packet Length Over Buffer Length.
4	LONG	RO	Received Packets Too Long.
3	RUNT	RO	Received Packets Too Short.
2	CRCERR	RO	Received Packets CRC Error.
1	BROADCAST	RO	Received Broadcast Packets.
0	MULTICAST	RO	Received Multicast Packets.

24.12 MMDIO: MDIO Control Register (20h)

Register Offset: 20h
Register Name: MMDIO: MDIO Control Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	MIIWR	MIIRD	PHYAD [4:0]					Reserved			REGAD [4:0]				

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14	MIIWR	R/W	MDIO Write. Set 1 to write MIIWDATA [15:0] to MDIO. It will be cleared after the operation is completed.
13	MIIRD	R/W	MDIO Read. Set 1 to read data from MDIO into MIIRDATA [15:0]. It will be cleared after the operation is completed.
12-8	PHYAD [4:0]	R/W	PHY address.
7-5	Rsvd	RO	Reserved
4-0	REGAD [4:0]	R/W	REG address.

24.13 MMRD: MDIO Read Data Register (24h)

Register Offset: 24h
Register Name: MMRD: MDIO Read Data Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIIRDATA [15:0]															

Bit	Name	Attribute	Description
15-0	MIIRDATA [15:0]	RO	MII Read Data. The data, read from MDIO, are put in this register.

24.14 MMWD: MDIO Write Data Register (28h)

Register Offset: 28h
Register Name: MMRD: MDIO Write Data Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIIWDATA [15:0]															

Bit	Name	Attribute	Description
15-0	MIIWDATA [15:0]	R/W	MII Write Data. The data, intended for being written to MDIO, are put in this register.

24.15 MTDSA0: TX Descriptor Start Address 0 (2Ch)

Register Offset: 2Ch
Register Name: MTDSA0: TX Descriptor Start Address 0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDSA [15:1]															0

PS. Initial this register only when XMTEN=0

Bit	Name	Attribute	Description
15-1	TDSA [15:1]	R/W	TX Descriptor Start Address Bit 15 - Bit 1 that are currently being sent.
0	0	RO	This bit must be 0.

Note: The first TX descriptor start address TDSA [23:0] = {MTDSA1 [7:0], MTDSA0 [15:0]} must be Double-Word alignment. MAC will update the TX descriptor start address when the previous TX has been finished.

24.16 MTDSA1: TX Descriptor Start Address 1 (30h)

Register Offset: 30h
Register Name: MTDSA1: TX Descriptor Start Address 1
Reset Value : 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TDSA [23:16]							

PS. **Initial this register only when XMTEN=0**

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	TDSA [23:16]	RW	TX Descriptor Start Address Bit 23-16 that are currently being sent.

24.17 MRDSA0: RX Descriptor Start Address 0 (34h)

Register Offset: 34h
Register Name: MRDSA0: RX Descriptor Start Address 0
Reset Value : 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDSA [15:1]															0

PS. **Initial this register only when RCVEN=0**

Bit	Name	Attribute	Description
15-1	RDSA [15:1]	R/W	RX Descriptor Start Address Bit 15-1.
0	0	RO	This bit must be 0.

Note: The first RX descriptor start address RDSA [23:0] = {MRDSA1 [7:0], MRDSA0 [15:0]} must be Double-Word alignment. MAC will update the RX descriptor start address after the previous RX has been finished.

24.18 MRDSA1: RX Descriptor Start Address 1 (38h)

Register Offset: 38h
Register Name: MRDSA1: RX Descriptor Start Address 1
Reset Value : 0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RDSA [23:16]							

PS. **Initial this register only when RCVEN=0**

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	RDSA [23:16]	RW	The first RX Descriptor Start Address Bit 23-16.

24.19 MISR: INT Status Register (3Ch)

Register Offset: 3Ch
Register Name: MISR: INT Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						PCHG	ECNTO	TXEI	Reserved		TXEND	RXEI	RXFF	RXDUA	RXEND

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved.
9	PCHG	RC	PHY Media Changed Interrupt status.
8	ECNTO	RC	Event Counter Overflow Interrupt status.
7	TXEI	RC	TX Early Interrupt status.
6-5	Rsvd	RO	Reserved.
4	TXEND	RC	This bit indicates Transmit Packet Finish Interrupt status.
3	RXEI	RC	RX Early Interrupt status.
2	RXFF	RC	RX FIFO Full Interrupt status.
1	RXDUA	RC	This bit indicates RX Descriptor Unavailable Interrupt status.
0	RXEND	RC	This bit indicates Receive Packet Finish Interrupt status.

Note: RC = Read Clear

24.20 MIER: INT Enable Register (40h)

Register Offset: 40h
Register Name: MIER: INT Enable Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						MCHGE	ECNTOE	TXEIEN	Reserved		TXENDE	RXEIE	RXFFE	RXDNAE	RXENDE

Bit	Name	Attribute	Description
15-10	Rsvd	RO	Reserved.
9	MCHGE	RW	PHY Link Changed Interrupt Enable Set 1: Enable MAC to generate interrupts to CPU.
8	ECNTOE	R/W	Event Counter Overflow Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
7	TXEIEN	R/W	TX Early Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.

6-5	Rsvd	RO	Reserved.
4	TXENDE	R/W	Transmit Packet Finish Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
3	RXEIE	R/W	RX Early Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
2	RXFFE	R/W	RX FIFO Full Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
1	RXDNAE	R/W	RX Descriptor Unavailable Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.
0	RXENDE	R/W	Receive Packet Finish Interrupt Enable. Set 1: Enable MAC to generate interrupts to CPU.

24.21 MECISR: Event Counter INT Status Register (44h)

Register Offset: 44h
Register Name: MECISR: Event Counter INT Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TDPCI	LCCI	STPCI	RFFCI	RDUCI	Rsvd	LONGCI	RUNTCI	CRCECI	BCCI	MCCI	SRPCI

The correspond bit in Event Counter INT status register will be set when the MSB bit in related Event Counter register is set to 1. Reading the Event Counter register will clear the corresponding bits. Those event counters will keep increasing until reaching 255 or 65535.

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TDPCI	RO	TX FIFO under-run Dropped Packet Counter Interrupt status.
10	LCCI	RO	TX Late Collision Counter Interrupt status.
9	STPCI	RO	TX Successfully package counter Interrupt status.
8	RFFCI	RO	RX FIFO Full Counter Interrupt status.
7	RDUCI	RO	RX Descriptor Unavailable Dropped Packet Counter Interrupt status.
6	Rsvd	RO	Reserved.
5	LONGCI	RO	RX Long Packet Counter Interrupt status.
4	RUNTCI	RO	RX Runt Packet Counter Interrupt status.
3	CRCECI	RO	RX CRC Error Packet Counter Interrupt status.
2	BCCI	RO	RX Broadcast Packet Counter Interrupt status.
1	MCCI	RO	RX Multicast Packet Counter Interrupt status.
0	SRPCI	RO	RX Successfully Packet Counter Interrupt status.

24.22 MECIER: Event Counter INT Enable Register (48h)

Register Offset: 48h
Register Name: MECIER: Event Counter INT Enable Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TDPCIE	LCCIE	STPCIE	RFFCIE	RDUCIE	Rsvd	LONGCIE	RUNTCIE	CRCECIE	BCCIE	MCCIE	SRPCIE

Bit	Name	Attribute	Description
15-12	Rsvd	RO	Reserved.
11	TDPCIE	RW	TX FIFO under-run Dropped Packet Counter Interrupt Enable
10	LCCIE	R/W	TX Late Collision Counter Interrupt Enable.
9	STPCIE	R/W	TX Successfully Packet Counter Interrupt Enable.
8	RFFCIE	R/W	RX FIFO Full Counter Interrupt Enable.
7	RDUCIE	R/W	RX Descriptor Unavailable Dropped Packet Counter Interrupt Enable.
6	Rsvd	RO	Reserved.
5	LONGCIE	R/W	RX Long Packet Counter Interrupt Enable.
4	RUNTCIE	R/W	RX Runt Packet Counter Interrupt Enable.
3	CRCECIE	R/W	RX CRC Error Packet Counter Interrupt Enable.
2	BCCIE	R/W	RX Broadcast Packet Counter Interrupt Enable.
1	MCCIE	R/W	RX Multicast Packet Counter Interrupt Enable.
0	SRPCIE	R/W	RX Successfully Packet Counter Interrupt Enable.

Note: Reading any one of all the following event counter registers will clear its value to 0.

24.23 MRCNT: Successfully Received Packet Counter Register (50h)

Register Offset: 50h
Register Name: MRCNT: Successfully Received Packet Counter Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRPCNT [15:0]															

Bit	Name	Attribute	Description
15-0	SRPCNT [15:0]	RC	Successfully Received Packet Counter

Note: RC = Read Clear

24.24 MECNT0: Event Counter 0 Register (52H)

Register Offset: 52h
Register Name: MECNT0: Event Counter 0 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCCNT [7:0]								MCCNT [7:0]							

Bit	Name	Attribute	Description
15-8	BCCNT [7:0]	RC	Receive Broadcast Packet Counter.
7-0	MCCNT [7:0]	RC	Receive Multicast Packet Counter.

Note: RC = Read Clear

24.25 MECNT1: Event Counter 1 Register (54h)

Register Offset: 54h
Register Name: MECNT1: Event Counter 1 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RUNCNT [7:0]								CRCECNT [7:0]							

Bit	Name	Attribute	Description
15-8	RUNCNT [7:0]	RC	Receive Run Packet Counter.
7-0	CRCECNT [7:0]	RC	Receive CRC Error Packet Counter.

Note: RC = Read Clear

24.26 MECNT2: Event Counter 2 Register (56h)

Register Offset: 56h
Register Name: MECNT2: Event Counter 2 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								LONGCNT [7:0]							

Bit	Name	Attribute	Description
15-8	Rsvd	RC	Reserved
7-0	LONGCNT [7:0]	RC	Receive Long Packet Counter.

Note: RC = Read Clear

24.27 MCENT3: Event Counter 3 Register (58h)

Register Offset: 58h
Register Name: MECNT3: Event Counter 3 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFFCNT [7:0]								RDUVCNT [7:0]							

Bit	Name	Attribute	Description
15-8	RFFCNT [7:0]	RC	RX FIFO Full Packet Counter.
7-0	RDUVCNT [7:0]	RC	RX Descriptor Unavailable Packet lost Counter.

Note: RC = Read Clear

24.28 MTCNT: Successfully Transmit Packet Counter Register (5Ah)

Register Offset: 5Ah
Register Name: MTCNT: Successfully Transmit Packet Counter Register
Reset Value : 0000h

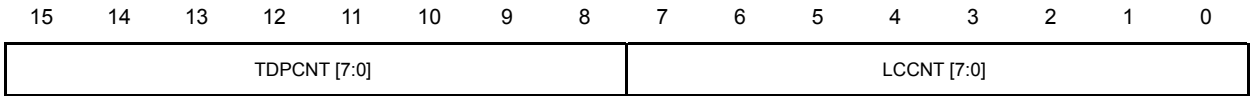
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STPCNT [15:0]															

Bit	Name	Attribute	Description
15-0	STPCNT [15:0]	RC	Successfully Transmitted Packet Counter.

Note: RC = Read Clear

24.29 MCENT4: Event Counter 4 Register (5Ch)

Register Offset: 5Ch
Register Name: MECNT4: Event Counter 4 Register
Reset Value : 0000h

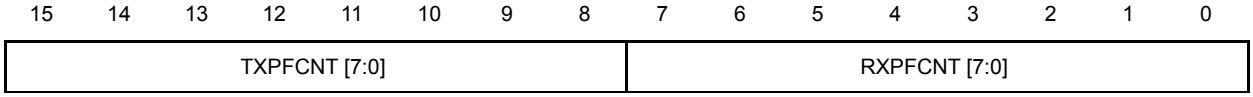


Bit	Name	Attribute	Description
15-8	TDPCNT [7:0]	RC	TX Dropped Packet Counter by TX FIFO under-run.
7-0	LCCNT [7:0]	RC	TX Late Collision Packet Counter.

Note: RC = Read Clear

24.30 MPCNT: Pause Frame Counter Register (5Eh)

Register Offset: 5Eh
Register Name: MPCNT: Pause Frame Counter Register
Reset Value : 0000h

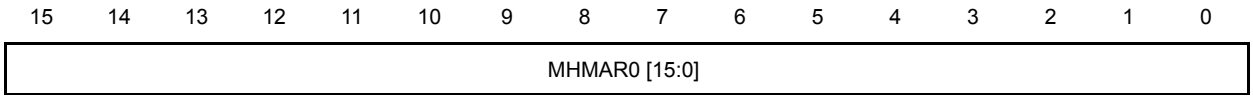


Bit	Name	Attribute	Description
15-8	TXPFCNT [7:0]	RC	Transmitted Pause Frame Counter.
7-0	RXPFCNT [7:0]	RC	Received Pause Frame Counter.

Note: RC = Read Only

24.31 MAR0 ~3: Hash Table Word 0 ~3 (60h, 62h, 64h, 66h)

Register Offset: 60h
Register Name: MAR0: Hash Table Word 0
Reset Value : 0000h



Bit	Name	Attribute	Description
15-0	MHMAR0 [15:0]	R/W	Hash Table Word 0.

Register Offset: 62h
Register Name: MAR1: Hash Table Word 1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR1 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR1 [15:0]	R/W	Hash Table Word 1.

Register Offset: 64h
Register Name: MAR2: Hash Table Word 2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR2 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR2 [15:0]	R/W	Hash Table Word 2.

Register Offset: 66h
Register Name: MAR3: Hash Table Word 3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MHMAR3 [15:0]															

Bit	Name	Attribute	Description
15-0	MHMAR3 [15:0]	R/W	Hash Table Word 3.

24.32 MID0 (68h, 6Ah, 6Ch)

Register Offset: 68h
Register Name: MID0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID0L [15:0]															

Register Offset: 6Ah
Register Name: MID0
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID0M [15:0]															

Register Offset: 6Ch
Register Name: MID0
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID0H [15:0]															

The MAC/Multicast address MID0 [47:0] = {MID0H [15:0], MID0M [15:0], MID0L [15:0]};

For example: MAC address is 01:02:03:04:05:06, the contents for MID are:

MID0L [15:0] = 0201h

MID0M [15:0] = 0403h

MID0H [15:0] = 0605h

Bit 15-0: MID0L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID0M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID0H [15:0], the two bytes in the last line of the MAC/Multicast address.

24.33 MID1 (70h, 72h, 74h)

Register Offset: 70h
Register Name: MID1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID1L [15:0]															

Register Offset: 72h
Register Name: MID1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID1M [15:0]															

Register Offset: 74h
Register Name: MID1
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID1H [15:0]															

The MAC/Multicast address MID1 [47:0] = {MID1H [15:0], MID1M [15:0], MID1L [15:0]};

Bit 15-0: MID1L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID1M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID1H [15:0], the two bytes in the last line of the MAC/Multicast address.

24.34 MID2 (78h, 7Ah, 7Ch)

Register Offset: 78h
Register Name: MID2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID2L [15:0]															

Register Offset: 7Ah
Register Name: MID2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID2M [15:0]															

Register Offset: 7Ch
Register Name: MID2
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID2H [15:0]															

The MAC/Multicast address MID2 [47:0] = {MID2H [15:0], MID2M [15:0], MID2L [15:0]};

Bit 15-0: MID2L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID2M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID2H [15:0], the two bytes in the last line of the MAC/Multicast address.

24.35 MID3 (80h, 82h, 84h)

Register Offset: 80h
Register Name: MID3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID3L [15:0]															

Register Offset: 82h
Register Name: MID3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID3M [15:0]															

Register Offset: 84h
Register Name: MID3
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MID3H [15:0]															

The MAC/Multicast address MID3 [47:0] = {MID3H [15:0], MID3M [15:0], MID3L [15:0]};

Bit 15-0: MID3L [15:0], the two bytes in the first line of the MAC/Multicast address.

Bit 15-0: MID3M [15:0], the two bytes in the second line of the MAC/Multicast address.

Bit 15-0: MID3H [15:0], the two bytes in the last line of the MAC/Multicast address.

25. DC Electrical Characteristics

25.1 Absolute Maximum Ratings (25℃)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VDDC	Core Supply Voltage	2.25	2.75	V	
VDDP1/VDDP2	PLL/DLL Supply Voltage	2.25	2.75	V	
VDDIO	I/O Supply Voltage	3.0	3.6	V	
Vil	Input Low Voltage	---	0.8	V	
Vih	Input High Voltage	2.0	---	V	
Vol	Output Low Voltage	---	0.4	V	
Voh	Output High Voltage	2.4	---	V	
Iin	Input leakage current	-10	10	uA	Vi = VDDO or 0
Ioz	Tri-State output leakage current	-10	10	uA	

Note: * Eq. C = (256/VCC) x Vout x (VCC - Vout)

** Eq. D = (98.0/VCC) x (Vout - VCC) x (Vout + 0.4VCC)

25.2 Temperature

Symbol	Parameter	Typ.	Unit	Conditions
T_{cop}	Case Surface Operating Temperature (case top)	40~45	℃	1. Ambient Temperature = 25℃ 2. Open case testing.
T_A	Ambient Temperature	0~70	℃	Temperature of the surrounding medium
T_{stg}	Storage Temperature	-65~125	℃	Dry Pack.

Note: *The IC should be mounted on PCB within 7 days after the dry pack is opened. If the IC is out of dry pack more than 7 days, it should be burned in oven (+125℃, > 12 hours) before mounted on PCB.*

26. AC Electrical Characteristics

26.1 Alphabetical Key to Switching Parameter Symbols

Parameter Symbol	No.	Description	Parameter Symbol	No.	Description
tAVCH	14	SAD Address Valid to Clock High	tCLDX	2	Data in Hold
tAVLL	12	SAD Address Valid to ALE Low	tCLRH	27	RD_n Inactive Delay
tAVRL	66	SAD Address Valid to RD_n Low	tCLRL	25	RD_n Active Delay
tAVWL	65	SAD Address Valid to WR_n Low	tDVCL	17	MCS_n/PCS_n Hold from Command Inactive
tAZRL	24	SAD Address Float to RD_n Active	tDXDL	1	Data in Setup
tCHCSV	67	SD_CLK High to UCS_n Valid	tLHLL	10	ALE Width
tCHCSX	18	MCS_n/PCS_n Inactive Delay	tLLAX	13	SAD Address Hold from ALE Inactive
tCHLH	9	ALE Active Delay	tRESIN	57	RST_n Setup Time
tCHLL	11	ALE Inactive Delay	tRHAV	29	RD_n Inactive to SAD Address Active
tCLAX	6	Address Hold	tRHDX	59	RD_n High to Data Hold on SAD Bus
tCLAZ	15	SAD Address Float Delay	tRHLH	28	RD_n Inactive to ALE High
tCLCSV	16	MCS_n/PCS_n Active Delay	tRLRH	26	RD_n Pulse Width
tCLDV	7	Data Valid Delay	tWLWH	32	WR_n Pulse Width

26.2 Numerical Key to Switching Parameter Symbols

No.	Parameter Symbol	Description	No.	Parameter Symbol	Description
1	tDVCL	Data in Setup	18	tCHCSX	MCS_n/PCS_n Inactive Delay
2	tCLDX	Data in Hold	24	tAZRL	SAD Address Float to RD_n Active
6	tCLAX	Address Hold	25	tCLRL	RD_n Active Delay
7	tCLDV	Data Valid Delay	26	tRLRH	RD_n Pulse Width
9	tCHLH	ALE Active Delay	27	tCLRH	RD_n Inactive Delay
10	tLHLL	ALE Width	28	tRHLH	RD_n Inactive to ALE High
11	tCHLL	ALE Inactive Delay	29	tRHAV	RD_n Inactive to SAD Address Active
12	tAVLL	SAD Address Valid to ALE Low	32	tWLWH	WR_n Pulse Width
13	tLLAX	SAD Address Hold from ALE Inactive	57	tRESIN	RST_n Setup Time
14	tAVCH	SAD Address Valid to Clock High	59	tRHDX	RD_n High to Data Hold on SAD Bus
15	tCLAZ	SAD Address Float Delay	65	tAVWL	SAD Address Valid to WR_n Low
16	tCLCSV	MCS_n/PCS_n Active Delay	66	tAVRL	SAD Address Valid to RD_n Low
17	tCXCSX	MCS_n/PCS_n Hold from Command Inactive	67	tCHCSV	SD_CLK High to UCS_n Valid

26.3 CPU Bus

● **Read Cycle (100 MHz)**

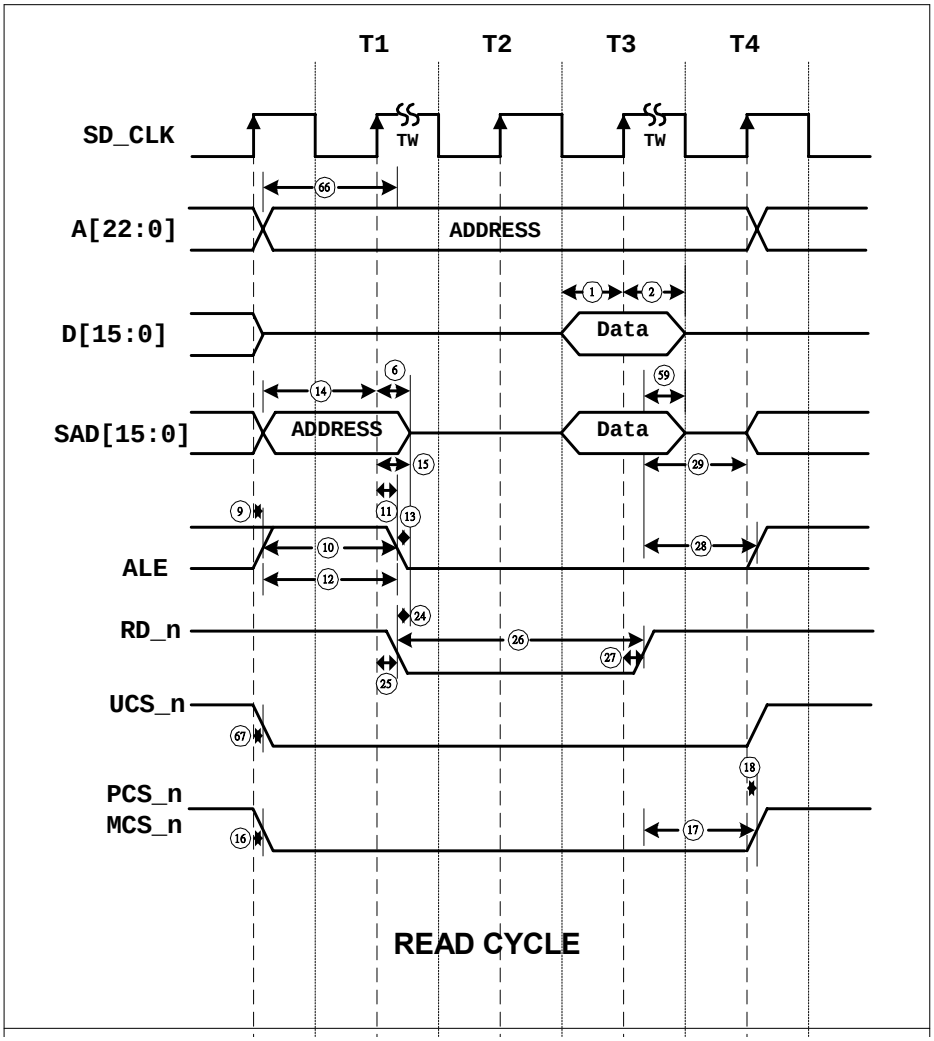
Parameter			Preliminary 100 MHz		Unit
No.	Symbol	Description	Min.	Max.	
General Timing Requirements					
1	tDVCL	Data in Setup	2.5	---	ns
2	tCLDX	Data in Hold(c)	0.0	---	ns
General Timing Responses					
6	tCLAX	Address Hold	3.0	---	ns
9	tCHLH	ALE Active Delay	2.8	---	ns
10	tLHLL	ALE Width	1T	2T	ns
11	tCHLL	ALE Inactive Delay	---	2.8	ns
12	tAVLL	SAD Address Valid to ALE Low(a)	10.0	10+T1 wait	ns
13	tLLAX	SAD Address Hold from ALE Inactive(a)	0.3	0.3+T1 wait	ns
14	tAVCH	SAD Address Valid to Clock High	---	7.0	ns
15	tCLAZ	SAD Address Float Delay	---	3.0	ns
16	tCLCSV	MCS_n/PCS_n Active Delay	4.0	---	ns
17	tCXCSX	MCS_n/PCS_n Hold from Command Inactive(a)	9.0	---	ns
18	tCHCSX	MCS_n/PCS_n Inactive Delay	4.0	---	ns
Read Cycle Timing Responses					
24	tAZRL	SAD Address Float to RD_n Active	---	0.0	ns
25	tCLRL	RD_n Active Delay	3.5	---	ns
26	tRLRH	RD_n Pulse Width	2T (0 wait)	2T+T3 wait	ns
27	tCLRH	RD_n Inactive Delay	3.5	---	ns
28	tRHLH	RD_n Inactive to ALE High(a)	9.0	---	ns
29	tRHAV	RD_n Inactive to SAD Address Active(a)	6.5	---	ns
59	tRHDX	RD_n High to Data Hold on SAD Bus(c)	0.0	---	ns
66	tAVRL	SAD Address Valid to RD_n Low(a)	---	10.5	ns
67	tCHCSV	SD_CLK High to UCS_n Valid	---	3.0	ns

Notes: All timing parameters are measured at 1.5 V with 50 pF loading on SD_CLK unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where V_{IH} = V_{CC} – 0.5 V.

a. Equal loading on referenced pins. T1 wait states should be inserted to increase hold time.

b. If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

● Read Cycle Waveforms



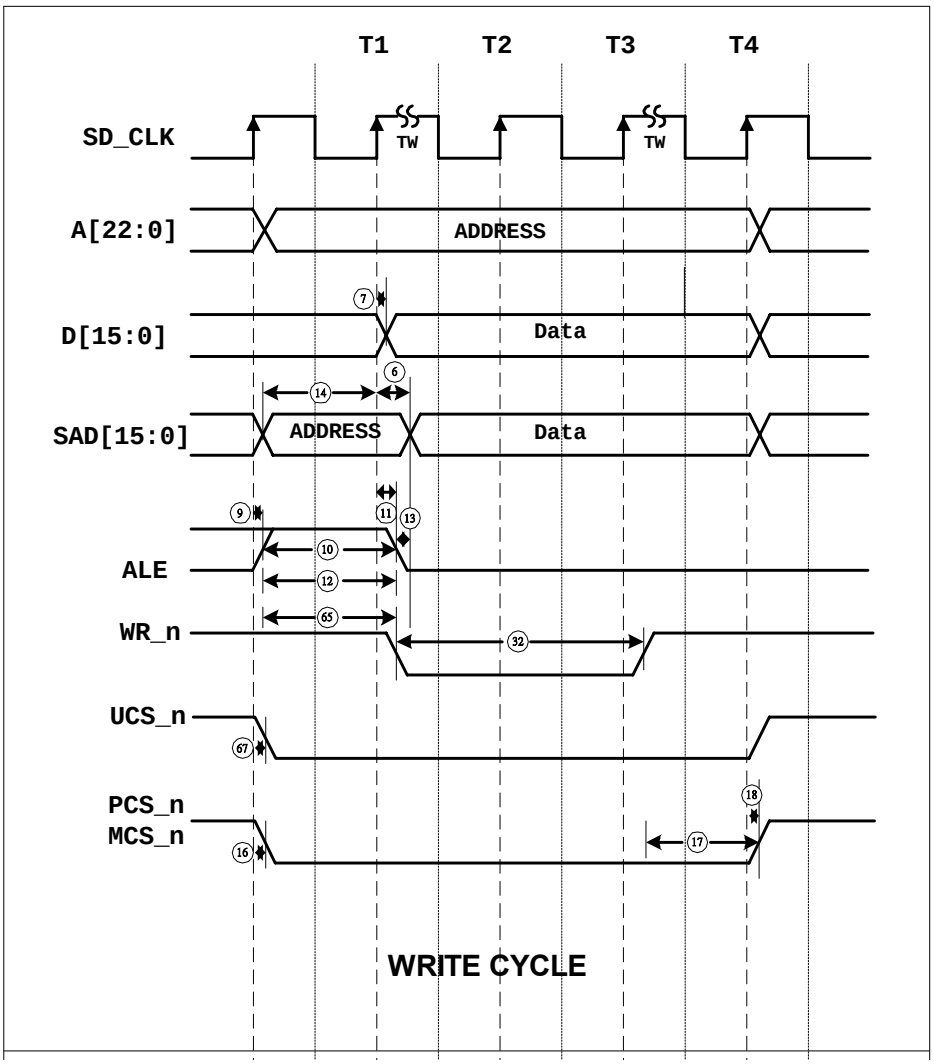
● Write Cycle (100 MHz)

Parameter			Preliminary 100 MHz		Unit
No.	Symbol	Description	Min.	Max.	
General Timing Responses					
6	t_{CLAX}	Address Hold	3.0	---	ns
7	t_{CLDV}	Data Valid Delay	3.0	---	ns
9	t_{CHLH}	ALE Active Delay	3.0	---	ns
10	t_{LHLL}	ALE Width	1T	2T	ns
11	t_{CHLL}	ALE Inactive Delay	---	2.8	ns
12	t_{AVLL}	SAD Address Valid to ALE Low[a]	10	10+T1 wait	ns
13	t_{LLAX}	SAD Address Hold from ALE Inactive[a]	0.25	0.25+T1 wait	ns
14	t_{AVCH}	SAD Address Valid to Clock High	---	7.0	ns
16	t_{CLCSV}	MCS_n/PCS_n Active Delay	4.0	---	ns
17	t_{CXCSX}	MCS_n/PCS_n Hold from Command Inactive[a]	9.0	---	ns
18	t_{CHCSX}	MCS_n/PCS_n Inactive Delay	4.0	---	ns
Write Cycle Timing Responses					
32	t_{WLWH}	WR_n Pulse Width	2T	2T+T3 wait	ns
65	t_{AVWL}	SAD Address Valid to WR_n Low	---	10.5	ns
67	t_{CHCSV}	SD_CLK High to UCS_n Valid	---	3.0	ns

Notes: All timing parameters are measured at 1.5 V with 50 pF loading on SD_CLK unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

a. Equal loading on referenced pins. T1 wait states should be inserted to increase hold time.

● Write Cycle Waveforms

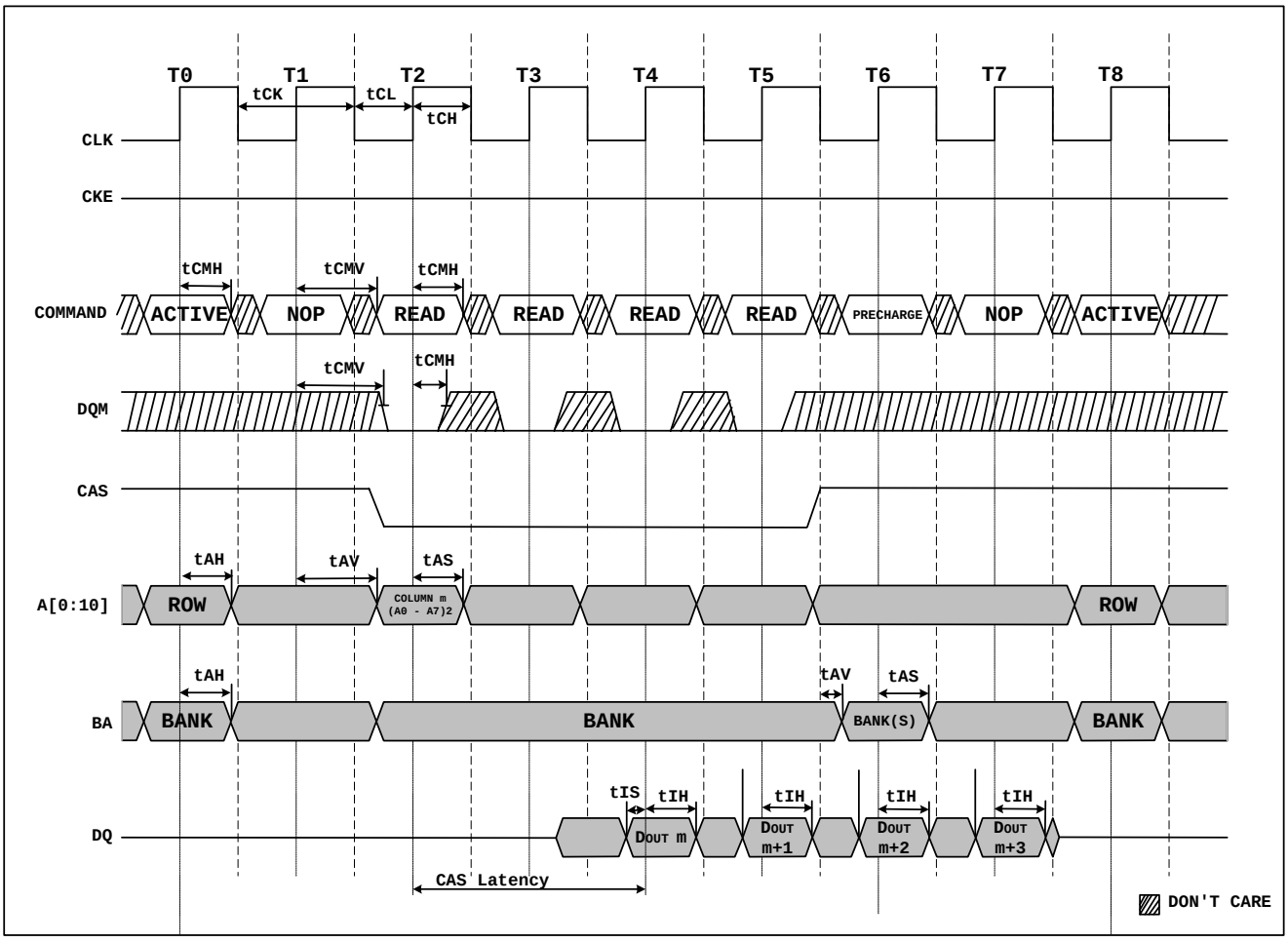


26.4 SDRAM Bus

● **SDRAM Read Cycle (100 MHz)**

Symbol	Description	Min. (ns)	Typ. (ns)	Max. (ns)
tCK	Clock Period time	10	---	---
tCL	Low Period time	---	5	---
tCH	Clock High Period time	---	5	---
tCMV	Command Valid Delay time	---	---	6.5
tCMH	Command Hold time	3	---	---
tAV	Address Valid Delay time	---	---	7
tAH	Address Hold time	4	---	---
tIS	Data Input Setup time	2	---	---
tIH	Data Input Hold time	1	---	---

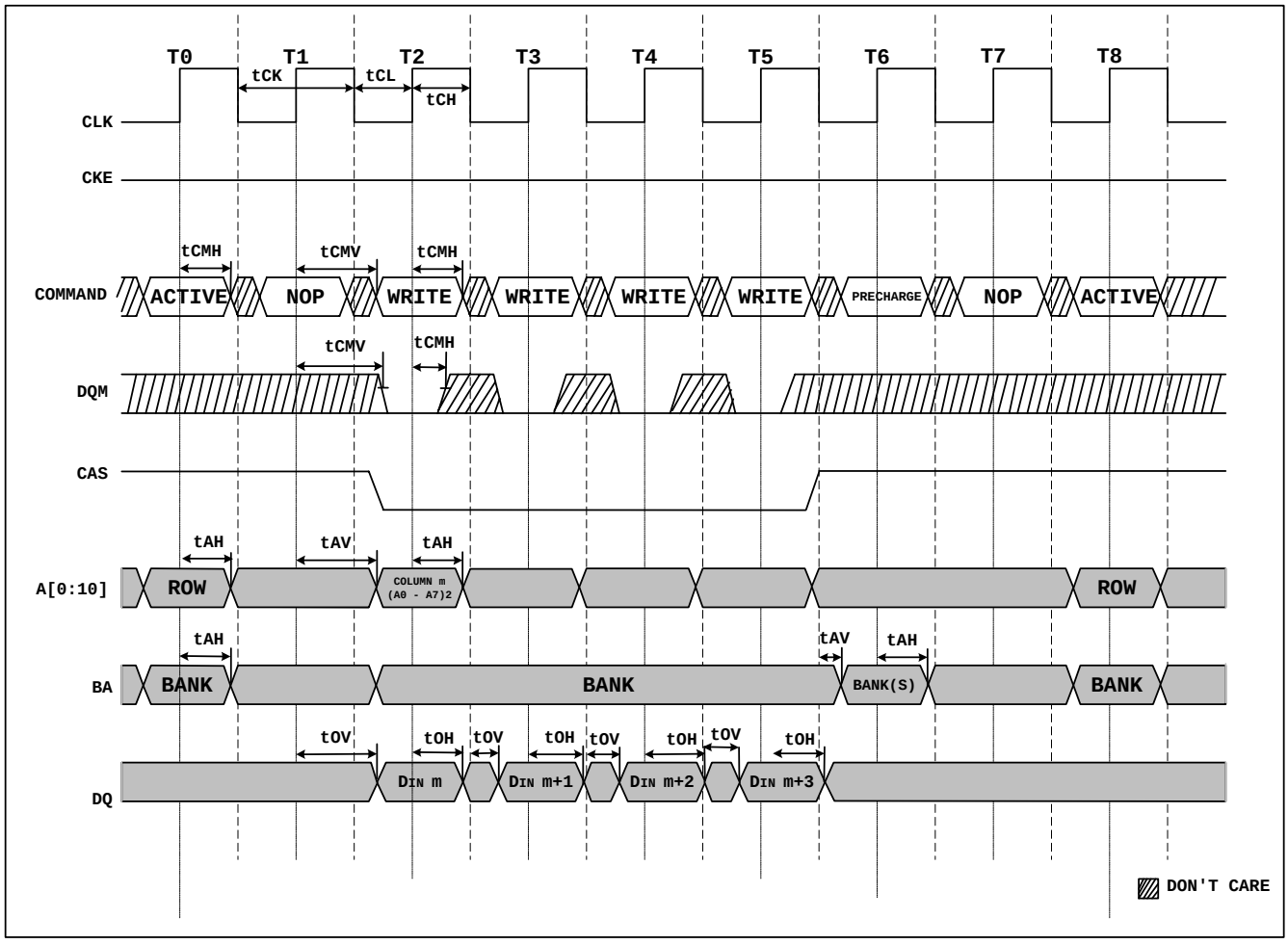
● **SDRAM Read Cycle Waveforms**



● SDRAM Write Cycle (100 MHz)

Symbol	Description	Min. (ns)	Typ. (ns)	Max. (ns)
tCK	Clock Period time	10	---	---
tCL	Low Period time	---	5	---
tCH	Clock High Period time	---	5	---
tCMV	Command Valid Delay time	---	---	6.5
tCMH	Command Hold time	3	---	---
tAV	Address Valid Delay time	---	---	7
tAH	Address Hold time	5	---	---
tOV	Data Output Valid Delay time	---	---	7
tOH	Data Output Hold time	2	---	---

● SDRAM Write Cycle Waveforms



26.5 CPU Reset

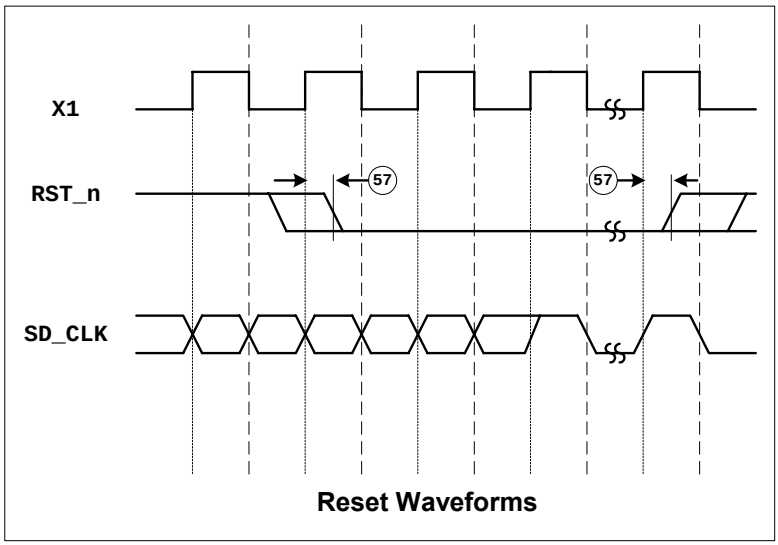
● Reset and Bus Hold (100 MHz)

Parameter			Preliminary 100 MHz		Unit
No.	Symbol	Description	Min.	Max.	
Reset and Bus Hold Timing Requirements					
15	t_{CLAZ}	SAD Address Float Delay	---	3.5	ns
57	t_{RESIN}	RST_n Setup Time	2	---	ns
58	t_{HVCL}	HOLD Setup[a]	2.5	---	ns

Note: All timing parameters are measured at 1.5 V with 50 pF loading on SD_CLK unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where V_{IH} = V_{CC} – 0.5 V.

a. This timing must be met to guarantee recognition at the next clock.

● Reset Waveforms



Reset Waveforms

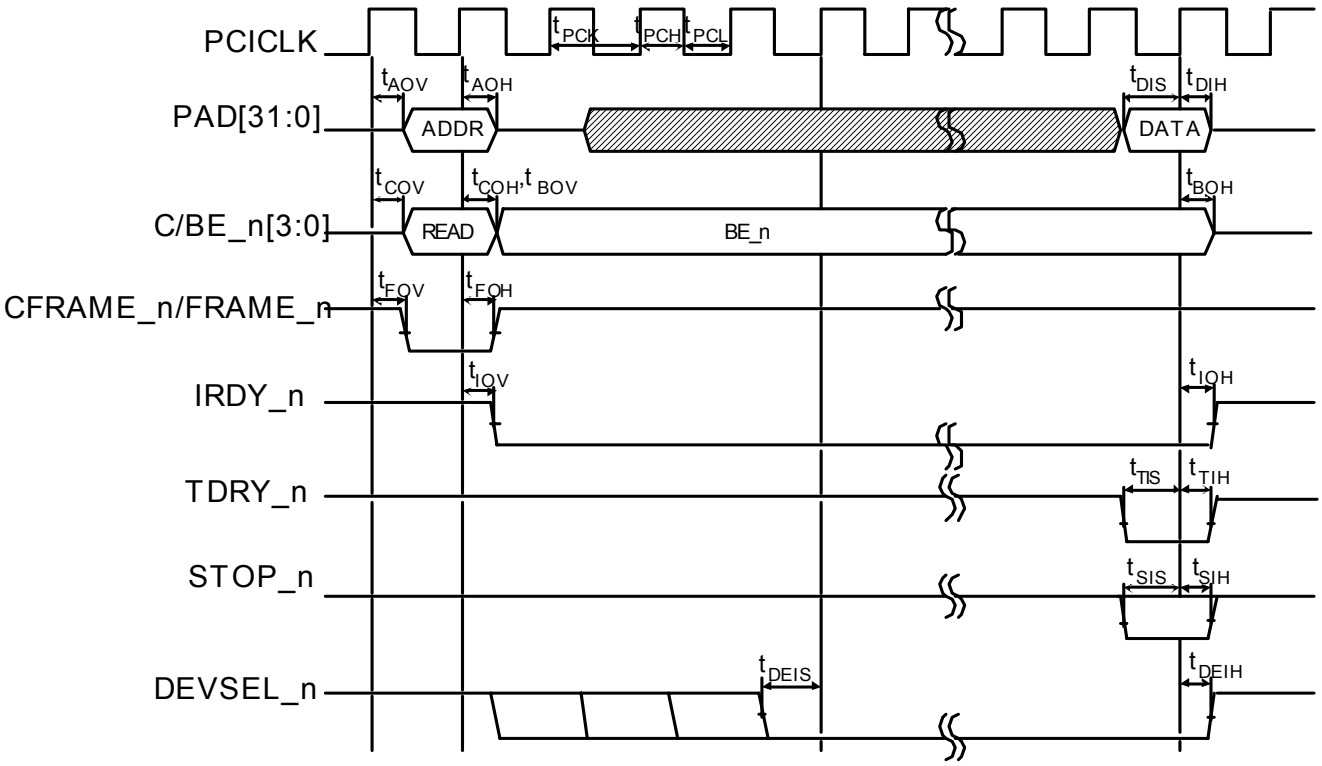
26.6 PCI Interface

26.6.1 R2880 as a PCI Master

- **Memory / I/O Read Cycle**

Symbol	Parameter	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
tPCK	PCI clock cycle time	30	---	---	
tPCH	PCI clock high-level width	---	15	---	
tPCL	PCI clock low-level width	---	15	---	
tAOV	Address output valid delay time	---	---	7.0	
tAOH	Address output hold time	1.0	---	---	
tDIS	Data input setup time	7.0	---	---	
tDIH	Data input hold time	0.0	---	---	
tCOV	Command output valid delay time	---	---	7.0	
tCOH	Command output hold time	1.0	---	---	
tBOV	Byte Enable output valid delay time	---	---	7.0	
tBOH	Byte Enable output hold time	1.0	---	---	
tFOV	FRAME_n output valid delay time	---	---	7.0	
tFOH	FRAME_n output hold time	1.0	---	---	
tIOV	IRDY_n output valid delay time	---	---	7.0	
tIOH	IRDY_n output hold time	1.0	---	---	
tTIS	TRDY_n input setup time	7.0	---	---	
tTIH	TRDY_n input hold time	0.0	---	---	
tSIS	STOP_n input setup time	7.0	---	---	
tSIH	STOP_n input hold time	0.0	---	---	
tDEIS	DEVSEL_n input setup time	7.0	---	---	
tDEIH	DEVSEL_n input hold time	0.0	---	---	

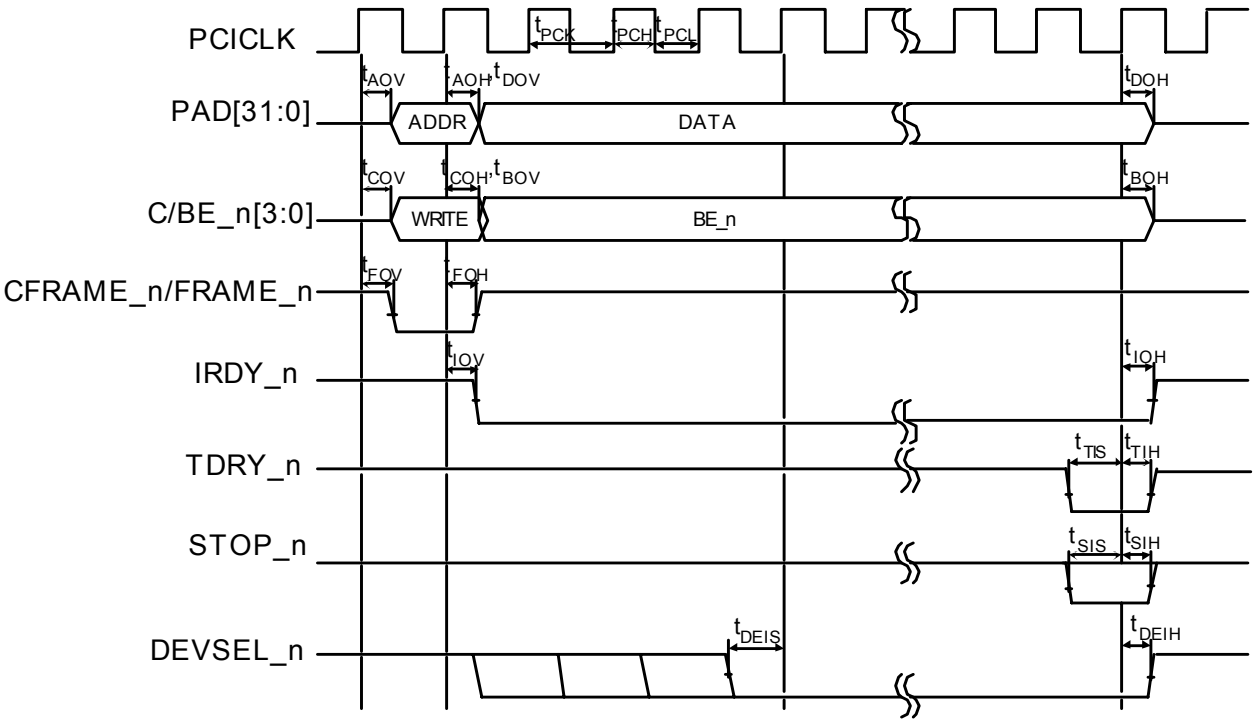
- **Memory / I/O Read Cycle Waveforms**



- **Memory / I/O Write Cycle**

Symbol	Parameter	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
tPCK	PCI clock cycle time	30	---	---	
tPCH	PCI clock high-level width	---	15	---	
tPCL	PCI clock low-level width	---	15	---	
tAOV	Address output valid delay time	---	---	7.0	
tAOH	Address output hold time	1.0	---	---	
tDOV	Data output valid delay time	---	---	7.0	
tDOH	Data output hold time	1.0	---	---	
tCOV	Command output valid delay time	---	---	7.0	
tCOH	Command output hold time	1.0	---	---	
tBOV	Byte Enable output valid delay time	---	---	7.0	
tBOH	Byte Enable output hold time	1.0	---	---	
tFOV	FRAME_n output valid delay time	---	---	7.0	
tFOH	FRAME_n output hold time	1.0	---	---	
tIOV	IRDY_n output valid delay time	---	---	7.0	
tIOH	IRDY_n output hold time	1.0	---	---	
tTIS	TRDY_n input setup time	7.0	---	---	
tTIH	TRDY_n input hold time	0.0	---	---	
tSIS	STOP_n input setup time	7.0	---	---	
tSIH	STOP_n input hold time	0.0	---	---	
tDEIS	DEVSEL_n input setup time	7.0	---	---	
tDEIH	DEVSEL_n input hold time	0.0	---	---	

- **Memory / I/O Write Cycle Waveforms**

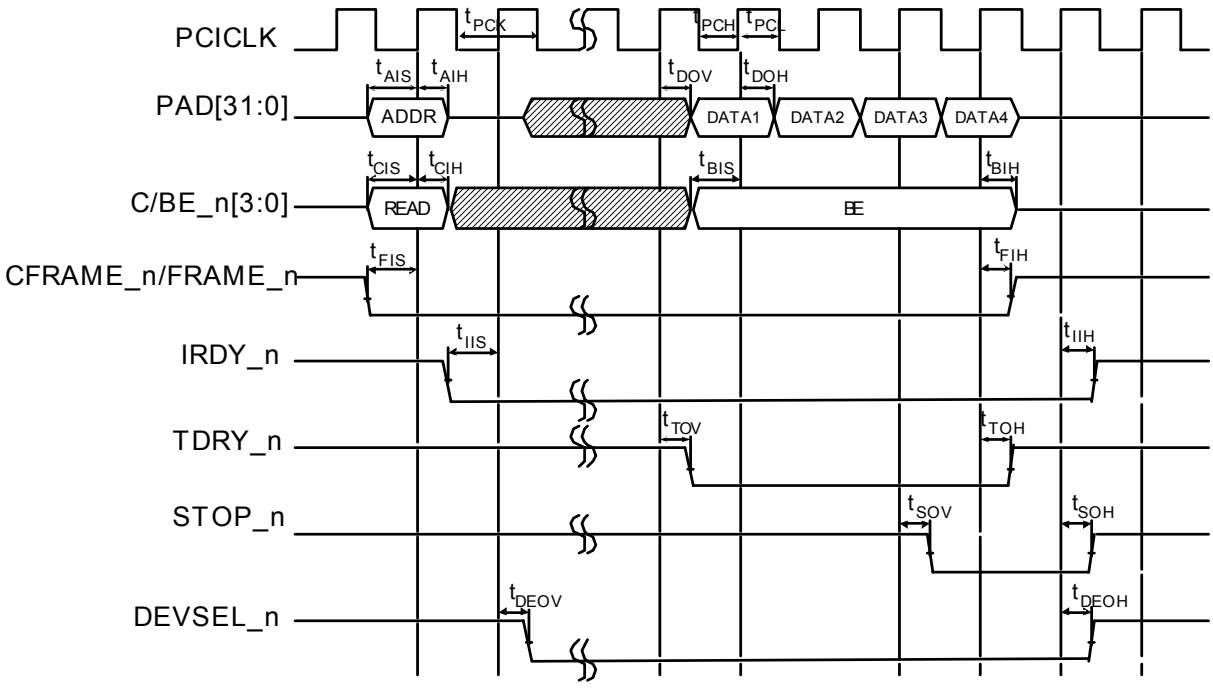


26.6.2 R2880 as a PCI Target

- **Read Cycle**

Symbol	Parameter	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
tPCK	PCI clock cycle time	30	---	---	
tPCH	PCI clock high-level width	---	15	---	
tPCL	PCI clock low-level width	---	15	---	
tAIS	Address input setup time	7.0	---	---	
tAIH	Address input hold time	0.0	---	---	
tDOV	Data output valid delay time	---	---	11.0	
tDOH	Data output hold time	1.0	---	---	
tCIS	Command input setup time	7.0	---	---	
tCIH	Command input hold time	0.0	---	---	
tBIS	Byte Enable input setup time	7.0	---	---	
tBIH	Byte Enable input hold time	0.0	---	---	
tFIS	FRAME_n input setup time	9.0	---	---	
tFIH	FRAME_n input hold time	0.0	---	---	
tIIS	IRDY_n input setup time	9.5	---	---	
tIIH	IRDY_n input hold time	0.0	---	---	
tTOV	TRDY_n output valid delay time	---	---	11.0	
tTOH	TRDY_n output hold time	1.0	---	---	
tSOV	STOP_n output valid delay time	---	---	11.0	
tSOH	STOP_n output hold time	1.0	---	---	
tDEOV	DEVSEL_n output valid delay time	---	---	11.0	
tDEOH	DEVSEL_n output hold time	1.0	---	---	

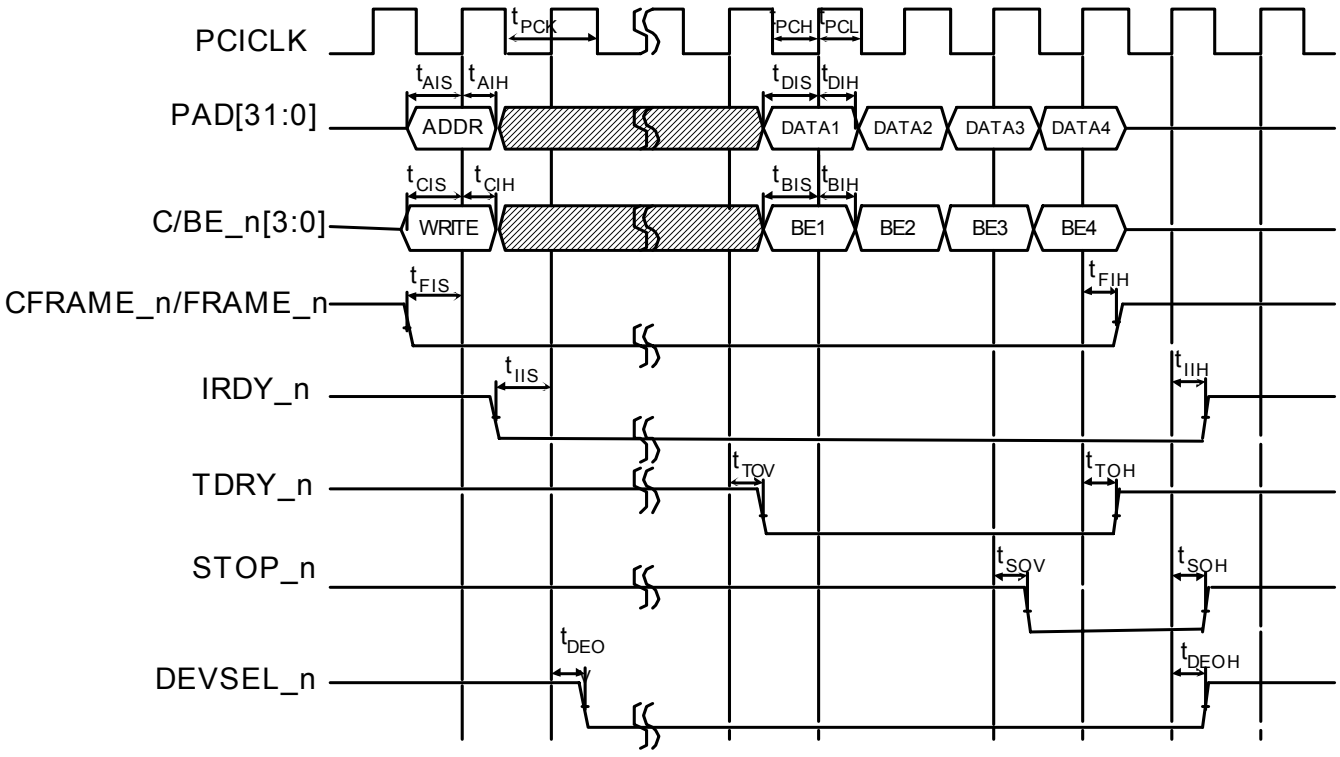
- **Burst Read Cycle Waveforms**



- **Write Cycle**

Symbol	Parameter	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
tPCK	PCI clock cycle time	30	---	---	
tPCH	PCI clock high-level width	---	15	---	
tPCL	PCI clock low-level width	---	15	---	
tAIS	Address input setup time	7.0	---	---	
tAIH	Address input hold time	0.0	---	---	
tDIS	Data input setup time	7.0	---	---	
tDIH	Data input hold time	0.0	---	---	
tCIS	Command input setup time	7.0	---	---	
tCIH	Command input hold time	0.0	---	---	
tBIS	Byte Enable input setup time	7.0	---	---	
tBIH	Byte Enable input hold time	0.0	---	---	
tFIS	FRAME_n input setup time	9.0	---	---	
tFIH	FRAME_n input hold time	0.0	---	---	
tIIS	IRDY_n input setup time	9.5	---	---	
tIIH	IRDY_n input hold time	0.0	---	---	
tTOV	TRDY_n output valid delay time	---	---	11.0	
tTOH	TRDY_n output hold time	1.0	---	---	
tSOV	STOP_n output valid delay time	---	---	11.0	
tSOH	STOP_n output hold time	1.0	---	---	
tDEOV	DEVSEL_n output valid delay time	---	---	11.0	
tDEOH	DEVSEL_n output hold time	1.0	---	---	

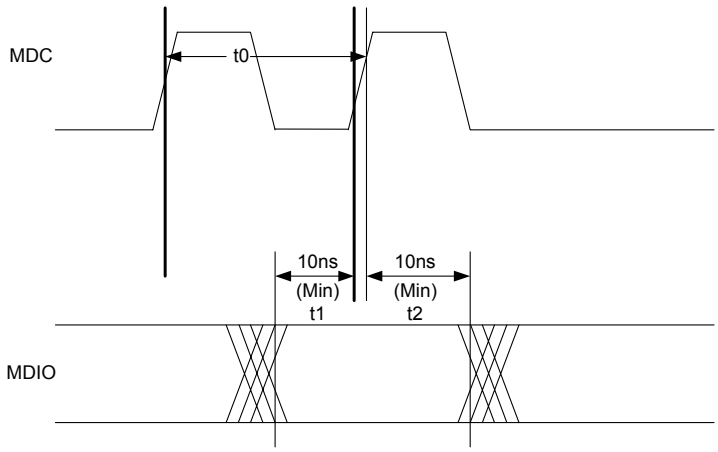
- **Burst Write with Disconnect without Data**



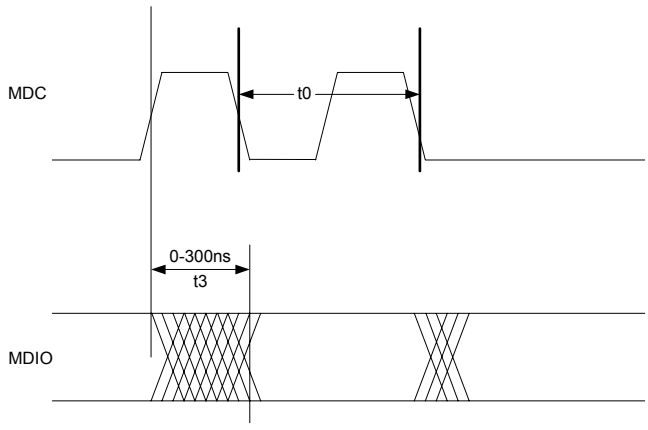
26.7 MDC/MDIO Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t0	MDC Cycle Time		TXC/10			
t1	MDIO Setup before MDC		MDC/2-10			
t2	MDIO Hold after MDC		MDC/2+10			
t3	MDC to MDIO Output Delay		10			

MDIO Timing When OUTPUT by R2880



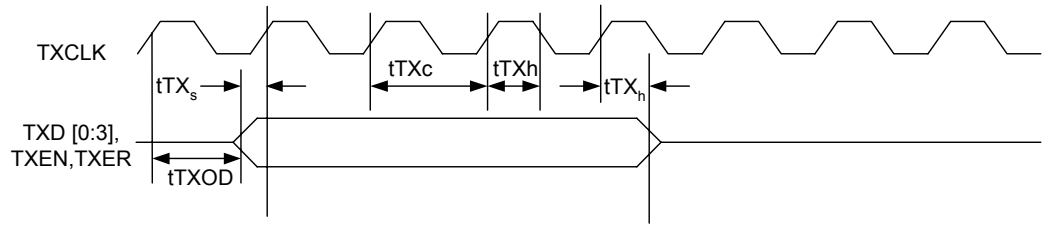
MIDO Timing When OUTPUT by PHY



26.8 TX Transmit Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tTXh, tTXl	TXCLK High/Low Time					
tTXs	TXD{0:3}, TXEN, and TXER Setup to TXCLK High	1T-6				
tTXh	TXD{0:3}, TXEN, and TXER Hold from TXCLK High			4		
tTXOD	TXCLK to Output Delay			6		
Typical Values are at 25℃ and for design aid only; not guaranteed and not subject to production testing.						

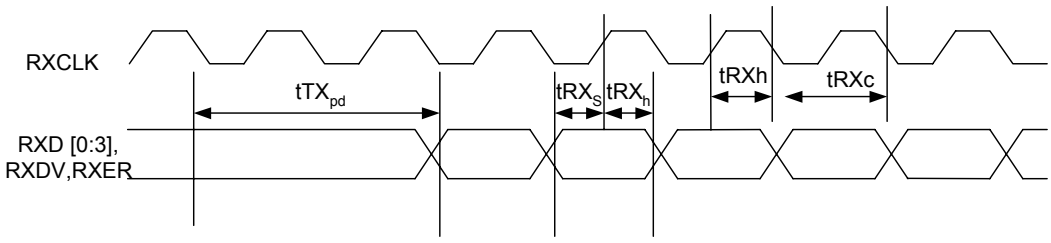
26.9 TX Transmit Timing Diagram



26.10 RX Receive Timing Parameters

Symbol	Parameter	Min.	Type	Max.	Unit	Conditions
tRXs	RXD{0:3}, RXDN, and RXER Setup to RXCLK High	0.8				
tRXh	RXD{0:3}, RXDN, and RXER Hold from RXCLK High	1				
Typical Values are at 25℃ and for design aid only; not guaranteed and not subject to production testing.						

26.11 RX Receive Timing Diagram



27. Instruction Set OP-Code and Clock Cycles

Function	Format				Clocks	Notes
DATA TRANSFER INSTRUCTIONS						
MOV = Move						
register to register/memory	1000100w	mod reg r/m			1/1	
register/memory to register	1000101w	mod reg r/m			1/6	
immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	1/1	
immediate to register	1011w reg	data	data if w=1		1	
memory to accumulator	1010000w	addr-low	addr-high		6	
accumulator to memory	1010001w	addr-low	addr-high		1	
register/memory to segment register	10001110	mod 0 reg r/m			3/8	
segment register to register/memory	10001100	mod 0 reg r/m			2/2	
PUSH = Push						
memory	11111111	mod 110 r/m			8	
register	01010 reg				3	
segment register	000reg110				2	
immediate	011010s0	data	data if s=0		1	
POP = Pop						
memory	10001111	mod 000 r/m			8	
register	01011 reg				6	
segment register	000 reg 111	(reg≠01)			8	
PUSHA = Push all	01100000				36	
POPA = Pop all	01100001				44	
XCHG = Exchange						
register/memory	1000011w	mod reg r/m			3/8	
register with accumulator	10010 reg				3	
XTAL = Translate byte to AL	11010111				10	
IN = Input from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
OUT = Output from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
LEA = Load EA to register	10001101	mod reg r/m			1	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		14	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		14	
ENTER = Build stack frame	11001000	data-low	data-high	L		
L = 0					7	
L = 1					11	
L > 1					11+10(L-1)	
LEAVE = Tear down stack frame	11001001				7	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				2	
PUSHF = Push flags	10011100				2	
POPF = Pop flags	10011101				11	
ARITHMETIC INSTRUCTIONS						
ADD = Add						
reg/memory with register to either	000000dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 000 r/m	data	data if sw=01	1/8	
immediate to accumulator	0000010w	data	data if w=1		1	

Function	Format				Clocks	Notes
ADC = Add with carry						
reg/memory with register to either	000100dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	1/8	
immediate to accumulator	0001010w	data	data if w=1		1	
INC = Increment						
register/memory	1111111w	mod 000 r/m			1/8	
register	01000 reg				1	
SUB = Subtract						
reg/memory with register to either	001010dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
SBB = Subtract with borrow						
reg/memory with register to either	000110dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 011 r/m			1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
DEC = Decrement						
register/memory	1111111w	mod 001 r/m			1/8	
register	01001 reg				1	
NEG = Change sign						
register/memory	1111011w	mod reg r/m			1/8	
CMP = Compare						
register/memory with register	0011101w	mod reg r/m			1/7	
register with register/memory	0011100w	mod reg r/m			1/7	
immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	1/7	
immediate with accumulator	0011110w	data	data if w=1		1	
MUL = multiply (unsigned)	1111011w	mod 100 r/m				
register-byte					13	
register-word					21	
memory-byte					18	
memory-word					26	
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m				
register-byte					16	
register-word					24	
memory-byte					21	
memory-word					29	
register/memory multiply immediate (signed)	011010s1	mod reg r/m	data	data if s=0	23/28	
DIV = Divide (unsigned)	1111011W	mod 110 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
IDIV = Integer divide (signed)	1111011w	mod 111 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
AAS = ASCII adjust for subtraction	00111111				3	
DAS = Decimal adjust for subtraction	00101111				2	
AAA = ASCII adjust for addition	00110111				3	
DAA = Decimal adjust for addition	00100111				2	
AAD = ASCII adjust for divide	11010101	00001010			14	
AAM = ASCII adjust for multiply	11010100	00001010			15	
CBW = Corrvert byte to word	10011000				2	
CWD = Convert word to double-word	10011001				2	

Function	Format				Clocks	Notes
BIT MANIPULATION INSTRUCTUIONS						
NOT = Invert register/memory	1111011w	mod 010 r/m			1/7	
AND = And						
reg/memory and register to either	001000dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1	1/8	
immediate to accumulator	0010010w	data	data if w=1		1	
OR = Or						
reg/memory and register to either	000010dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	1/8	
immediate to accumulator	0000110w	data	data if w=1		1	
XOR = Exclusive or						
reg/memory and register to either	001100dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	1/8	
immediate to accumulator	0011010w	data	data if w=1		1	
TEST = And function to flags , no result						
register/memory and register	1000010w	mod reg r/m			1/7	
immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	1/8	
immediate data and accumulator	1010100w	data	data if w=1		1	
Sifts/Rotates						
register/memory by 1	1101000w	mod TTT r/m			2/8	
register/memory by CL	1101001w	mod TTT r/m			1+n / 7+n	
register/memory by Count	1100000w	mod TTT r/m	count		1+n / 7+n	
STRING MANIPULATION INSTRUCTIONS						
MOVS = Move byte/word	1010010w				13	
INS = Input byte/word from DX port	0110110w				13	
OUTS = Output byte/word to DX port	0110111w				13	
CMPS = Compare byte/word	1010011w				18	
SCAS = Scan byte/word	101011w				13	
LODS = Load byte/word to AL/AX	1010110w				13	
STOS = Store byte/word from AL/AX	1010101w				7	
Repeated by count in CX:						
MOVS = Move byte/word	11110010	1010010w			4+9n	
INS = Input byte/word from DX port	11110010	0110110w			5+9n	
OUTS = Output byte/word to DX port	11110010	0110111w			5+9n	
CMPS = Compare byte/word	1111011z	1010011w			4+18n	
SCAS = Scan byte/word	1111001z	1010111w			4+13n	
LODS = Load byte/word to AL/AX	11110010	0101001w			3+9n	
STOS = Store byte/word from AL/AX	11110100	0101001w			4+3n	
PROGRAM TRANSFER INSTRUCTIONS						
Conditional Transfers — jump if:						
JE/JZ = equal/zero	01110100	disp			1/9	
JL/JNGE = less/not greater or equal	01111100	disp			1/9	
JLE/JNG = less or equal/not greater	01111110	disp			1/9	
JC/JB/JNAE = carry/below/not above or equal	01110010	disp			1/9	
JBE/JNA = below or equal/not above	01110110	disp			1/9	
JP/JPE = parity/parity even	01111010	disp			1/9	
JO = overflow	01110000	disp			1/9	
JS = sign	01111000	disp			1/9	
JNE/JNZ = not equal/not zero	01110101	disp			1/9	
JNL/JGE = not less/greater or equal	01111101	disp			1/9	
JNLE/JG = not less or equal/greater	01111111	disp			1/9	
JNC/JNB/JAE = not carry/not below /above or equal	01110011	disp			1/9	
JNBE/JA = not below or equal/above	01110111	disp			1/9	
JNP/JPO = not parity/parity odd	01111011	disp			1/9	

Function	Format			Clocks	Notes
JNO = not overflow	01110001	disp		1/9	
JNS = not sign	01111001	disp		1/9	
Unconditional Transfers					
CALL = Call procedure					
direct within segment	11101000	disp-low	disp-high	11	
reg/memory indirect within segment	11111111	mod 010 r/m		12/17	
indirect intersegment	11111111	mod 011 r/m	(mod≠11)	25	
direct intersegment	10011010	segment offset		18	
		selector			
RET = Retum from procedure					
within segment	11000011			16	
within segment adding immed to SP	11000010	data-low	data-high	16	
intersegment	11001011			23	
instersegment adding immed to SP	1001010	data-low	data-high	23	
JMP = Unconditional jump					
short/long	11101011	disp-low		9/9	
direct within segment	11101001	disp-low	disp-high	9	
reg/memory indirect within segment	11111111	mod 100 r/m		11/16	
indirect intersegment	11111111	mod 101 r/m	(mod ?11)	18	
direct intersegment	11101010	segment offset		11	
		selector			
Iteration Control					
LOOP = Loop CX times	11100010	disp		7/16	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp		7/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp		7/16	
JCXZ = Jump if CX = zero	11100011	disp		7/15	
Interrupt					
INT = Interrupt					
Type specified	11001101	type		41	
Type 3	11001100			41	
INTO = Interrupt on overflow	11001110			43/4	
BOUND = Detect value out of range	01100010	mod reg r/m		21-60	
IRET = Interrupt return	11001111			31	
PROCESSOR CONTROL INSTRUCTIONS					
CLC = clear carry	11111000			2	
CMC = Complement carry	11110101			2	
STC = Set carry	11111001			2	
CLD = Clear direction	11111100			2	
STD = Set direction	11111101			2	
CLI = Clear interrupt	11111010			5	
STI = Set interrupt	11111011			5	
HLT = Halt	11110100			1	
WAIT = Wait	10011011			1	
LOCK = Bus lock prefix	11110000			1	
ESC = Math coprocessor escape	11011MMM	mod PPP r/m		1	
NOP = No operation	10010000			1	
SEGMENT OVERRIDE PREFIX					
CS	00101110			2	
SS	00110110			2	
DS	00111110			2	
ES	00100110			2	

28. R2880 Execution Timing

The above instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

1. The opcode, along with data or displacement required for execution, has been prefetched and resided in the instruction queue at the time needed.

2. No wait states or bus HOLDs occur.

3. All word -data are located on even-address boundaries.

4. One RISC micro operation (*u*OP) maps one cycle (according to the pipeline stages described below), except the following case:

Pipeline Stages for single micro operation(one cycle):

Fetch → Decode → op_r → ALU → WB (For ALU function *u*OP)

Fetch → Decode → EA → Access → WB (For Memory function *u*OP)

4.1 *Memory read u*OP need 6 cycles for bus.

Pipeline stages for *Memory read u*OP(6 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB

Bus Cycle

4.2 *Memory push u*OP need 1 cycle if it has no previous *Memory push u*OP, and 5 cycles if it has previous *Memory push* or *Memory Write u*OP.

Pipeline stages for *Memory push u*OP after *Memory push u*OP (another 5 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB (1^{st} *Memory push u*OP)

(2^{nd} *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

pipeline stall

4.3 *MUL u*OP and *DIV* of ALU function *u*OP for 8-bit operation need both 8 cycles, for 16-bit operation need both 16 cycles.

4.4 All jumps, calls, ret and loopXX instructions required to fetch the next instruction for the destination address (*Unconditional Fetch u*OP) will need 9 cycles.

Pipeline stages for unconditional fetch:

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → Fetch (*Fetch u*OP)

(next *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

will be flushed

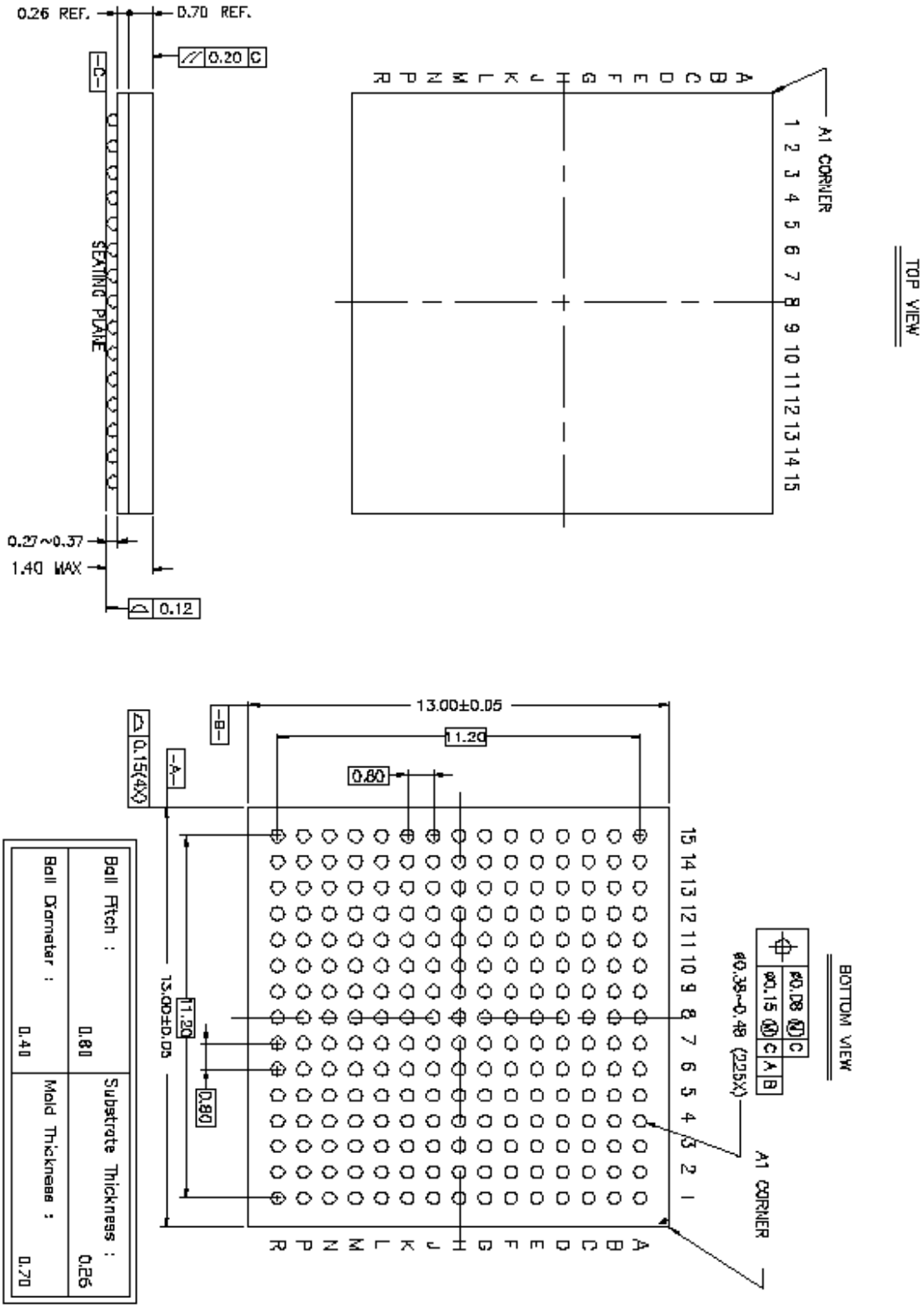
These 9 cycles caused branch penalty → Fetch → Decode → following stages...(New *u*OP)

Note: op_r: operand read stage, EA: Calculate Effective Address stage, Idle: Bus Idle stage, T0..T3: Bus T0..T3 stage,

Access: Access data from cache memory stage.

29. Package Information

29.1 BGA Package Drawing



30. Revision History

Rev.	Date	History
D01	10/24/2003	Draft Version 0.1
P01	04/12/2004	Preliminary Version 0.1
F10	05/21/2004	Formal Release – Final Version 1.0 Adding Ambient Temperature and Storage Temperature to Chapter 25.2.