AR-B1380/AR-B1380A
Half Size All-In-One
386SX CPU CARD
User's Guide

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0. PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

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0.2 WELCOME TO THE AR-B1380/1380A CPU BOARD

This guide introduces the Acrosser AR-B1380/1380A CPU card's functions, features, and how to start, set up and operate your AR-B1380/1380A. You can also find general system information here.

0.3 BEFORE YOU USE THIS GUIDE

If you have not already installed this AR-B1380/1380A, refer to Chapter 3, "Setting up the System" in this guide. Check the packing list, make sure all the accessories are included in the package.
The AR-B1380/1380A diskette provides the newest information about the card**. Please refer to the README.DOC file of the enclosed utility diskette**. It contains the modification and hardware & software information, and it has updates to product functions that may not be mentioned here.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires servicing, contact the dealer from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original shipping container for this purpose.

You can help assure efficient servicing of your product by following these guidelines:

1) Include your name, address, telephone, facsimile number and e-mail where you may be reached.

2) A description of the system configuration and/or software at the time of malfunction.

3) A brief description of the symptoms.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

User's comments are always welcome as they assist us in improving the usefulness of our products and the understanding of our publications. They form a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you supply in any way we believe appropriate without incurring any obligation. You may, of course, continue to use the information you supply.

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0.6 ORGANIZATION

This manual covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, "Overview," provides an overview of the system features and packing list.
- Chapter 2, "System Controllers," describes the major structure.
- Chapter 3, "Setting Up the System," describes how to adjust the jumpers, and the connector settings.
- Chapter 4, "CRT/LCD Flat Panel Displays", describes the configuration and installation procedure by using LCD and CRT displays.
- Chapter 5, "Software Installation," describes the utility diskette, solid state disk's write protect function, and the watchdog timer.
- Chapter 6, "Solid State Disk," describes the various type of SSD's installation methods.
- Chapter 7, "BIOS Console," providing the BIOS settings.
- Chapter 8, Specifications & SSD Types Supported
- Chapter 9, Using the Memory Banks
- Chapter 10, Placement & Dimensions
- Chapter 11, Programming the RS-485

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.
Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents that may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

1) **Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).**

2) **When unpacking and handling the board or other system components, place all materials on an antic static surface.**

3) **Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of every board.**

1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The AR-B1380/AR-B1380A is a new generation half size, 386 ISA interface card. This card offers much greater performance than the older cards such as support for 20MB DRAM using one 72-pin SIMM bank, 42 pin two SOJ one RS-232C/485 connector and one RS-232C port and 3MB/1.5MB/1.5MB solid state disk capacity for EPROM, FLASH and SRAM.

The 6 layer PCB CPU board is equipped with an IDE HDD interface, a floppy disk interface, 1 parallel port, and 2 serial ports and a watchdog timer. It provides 2 bus interfaces, ISA bus and a PC/104 compatible expansion bus. Based on the PC/104 expansion bus, you could easily install numerous PC/104 modules. This 386 CPU card is excellent for embedded systems, MMI's, work stations, medical applications or POS/POI systems. As well, an RS-232C/485 port is provided for remote control capabilities. RS-485 has not been offered until recently on 386 cards.

A watchdog timer, which has a software programmable time-out interval, is also provided on this CPU card. It ensures that the system does not hang up if a program can not execute normlallly.

For diskless application, the AR-B1380/AR-B1380A provides up to 3 MB of bootable EPROM, FLASH, or SRAM disk by using 64Kx8 to 1Mx8 memory chips.

The AR-B1380A has VGA and LAN onboard, and offers the most exciting possibilities yet to the industry. The onboard VGA/LCD controller brings about a whole new dimension of industrial computing. No longer do you have to worry about adding an extra card to your system. Space is saved by eliminating the need for a separate VGA card. The VGA/LCD unit comes with 1MB of V-RAM on board and uses the C&T 65545 Chipset, to support a wide range of LCD Panels.

1.2 PACKING LIST

These accessories are included with the system. Before you begin installing your AR-B1380/AR-B1380A CPU board, take a moment to make sure that the following items have been included inside the AR-B1380/AR-B1380A package.

For the AR-B1380 package, it includes

AR-B1380 Accessories	Description
1 Quick setup guide	Introduction of the hardware features of AR-B1380
1 AR-B1380 ISA interface CPU board	Well protected in the anti-static bag.
1 Keyboard adapter cable	PS/2 to IBM standard type adapt cable.
1 Hard diskette drive cable	2.54 mm 40 pin IDC type cable
1 Floppy disk drive interface cable	34 pin IDC type cable
1 Parallel port interface cable	26 pin Mini-IDC to DB-25 female
1 RS-232C interface cable + PS/2 Mouse	10 pin IDC to DB-9 male + PS2 Mouse
1 Utility diskette	Manual file in PDF format & S.S.D. utility

Table 1-1 AR-B1380 Packing List

AR-B1380A Accessories	Description
1 Quick setup guide	Introduction of the hardware features of AR-B1380A
1 AR-B1380A ISA interface CPU board	Well protected in the anti-static bag.
1 Keyboard adapter cable	PS/2 to IBM standard type adapt cable.
1 Hard diskette drive cable	2.54 mm 40 pin IDC type cable
1 Floppy disk drive interface cable	34 pin IDC type cable
1 Parallel port interface cable	26 pin Mini-IDC to DB-25 female cable
1 RS-232C interface cable+ PS2 Mouse	10 pin IDC to DB-9 male + PS2 Mouse
2 Utility diskette	Manual file in PDF format, S.S.D. utility and VGA and Ethernet drivers

Table 1-2 AR-B1380A Packing List

1.3 FEATURES

This system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- ALI M6117C, 80386SX-25/33/40 MHz CPU (33 MHz CPU is standard)
- ISA and non-stack through PC/104 extension bus
- 2 MB DRAM onboard system with a DRAM socket and SIMM bank for expansion
- On-board CRT and LCD panel displays (available for AR-B1380A only)
- Supports 2 IDE hard disk drive
- Supports 8-pin/4pin 2.5mm connector
- Supports 2 floppy disk drives with 34-pin 2.54mm connector (for 1380 only)
- Supports 1 SPP/EPP/ECP mode parallel port
- Supports 1 RS-232C and 1 RS-232C/RS-485 serial ports
- On-board Ethernet compatible 10 Base-T NE2000; shielded RJ-45 edge connector (for 1380A)
- PS/2 keyboard and mouse
- 3 sockets for up to 3MB/1.5MB / 1.5MB EPROM/FLASH/SRAM
- Supports 1 DiskOnChip
- Onboard buzzer or an external speaker with a 4-pin header
- Programmable watchdog timer
- 8 TTL level loads maximum (8 mil trace minimum)
- AMI Flash BIOS
- Built-in watchdog and power LEDs and 2 headers for external PW/WD and HDD LEDs
- Signal 5V power requirement
- Multi-layer PCB for noise reduction
- Dimensions : 185mmX122mm (7.28" x 4.80")

2. SYSTEM CONTROLLER

This chapter describes the major structure of the AR-B1380/AR-B1380A CPU board. The following topics are covered:

- Microprocessor
- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Real-Time Clock and Non-Volatile RAM
- Timer
- Serial Port
- Parallel Port
- Solid State Disks
- Ethernet Controller
- VGA Controller

2.1 MICROPROCESSOR

The AR-B1380/AR-B1380A uses the ALI M6117 CPU. It is designed to perform like Intel's 386SX system with deep green features.

The 386SX core is the same as the M1386SX of Acer Labs. Inc. and 100% object code compatible with the Intel 386SX microprocessor. System manufacturers can provide 386 CPU based systems optimized for both cost and size. Instruction pipelining and high bus bandwidth ensure short average instruction execution times and high system throughput. Furthermore, it can minimize charge leakage while the external clock is stopped, without storing the data in registers. The power consumption here is almost zero when the clock stops. The internal structure of this core is 32-bit and it's address bus with a very low supply current. Real mode as well as protected mode are available and can run MS-DOS, MS-Windows, OS/2 and UNIX.

2.2 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the AR-B1380/AR-B1380A CPU board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system DMA channel.

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Table 2-1 DMA Channel Controller

2.3 KEYBOARD CONTROLLER

The 8042 processor is programmed to support a keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to the keyboard controller until an acknowledgment is received for the previous byte. The "output buffer full" interruption may be used for both send and receive routines.

2.4 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B1380/AR-B1380A board. They accept requests from the peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indexed by the CPU to determine which interrupt service routine should be executed.

The following is the system interrupt levels:

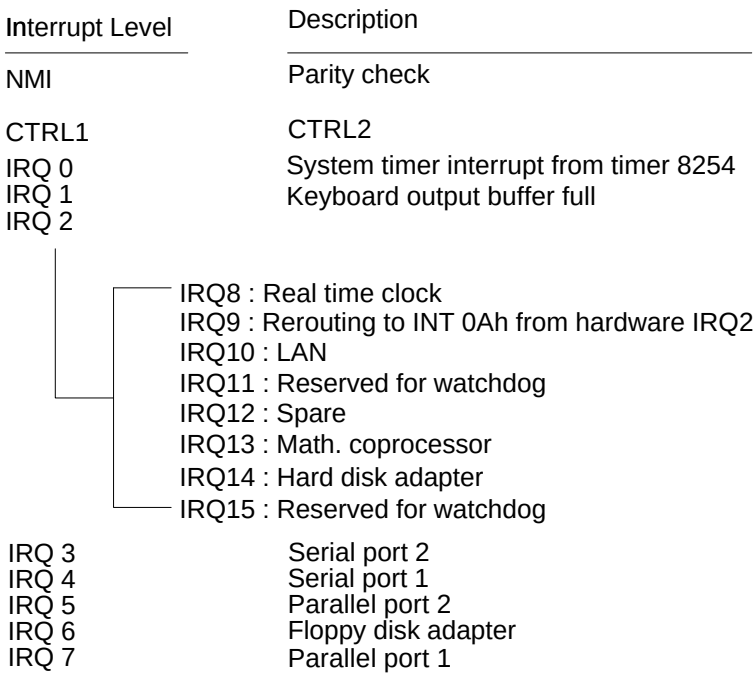


Figure 2-1 Interrupt Controller

2.4.1 I/O Port Address Map

Hex Range	Device	Factory Preset
000-01F	DMA controller 1	✓
020-021	Interrupt controller 1	✓
022-023	ALI M6117 chipset address	✓
040-04F	Timer 1	✓
050-05F	Timer 2	✓
060-06F	8042 keyboard/controller	✓
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)	✓
080-09F	DMA page registers	✓
0A0-0A1	Interrupt controller 2	✓
0C0-0DF	DMA controller 2	✓
0F0	Clear Math Co-processor	
0F1	Reset Math Co-processor	
0F8-0FF	Math Co-processor	
170-178	Fixed disk 1	
1F0-1F8	Fixed disk 0	✓
201	Game port	
208-20A	EMS register 0	
218-21A	EMS register 1	
278-27F	Parallel printer port 2 (LPT 2)	
2E8-2EF	Serial port 4 (COM 4)	
2F8-2FF	Serial port 2 (COM 2)	✓
300-31F	Prototype card/streaming type adapter	
320-33F	LAN adapter	
378-37F	Parallel printer port 1 (LPT 1)	
380-38F	SDLC, bisynchronous	
3A0-3AF	Bisynchronous	
3B0-3BF	Monochrome display and printer port 3 (LPT 3)	
3C0-3CF	EGA/VGA adapter	
3D0-3DF	Color/graphics monitor adapter	
3E8-3EF	Serial port 3 (COM 3)	
3F0-3F7	Floppy controller	
3F8-3FF	Serial port 1 (COM 1)	▲

Table 2-2 I/O Port Address Map

NOTE: The I/O address marked "✓" or "▲" is the BIOS default settings. "✓" means the I/O address is not adjustable; "▲" means it is adjustable in the BIOS setup.

2.4.2 I/O Channel Pin Assignment (Bus1)

I/O Pin	Signal Name	Input/Output	I/O Pin	Signal Name	Input/Output
A1	-IOCHCK	Input	B1	GND	Ground
A2	SD7	Input/Output	B2	RSTDRV	Output
A3	SD6	Input/Output	B3	+5V	Power
A4	SD5	Input/Output	B4	IRQ9	Input
A5	SD4	Input/Output	B5	-5V	Power
A6	SD3	Input/Output	B6	PDRQ2	Input
A7	SD2	Input/Output	B7	-12V	Power
A8	SD1	Input/Output	B8	PZWS	Input
A9	SD0	Input/Output	B9	+12V	Power
A10	/IORDY	Input	B10	GND	Ground
A11	AEN	Output	B11	-MEMW	Output
A12	SA19	Input/Output	B12	-MEMR	Output
A13	SA18	Input/Output	B13	-IOW	Input/Output
A14	SA17	Input/Output	B14	-IOR	Input/Output
A15	SA16	Input/Output	B15	-DACK3	Output
A16	SA15	Input/Output	B16	DRQ3	Input
A17	SA14	Input/Output	B17	-DACK1	Output
A18	SA13	Input/Output	B18	DRQ1	Input
A19	SA12	Input/Output	B19	-REFRESH	Input/Output
A20	SA11	Input/Output	B20	BUSCLK	Output
A21	SA10	Input/Output	B21	IRQ7	Input
A22	SA9	Input/Output	B22	IRQ6	Input
A23	SA8	Input/Output	B23	IRQ5	Input
A24	SA7	Input/Output	B24	IRQ4	Input
A25	SA6	Input/Output	B25	IRQ3	Input
A26	SA5	Input/Output	B26	-DACK2	Output
A27	SA4	Input/Output	B27	TC	Output
A28	SA3	Input/Output	B28	BALE	Output
A29	SA2	Input/Output	B29	+5V	Power
A30	SA1	Input/Output	B30	OSC	Output
A31	SA0	Input/Output	B31	GND	Ground

Table 2-3 I/O Channel Pin Assignments

I/O Pin	Signal Name	Input/Output	I/O Pin	Signal Name	Input/Output
C1	-SBHE	Input/Output	D1	-MEM16	Input
C2	LA23	Input/Output	D2	-IO16	Input
C3	LA22	Input/Output	D3	IRQ10	Input
C4	LA21	Input/Output	D4	IRQ11	Input
C5	LA20	Input/Output	D5	IRQ12	Input
C6	LA19	Input/Output	D6	IRQ15	Input
C7	LA18	Input/Output	D7	IRQ14	Input
C8	LA17	Input/Output	D8	-DACK0	Output
C9	-MRD16	Input/Output	D9	DRQ0	Input
C10	-MWR16	Input/Output	D10	-DACK5	Output
C11	SD8	Input/Output	D11	DRQ5	Input
C12	SD9	Input/Output	D12	-DACK6	Output
C13	SD10	Input/Output	D13	DRQ6	Input
C14	SD11	Input/Output	D14	-DACK7	Output
C15	SD12	Input/Output	D15	DRQ7	Input
C16	SD13	Input/Output	D16	+5V	Power
C17	SD14	Input/Output	D17	-MASTER	Input
C18	SD15	Input/Output	D18	GND	Ground

Table 2-4 I/O Channel Pin Assignments

2.5 REAL-TIME CLOCK AND NON-VOLATILE RAM

The AR-B1380/AR-B1380A contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long period of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte

Address	Description
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 2-5 Real-Time Clock & Non-Volatile RAM

2.6 TIMER

The AR-B1380/AR-B1380A provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

2.7 SERIAL PORTS

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, 1.5 (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a complete MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

Table 2-6 ACE Accessible Registers

(1) Receiver Buffer Register (RBR)
Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)
Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)
Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)
Bit 0: "0" if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(5) Line Control Register (LCR)
Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)
Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(7) Line Status Register (LSR)
Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

(8) MODEM Status Register (MSR)
Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock	Present Error Difference Between Desired and Actual
50	2304	---
75	1536	---
110	1047	0.026
134.5	857	0.058
150	768	---
300	384	---
600	192	---
1200	96	---
1800	64	---
2000	58	0.69
2400	48	---
3600	32	---
4800	24	---
7200	16	---
9600	12	---
14400	8	---
19200	6	---
28800	4	---
38400	3	---
57600	2	---

Table 2-7 Serial Port Divisor Latch

2.8 PARALLEL PORT

(1) Register Address

Port Address	Read/Write	Register
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

Table 2-8 Registers' Address

(2) Printer Interface Logic

The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level .

(3) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:

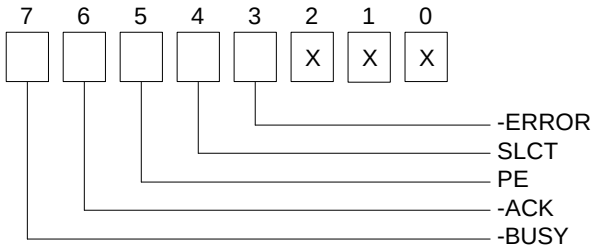


Figure 2-2 Printer Status Buffer

NOTE: X represents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and can not accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A1 means the printer has detected the end of the paper.

Bit 4: A1 means the printer is selected.

Bit 3: A0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

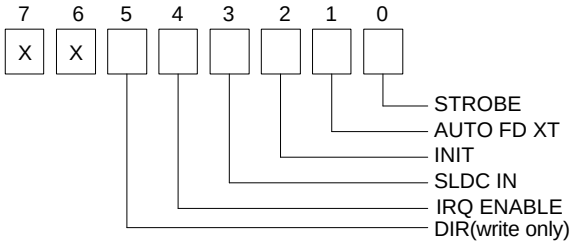


Figure 2-3 Bit Definitions

NOTE: X represents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write only.

Bit 4: A1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A1 in this bit position selects the printer.

Bit 2: A0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A1 causes the printer to line-feed after a line is printed.

Bit 0: A0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

2.9 SOLID STATE DISKS

The AR-B1380/1380A provides three JEDEC DIP sockets and supports three kinds of solid state disks, EPROM, FLASH, and SRAM. With EPROM, the total memory is up to 3MB, and FLASH or `SRAM is up to 1.5MB. The three sockets can be configured as three sockets for SSD or two sockets for SSD plus 1 socket for DiskOnChip. The DiskOnChip socket supports memory from 2MB to 144MB. The DiskOnModule is connected to the onboard IDE connector. All the flash disks are ideal for diskless systems, and are also highly reliable for high-speed access applications, as controllers for industrial use, or line test instruments, etc.

2.10 ETHERNET CONTROLLER

The Ethernet controller of the AR-B1380A is a highly integrated design that provides all Media Access Control (MAC) and Encode-Decode (ENDEC) functions in accordance with the IEEE 802.3 standard. The Ethernet controller can interface directly with the PC-AT ISA bus without any external device. The interface to PC-AT ISA bus is fully compatible with NE2000 Ethernet adapter cards, so all software programs designed for the NE2000 standard can run on the Ethernet controller card without any modification.

Microsoft's Plug and Play and the jumperless software configuration function are both supported. The capability of the PnP and Non-PnP mode autoswitch function allows the users to configure network cards. No jumpers or switches are needed to set additionally when using either the PC or PnP function. The integrated 8Kx16 SRAM and 10BASE-T transceiver make the Ethernet controller more cost-effective.

2.11 VGA CONTROLLER

AR-B1380A provides a super VGA controller for CRT and LCD displays. It supports CRT color monitors, STN, Dual-Scan, TFT (see note below), monochrome and color panels. It can be connected to create a compact video solution for the industrial environment. 1MB of VRAM on-boarded allows a maximum CRT resolution of 1280X1024 and a LCD resolution of 640X480 with 64K colors. TFT resolution can be set at 640X480 or at 800X600. It fulfills the needs for higher graphics performance.

3. SETTING UP THE SYSTEM

This section describes pin assignments for the system's external connectors and the jumper settings.

- Overview
- System Settings

3.1 OVERVIEW

The AR-B1380/AR-B1380A is an all-in-one half size, Pentium single CPU board. This section provides the hardware jumper settings, the connectors' locations, and the pin assignments.

CAUTION: This CPU board doesn't support double-sided SIMM-type DRAM. It only supports single-sided SIMMs.

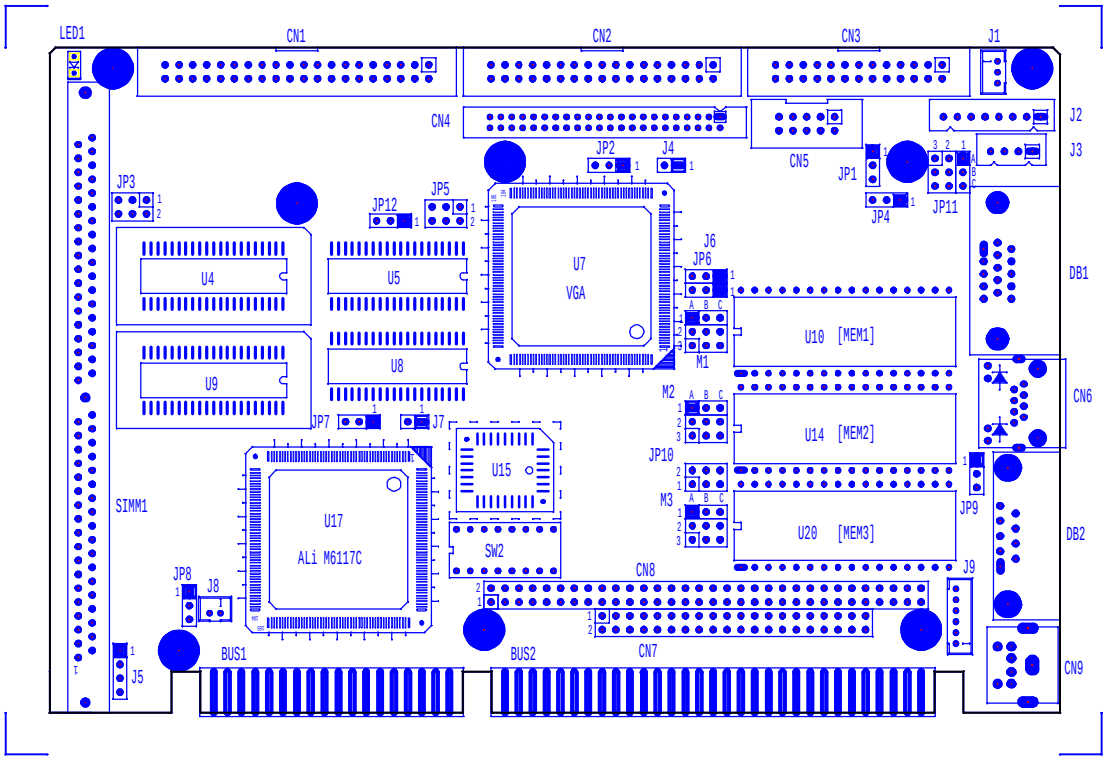


Figure 3-1 Jumper & Connector Placement

3.2 INDEX OF THE CONNECTORS AND JUMPERS

Name	Function		Page
CN1	Hard disk (IDE) connector		3-4
CN2	Floppy disk drive connector		3-5
CN3	Printer connector		3-5
CN4	2.00mm LCD panel display connector		33
CN5	RS-232C /RS-485 connector		3-13
CN6	RJ-45 header		3-6
CN7	PC/104 40-pin bus C&D		3-6
CN8	PC/104 64-pin bus A&B		3-6
CN9	PS/2 Mini-Din keyboard connector		3-9
DB1	Analog monitor (CRT) connector		32
DB2	Serial port A RS-232 connector		3-15
J1	3-pin JST touch screen connector		35
J2	8-pin JST power connector		3-10
J3	4-pin JST power connector		3-10
J4	HDD LED header		3-15
J5	External speaker header		3-10
J6	Power LED Header		3-15
J7	Reset header		3-10
J8	External battery header		3-11
J9	PS2/mouse connector		3-9
JP1/JP4	3 Pin RS-485 adapter selectors		3-14
JP2	3 Pin DE/E signal from M or LP		4-3
JP3	6 Pin CPU base clock selector		3-12
JP5	6 Pin LCD voltage selector		4-3
JP6	3 Pin 1MX8 EPROM selector		6-6
JP7	3 Pin PS/2 mouse selector		3-9
JP8	3 Pin battery charger selector		3-11
JP9	3 Pin RS-485 terminator selector		3-13
JP10	6 Pin S.S.D. &D.O.C. Selector		6-3
JP11	9 Pin RS-232/RS-485 selector for CN5		3-13
LED1	Power/Watchdog LED		3-16
M1~M3	Memory type setting		6-7
SIMM1	DRAM socket for SIMM memory socket		3-15
SW2	SW2-1 & SW2-2	Set the base I/O port address	6-2
	SW2-3 & SW2-4	Set the memory address	6-2
	SW2-5 & SW2-6	Set the drive number of solid state disk	6-4
	SW2-7 & SW2-8	Set the used ROM memory chips	6-5

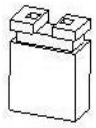
Table 3-1 Index of the Connectors and Jumpers

3.3 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

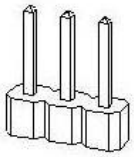
Jumper use:
Jumper caps are usually small plastic caps used to short two pins on a jumper block.

Most jumper caps look like this:



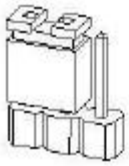
A Jumper Cap

Most jumper blocks look like this:

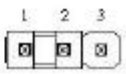


A 3 Pin Jumper Block

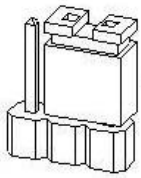
If the jumper is placed over pins one and two then 1-2 are ON.



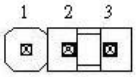
Jumper On Pins 1 + 2.



If the jumper is placed over pins two and three then 2-3 are ON.



Jumper On Pins 2 + 3.



Otherwise, the jumper can be left to the side or completely off the block to keep both 1-2 and 2-3 open/off.

We will show the locations of the AR-B1380/AR-B1380A jumper pins, and the factory-default settings.

CAUTION: Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

3.3.1 CN1: Hard Disk Drive Connector

A 40-pin header type connector (CN1) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 40-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use BIOS Setup program . The following table illustrates the hard disk drive's 40-pin connector pin assignments.

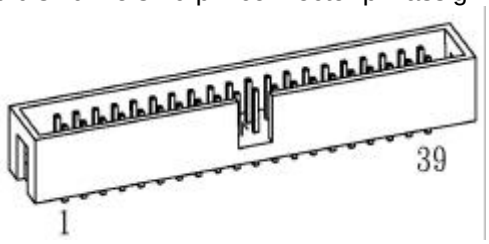


Figure 3-2 CN1: Hard Disk (IDE) Connector

Pin	Signal	Pin	Signal
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	VDOM
21	NOT USED	22	GROUND
23	-IOW	24	GROUND
25	-IOR	26	GROUND
27	-IORDY	28	HDALE
29	NOT USED	30	GROUND
31	IRQ 14	32	-IOCS16
33	HDA 1	34	NOT USED
35	HDA 0	36	HDA 2
37	/ HDCS0	38	/ HDCS1
39	/ HD LED	40	GROUND

Table 3-2 HDD Pin Assignment

3.3.2 CN2: Floppy Disk Drive Connector

The AR-B1380/AR-B1380A provides a 34-pin header type connector for supporting up to two floppy disk drives.

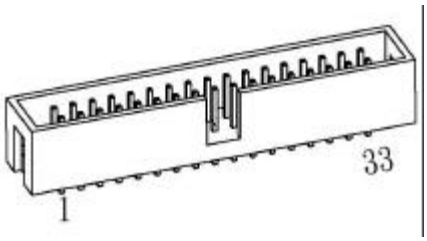


Figure 3-3 CN2: FDD Port Connector

Pin	Signal	Pin	Signal
1-33(odd)	GROUND	18	DIR
2	DRVEN 0	20	-STEP OUTPUT PULSE
4	NOT USED	22	/-WRITE DATA
6	DRVEN 1	24	/ WGATE
8	/ INDEX	26	/-TRK 0
10	/ MTR0	28	/-WRITE PROTECT
12	/DRV1	30	-READ DATA
14	/ DRV0	32	/HDSEL
16	/MTR1	34	DISKCHG

Table 3-3 FDD Pin Assignment

3.3.3 CN3: Parallel Port Connector

To use the parallel port, an adapter cable has connected to the CN3 (26-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B1380/AR-B1380A package. The connector for the parallel port is a 25 pin D-type female connector.

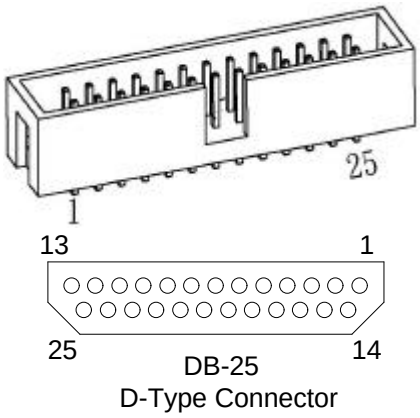


Figure 3-4 CN3: Parallel Port Connector

CN3	DB-25	Signal	CN3	DB-25	Signal
1	1	-Strobe	2	14	-Auto Form Feed
3	2	PD10	4	15	-Error
5	3	PD11	6	16	-Initialize
7	4	PD12	8	17	-Printer Select In
9	5	PD13	10	18	Ground
11	6	PD14	12	19	Ground
13	7	PD15	14	20	Ground
15	8	PD16	16	21	Ground
17	9	PD17	18	22	Ground
19	10	-Acknowledge	20	23	Ground
21	11	Busy	22	24	Ground
23	12	PS1	24	25	Ground
25	13	Printer Select	26	--	PRCG

Table 3-4 Parallel Port Pin Assignment

3.3.4 CN6: Ethernet RJ-45 Header

The system supports onboard network connectivity. To utilize this function, install the network driver from the utility diskette, and connect the cable to the following RJ-45 header.

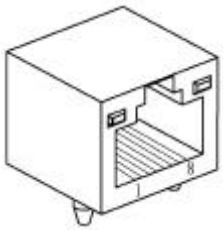


Figure 3-5 CN6: RJ-45 Header

J9:RJ45 HEADER	Signal	J9:RJ45 HEADER	Signal
1	TPTX+	8	No connection
2	TPTX-	9	No connection
3	TPRX+	10	No connection
4	No connection	11	LED -
5	No connection	12	LED +
6	TPRX-	13	LAN CG
7	No connection	14	LAN CG

Table 3-5 RJ-45 Pin Assignments

3.3.5 CN7 & CN8: PC/104 Connector

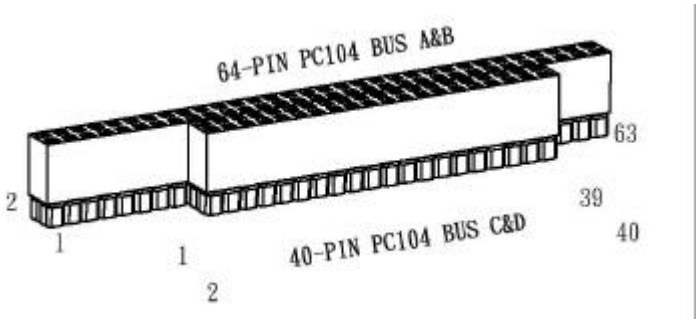


Figure 3-6 CN7&CN8: PC/104 Connector

(1) CN7: 40-Pin PC/104 Connector Bus C & D

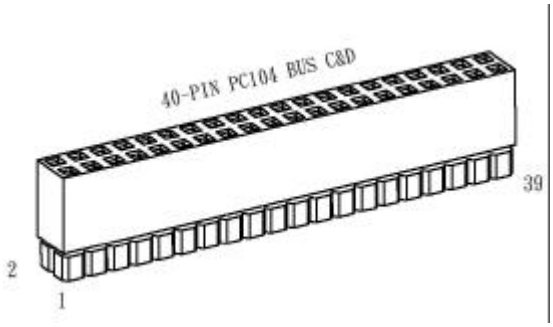


Figure 3-7 CN7: 40-Pin PC/104 Connector Bus C & D

(2) CN8: 64-Pin PC/104 Connector Bus A & B

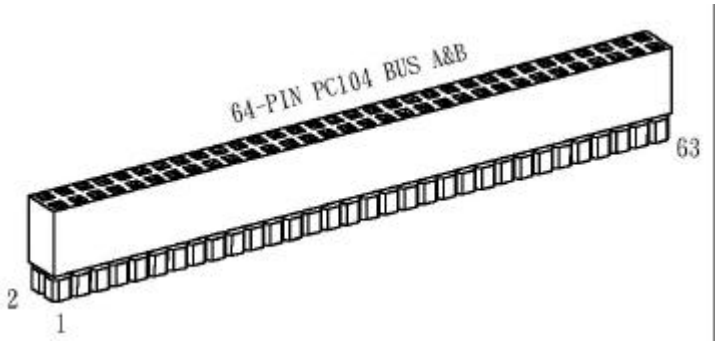


Figure 3-8 CN8: 64 Pin PC/104 Connector Bus A & B

(3) PC/104 Channel Signal Description

Name	Description
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset
SA0 - SA19 [Input / Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
LA17 - LA23 [Input/Output]	The Unlatched Address line run from bit 17 to 23
SD0 - SD15 [Input/Output]	System Data bit 0 to 15
BALE [Output]	The Buffered Address Latch Enable is used to latch SA0 - SA19 onto the falling edge. This signal is forced high during DMA cycles
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
IOCHRDY [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
-SMEMR [Output]	The System Memory Read is low while any of the low 1 mega bytes of memory are being used
-MEMR [Input/Output]	The Memory Read signal is low while any memory location is being read

Name	Description
-SMEMW [Output]	The System Memory Write is low while any of the low 1 mega bytes of memory is being written
-MEMW [Input/Output]	The Memory Write signal is low while any memory location is being written
DRQ 0-3, 5-7 [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
-DACK 0-3, 5-7 [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
AEN [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
-REFRESH [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
TC [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
SBHE [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus
-MASTER [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-MEMCS16 [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-IOCS16 [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
OSC [Output]	The Oscillator is a 14.31818 MHz signal used for the color graphic card
-ZWS [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

Table 3-6 I/O Channel Signal's Description

3.3.6 PS/2 Keyboard and Mouse

JP7: PS/2 Mouse Selector

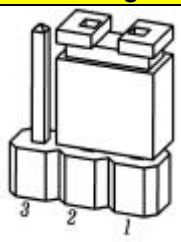
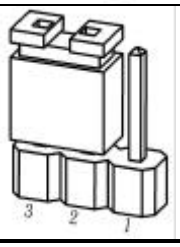
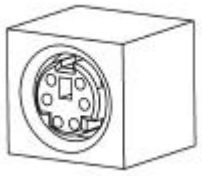
JP7	PS/2 Mouse Selector	Setting
1-2	IRQ12	
2-3 (Factory Preset)	PS/2 mouse	

Table 3-1 JP7: PS/2 Mouse Setting

Note: If you want to use PS/2 mouse, please select "2-3" for JP7, with which the PS/2 mouse device will occupy IRQ12. If "1-2" of JP7 is selected, IRQ12 can be configured for other devices.

CN9: 6-pin MiNi-Din PS/2 Keyboard Connector

CN9 is a Mini-DIN 6-pin connector with support for a PS/2 keyboard. This connector is also IBM-compatible with the keyboard adapter cable. When you use the PS/2 mouse, adjust JP7 to "2-3" and connect the adapter cable to CN9.

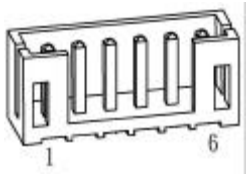


1. Data
2. N.C.
3. GND
4. VCC
5. Clock
6. N.C.

Figure 3-9 CN9: 6-Pin Mini Din Keyboard Connector

J9 PS/2 /Mouse Selector

A PC/AT compatible mouse can be used by connecting the provided adapter cable between J9 and the /mouse. The pin assignments of the J9 connector are as follows:



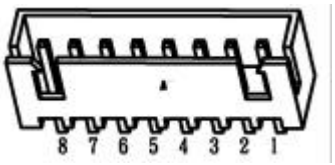
1 MSData
2 KBData
3. GND
4. VCC
5. MSclock
6. KBClock

Figure 3-10 J9: AUX. Keyboard Connector

3.3.7 Power Connector

(1) J2: 8-Pin Power Connector

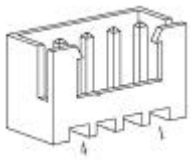
The J2 is an 8-pin power connector, you can directly connect the power supply to the on board power connector for stand alone applications.



1. GND
2. +5 VDC
3. +5 VDC
4. GND
5. GND
6. +12 VDC
7. –12 VDC
8. –5 VDC

Figure 3-2 J2: 8-Pin Power Connector

(2) J3: 4-Pin Power Connector

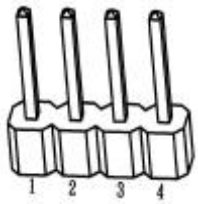


1. +5 VDC
2. GND
3. GND
4. 12 VDC

Figure 3-3 J3: 4-pin Power Connector

3.3.8 J5: External Speaker Header

Besides the on board buzzer, you can use an external speaker by connecting J5 header directly.

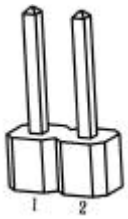


1. Speaker+
2. Speaker-
3. Speaker-
4. Speaker-

Figure 3-4 J5: External Speaker Header

3.3.9 J7: Reset Header

J7 is used to connect to an external reset switch. Shorting these two pins will reset the system.



1. Reset+
2. Reset-

Figure 3-5 J7: Reset Header

3.3.10 Board Battery Configuration

You may use either the onboard battery or connect an external battery to this board.

(1) JP8: External/Onboard Battery Selector

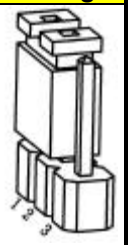
JP8	Battery Charger	Setting
1-2 (Factory Preset)	Rechargeable (Use of the onboard Battery)	
2-3	Non-rechargeable (Use of the external battery)	

Table 3-8 JP8: Battery Charger Selector

(2) J8: External Battery Connector

The J8 allows the users to connector an external 4.5 to 6 VDC battery to the AR-B1380/AR-B1380A. If the on-board battery is fully discharged, the SRAM disk will draw the battery current. The battery charger on AR-B1380/AR-B1380A doesn't source charge current to the external battery which connects to J8.

1 Battery+
2 Battery-

Figure 3-15 J8: External Battery Connector

3.3.11 JP3: CPU Base Clock Selector

The CPU base clock (Input clock) is twice as fast as the operating clock.

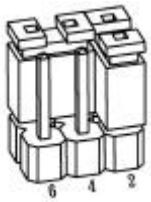
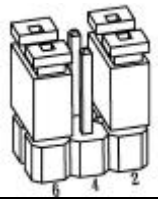
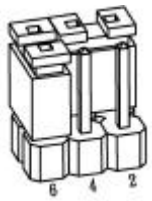
JP3	CPU Base Clock	Setting
1-2, 4-6	16.7 MHz	
1-2, 3-5	25 MHz	
1-2, 5-6	30 MHz	
1-3, 5-6 (Factory Preset)	33.3 MHz	
2-4, 5-6	37.5 MHz	
1-3, 2-4	40 MHz	

Table 3-9 JP1: CPU Base Clock Select

3.3.12 Serial Port

(1) JP11: RS-232/RS-485 Selector for CN5

The JP11 selects the on-board RS-232/RS-485 for COM B, if choose RS-232 connecting with CN7; if choose RS-485 connecting with J9.

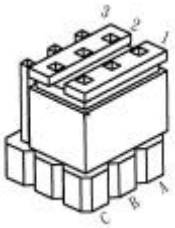
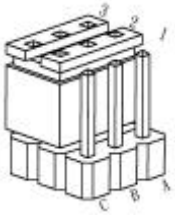
CN5: RS-232 or RS-485 Selector	Setting
CN5 is RS-485 compatible	1-2,4-5,7-8 
CN5 is RS-485 compatible (Factory Preset)	2-3,5-6,8-9 

Table 3-10 JP11: RS-232/RS-485 Select for CN5

(2) JP9: RS-485 Terminator Selector

RS-485 may need to be terminated when there are multiple blocks on one line.

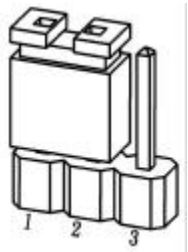
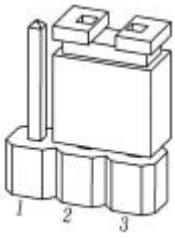
JP9	RS-485 Terminator	Setting
1-2	Enable	
2-3 (factory Preset)	Disable	

Table 3-11 JP9: RS-485 Terminator

(3) JP1 & JP4: External RS-485 Adapter Selector

JP1 and JP4 can be set independently. JP1 selects COMB port and JP4 selects COM A port. JP4 selects the external RS-485 for COMB port connecting with CN7. JP4 selects the external RS-485 for COMA connecting with DB2.

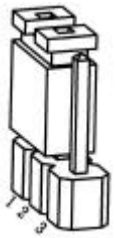
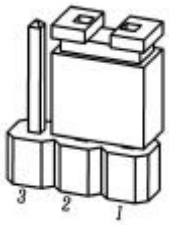
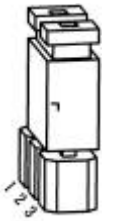
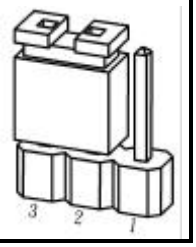
JP1/JP4	RS-485 Adapter Selector	JP1: CN5	JP4: DB2
1-2	Reserved for Acrosser's RS-485 Adapter		
2-3 (Factory Preset)	RS-232C		

Table 3-12 JP1 & JP4: External RS-485 Adapter Selectors

(4) CN5 & DB2: RS-232C Connector

There are two serial ports with an EIA RS-232C interface on the AR-B1380/AR-B1380A. COM A uses one on-board D-type 9-pin male connector (DB2) which is located at the top of the card, and COM B uses one 10-pin header (CN5). Use the BIOS Setup program to configure these two serial ports, and adjust the jumpers on JP1 and JP4.

CN5	DB2	Signal	CN7	DB2	Signal
1	1	-DCD	2	6	-DSR
3	2	RXD	4	7	-RTS
5	3	TXD	6	8	-CTS
7	4	-DTR	8	9	-RI
9	5	GND	10	--	Not Used

Table 3-13 Serial Port Pin Assignments

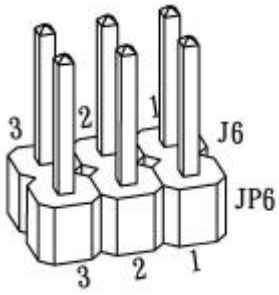
Note: CN5 can be configured for RS-232 or RS-485. When it is RS-485 compatible, you must set JP11 to "1-2, 4-5, 7-8" and JP1 to "1-2."

3.3.13 LED Headers and Indicator

This system provides LED headers and a LED indicator for the users to easily monitor the system's operation.

(1) J6: External Power LED Header

J6 is used to connect to the external power LED.



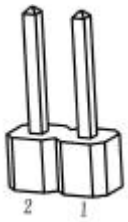
1 Power LED+
2 Power LED-
3 Power LED-

Figure 3-17 J6: External Power LED Header

Note: J6 & JP6 are aligned with each other. Please be careful with their orientation and pin locations during installation.

(2) J4: HDD LED Header

J4 is used to connect to the external Hard Disk LED.



1 LED+
2 LED-

Figure 3-18 J4: HDD LED Header

(3) LED1: Power/Watchdog LED

The AR-B1380/AR-B1380A provides a rectangular LED indicator to indicate the status of the Power/ Watchdog timer. LED1 is located at the upper-left corner of the board above the SIMM socket.

3.3.14 DRAM Configuration

There is 2MB DRAM onboard. For memory expansion, a SOJ socket and 72-pin SIMM socket are provided. The SIMM socket supports single-sided SIMM modules (Single-Line Memory Modules), which is designed to accommodate 256Kx36 bit to 4Mx36-SIMMs. This provides the user with up to 32MB of main memory. The 32-bit SIMM (without parity bit) also can be used on the AR-B1380/AR-B1380A board. There are six on-board memory configurations available. Please refer to the following table for details:

SIMM	Total Memory
1Mx32 (x36)	4MB
4Mx32 (x36)	16MB

Table 3-14 DRAM Configuration

4. CRT/LCD FLAT PANEL DISPLAYS

This section describes the configuration and installation procedure when using the LCD and CRT displays.

- Connecting the CRT Monitor
- LCD Flat Panel Displays
- Supported LCD Panels

4.1 DB1: CRT CONNECTOR

The DB1 is used to connect with a VGA monitor when you are using the on-board VGA controller as a display adapter. Pin assignments for the DB1 connector are as follows:

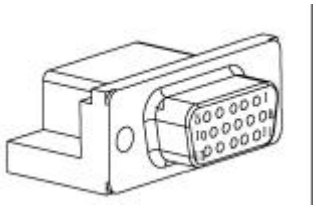


Figure 4-1 DB1: CRT Connector

DB1	Signal	DB1	Signal
1	Red	9	Not Used
2	Green	10	Ground
3	Blue	11	Not Used
4	Not Used	12	Not Used
5	Ground	13	Horizontal Sync
6	AGND	14	Vertical Sync
7	AGND	15	Not Used
8	AGND	--	

Table 4-1 CRT Connector Pin Assignments

4.2 LCD FLAT PANEL DISPLAY

This section describes the configuration and installation procedure for a LCD display. Skip this section if you are using a CRT monitor only. (AR-B1380 doesn't provide the LCD function).

Use the Flash Memory Writer utility to download the new BIOS file into the ROM chip to configure the BIOS default setting for different types of LCD panel. And then set your system properly and configure the AR-B1380A VGA module for the right type of LCD panel you are using.

If you are using a different LCD panel other than those listed, choose the type of LCD panel you are using. from the panel description column

The following shows the block diagram when using TK AR-B1380A for an LCD display.

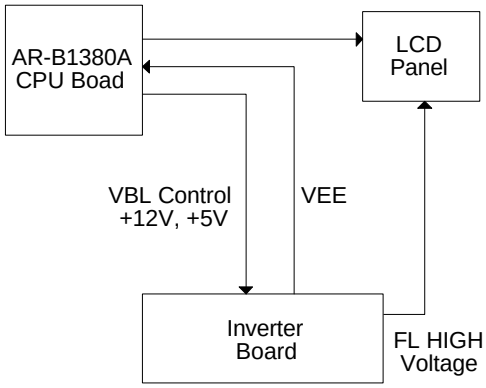


Figure 4-2 LCD Panel Block Diagram

This block diagram shows that the AR-B1380A still needs other components to be used for LCD panel. The inverter board provides the control for the brightness and the contrast of the LCD panel while the transfer is the one that supplies the high voltage to drive the LCD panel. Each item will be explained further in this section.

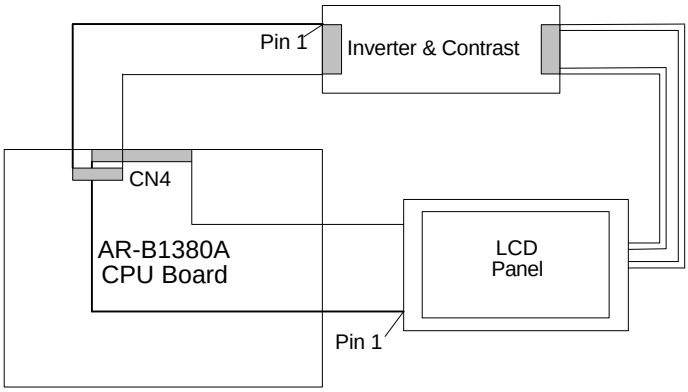


Figure 4-3 LCD Panel Cable Installation Diagram

NOTE: Be careful with the pin orientation when installing the connectors and the cables. A wrong connection can easily destroy your LCD panel. Pin 1 of the cable connector is indicated with a sticker and pin1 of the ribbon cable usually has a different color.

4.2.1 Inverter Board Description

The inverter board supplies the high voltage signals to drive the LCD panel by converting the 12 volt signal from the AR-B1380A into high voltage AC signal for LCD panel. It can be installed freely on the space provided over the VR board. If the VR board is installed on the bracket, you have to provide a place to install the inverter board into your system.

4.2.2 LCD Settings and Connectors

The AR-B1380A supports CRT color monitors, STN, Dual-Scan, TFT, monochrome and color panels. It can be connected to create a compact video solution for the industrial environment. 1MB of RAM on-boarded allows a maximum CRT resolution of 1024X768 and a LCD resolution of 640X480 with 64K colors. For different VGA display modes, your monitor must possess certain characteristics drives to display the mode you want.

(1) JP2: DE/E Signal from M or LP

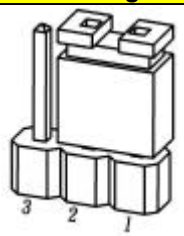
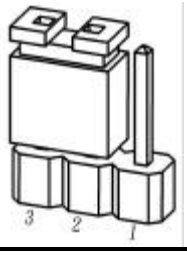
JP2	DE/M Signal	Setting
1-2 (Factory Preset)	DE/M	
2-3	E/LP	

Table 4-2 JP2: DE/E Signal from M or LP Select

(2) JP5: LCD Voltage Selector

JP5	LCD Voltage Selector	Setting
3-5, 4-6 (Factory Preset)	3.3 VDC	
1-3, 2-4	5 VDC	

Table 4-3 LCD Voltage Selector

(3) CN4: LCD Panel Display Connector

Attach a display panel connector to this 44-pin connector with pin assignments shown as below:

NOTE: AR-B1380 doesn't provide this function.

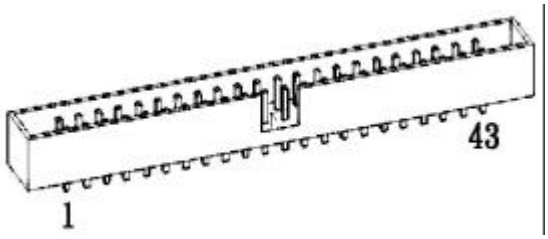


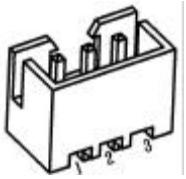
Figure 4-4 CN4: LCD Display Connector

Pin	Signal	Pin	Signal
1	GND	2	SHFCLK
3	GND	4	LP
5	FLM	6	GND
7	P0	8	P1
9	P2	10	P3
11	P4	12	P5
13	GND	14	P6
15	P7	16	P8
17	P9	18	P10
19	P11	20	GND
21	P12	22	P13
23	P14	24	P15
25	P16	26	P17
27	GND	28	P18
29	P19	30	P20
31	P21	32	P22
33	P23	34	GND
35	VLCD	36	VLCD
37	+12V	38	+12V
39	GND	40	GND
41	DE	42	ENABLK
43	GND	44	ENAVEE

Table 4-4 LCD Display Assignments

(4) J1: Touch Screen Connector

The J1 is a 3-pin JST connector connecting to the touch screen module to provide touch screen functionality.



1. RXD2F+
2. TXD2F
3. GND

Figure 4-5 J1: Touch Screen Connector

4.3 SUPPORTED LCD PANELS

At present, this VGA card can provide a solution with an inverter transfer board for the following list of standard LCD panels. Consult your Acrosser representative for new developments. When using other models of standard LCD panels in the market.

NO.	Manufacture	Model No.	Description
1	NEC	NL-6448AC30-10	TFT 9.4"
2	NEC	NL-6448AC32-10	TFT 10.2"
3	NEC	NL-6448AC33-10	TFT 10.4"
4	HITACHI	LMG5371	MONO 9.4" Dual Scan
5	HITACHI	LMG9200	DSTN 9.4"
6	HITACHI	LMG9400	DSTN 10.4"
7	ORION	OGM-640CN03C-S	DSTN 10.4"
8	SHARP	LQ10D321	TFT 10.4"

Table 4-5 LCD Panel Type List

CAUTION

1) If you want to use LCD panel, you must update the AR-B1380A's BIOS. Please contact Acrosser for the latest BIOS update.

2) If you need details to update the BIOS version or use other LCDs, please contact the sales department. The details about supported LCDs are listed at the Acrosser Web site, you can then download the suitable BIOS. The address is as follows:

http:\\www.acrosser.com

5. SOFTWARE INSTALLATION

This chapter describes the of the utility diskette installation procedure. The following topics are covered:

- Overview
- Utility Diskette
- Write Protect Function
- Watchdog Timer

5.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B1380/AR-B1380A CPU card. Please carefully read the details of the CPU card's hardware descriptions before installation, especially jumper settings, switch settings and cable connections.

The following lists the proper installation steps:

Step 1 : Read the CPU card's hardware description in this manual.

Step 2 : Install the SIMM module onto the CPU card.

Step 3 : Set the jumpers.

Step 4 : Make sure that the power supply connected to your passive CPU board backplane is turned off.

Step 5 : Plug the CPU card into a free AT-bus slot or PICMG slot on the backplane and secure it in place with a screw to the system chassis.

Step 6 : Connect all necessary cables. Make sure that the FDC, HDC, serial and parallel cables are connected to pin 1 of the related connector.

Step 7 : Connect the hard disk/floppy disk flat cables from the CPU card to the drives. Connect a power source to each drive.

Step 8 : Plug the keyboard into the keyboard connector.

Step 9 : Turn on the power.

Step 10: Configure your system with the BIOS Setup program then re-boot your system.

Step 11: If the CPU card does not work, turn off the power and read the hardware description carefully again.

Step 12: If the CPU card still does not perform properly, return the card to your dealer for immediate service.

5.2 UTILITY DISKETTE

AR-B1380 provides one diskette with the SSD utility and manual file

AR-B1380A provides two utility diskettes: DISK1 for the WIN31 and MS-DOS VGA drives; Disk2 for the LAN drover, SSD utilities and the manual file. If your operation system is neither WIN31 nor WIN95, please contact Acrosser for the proper VGA drivers. Also you may refer to the Readme.txt for any troubleshooting before installing the driver.

5.2.1 VGA Driver

(1) WIN 3.1 Driver
For the WIN31 operating system, you must decompress the compress file in the DOS mode. And then follow these steps:

Step 1: Execute the SETUP.EXE file in the DOS mode.
A:\>SETUP

Step 2: The screen shows the chip type. Press any key to enter the main menu.

Step 3: There are nine items in the main menu. Select the <Windows Version 3.1> item. Notice the function key defined. Press [ENTER] to select the <All Resolutions>. When this line appears with the [*] symbol, it means this item is selected. Press [End] to start the installation.

Step 4: The screen will show the dialog box to ask you to type the WIN31's path. The default is C:\WINDOWS.

Step 5: Follow the onscreen messages. When the setup is completed, the system will generate the message as follows.

Installation is done!

Change to your Windows directory and type SETUP to run the Windows Setup program. Choose one of the new drivers marked with an *. Please refer to the User's Guide to complete the installation.

Step 6: Press [Esc] key to return to the main menu, and re-press [Esc] again to return to the DOS mode.

Step 7: Enter WIN31. You can find the <Chips CPL> icon located in the {CONTROL PANEL} group.

Step 8: Adjust the <Refresh Rate>, <Cursor Animation>, <Font size>, <Resolution>, and <Big Cursor> functions.

5.2.2 SSD Utility

To support the AR-B1380/AR-B1380A solid state disk's operations, the following files have been provided on the enclosed diskette's directory <SSD>.

(A) WD1380.EXE/WD6117C.EXE

WD1380.EXE : These two programs demostrates how to enable and trigger the watchdog timer.
WD6117C.EXE: It allows you to test the <TIME-OUT & RESET> function when the watchdog timer is enabled.
Note: Please refer to Section 5.4 for details when using the watchdog timer.

(B) WD6117C.CPP

WD1380.EXE : This is the source file of the "WD6117C."

(C) WP1380.EXE

WP1380.EXE : This program demonstrates how to enable and disable the software write protected function. It also shows the current protect mode of write or read only memory.

(D) RFG.EXE

RFG.EXE : This program is used to generate the ROM pattern files in a binary format. Each ROM pattern file has the same size as the FLASH or EPROM and can be easily programmed on to the FLASH with an on-board programmer or on to EPROM with any EPROM programmer. If you have specified a DOS drive in the *.PGF file, RFG will generate bootable ROM pattern files for the EPROM or FLASH disk. The RFG supports the following commands DOS:MS-DOS, PC-DOS, DR-DOS, and X-DOS.

NOTE: If you want to use AR-B380/AR-B1380A with any DOS which is not supported by RFG, please send your requirement to Acrosser Technology Co., Ltd. or contract your local sales representative.

The RFG.EXE provided in the utility diskette is a program that converts the files you list in the PGF and convert them into a ROM pattern file. The RFG will determine how many EPROMs are needed and generate the same number of ROM pattern files. These ROM pattern files are named with the name assigned by the ROM_NAME in the PGF and the extension names are *.R01, *.R02 ...etc. To generate ROM pattern files.
The ROM File Generator main menu will be displayed on the screen. There are 7 options on the main menu. They serve the following functions:

Quit to DOS
Quits and exits to the DOS

OS Shell
Exits from the RFG temporarily to the DOS prompt. Type <EXIT> to return to the RFG main menu.

Load PFG File
If this option is used, the RFG will prompt you for the PGF file name. This option is useful if you have not previously entered a PGF name or you wish to use a different PGF file. The RFG will check and display the PGF filename, ROM pattern file name, EPROM capacity, DOS version and the number of ROM pattern files that will be generated.

Type Current PGF File
This option instructs the RFG to use the DOS type command to display the contents of the current PGF file.

Generate ROM File(s)
If there is no mistake in your *.PGF file, then this menu option will generate ROM pattern files. The number of ROM pattern files generated by the RFG will depend on the total capacity needed by your files. For instance, if 3 files are generated, then you will need to use 3 EPROMs (The size depends upon the number stated in your PGF). The ROM pattern files will have the same file names, but will have different extension names. For example:
TEST.R01, TEST.R02, TEST.R03 ..etc.

Display Error in PGF File
This option displays errors that were detected in your PGF.

Help to PGF File

This option gives information on how to write a PGF file and how to generate ROM pattern files. An example PGF is also included.

Move the reverse video bar to <Generate ROM File(s)> then press [ENTER]. The ROM pattern file is a binary file. The file size will be the same size as the EPROM that you assigned in the PGF. For example, if you are using 128KX8 EPROM memory chips, then the size of ROM patterns file will be 131072 bytes. For other chips the file size will be:

64KX8 EPROM----65536 bytes
256KX8 EPROM –262144 bytes
512KX8 EPROM---524288 bytes
1MX8 EPROM -----1048576 bytes

(E) RFGDEMO.PGF

RFGDEMO.PGF This file provides a sample PROGRAM GROUP FILE which illustrates how to create ROM pattern files correctly.

The PGF is an ASCII text file that can be created by using any text editor, word processor or DOS <COPY CON> command. The PGF lists what files will be copied and if DOS is going to be copied. This file can have any DOS filename, but the extension name must be *.PGF. For example,the followings are valid filenames.

RFGDEMO.PGF
MYRFG.PGF
MSDOS.PGF
…

An examples of the *.PGF file is as follows.

```
ROM_NAME=TEST1; ROM pattern file name is TEST1
;The output file names will be TEST1.R01, TEST1.R02..etc.
DOS_DRIVE=C:              ; DOS system drive unit is drive C:
;If user does not want to copy DOS
;system files onto the ROM disk
;write as DOS_DRIVE=NONE
ROM_SIZE=128        ;128 means 128KX8 (27C/29F010) EPROM size used
;256 means 512KX8 (27C/29F020) EPROM size used
;512 means 512KX8 (27C/29F040) EPROM size used
;1024 means 1MX8 (27C080) EPROM size used
```

The following two files are options which depending on whether you want the ROM disk to be bootable or not.

CONFIG.SYS
AUTOEXEC.BAT

```
;Below are user's files
A:\USER1.COM  ; File USER1.COM on root of drive A:
USER2.EXE     ; File USER2.EXE on current directory & drive
C:\TTT\USER3.TXT ; File USER3.TXT on sub-directory TTT of drive C:
```

Note: Anything appearing after a " ;" semicolon is considered a text note that does not affect the PGF file, but it is a good organizational idea to keep these notes for future use.0

5.3 WRITE PROTECT FUNCTION

The AR-B1380/AR-B1380A provides hardware and software write protect functions for small page 5V FLASH disks and only software write protected functions for SRAM disks. This is to prevent your data on 5V FLASH or SRAM disks from accidental ok deletion or overwrite. If your FLASH/SRAM disk is write protected, any write operation to the protected FLASH/SRAM disk will get a write protect error:

```
Write protect error writing drive A
About, Retry, Fail?
```

5.3.1 Hardware Write Protect

To enable the hardware protect function for small page 5V FLASH disk, please refer to the "Switch Setting".

5.3.2 Software Write Protect

If you need the write protect function and sometimes you have to write or update data on your FLASH/SRAM disk, you can use the software write protect instead of hardware write protect. The software write protect function is enabled or disabled by writing a data to an I/O port.

5.3.3 Enable the Software Write Protect

Writes data 80h to the base port+0 address

Example 1: (in assembly language)

```
MOV DX, 210H    ; If the base I/O address is 210H
MOV AL, 80H     ; Enable byte = 80h
OUT DX, AL
```

Example 2: (in BASICA language)

```
OUT &H210, &H80; REM If the base I/O address is 210h
```

Example 3: (in Turbo C language)

```
outportb(0x210,0x80);/*If the base I/O address is 210h*/
```

5.3.4 Disable the Software Write Protect

Writes data 0 to the base port+0 address

Example 1: (in assembly language)

```
MOV DX, 210H    ; If the base I/O address is 210h
MOV AL, 00H     ; Disable byte=00h
OUT DX, AL
```

Example 2: (in BASICA language)

```
OUT &H210, &H00; REM If the base I/O address is 210h
```

Example 3: (in Turbo C language)

```
outportb(0x210,0x00);/*If the base I/O address is 210h*/
```

5.4 WATCHDOG TIMER

This section describes how to use, disable, enable, and trigger the Watchdog Timer.

AR-B1380/AR-B1380A provides two methods for the users to utilize the watchdog timer function. One is the watchdog timer built in the chipset, which makes use of the CPU's registers to use the watchdog timer. The other is the watchdog timer program programmed by Acrosser which helps you to use the watchdog timer through the use of the IRQ11 and IRQ15.

The SSD directory in the diskette includes the watchdog timer utility files, "WD1380.EXE," WD6117C.EXE," and WD6117C.CPP." "WD6117C.EXE" and WD6117C.CPP" are ALI M6117C's built-in watchdog timer program. "WD6117C.EXE" demonstrates how to set/enable/disable/trigger the watchdog timer. "WD6117C" is the source file of the "WD6117C." The other is "WD1380.EXE" programmed by Acrosser. You may choose either the onchip watchdog timer or Acrosser's program to utilize the watchdog timer.

5.4.1 Acrosser's Watchdog Timer Program

The AR-B1380/AR-B1380A is equipped with a programmable time-out period watchdog timer. You can use this program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger it every time before it times out. If your program fails to trigger or disable this timer before it times out because of a system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be from 3 to 42 seconds.

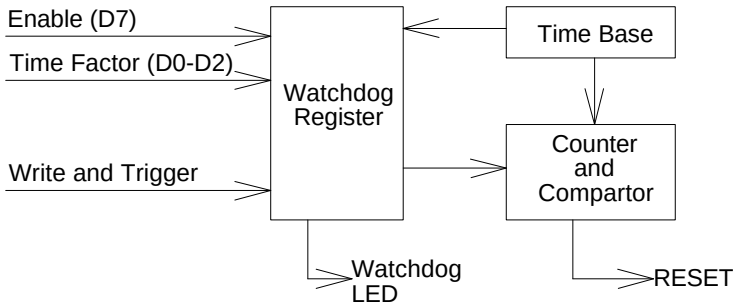


Figure 5-1 Watchdog Block Diagram

(1) Set up the Watchdog Timer by IRQ15/IRQ11

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system or trigger the IRQ15 signal to tell your program that the watchdog has timed out.

The factor of the watchdog timer time-out constant is approximately 6 seconds. The period for the watchdog timer time-out period is between 1 to 7 timer factors. If you want to reset your system when the watchdog times out, the following table lists the relation of timer factors between time-out period.

Time Factor	Time-Out Period (Seconds)
80H	3
81H	6
82H	12
83H	18
84H	24
85H	30
86H	36
87H	42

Table 5-1 Time-Out Setting

If you want to generate an IRQ15 signal to warn your program when the watchdog times out, the following table lists the relation of the timer factors between time-out periods. And if you use the IRQ15 signal to warn your program when the watchdog timer times out, please enter the BIOS Setup, in the <Peripheral Setup> menu, set the two items <OnBoard PCI IDE> and <IDE Prefetch> to ***Primary***.

Time Factor	Time-Out Period (Seconds)
0C0H	3
0C1H	6
0C2H	12
0C3H	18
0C4H	24
0C5H	30
0C6H	36
0C7H	42

Table 5-2 Time-Out Setting

If you want to generate an IRQ11 signal to warn your program when the watchdog times out, the following table lists the relation of timer factors between time-out periods. And if you use the IRQ11 signal to warn your program when the watchdog times out, please enter the BIOS Setup, in the <Peripheral Setup> menu, set the two items <OnBoard PCI IDE> and <IDE Prefetch> to ***Primary***.

Time Factor	Time-Out Period (Seconds)
0E0H	3
0E1H	6
0E2H	12
0E3H	18
0E4H	24
0E5H	30
0E6H	36
0E7H	42

Table 5-3 Time-Out Setting

NOTE

1. If you program the watchdog to generate an IRQ15 or IRQ11 signal when it times out, you should initial an IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too.

2. Before you initialize the interrupt vector of IRQ15/IRQ11 as well as enable the PIC, please enable the watchdog timer in advance. Otherwise, the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

(2) Enable the Watchdog Timer

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog register whose address is 214H or Base Port. The following is a BASICA program which demonstrates how to enable the watchdog timer and set the time-out period at 24 seconds.

```
1000    REM Points to command register
1010    WD_REG% = 214H
1020    REM Timer factor = 84H (or 0C4H)
1030    TIMER_FACTOR% = %H84
1040    REM Output factor to watchdog register
1050    OUT WD_REG%, TIMER_FACTOR%
  .,etc.
```

(3) Trigger the Watchdog Timer

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in the next trigger. Below is a BASICA program which demonstrates how to trigger the watchdog timer:

```
2000    REM Points to command register
2010        WD_REG% = 214H
2020    REM Timer factor = 84H (or 0C4H)
2030        TIMER_FACTOR% = &H84
2040    REM Output factor to watchdog register
2050        OUT WD_REG%, TIMER_FACTOR%
  .,etc.
```

(4) Disable Watchdog Timer

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
3000    REM Points to command register
3010        WD_REG% = BASE_PORT%
3020    REM Timer factor = 0
3030        TIMER_FACTOR% = 0
3040    REM Output factor to watchdog register
3050        OUT WD_REG%, TIMER_FACTOR%
  ., etc.
```

5.4.2 Built-in Watchdog Timer

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system or trigger an IRQ or NMI signal to tell your program that the watchdog has timed out. The time-out period can be programmed to be 30.5£ seconds to 512 seconds with 30.5 £ seconds per step.

The following are the watchdog timer registers:

- Index 37H : WD Enable Register
- Index 38H : WD Report Register
- Index 39H, 3AH, 3BH : WD 24-bit Timer Counter
- Index 3CH : WD Status Register

(1) INDEX 37H: WD Enable Register

This register is used to enable or disable the watchdog timer.

Bit 7	Reserved. Please do not set this bit. In the old version M6117C data sheet, this bit is counter read mode.
Bit 6=0	Disable the watchdog timer
Bit 6=1	Enable the watchdog timer
Bit 5-0	Other function. Please do not modify these bits.

5.4.3 INDEX 38H: WD Report register -

This register is used to select the watchdog report when the watchdog times out.

Bit 7-4	Watchdog Timer Time-out Report Signal Select
0000	No output signal
0001	IRQ3 selected
0010	IRQ4 selected
0011	IRQ5 selected
0100	IRQ6 selected
0101	IRQ7 selected
0110	IRQ9 selected
0111	IRQ10 selected
1000	IRQ11 selected
1001	IRQ12 selected
1010	IRQ14 selected
1011	IRQ15 selected
1100	NMI selected
1101	System reset selected
1110	No output signal
1111	No output signal
Bit 3-0	Other function. Please do not modify these bits.

Note

1) If you program the watchdog to generate an IRQ signal when it times out, you should initialize the IRQ interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable the CPU to process this interrupt. An interrupt service routine is required too.

2) Before you initiate the interrupt vector of the IRQ and enable the PIC, please enable the watchdog timer previously. Otherwise the watchdog timer will generate an interrupt at the time the watchdog timer is enabled.

(3) INDEX 39H, 3Ah, and 3Bh:WD TIMER COUNTER(24 bits) -

These registers are used to set the desired counter for the watchdog to count down. The time base of each count is 30.5£ sec.

INDEX	3Bh	3Ah	39h
Data Bit	D7 ..D0	D7 ..D0	D7 ..D0
24-bit Counter	D23 ..D16	D15 ..D8	D7 ..D0

For example:

INDEX			Watchdog Timer
3Bh	3Ah	39h	
00h	00h	01h	30.5 £ sec
00h	00h	02h	61.0 £ sec
00h	01h	00h	7.8 m sec
00h	02h	00h	15.6 m sec
01h	00h	00h	2 sec
02h	00h	00h	4 sec
0FFh	0FFh	0FFh	512 sec

(4) INDEX 3Ch: Timeout Status & Reset Watchdog

Bit 7(read only)	0: Timer timeout not happened
	1: Timer timeout happened
Bit 5	Write this bit "1" to reset timer The value on this bit has no meaning.
Bit 6, Bit 4-0	Other function. Please do not modify these bits.

(5) Basic Operation: Programming Watchdog

If you would like to access the M6117C configuration register, you need to unlock the register at first and lock it again after finishing the operation.

a) Unlock Configuration Register

```
Mov     al, 13h
Out     22h, al
Nop
Nop
Mov     al, 0c5h
Out     23h, al
Nop
Nop
```

b) Lock Configuration Register

```
Mov     al, 13h
Out     22h, al
Nop
Nop
Mov     al, 00h
Out     23h, al
Nop
Nop
```

c) Read the Value in the Configuration Register

Example 1: Read data from INDEX 3Ch

```
Unlock_Cfg_Reg      ;Unlock configuration register
Mov     al, 3ch     ;Points to index 3ch
Out     22h, al
Nop
Nop
In      al, 23h     ;Read out
Nop
Nop
Push    ax          ;Save to stack
Lock_Cfg_Reg        ;Lock configuration register
Pop     ax          ;Restore ax and result in al register
```

d) Write Data to Configuration Register

Example 1: Write data 68h to INDEX 3Bh

```
Unlock_Cfg_Reg      ;Unlock configuration register
Mov     al, 3bh     ;Points to index 3bh
Out     22h, al
Nop
Nop
Mov     al, 68h
Out     23h, al     ;Write data
Nop
Nop
Lock_Cfg_Reg        ;Lock configuration register
```

6. SOLID STATE DISK

The section describes the various type SSD installation steps as follows. This chapter describes the procedure of the installation. The following topics are covered:

- Overview
- Switch Setting
- Jumper Setting
- ROM Disk Installation

6.1 OVERVIEW

The AR-B1380A provides three 32-pin JEDEC DIP sockets which may be populated with up to 3MB of EPROM or 1.5MB of FLASH or 1.5MB of SRAM disk. It is ideal for diskless systems, high reliability and/or high speed access applications, as a controller for industrial or line test instruments, etc.

If small page (less or equal to 512 bytes per page) 5V FLASHs were used, you could format FLASH disk and copy files onto FLASH disk just like using a normal floppy disk. You can use all of the related DOS command (such as COPY, DEL ..etc.) to update files on the 5V FLASH disk.

The write protect function allows you to prevent your data on small page 5V FLASH or SRAM disk from accidental deletion or overwrite.

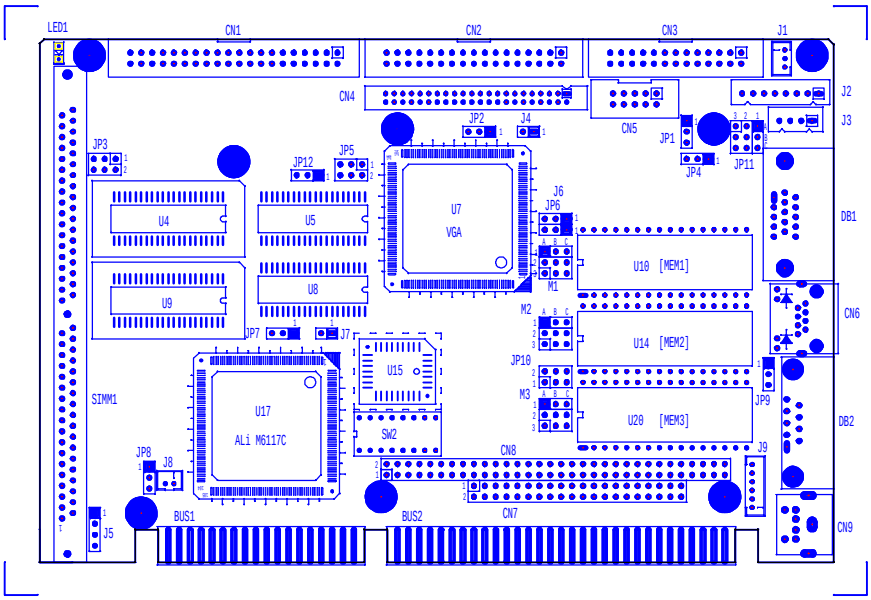
Data retention of SRAM is ensured by an on-board Lithium battery or an external battery pack that could be connected to the AR-B1380/AR-B1380A.

6.2 SWITCH SETTING

We will show the locations of the AR-B1380/AR-B1380A switch, and the factory-default settings.

CAUTION: Make sure the jumper settings and the switch setting are correct before starting up the system.

Figure 0-1 Switch & SSD Type Jumper Location



6.2.1 Overview

There is one DIP Switch(SW2) located on the AR-B1380/AR-B1380A. It performs the following functions:

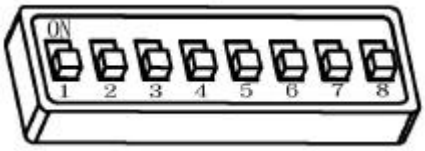


Figure 0-2 SW2: Switch Select

SW2-1& SW2-2	Set the base I/O port address
SW2-3 & SW2-4	Set the memory address
SW2-5 & SW2-6	Set the drive number for the solid state disks
SW2-7 & SW2-8	Set the ROM memory chips

6.2.2 SW2-1 & SW2-2: I/O Port Address Setup

SW2-1 & SW2-2 are provided to select one of the four base port addresses for the watchdog timer and the solid state disk. The AR-B1380/AR-B1380A occupies 6 I/O port addresses. Followings state selections of base port address. The following table lists the base port address selections for the solid state disks and watchdog timer.

SW2-1	SW2-2	Solid State Disk	Watchdog
OFF	OFF	210–213H	214-215H
OFF	ON	290-293H	294-295H
ON	OFF	310-313H	314-315H
ON	ON	390-393H	394-395H
X	X		76H-77H

Table 0-1 I/O Port Address Select

6.2.3 SSD & D.O.C. Setup

Before you are going to set up S.S.D. or D.O.C, you must adjust the settings of JP10 and SW2-3 & SW2-4. JP10 is a 6-pin jumper located between M3. It is used to select the SSD or DOC memory that the system is being installed. SW2-3 & SW2-4 are used to select the memory base address. The AR-B1380/AR-B1380A's SSD firmware occupies 8KB of memory. You must select an appropriate address so that the AR-B1380/AR-B1380A will not conflict with the memory installed on other add-on memory cards. Additionally, be sure not to use shadow RAM area or EMM driver's page frame in this area.

JP10 &SW2-3/SW2-4: SSD & DOC Setup

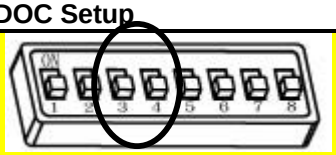
JP10	 SW2-3	SW2-4	S.S.D	D.O.C
1-2, 3-4	OFF	OFF	C800H	---
1-2, 3-4	OFF	ON	CC00H	---
1-2, 3-4	ON	OFF	D800H	---
1-2, 3-4	ON	ON	DC00H	---
3-4, 5-6	OFF	OFF	C800H	CA00H
3-4, 5-6	OFF	ON	CC00H	CE00H
3-4, 5-6	ON	OFF	D800H	DA00H
3-4, 5-6	ON	ON	DC00H	DE00H

Table 0-2 S.S.D./D.O.C. Firmware Address Selectors

If you are not going to use the solid state disk (S.S.D.), you can use BIOS setup program to disable the S.S.D. under a BIOS. The AR-B1380A will not occupy any memory address if the SSD BIOS is disabled.

If you are going to install the EMM386.EXE driver, please use the [X] option to prevent EMM386.EXE from using the particular range of segment address as an EMS page which is used by AR-B1380A. For example, write a statement in the CONFIG.SYS file as follow: (If the memory configuration of AR-B1380/AR-B1380A is C800:0)

DEVICE=C:\DOS\EMM386.EXE X=C800-C9FF

6.2.4 SW2-5 & SW2-6: SSD Drive Number Selector

The AR-B1380/AR-B1380A's SSD can simulate one or two disk drives. You can assign the drive letter of the AR-B1380/AR-B1380A by configuring SW2-5 & SW2-6.

You can make the computer to boot from SSD by copying DOS boot files into the SSD. If your SSD does not have abootable os., the computer will boot from your hard disk or floppy disk. In this condition, the SSD BIOS of AR-B1380/AR-B1380A will set the drive letter of the SSD to the desired drive letter automatically.

The SSD BIOS will simulate one disk drive when only (FLASH) EPROM or SRAM (starting from MEM1 socket) is installed. The drive numbers with respect to the switch setting when the AR-B1380/AR-B1380A simulates single disk drives.

SW2-5	SW2-6	Occupies floppy disk number (SSD)
OFF	OFF	0 or 1 (Note 1)
ON	OFF	0 or 2 (Note 2)
OFF	ON	0
ON	ON	0

Table 0-3 SSD Drive Number

NOTE

1. If there is no Dos on this SSD, the disk number will 1 (B:). If any DOS is found by the AR-B1380/AR-B1380A SSD BIOS, the disk number will be 0 under advanced cmos setup menu, you can change the disk number from 0(A:) to 1(B) of network at the first boot device by pressing the <ESC> during system bootup. (A:) But, you can change the disk number from 0 to 1 by pressing the <ESC> key during system bootup.

2. If there is no Dos on this SSD, the disk number will be 2 (C: or D: or ..). If any Dos is found by the AR-B1380/AR-B1380A SSD BIOS, the disk number will be 0 under advanced cmos setup menu, you can change the disk number from 0(A:) to 1(B) of network at the first boot device by pressing the <ESC> during system bootup.

(1) Simulate 2 Disk Drive

When (FLASH) EPROM and SRAM are both used on the AR-B1380/AR-B1380A, or you only have installed SRAM that does not start from the MEM1 socket, the AR-B1380/AR-B1380A will simulate two disk drives. The drive numbers respect to those switch settings when AR-B1380/AR-B1380A simulates two disk drives.

SW2-5	SW2-6	Occupies floppy disk number	
		FLASH (EPROM)	SRAM
OFF	OFF	0 or 1 (Note 1)	2
ON	OFF	0 or 2 (Note 2)	3
OFF	ON	0	1
ON	ON	0	2

Table 0-4 SSD Drive Number when Simulating 2 Disk Drives

NOTE

1) If there is no DOS on this SSD, the disk number will be 1 (B:). If any DOS is found by the AR-B1380/AR-B1380A SSD BIOS, the disk letter will be 0 (A:). under advanced cmos setup menu, you can change the disk number from 0(A:) to 1(B) of network at the first boot device by pressing the <ESC> during system bootup.

2) If there is no DOS on this SSD, the disk number will be 2 (C: or D: or ...). If any DOS is found by the AR-B1380/AR-B1380A SSD BIOS, the disk number will be 0 (A:). under advanced cmos setup menu, you can change the disk number from 0(A:) to 1(B) of network at the first boot device by pressing the <ESC> during system bootup.

(2) Disk Drive Name Arrangement

If any logical hard disk drives exist in your system, there will also be a different disk number depending on which version DOS you are using.

The solid state disk drive number with there respective DOS drive designation are listed in table as follows. The solid state disk drive number is changeable as the DOS version. The following table expresses the variety.

Condition	Floppy disk No.				Logical hard disk			
	0	1	2	3	1	2	3	4
No Logical hard disk	A:	B:	C:	D:	--	--	--	--
1 Logical hard disk	A:	B:	C:	D:	E:	--	--	--
2 Logical hard disk	A:	B:	C:	D:	E:	F:	--	--
3 Logical hard disk	A:	B:	C:	D:	E:	F:	G:	--
4 Logical hard disk	A:	B:	C:	D:	E:	F:	G:	H:

Table 0-5 SSD Drive Number for DOS Version before 5.0

Condition	Floppy disk No.				Logical hard disk			
	0	1	2	3	1	2	3	4
No Logical hard disk	A:	B:	C:	D:	--	--	--	--
1 Logical hard disk	A:	B:	D:	E:	C:	--	--	--
2 Logical hard disk	A:	B:	E:	F:	C:	D:	--	--
3 Logical hard disk	A:	B:	F:	G:	C:	D:	E:	--
4 Logical hard disk	A:	B:	G:	H:	C:	D:	E:	F:

Table 0-6 SSD Drive Number for DOS Version 5.0 and Newer

6.2.5 SW2-7 & SW2-8: ROM Type Select

SW2-7 & SW2-8 are used to select the of ROM disk section memory type

SW2-7	SW2-8	EPROM Type
OFF	OFF	UV EPROM (27Cxxx)
ON	OFF	5V FLASH 29Fxxx (*Note)
OFF	ON	5V FLASH (29Cxxx & 28Eexxx)
ON	ON	12V FLASH (28Fxxx)

Table 0-7 ROM Type Select

NOTE: It is also used to perform the hardware write protection of the small page 5V FLASH (29Cxxx or 28EExxx) disk.

6.3 M1-M3: MEMORY TYPE SETTINGS

Before installing the memory into memory sockets MEM1 through MEM3 (U31, U32 and U33 respectively), you have to configure the memory type which will be used (ROM/RAM) on the AR-B1380/AR-B1380A. Each socket is equipped with an jumper to select the memory type.

You can configure the AR-B1380/AR-B1380A as a (FLASH) EPROM disk (ROM only), a SRAM disk (SRAM only) or a combination of (FLASH) EPROM and SRAM disk.

It is not necessary to insert memory chips into all of the sockets. The number of SRAM chips required depends on your RAM disk capacity. The number of EPROM chips required depends on the total size of files that you plan to copy onto the ROM disk and whether or not it will be bootable.

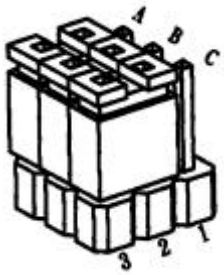
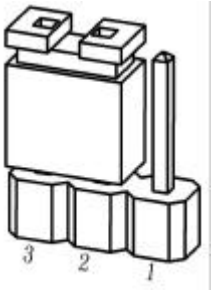
Insert the first memory chip into MEM1 if you are going to configure it as a ROM or SRAM disk. If you use a combination of ROM and RAM, then insert the (FLASH) EPROM chip starting with the MEM1, and insert the SRAM chips starting from the first socket which is configured as SRAM.

- M1:is used to configure the memory type of MEM1
- M2:is used to configure the memory type of MEM2
- M3:is used to configure the memory type of MEM3

CAUTION: When the power is turned off, please note the following precautions.

1) If your data has been stored in the SRAM disk, do not change the jumper position or data will be lost.

(2) Make sure jumpers are set properly. If you mistakenly set the jumpers for SRAM and you have EPROM or FLASH installed, the EPROM or FLASH will drain the battery's power.

Function	M1-M3 Setting	JP6 Setting
1MX8 EPROM (ONLY)		2-3 

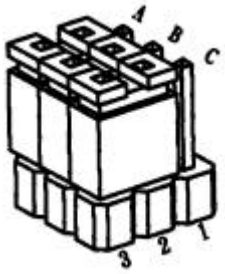
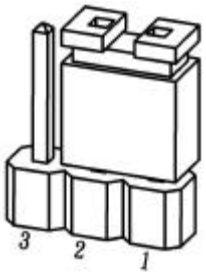
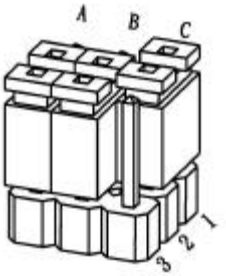
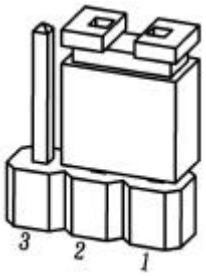
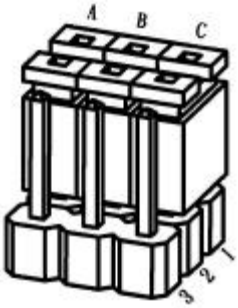
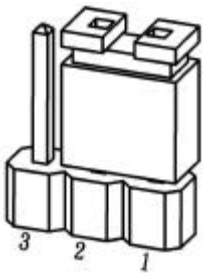
EPROM: 128Kx8, 256Kx8, 512Kx8 **5V/12V FLASH** (64Kx8M, 128Kx8, 256Kx8) (Factory Preset)		
5V FLASH (512K*8 only)		
SRAM only		

Table 0-8 M1~M3 & JP6: Memory Type Setting

Note: J6 and JP6 are aligned with each other. Please be careful with these two jumpers during installation.

6.4 ROM DISK INSTALLATION

This section describes the various types of SSDs' installation steps as follows.

6.4.1 UV EPROM (27Cxxx)

(1) Switch and Jumper Setting

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number and EPROM type on SW2.

Step 3: Insert programmed EPROM(s) or FLASH(s) chips into sockets starting at MEM1.

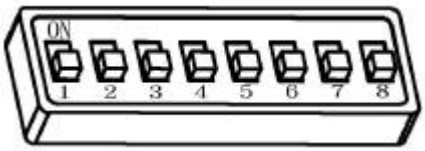


Figure 0-4 UV EPROM (27CXXX) Switch Setting

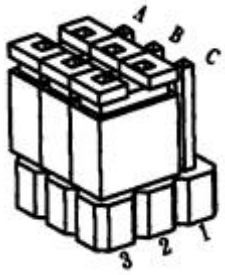
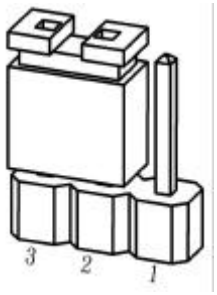
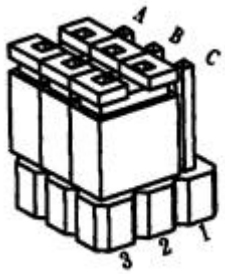
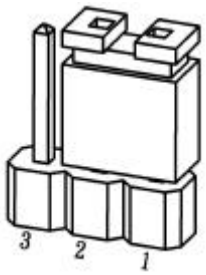
Function	M1-M3 Setting	JP6 Setting
1MX8 EPROM (ONLY)		
EPROM: 128Kx8, 256Kx8, 512Kx8		

Table 0-9 UV EPROM Jumper Setting

(2) Software Programming
Using the UV EPROM, please refer to the follow steps:

Step 1: Turn on the power and boot DOS from the hard disk drive or floppy disk drive.

Step 2: Make a Program Group File (*.PGF file)

Step 3: Use the RFG.EXE to generate ROM pattern files, and count the ROM numbers as the pattern files edited by the user.

Step 4: Under DOS prompt type the command as follows.

```
C:\>RFG [file name of PGF]
```

Step 5: In the RFG.EXE main menu, choose the <Load PGF File> item, that is *.PGF file.

Step 6: Choose the <Generate ROM File(s)>, the tools program will generate the ROM files, for programming the EPROMs.

Step 7: Program the EPROMs
Using the instruments of the EPROM writer to load and write the ROM pattern files into the EPROM chips. Make sure that the EPROMs are verified by the program without any error.

Step 8: Install EPROM chips
Be sure to place the programmed EPROMs (R01, R02…) into socket startin
g from MEM1 and ensure that the chips are installed in the sockets in the proper orientation.

6.4.2 Large Page 5V FLASH Disk

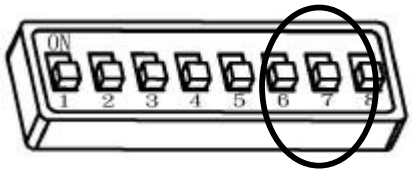
If you are using large page 5V FLASH as ROM disk, it has the same installation procedure as step 1 to step 4 when using the UV EPROM.

(1) Switch and Jumper Settings

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number and large page 5V FLASH type on SW2.

Step 3: Insert programmed EPROM(s) or FLASH(s) chips into sockets starting at MEM1.



SW2-1~SW2-6（Off）
SW2-7（On）
SW2-8（Off）

Figure 0-6 5V Large FLASH (29FXXX) Switch Setting

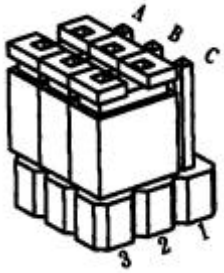
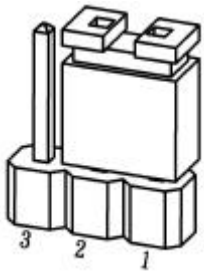
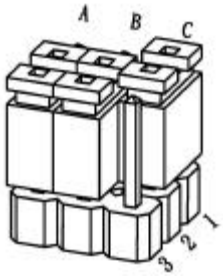
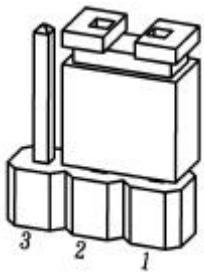
Function	M1-M3 Setting	JP6 Setting
5V/12V FLASH (64Kx8M, 128Kx8, 256Kx8)		
5V FLASH (512K*8 only)		

Figure 0-7 Large Page 5V FLASH Jumper Setting

(2) Software Programming

Then, you should create a PGF and generate the ROM pattern files by using the RFG.EXE.

Step 1: Make a Program Group File (*.PGF file)

Step 2: Generate ROM pattern files

Step 3: Turn off your system, and then install the FLASH EPROMs into the sockets.

NOTE: Place the appropriate number of FLASH EPROM chips (the numbers depends on the ROM pattern files generated by RFG.EXE) into the socket starting from MEM1 and ensure that the chips are installed in the sockets in the proper orientation. Line up and insert the AR-B1380/AR-B1380A board into any free slot of your computer.

6.4.3 Small Page 5V FLASH ROM Disk

(1) Switch and Jumper Settings

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number and EPROM type on SW2.

Step 3: Insert programmed EPROM(s) or FLASH(s) chips into sockets starting at MEM1.

SW2-1~SW2-7(Off)
SW2-8 (On)

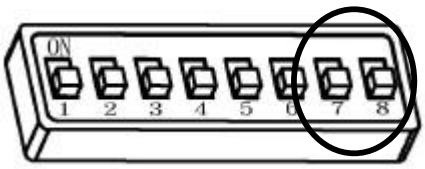


Figure 0-8 5V FLASH (29CXXX & 28EEXXX) Switch Setting

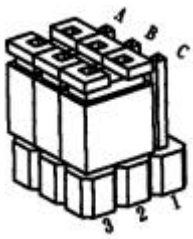
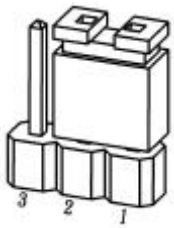
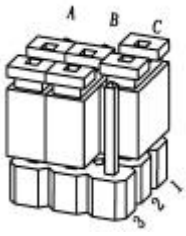
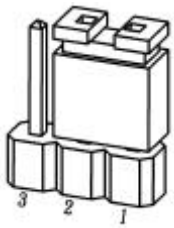
Function	M1-M3 Setting	JP6 Setting
5V/12V FLASH (64Kx8M, 128Kx8, 256Kx8)		
5V FLASH 512K*8 only		

Figure 0-9 5V FLASH (29CXXX & 28EEXXX) Jumper Setting

(2) Using Tool Program

If small page 5V FLASH EPROMs are used, it is the same procedure as step 1 to step 4 of using the UV EPROM:

Step 1: Making a Program Group File (*.PGF file)

Step 2: Generating ROM pattern files

Step 3: Installing FLASH EPROMs

Step 4: Programming FLASH EPROMs

Step 5: Reboot system

(3) Typing DOS Command

You can use another way to format and copy files to the 5V FLASH EPROM. This method provides the convenience of using a RAM disk. You can use the DOS <FORMAT> and <COPY> command to format and copy files. Follow the following steps to format and copy files to the FLASH disk. it is the same procedure as step 1 to step 4 of using the UV EPROM.

Step 1: Turn on your computer, when the screen shows the SSD BIOS menu, please hit the <Ctrl+ ->key during the system boot-up, this enables you to enter the FLASH setup program. If the program does not show up, check the switch setting of SW2.

Step 2: Use <Page-Up>, <Page-Down>, <Right>, and <Left> arrow keys to select the correct FLASH memory type and how many memory chips are going to be used.

Step 3: Press the [F4] key to save the current settings.

Step 4: After the DOS is loaded, use the DOS [FORMAT] command to format the FLASH disk.

To format the disk and copy DOS system files to the disk.

C:\>FORMAT [ROM disk letter] /S /U

To format the disk without copying DOS system files.

C:\>FORMAT [ROM disk letter] /U

Step 5: Copy your program or files to the FLASH disk by using DOS [COPY] command.

CAUTION: It is not recommended that the user format the disk and copy files to the FLASH disk very often. Since the FLASH EPROM's write cycle life time is from 10,000 to 100,000 times, writing data to the FLASH too often will reduce the life time of the FLASH EPROM chips, especially the FLASH EPROM chip in the MEM1 socket.

6.4.4 RAM Disk

(1) Switch and Jumper Setting

Step1: Use jumper block to set the memory type as ROM (FLASH).

Step2: Select the proper I/O base port, firmware address, disk drive number on SW2.

Step3: Insert programmed SRAM chips into sockets starting at MEM1.

NOTE: If you use the SRAM, please skip the SW2-7 & SW2-8 setting.

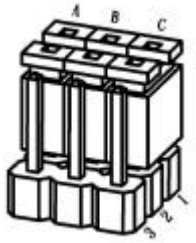
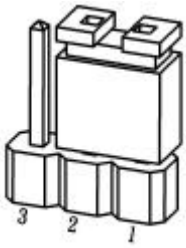
Function	M1-M3 Setting	JP6 Setting
SRAM		

Figure 0-10 SRAM Jumper Setting

(2) Software Programming

It is very easy to use the RAM disk. The RAM disk operates just like a normal floppy disk. A newly installed RAM disk needs to be formatted before files can be copied to it. Use the DOS command [FORMAT] to format the RAM disk.

Step 1: Use jumper block to select the memory type as SRAM refer.

Step 2: Select the proper I/O base port, firmware address and disk drive number on SW2.

Step 3: Insert SRAM chips into sockets starting from MEM1

Step 4: Turn on power and boot DOS from hard disk drive or floppy disk drive.

Step 5: Use the DOS command [FORMAT] to format the RAM disk. If you are installing SRAM for the first time.
To format the RAM disk and copy DOS system files onto the RAM disk.

```
C:\>FORMAT [RAM disk letter] /S /U
```

To format the RAM disk without copying DOS system files into the RAM disk.

```
C:\>FORMAT [RAM disk letter] /U
```

Step 6: Use the DOS command [COPY] to copy files onto the RAM disk. For example, if you want to copy file <EDIT.EXE> to the RAM disk from drive C: and the RAM disk is assigned as drive A:.

```
COPY C:EDIT.EXE A:
```

NOTE: In addition, you can use any other DOS command to operate the RAM disk.

6.4.5 Combination of ROM and RAM Disk

The AR-B1380/AR-B1380A can be configured as a combination of one ROM disk and one RAM disk. Each disk occupies a drive unit.

Step 1: Use jumper block to select the proper ROM/RAM configuration you are going to use.

Step 2: Insert the first programmed EPROM into the socket mem1, the second into the socket MEM2, etc.

Step 3: Insert the SRAM chips starting from the first socket assigned as SRAM.

Step 4: Select the proper I/O base port, firmware address and disk drive number on SW2.

Step 5: Turn on power and boot DOS from hard disk drive or floppy disk drive.

Step 6: Use the DOS command [FORMAT] to format the RAM disk.

```
C:\>FORMAT [RAM disk letter] /U
```

Step 7: If 5V FLASH (small page) is being used for the first time.
And then use the DOS command [FORMAT] to format the FLASH disk.

Step 8: If large page 5V FLASH is being installed for the first time, please use the FLASH programming utility RFG.EXE to program ROM pattern files.

NOTE: Users can only boot DOS from the ROM disk drive if the AR-B1380/AR-B1380A is configured as a ROM and a RAM disk. You don't need to copy DOS onto the RAM disk.

7. BIOS CONSOLE

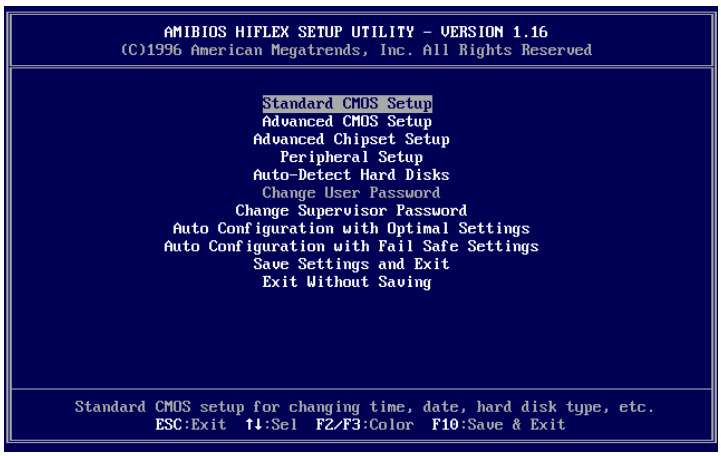
This chapter describes the AR-B1380/AR-B1380A BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Password Setting
- Load Default Setting
- BIOS Exit
- BIOS Update

7.1 BIOS SETUP OVERVIEW

BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drive, and the keyboard.
The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.
The BIOS Default Values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.
After the computer turned on, the BIOS will perform a diagnostics of the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.
The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure the option and configure the functions.

CAUTION



1) AR-B1380/AR-B1380A BIOS the factory-default setting is used to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can contact the technical support engineer.

2) If the BIOS loss setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option is best-case values that should optimize system performance.

3) The BIOS settings are described in detail in this section.

7.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

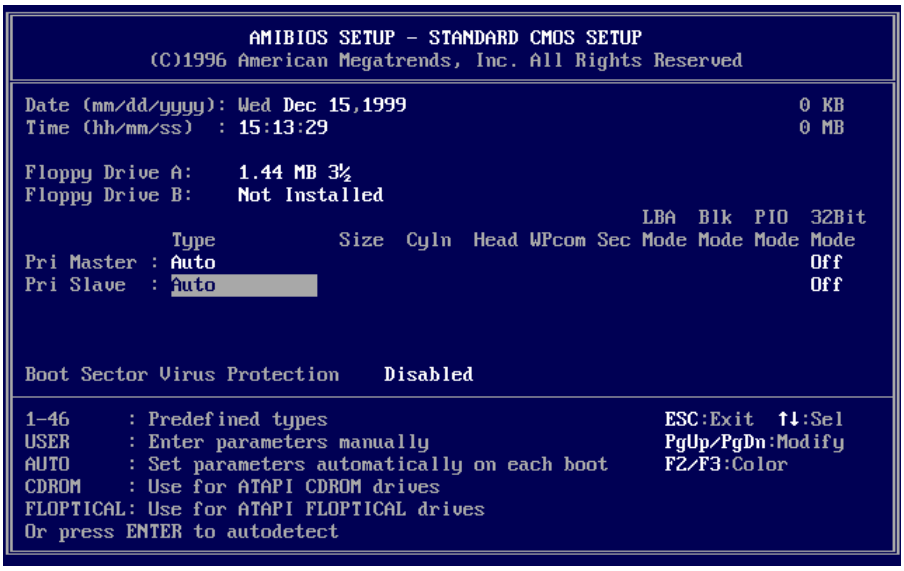


Figure 0-2 BIOS: Standard CMOS Setup

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master> and <Pri Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

Boot Sector Virus Protection
This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <***Disabled***>. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

7.3 ADVANCED CMOS SETUP

The <Advanced CMOS SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board¡ s design to remained in their default settings.

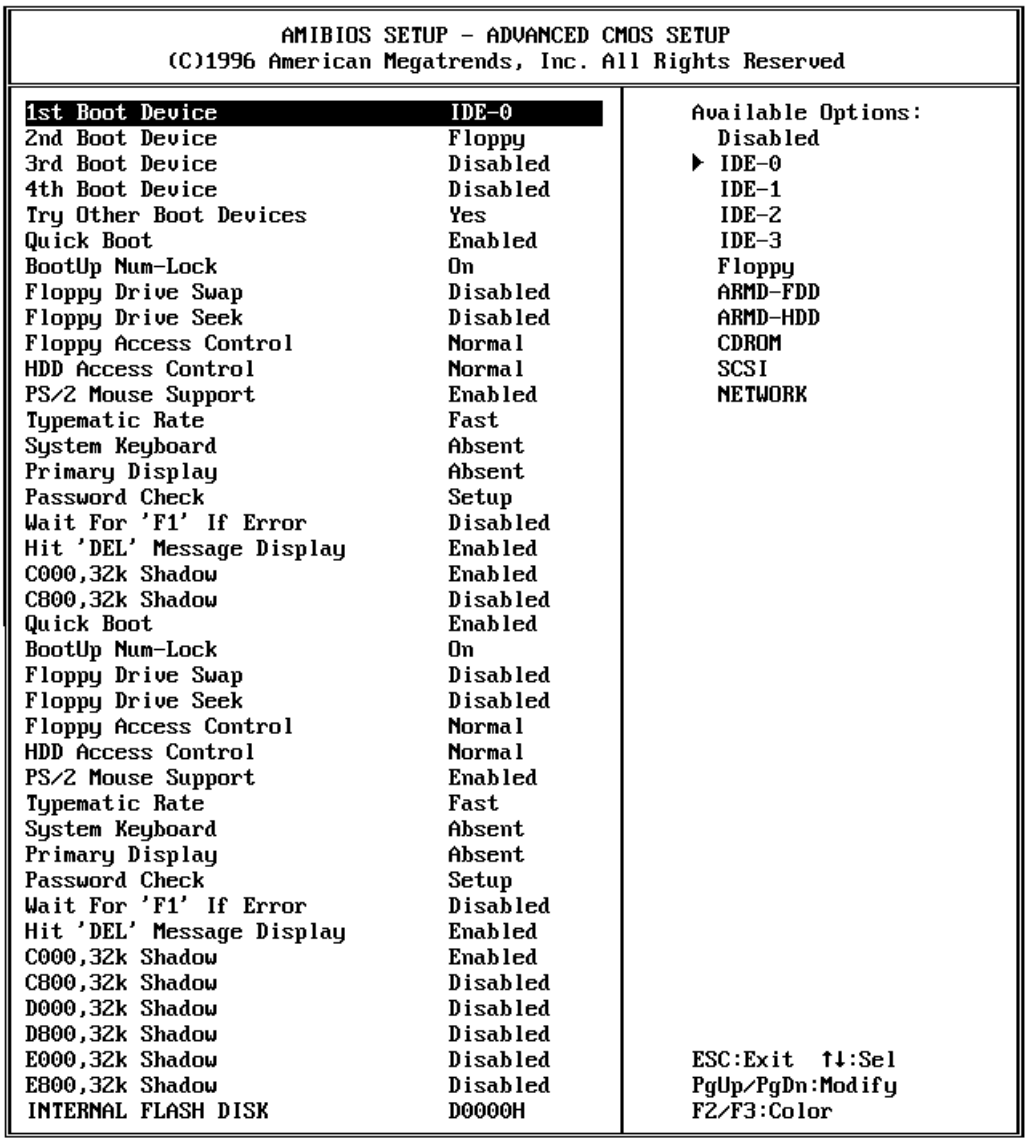


Figure 0-3BIOS: Advanced CMOS Setup

1st Boot Device
2nd Boot Device
3rd Boot Device
4th Boot Device

These options determine the priority of the bootup devices which the system looks for first to boot the system. According to the default setting, the system searches the hard disk first, then the floppy drive, and last the CDROM.
Available options: Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM, SCSI, NETWORK

Boot From Card BIOS
Select **Yes** to boot up the system from the SSD BIOS, and **No** to boot the system from the sysyem's onboard BIOS.
Available options: No,Yes
Note: It is recommended to configure this function at it's default setting, Yes.

Try Other Boot Devices
If you have other bootup device other than the above mentioned devices, such as **IDE-0, IDE-1, IDE-3, IDE-4, Floppy, ARMD-FDD, CDROM, SCSI, and network,** choose yes. This device is prior to the above devices mentioned above.
Available options: No, Yes

Quick Boot
This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to enabled, BIOS will shorten or skip some check items during POST.
Available options: Disabled, enabled

Floppy Drive Swap
The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the setting is <***Enabled***>, the BIOS will be swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.
Available options: Disabled, Enabled

Floppy Drive Seek
If the <Floppy Drive Seek> item is setting ***Enabled***, the BIOS will seek the floppy <A> drive one time upon bootup.
Available options: Disabled, Enabled

Floppy Access Control
This option determines the floppy access method, which can be either read only or normal (read/write). When set to read only, the data in the hard disk is allowed to be read instead of being written." Normal" allows the floppy to be read or written.
Available options: Normal, Read only

HDD Access Control
This option determines the floppy access method, which can be either read only or normal (read/write). When set to read only, the data in the hard disk is allowed to be read instead of being written." Normal" allows the floppy to be read or written.
Available options: Disabled, Enabled

PS/2 Mouse Support
The setting of **Enabled** allows the system to detect a PS/2 mouse on bootup. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards and therefore the PS/2 mouse will not function.
Available options: Disabled, Enabled

Typematic Rate
This item specifies the speed at which a keyboard keystroke is repeated.
Available options: Fast ,Slow

System Keyboard
This function specifies that a keyboard is attached to the computer.
Available options: Absent, Present

Primary Display
The option is used to set the type of video display card installed in the system.
Available options: Absent, VGA/EGA, CGA40x25, CGA80x25

Password Check
This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.
Available options: Setup, Always

Wait for 'F1' If Error
AMIBIOS POST error messages are followed by:

Press <F1> to continue

If this option is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.
Available options: Disabled,Enabled

Hit 'DEL' Message Display
Set this option to ***Disabled*** to prevent the message as follows:

Hit 'DEL' if you want to run setup

It will prevent the message from appearing on the first BIOS screen when the computer boots.
Available options: Disabled,Enabled

C000, 32K Shadow

C800, 32K Shadow

D000, 32K Shadow

D800, 32K Shadow

E000, 32K Shadow

E800, 32K Shadow

These options control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus.

The settings are:

SETTING	DESCRIPTION
Disabled	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
Enabled	The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.

Table 0-1 Shadow Setting

INTERNAL –FLASH-DISK

This option selects the SSD BIOS memory address.

Available options: Disabled, C8000H, D0000H, D8000H, E0000H, E8000H

7.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

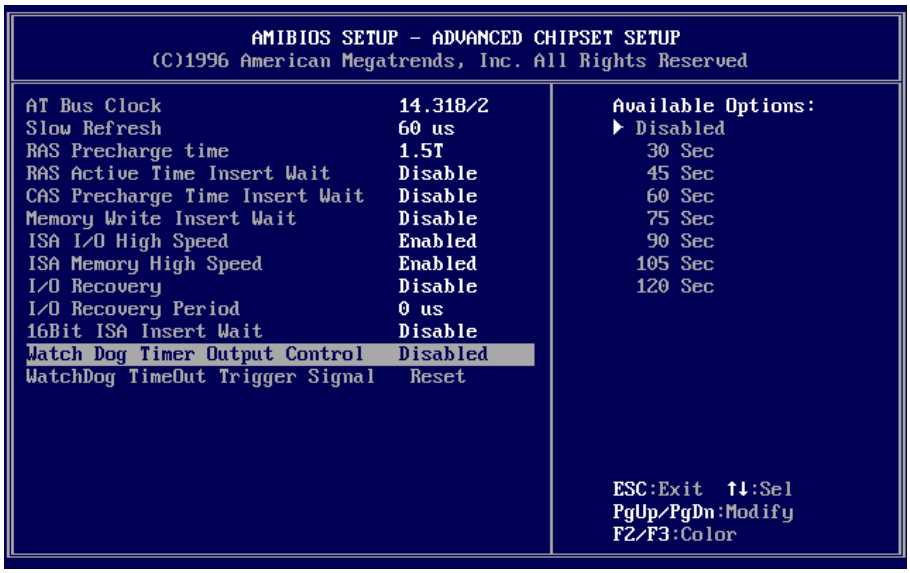


Figure 0-4BIOS: Advanced Chipset Setup

AT Bus Clock

This option sets the polling clock speed of ISA Bus (PC/104).

Available options: 14.318/2, PLCK2/3, PLCK2/4, PLCK2/5, PLCK2/6, PLCK2/8, PLCK2/10, PLCK2/12

NOTE: 1. PCLK means the CPU inputs clock.
2. Acrosser recommends user setting at the range of 8MHz to 10MHz.

Slow Refresh

This option sets the DRAM refresh cycle time.

Available options: 15us, 60us, 120us

RAS Precharge time
The DRAM RAS precharge time.
Available options: 1.5T,2.5T, 3.5T

RAS Active Time Insert Wait
The options sets the DRAM time insert wait: RAS Active and CAS Precharge function setting.
Available options: Enabled, Disabled

CAS Precharge Time insert Wait
Whenever memory reads or writes, it will insert 1T between the falling edges for both RASJ and CASJ, if D(4) of index 11h is set to high.
Available options: Enabled, Disabled

Memory Write Insert Wait
This opton sets the Memory Write Insert Wait
Available options: Enabled, Disabled

ISA I/O High Speed
This option allows the ISA card to operate at a higher ATCLK during specific I/O accessing cycles. The below table describes the frequency that it can improve.

High Frequency	Normal Frequency(AT Bus Clock)
7.159 MHz	7.159MHz
PCLK2/2	PCLK2/3
PCLK2/3	PCLK2/4
PCLK2/4	PCLK2/5
PCLK2/5	PCLK2/6
PCLK2/6	PCLK2/8
PCLK2/8	PCLK2/10
PCLK2/10	PCLK2/12

Available options: Enabled, Disabled

ISA Memory High Speed
This option allows the ISA card to operate at higher ATCLK during specific memory accessing cycles. Same as ISA I/O High Speed, the above table describes the frequency that it can improve.
Available options: Enabled, Disabled

ISA Write cycle end insert wait

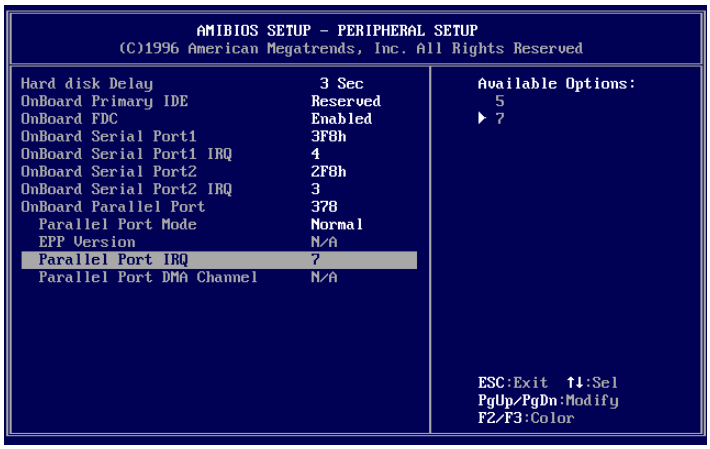
I/O Recovery / Recovery Period
If **I/O Recovery** Feature options is enabled, the BIOS inserts a delay time between two I/O commands. The delay time is defined in **I/O Recovery Period option.**
Available options for I/O Recovery: Enabled, Disabled
Available options for I/O Recovery: 0 us, 0.25 us, 0.50 us, 0.75 us, 1.00 us, 1.25 us, 1.50 us, 1.75 us, 2.00 us, 2.25 us, 2.75 us, 3.00us, 3.25us, 3.50 us
16Bit ISA Insert Wait
This option enables the 16Bit ISA Insert Wait Function. When the system is at read/write status, it will insert the wait time to extend the read/write time.
Available options: Enabled, Disable

Watch Dog Timer Output Control
This option selects the Watch Dog Timer period which is from **30 Seconds to 120 Seconds**. The default value is **Disabled** which the watch dog Timer function disables.
Available options: 30SEC, 60SEC, 75SEC, 90SEC, 105SEC, 120SEC,

Watch Dog Timeout Period Trigger Signal
To configure this function, the user must select a period of time in the above item to enable the watch dog Timer. The vaule, Reset, means to reset the system every certain period of time. When another vaule, (either IRQ3, IRQ4, IRQ9, IRQ10, IRQ11, IRQ12, or IRQ15) is selected, the watch dog Timer will generate a pulse to trigger the device set to that IRQ every certain period of time.
Avilable options: IRQ3, IRQ4, IRQ10, IRQ10, IRQ11, IRQ12, IRQ12, IRQ12, IRQ15, RESET

7.5 PERIPHERAL SETUP

This section is used to configure the peripheral features.



Hard Disk Delay
If this option is set to **Disabled** and the system BIOS executes too fast, the result is that the BIOS can't find the hard disk drive. Therefore, it is recommended to select a hard disk delay period to prevent the BIOS from executing too fast.
Availabie options: 3sec, 5sec, 10sec, 15sec.

OnBoard Primary IDE
This options specifies the onboard IDE controller channels that will be used.
Availabie options: Enabled, Disabled.

OnBoard FDC
This option enables the floppy drive controller on the AR-B1380/1380A.
Availabie options: Auto, Enabled, Disabled.

OnBoard Serial Port 1
This option enables the serial port on the AR-B1380/1380A.
Available options: Disabled, 3F8h, 2F8h, 3E8h, 2E8h

OnBoard Serial Port 1 IRQ
This option selects the IRQ for the onboard serial port.
Available options: 3,4,5,9

OnBoard Serial Port 2
This option enables the serial port on the AR-B1380/1380A.
Available options: Disabled, 3F8h, 2F8h, 3E8h, 2E8h

OnBoard Serial Port2 IRQ
This option selects the IRQ for the onboard serial port2.
Available options: 3,4,5,9

Onboard Parallel Port
This option configures the onboard the parallel port.
Available options:Auto, disabled,378, 278, 3BC

Parallel Port Mode
This option specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications.
Available options:Normal, ECP, EPP

EPP version
This option specifies the EPP version.
Available options: Normal, 1.9, 1.7

Parallel Port IRQ
This option selects the IRQ for the parallel port IRQ.
Available options: 5, 7

Parallel Port DMA Channel
This option is only available if the setting for the parallel Port Mode option is ECP.
Available options: 0. 1, 3

7.6 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

7.6.1 Setting Password

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

```
Enter new supervisor password:
```

7.6.2 Password Checking

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing on the keyboard. As user select Supervisor or User. The BIOS prompts for a password, user must set the Supervisor password before user can set the User password. Enter 1-6 character as password. The password does not appear on the screen when typed. Make sure you write it down.

7.7 LOAD DEFAULT SETTING

In this section permit user to select a group of setting for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

7.7.1 Auto Configuration with Optimal Setting

User can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance settings (Y/N) ?
```

7.7.2 Auto Configuration with Fail Safe Setting

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.
The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N) ?
```

7.8 BIOS EXIT

This section is used to exit the BIOS main menu in two types situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

7.8.1 Save Settings and Exit

This item set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

7.8.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

```
Quit without saving (Y/N) ?
```

7.9 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The AR-B1380/AR-B1380A provides FLASH BIOS update function for you to easily upgrade newer BIOS version. Please follow the operating steps for updating new BIOS:

Step 1: Turn on your system and press <F5> to skip the CONFIG.SYS and AUTOEXEC.BAT files. Keep your system in the real mode.

Step 2: Insert the FLASH BIOS diskette into the floppy disk drive.

Step 3: In the MS-DOS mode, you can type the AMIFLASH program.

A:\>AMIFLASH

Step 4: The screen will show the message as follows:

Enter the BIOS File name from which Flash EPROM will be programmed.
Press <ENTER> after inserting the file name or press <ESC> to exit.

Step 5: And then please enter the file name to the box of <Enter File Name>. And the box of <Message> will show the notice as follow. In the bottom of this window always show the gray statement.

Flash EPROM Programming is going to start. System will not be usable until Programming of Flash EPROM is successfully complete. In case of any error, existing Flash EPROM must be replaced by new program Flash EPROM.

Step 6: When the above statement disappears, press the <Y> key to updating the new BIOS. And then the <Message> box will show the <Programming Flash EPROM>, and the gray statement shows <Please Wait>.

Step 7: The BIOS update is successful, the message will show <Flash Update Completed - Pass>.

NOTE

1) If the system didn't detect the boot procedure, during power on, please press the [F5] key immediately. The system will pass the CONFIG.SYS and AUTOEXEC.BAT files.

. 2) Now the onboard BIOS is the newest BIOS, if user needs to add some functions in the future, please contact technical supporting engineers, they will provide the newest BIOS for updating.

3) The included file of ***AMIFLASH.EXE*** is ***Version 6.31***.

http:\\www.acrosser.com

8. SPECIFICATIONS & SSD TYPES SUPPORTED

8.1 SPECIFICATIONS

CPU & Chipset:	ALI M6117, 25/33/40 MHz (onboard 33 MHz for standard)
Bus Interface:	ISA and PC/104 bus
DRAM:	2 MB EDO RAM onboard with one SOJ socket and one 72-pin SIMM socket for 16MB or 4MB
CRT/LCD Display:	(C&T (PC/AT) VGA chipset with 1 MB VRAM (1024X768/256 colors)
(AR-B1380A only)	CRT with 15-pin HDB connector LCD with 44-pin 2.0mm connector
HDD:	Supports two IDE drives or one IDE flash module
FDC:	Supports two 5.25" or 3.5" floppy disk drives
Serial Port:	1 RS-232C port with DB-9 male connector 1 RS-232C/RS-485 with DB-9 male connector
Parallel Port:	1 SPP/EPP/ECP mode printer port with 26-pin 2.54mm connector
Keyboard and Mouse:	PS/2 compatible with 6-pin Mini-DIN and 6-pin 2.0 mm JST connector
Real Time Clock:	M48T86PC1 or compatible chips
BIOS:	Legal flash system and video BIOS
Watchdog:	Programmable watchdog timer
Solid State Disks:	3 sockets for 1.5MB/ 1.5MB/3MB Flash/SRAM/EPROM disk The 3 sockets can be three S.S.D. sockets or two S.S.D sockets and one D.O.C. socket
Speaker	Onboard buzzer and 4-pin header for external speaker
DMA Channels:	7 DMA channels
Interrupt Levels:	15 vectored interrupt levels
Bus Speed:	7.159MHz
LED Indicator:	Power LED, hard disk LED, and 2 headers for external PW/WD and HDD LEDs
Power Connector:	One 8-pin (2.5mm) power connector and one 4-pin(2.5)mm
Power Req.:	+5V only, 1.0A maximum (based on 33 MHz CPU)
Operating Temp.:	0 to 60 degree C. (140 degree F.)
Storage Temp.:	-10 to 75 degree C.
Humidity:	0 to 85% (non-condensing)
PC Board:	6 layers
Dimensions:	185 mmX122mm (7.29"X4.80")
Weight:	AR-B1380 –285g (w/o memory chips & DRAM SIMMs)

5.2 SSD TYPES SUPPORTED

The following list contains SRAMs supported by the AR-B1380/AR-B1380A:

AKM	AKM628128	(128Kx8, 1M bits)
HITACHI	HM628128	(128Kx8, 1M bits)
NEC	UPD431000A	(128Kx8, 1M bits)
SONY	CXK581000P/M	(128Kx8, 1M bits)
HITACHI	HM628512	(512Kx8, 4M bits)
NEC	UPD434000	(512Kx8, 4M bits)
SONY	CXK584000P/M	(512Kx8, 4M bits)

The following list contains large page 5V FLASHs supported by the AR-B1380/AR-B1380A:

AMD	Am29F512	(64Kx8, 512K bits)

AMD	Am29F010	(128Kx8, 1M bits)
AMD	Am29F020	(256Kx8, 2M bits)
AMD	Am29F040	(512Kx8, 4M bits)

The following list contains small page 5V FLASHs supported by the AR-B1380/AR-B1380A:

ATMEL	AT29C512	(64Kx8, 512K bits)
SST	PH29EE512	(64Kx8, 512K bits)
ATMEL	AT29C010	(128Kx8, 1M bits)
SST	28EE010	(128Kx8, 1M bits)
SST	28EE011	(128Kx8, 1M bits)
SST	PH29EE010	(128Kx8, 1M bits)
WINBOND	W29EE011	(128Kx8, 1M bits)
ATMEL	AT29C020	(256Kx8, 2M bits)
ATMEL	AT29C040	(512Kx8, 4M bits)
ATMEL	AT29C040A	(512Kx8, 4M bits)
SST	PH28SF040	(512Kx8, 4M bits)

The following list contains EPROMs supported by the AR-B1380/AR-B1380A:

AMD	Am27C010	(128Kx8, 1M bits)
ATMEL	AT27C010	(128Kx8, 1M bits)
FUJITSHU	MBM27C1001	(128Kx8, 1M bits)
HITACHI	HN27C101	(128Kx8, 1M bits)
INTEL	D27C010	(128Kx8, 1M bits)
MITSHUBISHI	M5M27C101	(128Kx8, 1M bits)
NEC	D27C1001	(128Kx8, 1M bits)
NS	NM27C010	(128Kx8, 1M bits)
SGS-THOMSON	M27C1001	(128Kx8, 1M bits)
TI	TMS27C010	(128Kx8, 1M bits)
TOSHIBA	TCS711000	(128Kx8, 1M bits)
AMD	Am27C020	(256Kx8, 2M bits)
ATMEL	AT27C020	(256Kx8, 2M bits)
FUJITSU	MBM27C2001	(256Kx8, 2M bits)
HITACHI	HN27C201	(256Kx8, 2M bits)
INTEL	D27C020	(256Kx8, 2M bits)
MITSHUBISHI	M5M27C201	(256Kx8, 2M bits)
NEC	D27C2001	(256Kx8, 2M bits)
NS	NM27C020	(256Kx8, 2M bits)
SGS-THOMSON	M27C2001	(256Kx8, 2M bits)
TI	TMS27C020	(256Kx8, 2M bits)
TOSHIBA	TCS712000	(256Kx8, 2M bits)
AMD	Am27C040	(512Kx8, 4M bits)
ATMEL	AT27C040	(512Kx8, 4M bits)
FUJITSU	MBM27C4001	(512Kx8, 4M bits)
HITACHI	HN27C401	(512Kx8, 4M bits)
INTEL	D27C040	(512Kx8, 4M bits)
MITSUBISHI	M5M27C401	(512Kx8, 4M bits)
NEC	D27C4001	(512Kx8, 4M bits)
NS	NM27C040	(512Kx8, 4M bits)
SGS-THOMSON	M27C4001	(512Kx8, 4M bits)
TI	TMS27C040	(512Kx8, 4M bits)
TOSHIBA	TCS714000	(512Kx8, 4M bits)
ATMEL	AT27C080	(1Mx8, 8M bits)

9. USING MEMORY BANKS

This appendix provides the information about how to access the memory on the AR-B1380/AR-B1380A without using the AR-B1380/AR-B1380A SSD BIOS. The AR-B1380/AR-B1380A hardware divides every 8K bytes of memory into a memory bank. To access the data in the memory, you have to assign the chip number and the bank number. On every chip, the memory bank number starts from zero. The last memory bank number depends on the size of the memory chip used on the AR-B1380/AR-B1380A. For example, if you use the 256K bytes memory chip, the bank number on every chip would be in the range of 0 to 31. The chip numbers and the bank numbers are determined by the bank select register on the AR-B1380/AR-B1380A.

The I/O address of these registers are determined by SW2-1/SW0-1
. The memory address of the memory bank is located on the range selected by SW2-3/SW2-4.

The I/O port address of the bank select register is base port+0, and the I/O port address of the chip select register is base port +2. The following is the format of the bank select register and bank enable register.

Register	I/O Port	D7	D6	D5	D4	D3	D2	D1	D0
Bank Select Register	Base +0	WPE	A6	A5	A4	A3	A2	A1	A0
Chip Select Register	Base +2	0	0	0	1	CS1	CS0	X	X

Where:

WPE	Write protect enable bit
A6~A0	Bank select bits, A0 is the LSB
CS1~CS0	Chip select bits of MEM1 to MEM3

Where:
CS1-CS0 : Chip select

CS1	CS0	Socket
0	0	Disable
0	1	MEM1
1	0	MEM2
1	1	MEM3

For different types of memory, A0 to A6 have different explanations. These bits are used to select the bank number of specific memory located in CS0 and CS1.

Memory	A6	A5	A4	A3	A2	A1	A0
64KB EPROM (FLASH)	0	0	1	0	BS2	BS1	BS0
128KB EPROM (FLASH)	0	0	0	BS3	BS2	BS1	BS0
256KB EPROM (FLASH)	0	BS4	1	BS3	BS2	BS1	BS0
512KB EPROM (FLASH)	0	BS4	BS5	BS3	BS2	BS1	BS0
1MB EPROM (FLASH)	BS6	BS4	BS5	BS3	BS2	BS1	BS0
128KB SRAM	0	1	0	BS3	BS2	BS1	BS0
512KB SRAM	0	BS5	BS4	BS3	BS2	BS1	BS0

NOTE : BS0 to BS5 are the memory bank select bits. For example, 128KB memory has sixteen 8K-byte banks, so 4 bits (BS0 to BS3) are needed.

Example 1: Select the 10th bank of the MEM1 on the AR-B1380/AR-B1380A. The AR-B1380/AR-B1380A is using 27C020 (256K*8), and the base port is &H210.

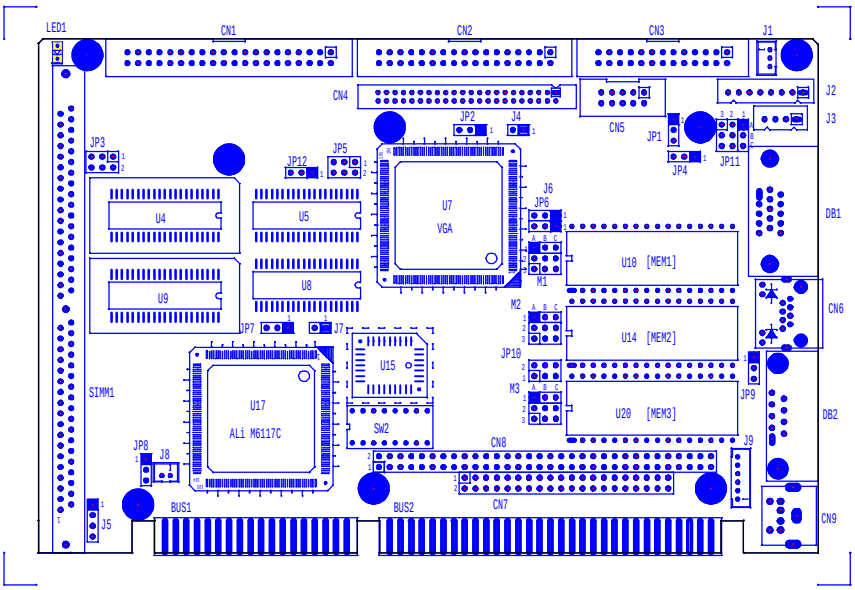
```
100 base_port=&H210
110 OUT base_port+0,&H59
```

Example 2: Select the 40th bank of MEM3 on the AR-B1380/AR-B1380A. The AR-B1380/AR-B1380A is using 27C040 (512K*8), and the base port is &H390.

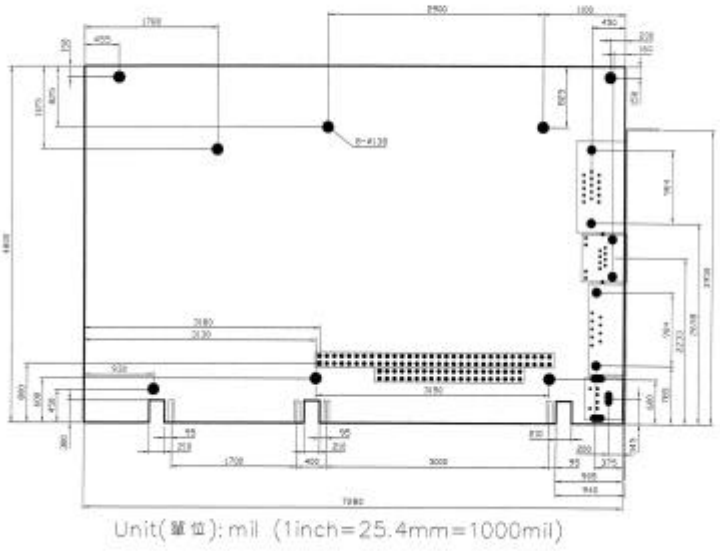
```
200 base_port=&H290
210 OUT base_port+0,&HD7
```

10. PLACEMENT & DIMENSIONS

10.1 PLACEMENT



10.2 DIMENSIONS



Unit: mil (1 inch = 25.4 mm = 1000 mil)

11. PROGRAMMING THE RS-485

The majority of the communicative operations of the RS-485 are the same as the RS-232. When the RS-485 proceeds with the transmission which needs control the TXC signal, the installation steps are as follows:

Step 1: Enable TXC (Data Terminal Relay)

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

NOTE: Please refer to Section 3.13.3.12 space of the "Serial Port" for the detailed description of the COM port's register.

(1) Initialize COM port

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets to "0".

NOTE: Set the AR-B1380/AR-B1380A CPU card's DTR signal to the control RS-485's TXC communication.

(2) Send out one character (Transmit)

Step 1: Enable the TXC signal, and the bit 0 of the address of offset+4 sets to "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check the transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are set to "0".

Step 4: Disabled the TXC signal, and the bit 0 of the address of offset+4 sets to "0"

(3) Send out one block data (Transmit – the data more than two characters)

Step 1: Enable the TXC signal, and the bit 0 of the address of offset+4 sets to"1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are set to "0".

Step 4: Disabled the TXC signal, and the bit 0 of the address of offset+4 sets to "0"

(4) Receive data
The RS-485's operation of receiving data is the same as RS-232's.

(5) Basic Language Example
a.) Initialize 86C450 UART

```
10   OPEN "COM1:9600,m,8,1" AS #1 LEN=1
20   REM Reset DTR
30   OUT &H3FC, (INP(%H3FC) AND &HFA)
40   RETURN
```

b.) Send out one character to COM1

```
10   REM Enable transmitter by setting DTR ON
20   OUT &H3FC, (INP(&H3FC) OR &H01)
30   REM Send out one character
40   PRINT #1, OUTCHR$
50   REM Check transmitter holding register and shift register
60   IF ((INP(&H3FD) AND &H60) >0) THEN 60
70   REM Disable transmitter by resetting DTR
80   OUT &H3FC, (INP(&H3FC) AND &HEF)
90   RETURN
```

c.) Receive one character from COM1

```
10   REM Check COM1: receiver buffer
20   IF LOF(1)<256 THEN 70
30   REM Receiver buffer is empty
40   INPSTR$"
50   RETURN
60   REM Read one character from COM1: buffer
70   INPSTR$=INPUT$(1,#1)
80   RETURN
```