

A White Paper on the Benefits of Chipkill- Correct ECC for PC Server Main Memory

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Abstract

As the network-centric model of computing continues to mature, customers are constantly trying to evaluate what the correct price/performance point is for their business. For the growing number of businesses that choose a PC Server for a departmental, workgroup, or application server function, one of the key parameters is the reliability of the server. This paper addresses one area of concern in the RAS (Reliability, Availability, and Serviceability) arena of PC Servers that has been addressed thoroughly at the mainframe and midrange class of machines, but not at the lower end of the server spectrum: error recovery when an entire DRAM chip fails.

Executive Overview

The Market

- Network-centric computing is becoming increasingly ubiquitous
- PC Servers are becoming an increasingly attractive price/performance option
- This business model requires increasingly better network support and reliability
- While some strides have been made, PC Servers are playing catch-up in many areas
- Fault tolerance is an increasingly important differentiator in the PC Server market
 - ***the market demand is NO DOWN TIME!***

The Background

- Fault tolerance has been applied in a haphazard manner to the PC Server space
- In 1992, ECC was non-existent on the low- and mid-range of the PC Server space
- In 1992, RAID disk drive redundancy was not very prevalent
- Today all servers except the very low end support Single Error Correct (SEC) ECC
- Today all servers except the very low end offer some kind of RAID adapter

The Problem

- Memory subsystem fault tolerance is behind that of the DASD subsystem:
 - RAID 5 will fix any single hard disk failure on the fly
 - SEC ECC will only fix a single bad bit out of a x4, x8, or x16 DRAM chip
- Multibit DRAM failure modes are increasing due to a strong move to lower power DRAM architectures; they are *not* corrected by SEC ECC
- Both the DRAM hard error rate (failures in the silicon) *AND* soft error rate (temporary failures due to charged particles) can be increased by architecture changes
- Today's 1GB SEC ECC server has the same uncorrectable error rate as yesterday's 32MB parity server! *That rate was unacceptable then, and is unacceptable now*

The Solution

- Chipkill-correct ECC should be available on all servers; this capability has also been called RAID-M (Redundant Array of Inexpensive DRAMs - for Memory)
- Native solutions have historically been offered on some platforms due to architecture; examples are IBM's AS/400 series and Compaq's Proliant 4000 series
- IMD now has a retrofittable memory module that will allow a non-chipkill-protect server to be upgraded to fully support RAID-M

The Bottom Line

RAID-M is an effective means of solving a real customer problem and is an opportunity to provide market leadership in the PC Server space

Introduction

In 1992, the client-server computing paradigm was enjoying significant acceptance and growth in the business environment. Companies were simultaneously recognizing that not only was the availability and usability of information becoming more and more important to the successful operation of any business, large or small, but that the means to implement that connectivity at a much lower price point than was previously attainable by means of the “glass house” mainframe and dumb terminals that were so prevalent in the large businesses was now available.

The move to client-server computing in general, and the use of relatively low-end servers based on Intel¹ microprocessors, was, however, not done without a good deal more difficulty than was originally anticipated. Although the PC-like system structure (hence the name “PC Server”) could run basic file-, workgroup-, and application-server functions, the whole approach suffered from major drawbacks in several areas such as raw processing power, robust operating system support, scalability, security, fault-tolerance and high-availability. This led to the now widely accepted understanding that even though PC Servers have a very low initial price point -- and even a favorable price/performance point -- their deficiencies are serious enough to warrant careful consideration before declaring them fit for major enterprise usage. Indeed, the rumors of the mainframe's demise *were* greatly exaggerated.

Increased Performance

Since 1992, however, there have been significant and, perhaps, even fundamental changes to both the hardware and software available on the PC Server class of machine. First, the rather anemic performance obtained from a 486-class microprocessor running a system bus at 33 Mhz and internally at 66 MHz has been replaced by a 686-class microprocessor running a double-wide system bus at 66 MHz and internally at 200+ MHz. This clearly moves PC Server system performance up several orders of magnitude. Second, the emergence of multitasking, server-oriented operating systems has significantly increased the acceptance of PC Servers in enterprise environments. In fact, a popular version of UNIX (SCO UNIX²) allows PC Servers to run legacy RISC applications on the same hardware that can run legacy Windows³ operations under Windows NT. Third, fault-tolerance and security features are becoming much more available in the PC Server space. RAID (Redundant Array of Inexpensive DASD) controllers that allow several flexible and changeable variations on hard drive fault-tolerance. Various error logging and remote maintenance packages are being offered by major PC Server vendors. However, the most pertinent and revealing advancement related to this paper is the near total acceptance -- and even demand -- of error correction code (ECC) protection of the main memory subsystem. The ubiquity of ECC in the PC Server space is a telling sign of both the maturity of the marketplace and the maturity of the hardware in being able to

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1. Intel is a registered trademark of Intel, Inc.
 2. SCO UNIX is a trademark of The Santa Cruz Operation, Inc.
 3. Windows and Windows NT are trademarks of Microsoft, Inc.

The Memory Subsystem

meet this market need. Clearly the single-error-correct (SEC) ECC has become a checklist item for all but the very low-end of this marketing segment. Not only do the currently available PC Server chipsets support ECC, but even the Pentium Pro⁴ processor itself supports SEC ECC on its system bus.

These basic steps forward in software and hardware have allowed the PC Server to invade more and more territory once held solely by RISC workstations and mid-range computers. However, two other factors have come into play. First is the slow but sure realization by the marketplace that in spite of all the current advancements in technology, the PC Server is still a very weak sister when compared to the mainframe legacy for fault-tolerance and security. Second is the fundamental change in computing connectivity to a network-centric model.

Network Centric

The network-centric computing paradigm is based on the need for businesses to both obtain and distribute information all over the world instantaneously. The ramifications of this paradigm are far reaching and can be linked to phenomena as diverse as the resurgence of the mainframe to the emergence of the network PC. However, for our purposes, the most plain and simple consequence of this approach is an ever increasing demand on the reliability and availability of the network, including -- and perhaps *especially including*, due to their increasingly important role without a commensurately increasing fault-tolerance and robustness -- the PC Server.

If one accepts the dual premise that within the world of computing, the client-server, network-centric model is fast becoming the dominant approach, and that within the client-server, network-centric model the PC Server is fast becoming the price-performance hardware of choice, then it seems to follow logically that the market is demanding, and will continue to make greater demands on, the reliability and availability of PC Servers.

We will now focus on one area of the PC Server that is a constituent component of the total system reliability and availability: the memory subsystem.

The Memory Subsystem

The memory subsystem of PCs in general, and PC Servers in particular, is an interesting study in contrasts. While it is recognized as one of the most important links to better performance, it often gets designed in as an almost-after-thought. While it enables the operating system to work much more efficiently, it is viewed universally as a pure commodity-class product. While it sits on the highest bandwidth bus in the system, it has no crisply defined net structure and electrical interface requirements. And while the price per Megabyte, power con-

4. Pentium Pro is a trademark of Intel, Inc.

The Memory Subsystem

sumption, and functional compatibility are all watched with a righteous zeal, the ability of a DRAM failure to bring down the system is often glossed over or even entirely ignored.

The memory subsystem consists of more than just DRAMs, and from a design standpoint, the controller, nets, sockets, wiring, cache, etc., are all important and interrelated. But there is no doubt that the system vendors worry most about the DRAM when dealing with the memory subsystem. After all, the sockets and wiring never constitute more than 50% of the total system cost like the DRAMs do any time a system is shipped with the highest density, leading edge memory technology available. And after all, the SRAM L2 cache isn't replicated up to 16 times, providing a 16X increase in power consumption. And especially, after all, the one time purchase and qualification of a complex memory controller pales in comparison to the hundreds and hundreds of hours that go into qualifying a box with several different memory vendors' products. Indeed, it is no wonder that the cheap, commodity DRAM becomes the center of attention in many instances, and many of those instances, unfortunately, happen after the system is shipped.

Proliferation of Parts

Another complicating factor is the memory vendors' dual objective of expanding his product line to accommodate not only every product that will help fill the system vendor's exact price-performance niche, but also to have some percentage of product fall into the "value add" category, such that a small profit can be made over the traditionally cutthroat pricing of the commodity product. The result of these objectives is an incredible menu of possible products including:

- 50ns, 60ns, and 70ns speed sorts
- Fast Page Mode (FPM) and Extended Data Out (EDO)
- TSOP and SOJ packaging
- 3.3V and 5.0V power supplies
- Low power and standard power parts
- Synchronous DRAM and Double Data Rate (DDR) SDRAM
- Rambus DRAM and SLDRAM
- x4, x8, x16 and (soon to come) x32 data widths

And this short list doesn't include DRAMs geared toward graphics applications!

Furthermore, each basic DRAM die must be redesigned into more aggressive technology groundrules at least once each year in order to keep increasing the productivity, or chips per wafer. One memory vendor recently boasted of being on their sixth shrink of their 16Mb chip. This in spite of being in production for less than four years!

However, none of the aforesaid product diversity and complexity may affect product quality! As demanding as the system customer is on price, power and function, there can be no letup in the quest for higher quality. Whether six sigma or ISO 9000 plans are implemented, a memory vendor's product quality is carefully monitored and controlled. Top tier system vendors, primarily through their

component purchasing engineering group, almost always have aggressive quality goals for both incoming defect levels (sometimes called Shipped Product Quality Level, or SPQL) and field reliability (as is usually measured by accelerated temperature and voltage stress cells back at the factory called Group C reliability monitor).

In fact, over the last ten years, tremendous gains have been made in semiconductor reliability, both at the technology level and at the product level. Furthermore, the gains have been made in such a way as to be effective for both actual physical defects in the silicon and metallization, which are permanent for the most part and are called hard errors, and also the DRAM's susceptibility to alpha particles or cosmic rays, which are not permanent for the most part and are called soft errors. Thus in spite of all the economic challenges presented to DRAM manufacturers, the market has still demanded -- and received -- a very high level of overall memory reliability.

Finally, one has to consider the way a typical memory subsystem implements ECC. A great step forward was made when system busses increased to 8 bytes in width. Because at the 8 byte width ECC can be done with the same number of extra bits (called check-bits) as standard parity requires, the biggest hurdle to supporting ECC in the PC space was obviated. That is, it no longer costs any more to supply the DRAMs to accomplish ECC than it does to supply the extra bits to accomplish parity: at the 8 byte level, both parity and SEC ECC require only 8 extra bits. Furthermore, because parity bits were generally specialized DRAMs (either x1 DRAMs or quad-CAS DRAMs), and ECC checkbits are generally the same DRAMs that are used for data, an 8 byte ECC memory subsystem will actually *cost* less than an 8 byte parity subsystem. This plus the advent of dense gate arrays available for memory controller design have allowed SEC ECC to be added to a PC Server memory subsystem largely transparently. In fact, many of the first ECC boxes used vanilla parity SIMMs in pairs to provide the 72/64 ECC word required.

ECC Performance

The one area that is not as easy to hide in an ECC subsystem is the performance penalty. There are two separate issues to ECC performance. First, on a read, there is extra logic to traverse to implement the ECC algorithm. ECC is fundamentally a cascade of exclusive OR (XOR) blocks that are typically not the fastest gates available in an ASIC library. Many of today's systems accept an increase in processor access time as the price they have to pay to get ECC. This translates to an EDO DIMM being run at an X-3-3-3 burst rate rather than the X-2-2-2 rate it is capable of. Second, on a write, while there is additional logic to traverse for the generation of checkbits -- the complexity being less than that required in the read direction -- there is not a general loss of performance due to the ECC itself. However, there is a potentially very large loss of performance due to the fact that any write attempted that is less than the full 8 byte ECC word can not be done directly. To understand why, one must realize that the checkbits for any given ECC data field are generated over that entire field. In other words, all 8 bytes of data are taken into account in generating the 8 checkbits associated with that data. If any changes were to occur to any of the data bytes, the checkbits would no longer be correct and one would have instant gar-

bage. To avoid this, ECC systems can not support single byte writes (or for that matter, any number of bytes that is less than the full data word) directly, but must first read the whole old data word, modify the necessary byte(s) and then regenerate the checkbits across the modified 8 bytes, and then store the entire ECC word back into memory. This process is very common and is called generically a read-modify-write (RMW).⁵ The problem with this approach is that if it is not done correctly, it can have, under the worst case conditions, a disastrous effect on system performance with upwards of a 20% slowdown possible!

Clearly this level of performance degradation is unacceptable, and much time and effort has gone into developing hardware that mitigates this problem. The most common approach is to employ so called “write back” buffers, which enable the controller to temporarily store pending partial writes in the anticipation that many times the rest of the word will be written forthwith. A simple example of how effective this can be is to consider a 2-byte floppy drive controller that may be writing many hundreds of bytes of data to main memory, but only 2 bytes at a time. In this case, simply being patient and “pooling” the writes will have tremendous performance benefits because after every four 2-byte transfers from the floppy, the memory can do a normal, efficient store of 8 bytes and avoid the RMW penalty entirely. Of course the real world is much more complicated than this, but the point is with clever engineering, the ECC RMW penalty can be almost entirely eliminated.

Thus with DRAM main memory well understood, and a SEC ECC memory subsystem firmly in place, let us examine how this traditional approach can get into serious, unintended trouble.

The Dark Side of Memory Reliability

In spite of the overall excellent state of DRAM reliability, there is a dark side of the picture that few people fully recognize, even though at it’s core, it is a fundamentally basic concept. The question is quite straightforward: when a DRAM does fail, either with a hard error or a soft error, how many data bits (called DQs) stop working? This issue is of paramount importance in an SEC ECC system. If a failure affects more than one bit of an SEC ECC data word, then the ECC is helpless in fixing the failure, and perhaps even useless because it may pass the failure along with no notification to the system whatsoever that an error has occurred!

Chipkill Schemes

The possibility of a DRAM failure to cause either a system crash (uncorrectable error or UE) or a data integrity problem (undetected uncorrectable error or the “Million Dollar Check”) has been absolute anathema to the designers of main-

5. This read-modify-write is not identical with the read-modify-write found in DRAM data sheets, although on DIMMs, the DRAM RMW could be used to support the controller RMW.

frame-class systems. Historically, high-end and mid-range systems have conquered this danger by three different approaches.

Architecture

For those systems requiring the highest availability, such as the S/390 class of enterprise servers, the problem of multibit or chipkill DRAM failures is handled by architectural means in the main memory (L3). The memory subsystem design is such that a single chip, no matter what its data width, would not affect more than one bit in any given ECC word. For example, if x4 DRAMs were in use, each of the 4 DQs would feed a different ECC word, that is, a different address of the memory space. Thus even in the case of an entire chipkill, no single ECC word⁶ will experience more than one bit of bad data -- which is fixable by the SEC ECC -- and thereby the fault-tolerance of the memory subsystem is maintained.

The downside of this common approach is that any given data access, either read or write, is by nature 4 times larger than it would ordinarily be. There is therefore not only a penalty to be paid for read-modify-write operations on data less than 8 bytes, but there is the same penalty for any write of less than four times 8 bytes, or 32 bytes. This kind of interleaved approach likewise causes all hardware upgrades to be done in sets of four, which could present a minimum upgrade, or granularity, problem to the customer. In spite of these drawbacks, this approach is the most commonly used, spanning the range from the afore-said S/390 systems to the high-end AS/400 midrange systems down to the highest end of the PC Server range, such as the HP Netserver LX. Ironically, the now-considered-lowly PC Server 195 that IBM developed in conjunction with Parallax Corporation and was available in 1992 had chipkill protection using a variation of this scheme: it simply used only x1 DRAMs to automatically gain chipkill fault tolerance! This was not the only box to use this approach. The add-on DASD units for mainframes made by EMC also used this approach exclusively to obtain chipkill protection.

Robust Codes

A second way of providing chipkill correction in the mainframe world is by use of a very wide ECC word, usually 16 bytes or wider, and using a very robust ECC algorithm. This was done occasionally in the so-called expanded store or L4 of the mainframe. This scheme takes advantage of the fact that as ECC words increase in width, the efficiency of a given number of code checkbits increases. As mentioned earlier, that is the reason it was so easy to switch to ECC when an 8-byte bus was adopted: the bit overhead to perform SEC ECC at the 8-byte level is the same as it is to perform parity across 8 bytes, namely, only 8 extra bits are required. The downside of this approach is that any writes less than the full ECC word width will have to be performed as RMWs, also as mentioned above. Mitigating this effect for L4 applications is the fact that most transfers to and from this high level of memory are done in big blocks, so the chances are that a partial write will only have to be done at the end of a transfer, where the

6. I am using "word" in a generic sense; the actual number of bytes in an ECC "word" could be 4, 8, 16, or greater, and would be referred to in more specific literature as a double-word, quad-word, etc.

end of the data stream is most likely not to align with a ECC word boundary. Of course, combinations of the two methods can be employed if the downsides of the RMW penalty, minimum granularity, and memory subsystem complexity can be accommodated.

Ignore

The third way of handling chipkills is to accept the fact that they will happen with some small but finite frequency and to be satisfied with allowing them to cause a UE but not a data integrity problem. That is, utilize an ECC algorithm that will support chipkill detect, but no chipkill correct. In this manner, a simpler architectural design of the memory subsystem is facilitated with a minimal amount of extra checkbits and thus DRAM overhead. In years past, this approach has been satisfactory for many low-end to midrange systems because of the low proportion of multibit failure mechanisms in relation to the total failure rate. Some examples of systems that utilized this approach are PS/2's that support a x39 SIMM, almost all of the RS/6000's that have been shipped and utilize a x39 SIMM, and more recently, the Pentium Pro itself claims an ECC that supports chipkill, or packet, detect. Additionally, these codes are being expanded to provide SEC with error location capability of a subsequent chipkill.⁷ However, even with this progress, this scheme, while acceptable in most low-end markets in the past, is very vulnerable to the evolutionary and sometimes subtle changes occurring to DRAM architectures that can make it a dangerous choice in the future for systems upon which customers are "betting their business" on not having any down time.

A clever idea but...

An alternative way of protecting a memory subsystem from chipkills has been employed by Compaq in some of their PC Servers and dubbed "Advanced ECC." This scheme is described in United States Patent #5,490,155⁸, and allows a system to achieve chipkill protection by interleaving two banks of 72 bits each. To accomplish this, two bits from a given x4 DRAM are combined with 2 bits from an associated DRAM on the other bank. In addition, the 72/64 ECC is structured such that it can *correct* up to two adjacent bits. In this manner, if a chipkill occurs, then two of the bits are corrected in one ECC word and two of the bits are corrected in another ECC word. This partitioning thereby allows an ECC algorithm that can normally only correct a single bit error to provide chipkill correction with no more DRAM overhead than is required to support parity! In fact, the systems that initially supported this concept were designed to use x36 parity SIMMs as the memory module of choice.

... no free lunch

Unfortunately, there is no such thing as a free lunch. The cost of achieving 2-bit correct in a 72/64 code is *losing the assured detection of any further errors*.⁹

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7. M. Kitakami, *et al.*, "A Class of Error Locating Codes," IEICE Trans. Fundamentals, Vol. E78-A, No. 9, pp. 1086 - 1091 (September, 1995).
 8. D.G. Abdoo, *et al.*, "Error Correction System for N Bits Using Error Correcting Code Designed for Fewer than N Bits." U. S. Patent 5,490,155 (Feb. 6, 1996).
 9. T. R. N. Rao, *et al.*, Error Control Coding for Computer Systems, Englewood Cliffs, NJ: Prentice Hall, pp. 222 - 230, (1989).

Thus if a DRAM has failed and the code is correcting the chipkill, any subsequent single-bit error, such as a soft error due to cosmic rays, occurs, the code may not detect it and a data integrity problem would then exist. This trade-off, although clever and efficient, is not considered good RAS practice by some standards, and is therefore not recommended.

It is obvious that a variety of means exist to provide chipkill protection in computer main memory. The question becomes, "Why should this level of fault-tolerance" be extended into the PC Server space. To answer that question, we shall now examine what trends in DRAM design may have a deleterious effect on the ability of traditional SEC/DEC codes to efficaciously correct memory failures.

DRAM Specifications

As previously discussed, there are tremendous market pressures on the design of a commodity DRAM to be both highly compatible with other vendors' parts and low in cost to produce. Only by achieving both of these elements can a DRAM manufacturer be successful. In a commodity world, one is always told that second sourcing is a requirement. However, perhaps a more accurate term would be "assurance of supply," because very often the most important part of a system design, the microprocessor, is sole-sourced. Nonetheless, it is essential that commodity items be widely available and interchangeable.

Timings

DRAM specifications are the primary means by which initial compatibility is first judged. The first objective criteria examined in a DRAM specification are the timings. The timings are clearly of paramount importance, and the DRAM vendors have largely provided a standard set of timings that are compatible for all manufacturers. And while certain subtle variations will always exist, especially when a new generation or product type is first available,¹⁰ timings quickly settle into a predictable mold.¹¹

Currents

The second parameter specified, and of increasing importance to most systems, is current. The I_{CC} parameters are key to battery life in portables, power supply design in desktops, and battery-backup capability in servers. These

10. The initial version of the SDRAM specification, for example, was more widely variant than usual due to the significant changes encountered in moving to a synchronous interface and the lack of clear market direction. To address these first discrepancies, the system vendors drove commonality for second and third generation devices and have gone so far as to start to standardize the key timing parameters in JEDEC, which is a device and module standardizations body under the auspices of the EIA (Electronics Industries of America) organization.

11. It should be noted that compatibility of timing parameters does not guarantee interoperability. The reasons why system vendors have to spend millions of dollars on compatibility testing on a system by system and vendor by vendor basis is beyond the scope of this paper.

parameters are clearly specified and easy to measure. Like timings, they provide a means of comparing various vendors' products and driving consistency to the system designer's satisfaction.

Reliability

While timings and currents are easily specified and verified, reliability is a much different consideration. By its very nature, defect-driven failure rate is probabilistic and statistical. One can not put a DRAM on a tester and get a go/no-go test result in a few seconds. Reliability is not generally specified in an application specification. And, in fact, also by nature, and because the actual defect densities that drive failure rate are in general excellent -- that is very low -- the measurement and validation by the DRAM vendor of their stated reliability is done by analytical means, accelerated testing and inference. To further compound the problem, and once again by the nature of the subject, the better the reliability, the more difficult it is to verify the stated failure rate. A typical quality report may show several thousand device samples spread over a dozen or two test cells (in reality, many of the samples are reused over several test cells) *and not have a single failure!*¹² While this result is a statistically valid confirmation of a reliability probability, it is rather unsatisfactory in terms of being able to empirically corroborate a specification -- as can easily be done for timings and current.

While the above-mentioned approach to the verification and validation of quoted hard error failure rates may be unsatisfactory, it is nonetheless considered to be valid. The acceleration factors associated with various stress cells, such as 125°C and 7.0V (for a 5V part) are well known, discussed, and debated in the reliability community. However, an entirely different situation exists for determining soft error rate. Unfortunately, even the fundamental causes for SER are not that well understood,¹³ although there is a growing awareness of the roles of alpha particles and cosmic rays in causing DRAM and SRAM soft errors¹⁴. The confusion about this issue lies in its historical development and original solutions.

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12. Y. H. Jin, "Qualification Summary for the Goldstar 16M DRAM," LG Semicon, Ltd., (January 10, 1995).
 13. For the typical understanding of DRAM SER see: S. Schaefer, "DRAM Soft Error Rate Calculations," Micron Design Line, Volume 3, Issue 1 (1Q94).
 14. For a more detailed discussion of the emerging understanding of cosmic rays in causing DRAM soft errors see: T. J. O'Gorman, "The Effect of Cosmic Rays on the Soft Error Rate of a DRAM at Ground Level," IEEE Trans. on Electron Devices, Vol. 41, No. 4 (April 1994).

DRAM Soft Errors - Alpha-particles

Some twenty years ago, a crisis emerged in the semiconductor RAM industry because it became well-known that alpha-particles could cause an unacceptably high rate of soft errors in 16Kb DRAMs¹⁵. This watershed discovery by Intel caused all DRAM manufacturers to examine both the purity of their materials and the design of their DRAMs. The nature of alpha-particles is such that they are relatively low energy -- able to be stopped by a thin coating of a material whose density is not much more than that of a sheet of ordinary writing paper. Thus it is clear that for alpha-particles to cause a DRAM soft error, they need to be generated in near proximity to the DRAM surface itself. This being the case, the means of stopping alpha-particle soft errors is simply to maintain chemical purity in the silicon processing steps and prevent the use of radioactive materials in the packaging and attachments. While this sounds fairly straightforward, there are many horror stories regarding the contamination of processing and packaging materials.¹⁶ Other DRAM vendors, such as Micron Semiconductor, Inc., have also reported techniques to monitor and control alpha-particle contamination.¹⁷

In light of the controllable nature of alpha-particle soft errors, it is not surprising that, for the most part, the industry vendors have, in effect, called the problem solved. Literature from both DRAM suppliers and DRAM consumers indicates that prevailing wisdom considers the issue dead. In conjunction with the already excellent hard error rate of today's DRAMs, this view of soft errors being a non-problem manifests itself most prominently in influencing the industry trend to drop parity¹⁸. The argument is that, for example, a 16MB memory subsystem built with 4Mb technology would experience a soft error due to alpha-particles only every 16 years!¹⁹ With this kind of thinking prevalent in the industry, it is no wonder that parity is, for all practical purposes, a dead-end product offering.

The only problem with the whole direction of the industry is that alpha-particles are only a small fraction of the cause of DRAM soft errors!

15. T. C. May, et al., "Alpha-Particle-Induced Soft Errors in Dynamic Memories," IEEE Trans. on Electron Devices ED-26, 2 (1979).

16. For an excellent overview of IBM's experiences in this area see: J. F. Ziegler, et al., "IBM Experiments in Soft Fails in Computer Electronics (1978 - 1994)," IBM J. Res. Development, Vol. 40, No. 1, pp. 3 - 18 (January 1996).

17. A. Ditali, et al., "Monitoring Alpha Particle Sources During Wafer Processing," Semiconductor International, Vol. 16, No. 7, pp. 136 -140 (June 1993).

18. See for example: Micron Semiconductor Technical Note, "DRAM Considerations for PC Memory Design," TN-04-15, pp 1 - 3 (April 1994);

19. Intel White Paper, "Evaluating the Need for Parity in Desktop PCs," Intel Apps Fax-Back No. 7546, pp. 1 - 11 (May 1995).

DRAM Soft Errors - Cosmic Rays

Once the discovery of alpha-particle-induced DRAM soft errors was made, IBM researchers began investigating the potential of terrestrial cosmic rays in causing a similar class of soft errors, or single event upsets (SEU) as they are sometimes called. The IBM investigations spanned many years and several sites, but the clear leader in this line of investigation was Dr. J. F. Ziegler of the IBM Watson Research Center in Yorktown Heights, New York. Dr. Ziegler was a guest editor of a recent issue of the *IBM Journal of Research and Development* that was entirely devoted to the subject of cosmic rays and their relation to semiconductor soft errors.²⁰ This landmark contribution to the understanding of cosmic rays and their influence on soft errors is an outstanding reference on the subject. In addition, it presents significant data that absolutely and with finality describes the pervasive effects of cosmic rays on DRAMs that heretofore has been classified proprietary and thus not fully divulged to the industry at large.

Documentation

One example of the magnitude of the cosmic ray soft error phenomenon demonstrated that with a certain sample of non-IBM DRAMs the soft error rate as measured under purely real life conditions, and with the benefit of millions of device hours of testing, the soft error rate at sea level was measured at 5950 FIT per chip. When the exact same test setup and DRAMs were moved to an underground vault, shielded by over 50 feet of rock, which effectually eliminates all cosmic rays, *absolutely ZERO fails were recorded!*²¹ Not only does this result emphatically validate the existence of a significant soft failure rate due to cosmic rays, but it simultaneously eliminates the possibility that alpha-particle soft error is even a contributor in the same order of magnitude because of the zero fails underground.

Over the last several years, the effects of cosmic rays on DRAMs has been more thoroughly documented in the industry. The first interest has always been for space applications,²² but now research is being published corroborating the IBM results for terrestrial applications. In addition, considerable attention is being paid to cosmic ray effects in SRAMs, where their effect can be even greater than in DRAMs²³. The reason for this is that the amount of charge required to flip the cross-coupled inverters that comprise the basic SRAM cell is actually less than is required to flip a DRAM cell capacitor! As the effects of cos-

20. IBM Journal of Research and Development, Vol. 40, No. 1, pp 1 - 129 (all articles) (January 1996).

21. *ibid.*, p. 46.

22. P. Calvel, et al., "Space Radiation Evaluation of 16Mb DRAMs for Mass Memory Applications," IEEE Trans. on Nuclear Science, Vol. 41, No. 6, (December 1994).

23. C. Lage, et al., "Soft Error Rate and Stored Charge Requirements in Advanced High-Density SRAMs," 1993 IEDM Technical Digest, pp. 821 - 824 (December 1993).

mic ray soft errors are more fully understood, I expect the amount of published research for both DRAM and SRAM products to greatly increase²⁴.

Reluctance

It should be noted that in spite of the mounting evidence all pointing to cosmic ray SER as being the predominant factor in both DRAM and SRAM designs, there still exists in some portions of the industry a reluctance to embrace the cosmic ray SER model. I would speculate that the reason is twofold. First, neither DRAM producers nor DRAM customers have much of an incentive to admit to the world that a real and significant reliability exposure exists. The random and transient nature of a soft error can be much more easily explained away by voltage spikes or unstable software (especially new releases of an operating system!) than on an inherent technology problem²⁵. Second, the DRAM producers have for so many years relied upon a validation technique of their SER that includes both accelerated and life testing that indicates *there is no problem*. This historic usage of an invalid testing methodology is gradually giving way to more realistic evaluations as is demonstrated by the growing body of work on cosmic rays. Part of the problem in the historic testing is the apparent corroboration of the alpha-particle accelerated testing with the occasional life testing that is done. Both results, however, are scaled to cycle time; the problem is that the fundamental scaling of alpha-particle SER is very different than cosmic ray SER. Thus while no one disputes the data taken, the way the data is applied to achieve a real life system SER is flawed, and the resulting SER claims are likewise flawed.

A final note on the current state of the industry's position on SER. It is very interesting and, I think, telling that almost never is there a suggestion that *for server applications* the system should not use -- at the very least -- parity protected memory. In fact, most sources of reliability data that I've seen recommend ECC protection for server applications where data integrity and high availability are of the most concern. There is no doubt that *the market has decided* that ECC is a checklist item for all but the low-end of the PC Server space. Let us now examine whether the ECC implementation of choice, the SEC/DED (single error correct/double error detect) will be efficacious in dealing with the emerging failure rate trends of future DRAMs.

24. W. R. McKee, et al., "Cosmic Ray Neutron Induced Upsets as a Major Contributor to the Soft Error Rate of Current and Future Generation DRAMs," 1996 IEEE Reliability Physics Symposium, pp. 1 - 6 (1996).

25. It should be strongly noted that a class of DRAM failures exist that are also attributed to noise or operating system instability when in fact they are real, hard defects in the silicon that have escaped to the field in spite of the manufacturer's best efforts. Depending on the state of any given vendor's DRAM test efficiency, this failure mechanism can swamp out any traditional DRAM hard or even soft error rate. Avoiding this kind of quality exposure is a continual struggle for the DRAM manufacturer. The scope of this paper limits it to consideration of real reliability failures, both hard and soft, not the prevention of manufacturing defects from escaping to the field. This would be a very interesting topic for another paper.

DRAM Failure Modes

Back in the days of the almost universal usage of x1 DRAMs, that is, the use of DRAMs that are organized with only one data input and one data output, the question of failure modes and their effect on ECC algorithms was almost entirely moot. Whether a single cell failed or the entire chip failed or any sub-component failed (such as a bitline, wordline, partial array, etc.), an SEC ECC would fix the failure and go on. As modeling techniques grew more sophisticated, the exact type of failure became more important, because a statistical simulation was performed that took into account the probabilistic distribution of fails in various segments of all the DRAMs involved in an ECC word to more accurately represent what would happen in real life.^{26 27} For example, if a single cell failed in one DRAM, the chances of it aligning (at the same address) with another random single cell fail in a different DRAM are very small. However, if one of the DRAMs has experienced a chipkill, which in this case only affects one data I/O and therefore does not overwhelm the ECC, and another DRAM has but a single, solitary cell failure, when that address is read, an uncorrectable error will occur and the system will be brought down. It should be noted that any fail type can potentially align with any other fail type to cause a UE -- including all classes of soft fails. The fact that an error will not reappear once the system has been restarted is of little consolation to the customer whose data has been lost. The general term used to relate the various probabilities of failure modes to the overall DRAM failure rate is called the *piecepart distribution*.

Pieceparts

The piecepart distribution of DRAMs is generally not a well-published piece of data. It is not a trivial task to analytically determine what the pieceparts of a new DRAM design will be. It is a downright difficult task to assure that this distribution will be evident in the field performance of one's DRAM reliability. I know of no DRAM manufacturer who will assure a piecepart distribution of their DRAMs. The data, if given at all, is provided solely for planning purposes and is not guaranteed.

With that background, it starts to become apparent why this is a critical issue for the large memory subsystems that will be implemented in the mission-critical class of PC Servers. For power and granularity reasons, the x1 DRAM that was so prevalent in the days of the 30-pin SIMM gave way almost exclusively to the x4 device on the 72-pin SIMM (although the 72-pin SIMM was often found with a x1 device being used for the parity bits -- until parity all but went away). Now the market is moving strongly into 168-pin DIMMs. These DIMMs are architected to be compatible with x4, x8, and x16 DRAMs with support extending to x32 devices in the future. ***It is therefore totally manifest that any piecepart failure mode that effects more than one DRAM DQ will overwhelm a standard***

26. M. R. Libson and H. E. Harvey, "A General Purpose Memory Reliability Simulator," IBM J. Res. Develop., Vol. 28, No. 2, pp. 196 - 205 (March 1984).

27. C. L. Chen and R. A. Rutledge, "Fault-Tolerant Memory Simulator," IBM J. Res. Develop., Vol. 28, No. 2, pp. 184 - 195 (March 1984).

SEC ECC, unless some kind of architectural provision is made, as was previously discussed. The question then becomes a simple to formulate but hard to answer proposition of, "Is the multibit failure mode of the memory subsystem I am designing acceptably low enough as to not be a problem for my customer?"

The answer to this question, which is the crux of this paper, is, I believe, "Probably 'yes' today, but definitely 'no' tomorrow!"

Multibit Failure Modes - Hard Fails

If the problem of the multibit failure piecepart rate was limited to simply the architecture change at the memory subsystem level of moving from x1 to x4 to x8 and wider DRAMs, then the issue would be well contained and relatively easy to deal with. Unfortunately, there is an underlying movement in the design practices of the DRAM device itself that severely complicates the issue.

Looking back at the design practices used in DRAMs developed primarily for mainframe applications, where reliability and compatibility to mainframe RAS and performance objectives were paramount, it becomes apparent that some of the basic trade-offs made were guided precisely by this dictum. For example, a 4Mb DRAM chip that is organized x4 can be partitioned in several ways. In order to maintain the lowest possible multibit piecepart failure rate, one scheme used was to divide the chip into four quadrants. Each quadrant would provide one of the DQs, and all of the address decoding, wordline and bitline circuitry, sense amplifiers, etc., was replicated for each quadrant. Thus if almost any defect occurred (except in the most global circuitry such as address and control receivers, master timing chain, etc.), it only affected one quadrant of the device and there was a resulting extremely good piecepart rate for fails affecting only a single bit.

Design Tradeoffs

Different but sometimes synergistic design trade-offs can be made for the high performance aspect of the mainframe DRAM design point. For example, a forerunner of the emerging double data rate (DDR) SDRAM, called toggle mode, was implemented in conjunction with the low multibit piecepart architecture. The cumulative effect of these design trade-offs was to present a DRAM that was very fast and very RAS-friendly, but also very big, very hot, and very non-standard.

When a device is targeted at a specific market, the aforementioned attributes of size, power consumption, and uniqueness are perfectly acceptable, and in some cases desirable. This is because if a special design provides a competitive advantage, then sole sourcing of a part is an advantage. However, in the commodity market, these attributes are disastrous.

In order to provide an industry standard DRAM, one whose measurable parameters such as timings and currents, all of the hundreds and hundreds of design trade-offs that must be made are geared precisely toward that end. To wit, in

today's highly competitive commodity DRAM market, design trade-offs that favor die size and power consumption will ALWAYS be made over those that favor multibit piecepart failure reduction.

Furthermore, the trade-offs are becoming more difficult as device sizes and data widths continue to increase. It has been laughingly stated that the first 4Gb DRAM die will not even fit on one's business card! The sheer length of the wordlines and bitlines in such a design drives huge capacitances. Every time that capacitance is charged and discharged, energy is expended. And, this increase in power is only partially balanced by lowering the power supply voltage -- which has very difficult problems of its own as device thresholds are approached.

Wider I/O

Additionally, wider I/O devices are becoming necessary for granularity reasons. If a 168-pin DIMM is employed, the total DIMM data width is 72 bits for an ECC system. If x4 DRAMs are employed from the 16Mb generation (4Mx4), then 18 devices are required to provide the data width, and the capacity of the DIMM is 32MB. Also, whenever the DIMM is accessed, all 18 DRAMs are activated at once. If a x8 DRAM is used, then a minimum of 9 2Mx8 devices are needed, and the capacity of the DIMM is 16MB. Even if a 32MB DIMM is built by using two banks of x8 DRAMs (the DQs are dotted together in this case), a x8-based DIMM will only need to have 9 devices activated, and the active current requirement for every access is roughly cut in half. Similar benefits accrue to x16 and even x32 DRAMs, but their usage is limited in ECC systems because while they both are integer divisors of a non-parity 8-byte interface (64 bits), neither works particularly well with the 72 bits typically required for an 8-byte ECC interface.

With the market thus driving DRAM manufacturers to include wide I/O parts in their menu, and with design trade-offs being made that favor die size and power consumption as the paramount design guidelines, it is not in the least surprising that the multibit piecepart failure rate is increasing for both increasing DRAM data width designs and increasing DRAM density designs.

One can therefore say with assurance that, in general, a shrunk 256Mb x16 DRAM will have a higher multibit failure piecepart than a x4 4Mb DRAM. The problem then becomes one of quantifying the data. Table 1 was generated from internal IBM specifications, group C reliability monitoring data, and Procurement-gathered vendor questionnaire data on this topic.²⁸

28. Customers can generally obtain limited data of this type from their DRAM suppliers by working through their Procurement organizations; the information is not generally published.

DRAM Size	x4 Multibit %	x8 Multibit %	x16 Multibit %
4Mb - vendor A	7%	7%	--
16Mb - vendor B	16%	16%	24%
16Mb - vendor C	13%	19%	19%
64Mb - vendor D	3%	12%	12%
64Mb - vendor E	13%	18%	18%

Table 1. Percentage of Total Chip Fails that Affect More Than One I/O

As can be seen, in general, the wider I/O, denser parts are more susceptible to multibit fails than the narrower, older devices. Of course, this data is just starting to emerge, and a much more complete picture will develop over the next couple of years. And while this limited data can be taken to give conflicting results if misapplied, my concern is the trend that shows an almost 3X increase in fails that will overwhelm an SEC ECC and bring a server crashing to the ground. This picture gets much worse when we consider the effects of soft errors.

Multibit Failure Modes - Soft Fails

The possibility of multibit failures extending to the soft error rate is truly significant. Some industry experts who are not even true proponents of the cosmic ray SER model nonetheless admit that soft errors can account for more than 98% of the failures experienced by any given DRAM.²⁹ It is worthwhile to investigate the effects of soft errors on SEC ECC just on that data alone.

It is predominantly accepted that, in general, the fails caused by cosmic rays or alpha-particles affect only one bit at a time. This is predicated on two factors. First, the upset event itself often affects only a single cell or bitline. The energy that causes charge to be distributed in a RAM device is present over an incredibly wide range.³⁰ Not every incident alpha-particle or cosmic-ray-produced proton or neutron has enough energy to cause flipped bits. However, as cell geometries continue to shrink, an important parameter that indicates the charge storing capability of a RAM cell, Q_{crit} is moving dangerously to an area where two phenomena can occur: the once-designed-out alpha-particles start affecting cells rather than just open bitlines, and the more energetic cosmic-ray-produced particles start causing multiple bit failures. In fact, accelerated proton beam testing has shown that a cluster of fails is sometimes produced by, osten-

29. P. Mazumder, "Design of a Fault-Tolerant Three-Dimensional Dynamic Random-Access Memory with On-Chip Error-Correcting Circuit," IEEE Trans. on Computers, Vol. 42, No. 12 (December 1993).

30. McKee et al, p. 1.

Reliability Comparison

sibly, a single SER event³¹. This leads to the second reason SER-induced fails seem to affect only one bit a time. Because the exact same architectural considerations that have lead to hard errors only affecting a single DRAM DQ are operational for soft errors, the effect of any multibit soft upsets on an SEC ECC is almost completely mitigated. Conversely, *the same architectural trade-offs that increase hard error multibit piecepart failure rates also have an equally deleterious effect on the SER pieceparts.*

Increasing Multibit?

This scenario presents a double measure of SER multibit failure rate increase. First, the raw SER component is increasing because of shrinking cell geometries and stored charge,³² and second, the architectural trade-offs are making the increased number of soft error events more likely to cause a multibit fail at the system level. The question then becomes, in light of the lack of hard data for the 64Mb shrink and 256Mb DRAMs that will be populating the next generation of PC Servers, what is the exposure to this kind of phenomenon? It has been predicted that the incident SER of a 64Mb DRAM will be double that of a 16Mb third generation shrink, and that a 256Mb DRAM will be almost quadruple that number!³³

How can all this data be digested into a realistic, rational failure rate for a PC Server?

Reliability Comparison

To make a practical reliability assessment of the effects of multibit failures on an SEC ECC system, it is necessary to make conservative, but realistic, assumptions on which to base the analysis. If all the possible bad effects are taken into account at once, the result becomes unbelievably poor and the analysis is not useful. Bounding the question on the other side would be the position that things are not getting any worse with respect to multibit failure mechanisms, and that the future will be the same as the present. Between these two extremes, there are a myriad of possible scenarios from which I have chosen one as a strawman analysis vehicle. My assumptions are:

1. PC Server Memory Subsystem consisting of 8 128MB DIMMs (1GB total)
2. DIMMs consist of 64Mb DRAMs in a x4 configuration
3. DRAM failure rate only is considered (no solder, socket, raw board, supports, etc.)

31. L. W. Massengill, "Cosmic and Terrestrial Single-Event Radiation Effects in Dynamic Random Access Memories," IEEE Trans. on Nuclear Science, Vol. 43, No. 2, pp 576 - 593 (April 1996).

32. op cit, pp. 3 - 4.

33. ibid, p. 4.

Reliability Comparison

4. Server is in continuous use (720 power-on hours per month)
5. Incident SER is 500 FITs
6. Incident HER is 25 FITs
7. *SER multibit piecepart is 4%*
8. *HER multibit piecepart is 15%*

Monte Carlo Simulation

Using these conditions, a BMRS simulation was run.³⁴ BMRS uses a Monte Carlo simulation with a random scattering of fails and monitors when any of those fails will cause an uncorrectable error. In the case of parity, all fails will cause a UE. In the case of SEC ECC, all fails affecting only one data bit are corrected, and the UE rate is determined by any left over multibit hard fails, multibit soft fails, and any alignments that may occur over time. For the chipkill-correct ECC, all single and multibit fails, both hard and soft, that occur within a single chip boundary are corrected. The only UEs occur when there is an alignment between fails in two chips.

The data is shown for three time intervals: 1 month, 12 months, and 36 months. The 1 month data point (720 hours) contains most of the initial life errors that are expected on the classic “bathtub” curve of reliability mechanisms. At 36 months, there is not yet any wearout phenomena occurring.

The data obtained from the simulation shows foremost and obviously that SEC ECC is better than parity (remember that the parity data points are for a 32MB subsystem, while the other data points are for 1GB subsystems), and that chipkill correct ECC is better than SEC ECC, in terms of improving memory reliability. Second, although not broken out in this chart, the soft error rate for ECC systems is on the order of 30X greater than the hard error rate. This is not surprising to those familiar with the full effects of cosmic ray generated soft errors. It may be surprising that the 30X occurs even when the very conservative rate of 500 FIT soft errors is chosen. Data exists that suggests some 16Mb DRAM chip designs will actually experience incident soft errors in the 24,000 FIT range!³⁵

The most compelling data gathered from the simulations, though, is the relationship between the failure rates of a 32MB parity system and a 1GB SEC ECC system. Astonishingly, they are fundamentally equivalent in causing system UEs!

34. BMRS is described in the Libson reference. Thanks to A. Brearley, of the IBM Microelectronics Division Memory Development Organization, for his helpful work in setting up and running the models.

35. J. F. Ziegler, et al., “Cosmic Ray Soft Error Rates of 16Mb Memory Chips,” IBM Research Division Research Report - submitted for publication (March 21, 1997).

Figure 1. 1GB Chipkill ECC vs 1GB SEC ECC vs 32MB Parity Reliability Comparison

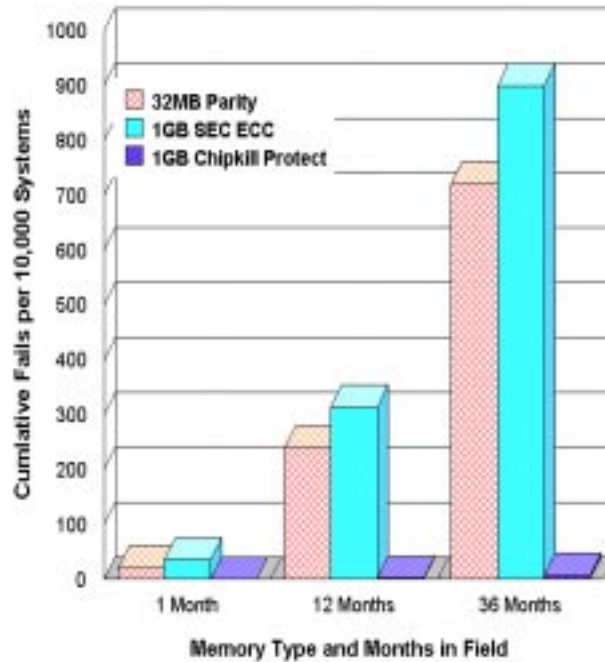


Figure 1 shows that a 32MB parity memory subsystem will fail at a rate of a little over 700 fails per 10,000 systems per three years. The 1GB SEC ECC memory subsystem will fail at about 900 fails per 10,000 systems per three years. The chipkill-correct ECC memory subsystem will fail at about a rate of 6 fails per 10,000 systems per three years. Thus there is approximate equivalence between the 32MB parity subsystem and the 1GB SEC ECC subsystem in terms of overall reliability. The chipkill-correct subsystem fails at a rate about two orders of magnitude less than the SEC ECC subsystem.

Reliability Conclusion

If the assumptions and methodology of the reliability comparison are realistic and rational, and if the demand in the marketplace for SEC ECC on almost all servers is based on expectation of failure rate and is not totally whimsical, then it would follow logically that because future PC Server market requirements will include better memory subsystem reliability, not worse, there will be a market demand for the reliability provided by chipkill correct ECC. Stated differently, ***the same market forces that drove yesterday's 32MB PC Server to include single error correction ECC as a checklist item will drive tomorrow's 1GB PC Server to include chipkill correction ECC as a checklist item.***

In retrospect, this conclusion is not surprising based on the direction set by the mainframe arena. If one concedes that the mainframe model was a precursor to the distributed, network-centric model of client-server computing, then it seems inevitable that the RAS and fault-tolerance features of the mainframe will, at some point, be demanded in the PC Server arena.

DASD Subsystem Analogy: RAID-M

Perhaps an analogous situation in the DASD subsystem is instructive. Five years ago it was difficult to find a PC Server with RAID support for the hard drive subsystem. Because it is more obvious that a separately housed hard drive can and will fail in its entirety, RAID fault tolerance was developed that allowed a level of redundancy for automatic and on-the-fly data recovery from any single hard drive failure. This feature is in addition to the layers of ECCs, sector de-allocations and data retries that already exist in the hard drive.

The capability that the data shows will be needed for the memory subsystem is fundamentally the same. In fact, speaking from a marketing perspective, it could be called RAID-M for Redundant Array of Inexpensive DRAMs for main Memory. This moniker captures the essence of chipkill correct ECC: on-the-fly, automatic data recovery for an entire DRAM fail.

Implementing RAID-M in a PC Server

The most straightforward approach to providing chipkill-correct ECC for a PC Server is to architect the memory subsystem such that only one I/O per chip is used in each of several ECC words. This does present some design hurdles, such as minimum granularity and support for wider chips -- such as the very common x8 DRAM, but for a system designed from scratch, they can be overcome.

Unfortunately, because these products are PC Servers and not other kinds of servers, the market has similar expectations of price-performance and fre-

Summary

quency of new product introductions to desktop PCs. Therefore many PC Server product offerings are designed with readily available components. For those systems designed with off-the-shelf components, that can not afford the luxury of tailoring their memory subsystem to support native RAID-M, another approach is needed. The only known alternative method is to deploy a standard memory subsystem framework and populate it with DIMMs that incorporate a retrofittable and plug-compatible on-DIMM chipkill-correct ECC. This class of product (known as "Chipkill Protect ECC DIMMs" in the IBM Microelectronics menu) provides an instantaneous upgrade from an existing SEC ECC memory subsystem to a chipkill-correct or RAID-M ECC subsystem.

Thus while providing native chipkill-correct ECC is the preferred design point, an alternative exists for those systems that, for whatever reason, can not integrally support RAID-M.

Summary

A discussion of the various elements of PC Server memory subsystem reliability was attempted in the context of the PC Server market and historical development. It was seen that the same historical market drivers that were in effect for the mainframe are in effect for the PC Server. After an excursion into the methodology behind DRAM failure rates in general, and multibit piecepart failure rates in specific, the approximate equivalence in failure rate of a 32MB parity system and a 1GB SEC ECC system was demonstrated. This was accomplished using conservative assumptions of DRAM hard and soft error rates. Finally, the logical conclusion of an emerging PC Server requirement to provide RAID-M support was presented.

The net of this analysis is that chipkill-correct ECC in a PC Server will help meet the market demand for NO DOWN TIME.

Future work in this area includes collecting further data on the trends of 64Mb DRAM reliability for both hard and soft error rates, with a particular view towards monitoring the multibit piecepart failure rates. Additionally, work needs to be done on the effects of TSOP packaging failure rates³⁶ -- which have not been factored in to this analysis.

36. J. Seyyedi, et al, "Reliability Evaluation of TSOP Solder Joints for PC Card Application," Soldering & Surface Mount Technology, No. 23 (June 1996).



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