DRAFT
SMPTE STANDARD

SMPTE 316M
Revision of
SMPTE 316M-1999

for Television Digital Recording — 12.65-mm Type D-9 Component Format — Video Compression — 525/60 and 625/50

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1 Scope

This standard specifies the content, format, and recording method of the data blocks containing video, audio, and associated data that form the helical records on 12.65-mm tape in cassettes. In addition, it specifies the content, format, and recording method of the longitudinal record containing tracking information for the scanning head associated with the helical records, cue audio, and control tracks.

One video channel and four independent audio channels are recorded in the digital format. Each of these channels is capable of independent editing.

The video channel records and reproduces a component television signal in the 525-line system with a frame frequency of 29.97 Hz (hereafter referred to as the 525/60 system) and the 625-line system with a frame frequency of 25 Hz (hereafter referred to as the 625/50 system).

Intraframe bit-rate reduction is applied to video data prior to recording.

2 Normative references

The following standards, through reference in this text, constitute provisions of this standard. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

SMPTE 12M-1999, Television, Audio and Film — Time and Control Code

ITU-R BT.470-7 (02/05), Conventional Analogue Television Systems

ITU-R BT.471-1 (07/86), Nomenclature and Description of Colour Bar Signals

ITU-R BT.601-5 (10/95), Studio Encoding Parameters of Digital Television for Standard 4:3 and Wide-Screen 16:9 Aspect Ratios

3 Acronyms

AAUX	Audio auxiliary data
AP1	Audio application ID
AP2	Video application ID
AP3	Subcode application ID
APT	Track application ID
Arb	Arbitrary
AS	AAUX source pack
ASC	AAUX source control pack
B/W	Black-and-white flag
CGMS	Copy generation management system
DBN	DIF block number
DCT	Discrete cosine transform
DIF	Digital interface
DSF	DIF sequence flag
ECC	Error correction code
EFC	Emphasis channel flag
EOB	End of block
IDP	ID parity
ITI	Initial track information
LF	Locked mode flag
OM	Overwrite margin
QNO	Quantization number
QU	Quantization
Res	Reserved for future use (default value shall be set to 1)
SMP	Sampling frequency
SSA	Start sync area
SSYB	Subcode sync block number
STA	Status of the compressed macro block
Syb (SYB)	Sync block number
TF	Transmitting flag
TIA	Track information area
Trp	Track pair number
VAUX	Video auxiliary data
VLC	Variable length coding
VS	VAUX source pack
VSC	VAUX source control pack
VSM	Vibrating sample magnetometer

4 Environment and test conditions

4.1 Environment

Tests and measurements made on the system to check the requirements of this standard shall be carried out under the following conditions:

Temperature:	20°C ± 1°C
Relative humidity:	(50 ± 2) %
Barometric pressure:	86 kPa to 106 kPa

Tape conditioning:	Not less than 24 h
Tape tension:	0.3 N to 0.45 N (measured at the entrance of the drum)

4.2 Reference tape

Blank tape for reference recordings shall be available from any source meeting the tape characteristics as defined by this standard.

4.3 Calibration tape

The calibration tapes meeting the requirements of 4.3.1 and clause 5 should be available from manufacturers who produce digital tape recorders and players in accordance with this standard.

4.3.1 Record locations and dimensions

Tolerances shown in table 1 will be reduced by 50%.

4.3.2 Calibration signals

Video, audio, and cue channels shall be recorded on the calibration tape:

Video:	100/0/100/0 color bars
Audio and cue:	1 kHz tone at 20 dB below full scale

5 Video tape

Window and label areas shall be as specified in figures 2 and 3 .

5.1 Base

The base material shall be polyester or its equivalent.

5.2 Width

The tape width shall be 12.650 mm ± 0.010 mm.

5.3 Width fluctuation

Width fluctuation of the video tape shall be less than 6 μm.

5.4 Reference edge straightness

Maximum deviation of the reference edge straightness shall be 6 μm peak to peak. Edge straightness fluctuation is measured at the edge of a moving tape positioned by three guides all having contact on the same edge of the tape. The distance between guides is 85 mm from the first to second guide, and 85 mm from the second to third guide. Edge measurements are averaged over a 10-mm length of tape. Measurements are made at a point 5 mm in the direction toward the first guide from the midpoint between the first and second guides.

5.5 Tape thickness

The tape thickness shall be 14.4 μm ± 0.5 μm or 12.4 μm ± 0.4 μm.

5.6 Transmissivity

Transmissivity shall be less than 1.2%, measured over the range of wavelengths 800 nm to 1000 nm.

5.7 Yield strength

The yield strength shall be 18 N or more by the following test method: Fix one end of a sample tape with a length of 200 mm and pull the other end at a speed of 100 mm per minute. The yield strength is the force at which 5% elongation is observed.

5.8 Magnetic coating

The magnetic layer of the tape shall consist of a coating of metal particles or equivalent, and the coercivity shall be class 1800 (approximately 1800 Oe / 143,000 A/m) with an applied field of 800,000 A/m (10,000 Oe) as measured by a vibrating sample magnetometer (VSM).

6 Helical recording — Physical characteristics

6.1 Tape speed

The tape speed shall be 57.737 mm/s for the 525/60 system and 57.795 mm/s for the 625/50 system. The tolerance is ± 0.5%.

6.2 Sectors

Each recorded track contains ITI sectors, audio sectors, video sectors, and subcode sectors.

6.3 Record location and dimensions

6.3.1 Location and dimensions of recorded tracks

Record location and dimensions for continuous recording shall be as specified in figure 1 and table 1. In recording, sector locations on each helical track shall be contained within the tolerance specified in figure 2 and tables 2 and 3. Sector locations are derived from clause 7, figure 5, and the total length of the helical track (L).

The reference edge of the tape and dimensions specified in this standard shall be the lower edge as shown in figure 1. The magnetic coating, with the direction of tape travel as shown in figure 1, is on the side facing the observer.

6.3.2 Erasure

Full erasure is necessary prior to recording. In addition, flying erasure is also required in insert editing.

6.3.3 Track pitch

As indicated in figure 1, the pitch between helical track pairs shall be 40 µm, with a guard band of a nominal 6 µm between track pairs. Track pairs consist of two nominally equal width tracks.

6.4 Helical track record tolerance zones

The lower edges of the upper heads of any two consecutive track pairs shall be contained within the pattern of the two tolerance zones defined in figure 2. Each zone is defined by two parallel lines which are inclined at an angle of 5.95892° with respect to the tape reference edge. The centerlines of all zones shall be spaced in accordance with figure 2. These zones are established to contain track angle errors and track straightness errors, and maintain vertical head offset tolerance.

6.5 Relative positions of recorded information

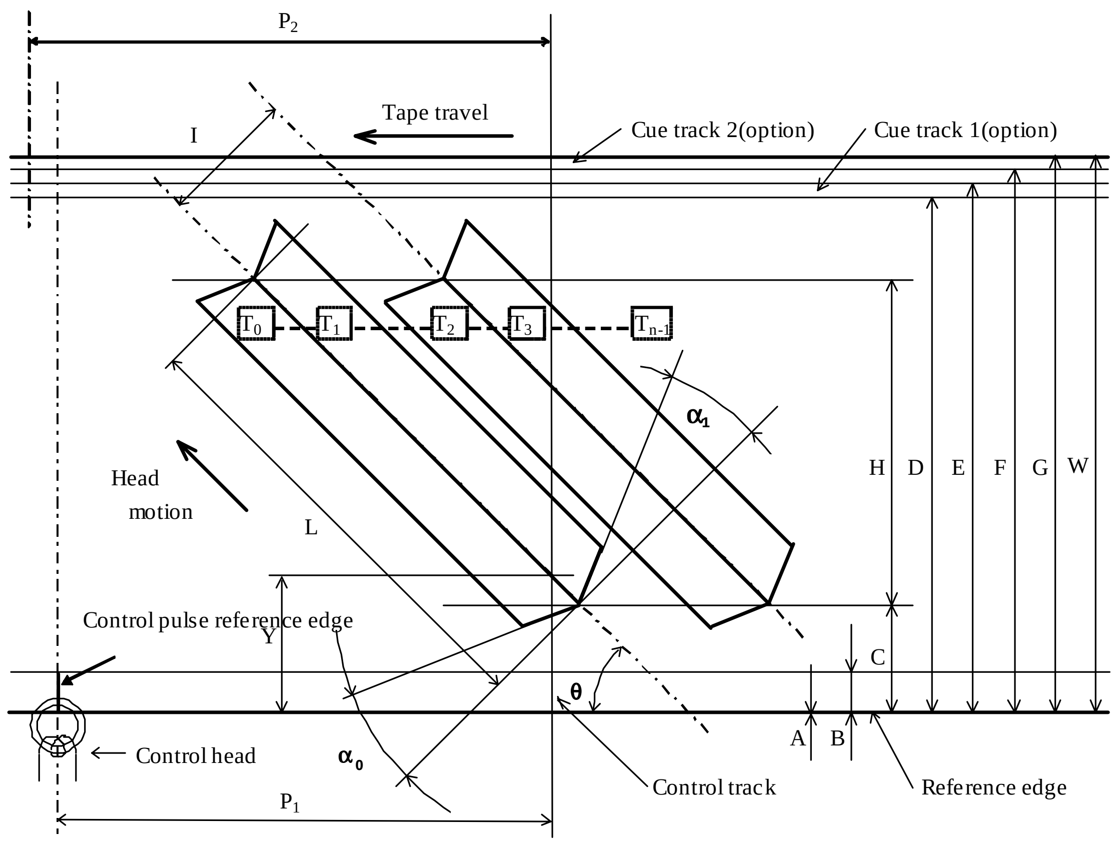
6.5.1 Relative positions of longitudinal tracks

Audio, video, control track, and cue track with information intended to be time coincident shall be positioned as shown in figures 1 and 3. Specifications in figures 1 and 2 are defined in tables 1 and 2.

6.5.2 Program area reference point

The program area reference point is determined by the intersection of a line parallel to the reference edge of the tape at distance Y from the reference edge and the lower leading edge of the odd track (see figure 1).

The relationship between the reference point and the program track data is specified in clause 7.



NOTE – Numbers of tracks in a frame = 10 for 525/60 system, 12 for 625/50 system

Figure 1 – Location and dimensions of recorded tracks

Table 1 – Record location and dimensions

Dimensions			Nominal		Tolerance
			525/60	625/50	
A	Control track lower edge	mm	0	←	Basic
B	Control track upper edge	mm	0.750	←	± 0.050
C	Program area lower edge	mm	1.710	←	Derived
D	Cue track 1 lower edge	mm	11.650	←	± 0.050
E	Cue track 1 upper edge	mm	12.000	←	± 0.050
F	Cue track 2 lower edge	mm	12.300	←	± 0.050
G	Cue track 2 upper edge	mm	12.650	←	See note
H	Program area width	mm	9.244	9.253	Derived
I	Helical track pair pitch	mm	0.040	←	Reference
L	Helical track total length	mm	89.039	89.128	Derived
P_1	Position of control track record	mm	166.797	166.132	± 0.050
P_2	Position of cue audio track record	mm	167.350	168.150	± 0.050
Y	Program area reference	mm	1.780	←	± 0.010
W	Tape width	mm	12.650	←	± 0.010
V	Tape speed	mm/s	57.737	57.795	± 0.5%
θ	Track angle	°	5.95892	←	Basic
α_0	Azimuth angle (Even track)	°	14.976	←	± 0.150
α_1	Azimuth angle (Odd track)	°	–15.024	←	± 0.150
Note – Cue track 2 upper edge = to upper edge of tape.					

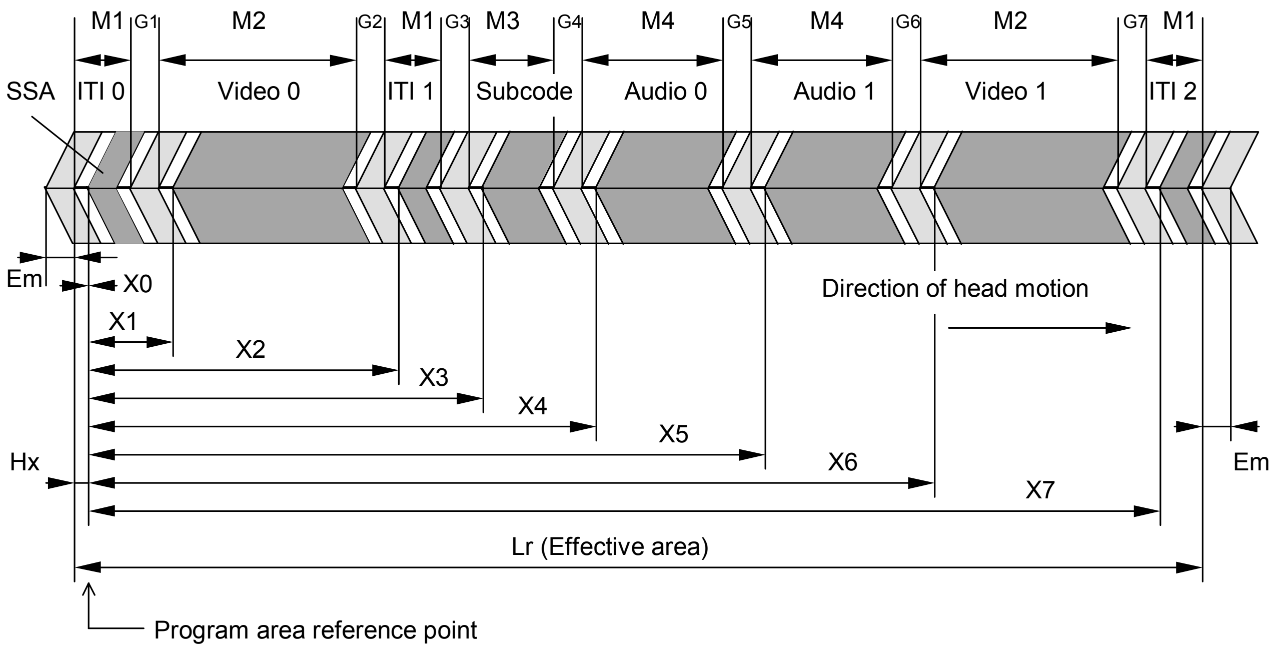


Figure 2 – Sector location from program area reference point

Table 2 – Sector location from program area reference point (525/60 system)

Dimensions in millimeters

Dimensions		Nominal	Tolerance
Em	Length of overwrite margin	0.264	—
Hx	Length of ITI pre-amble	1.057	± 0.005
X0	Beginning of SSA	0	—
X1	Beginning of video 0 sync block	2.247	± 0.061
X2	Beginning of SSA of ITI 1	37.325	± 0.237
X3	Beginning of subcode sync block	39.571	± 0.248
X4	Beginning of audio 0 sync block	41.891	± 0.259
X5	Beginning of audio 1 sync block	47.089	± 0.285
X6	Beginning of video 1 sync block	52.316	± 0.312
X7	Beginning of SSA of ITI 2	87.453	± 0.487
M1	Length of ITI sector	1.057	± 0.005
M2	Length of video sector	33.683	± 0.168
M3	Length of subcode sector	1.087	± 0.005
M4	Length of audio sector	3.950	± 0.020

Table 3 – Sector location from program area reference point (625/50 system)

Dimensions in millimeters

Dimensions		Nominal	Tolerance
Em	Length of overwrite margin	0.265	—
Hx	Length of ITI pre-amble	1.058	± 0.005
X0	Beginning of SSA	0	—
X1	Beginning of video 0 sync block	2.249	± 0.061
X2	Beginning of SSA of ITI 1	37.362	± 0.237
X3	Beginning of subcode sync block	39.611	± 0.248
X4	Beginning of audio 0 sync block	41.933	± 0.260
X5	Beginning of audio 1 sync block	47.136	± 0.286
X6	Beginning of video 1 sync block	52.369	± 0.312
X7	Beginning of SSA of ITI 2	87.541	± 0.488
M1	Length of ITI sector	1.058	± 0.005
M2	Length of video sector	33.717	± 0.169
M3	Length of subcode sector	1.088	± 0.005
M4	Length of audio sector	3.954	± 0.020

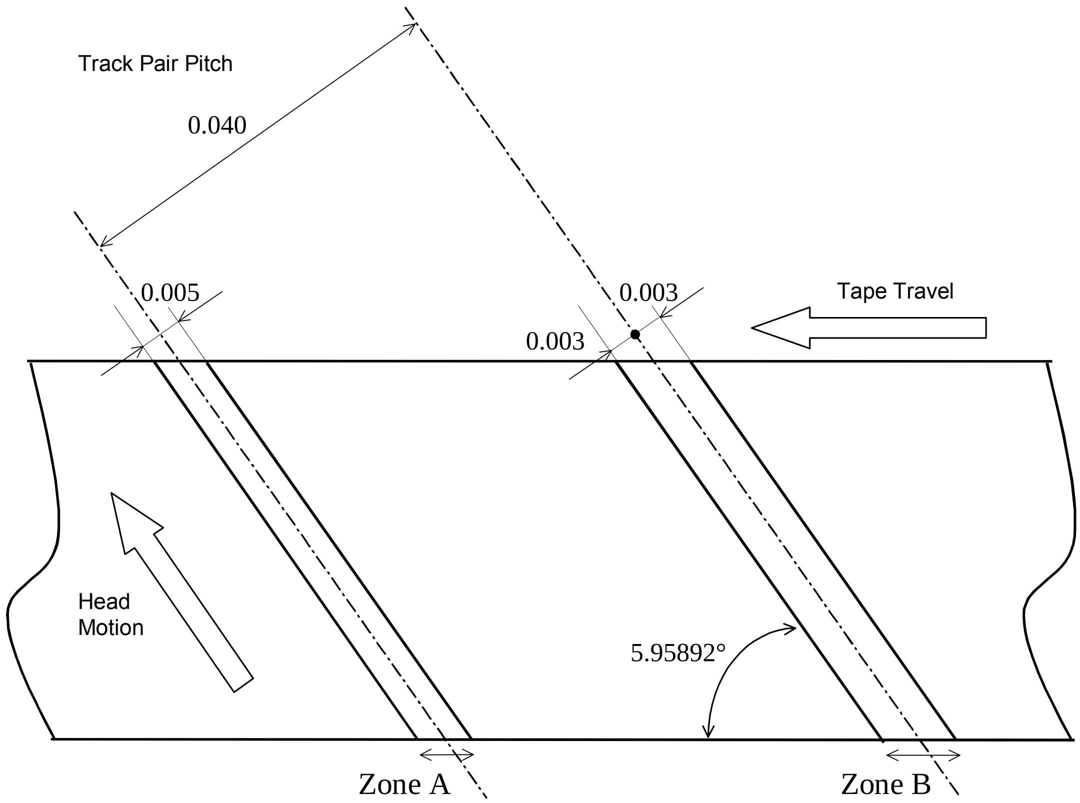


Figure 3 – Location and dimensions of tolerance zone of helical track record

6.6 Gap azimuth

6.6.1 Cue and control track

The azimuth angle of the cue and control track head gaps used to produce longitudinal track recordings shall be perpendicular to the track recording direction.

6.6.2 Helical track

The azimuth of the head gap used for the helical track shall be inclined at angles α_0 and α_1 as specified in table 1, with respect to a line perpendicular to the helical track. The azimuth of the even track of every frame shall be oriented in the clockwise direction with respect to a line perpendicular to the helical track direction when viewed from the face of the tape with a magnetic coating.

6.7 Transport and scanner

The effective drum diameter, tape tension, helix angle, and tape speed taken together determine the track angle. Different methods of design and/or variations in drum diameter and tape tension can produce equivalent recordings for interchange purposes. A possible configuration of the transport uses a scanner with an effective diameter of 62.00 mm. Scanner rotation is in the same direction as tape motion during normal playback mode. Data are recorded by two groups of heads mounted 180° apart. Figure 4 shows a possible mechanical configuration of the scanner. Table 4 shows the corresponding mechanical parameters. Other mechanical configurations are allowable provided the same footprint of recorded information is produced on the tape.

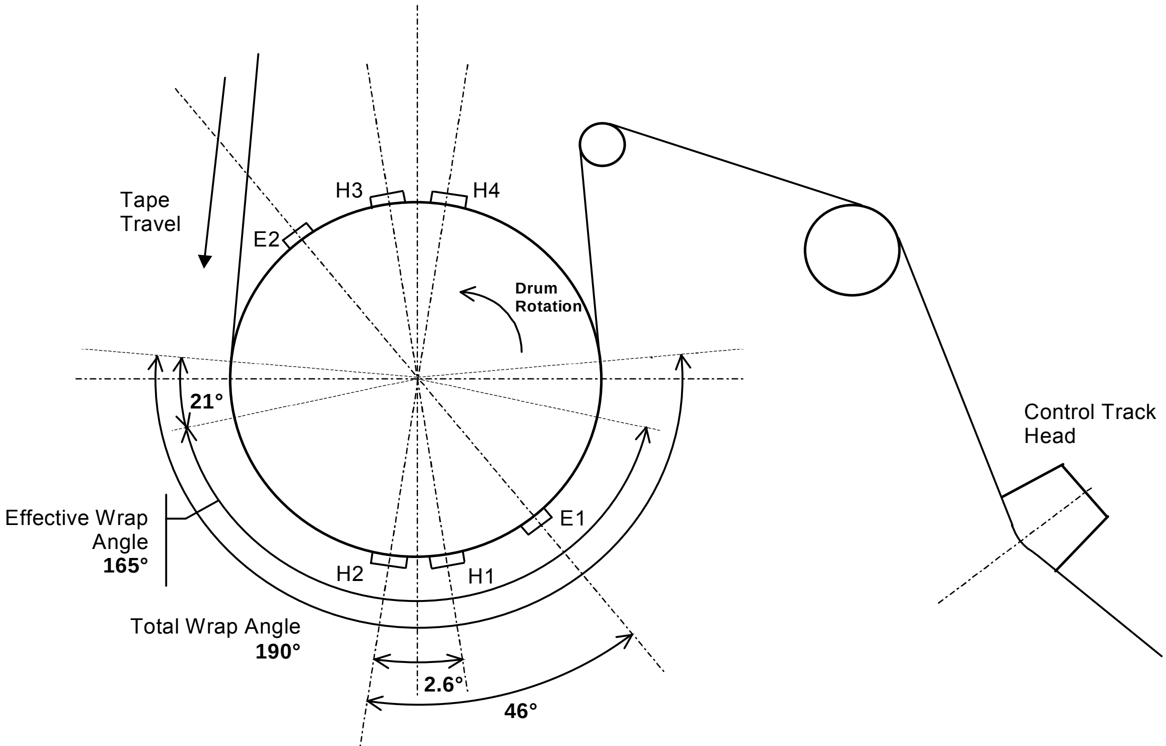


Figure 4a – Overhead view

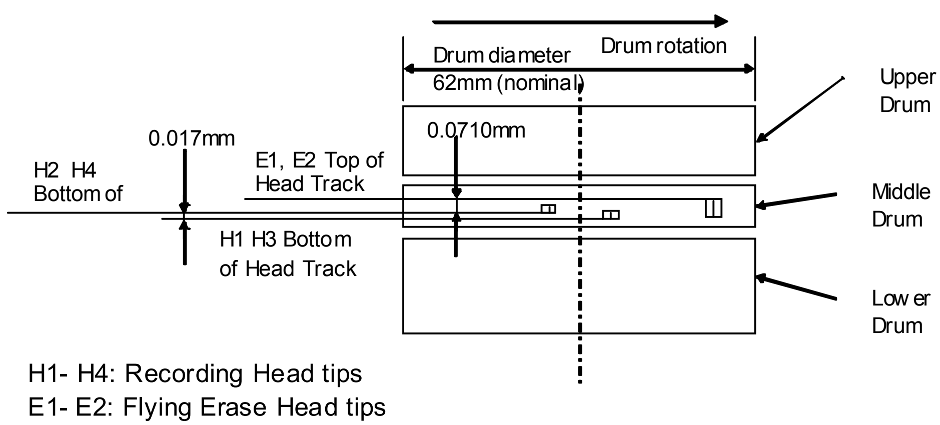


Figure 4b – Side view

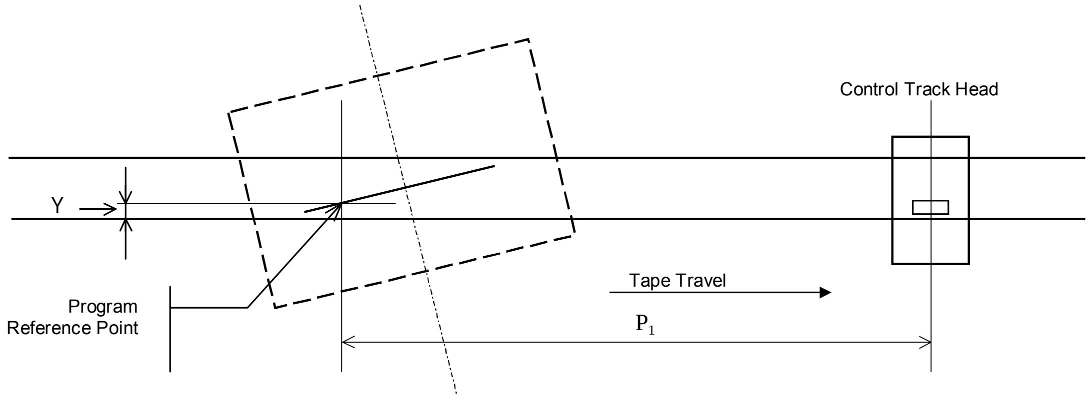


Figure 4c – Side view with control track head

Figure 4 – Possible scanner configuration (525/60 and 625/50 system)

Table 4 – Possible scanner design parameters (525/60 and 625/50 system)

Dimensions		525/60 system	625/50 system
D	Scanner diameter	62.0 mm	62.0 mm
θs	Scanner lead angle	5.93539°	5.93539°
Rs	Scanner rotation speed	(75 / 1.001) s^{-1}	75 s^{-1}
Nt	Tracks / scanner rotation	4	4
θe	Effective wrap angle	165.22°	165.22°
Tw	Recording head track width	17.0 µm	17.0 µm
NOTE – The scanner rotation speed and the tape speed should be changed in proportion to the average frame frequency of the input video signal.			

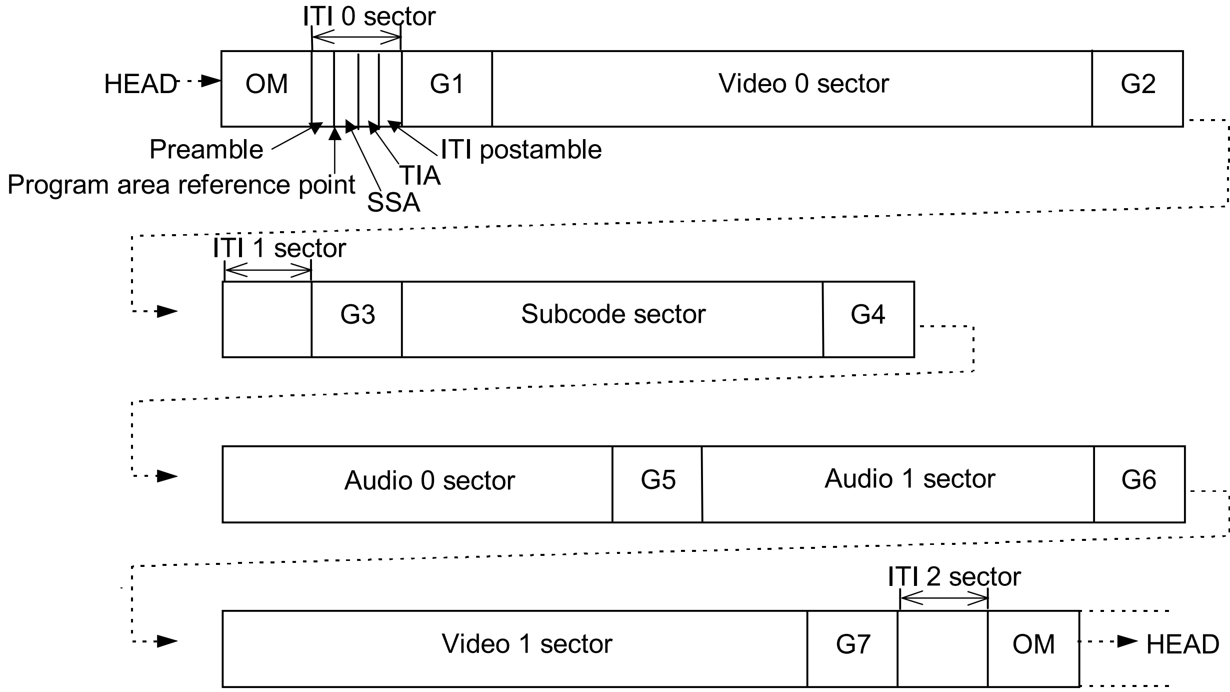
7 Helical recording — Electrical characteristics

7.1 Track contents

7.1.1 Track contents and duration

Each television frame is recorded on 10 tracks for the 525/60 system or 12 tracks for the 625/50 system. The helical tracks contain digital data of the ITI sectors, video sector, audio sector, and subcode sector. The end of the preamble and beginning of SSA in the ITI 0 sector shall be recorded at the program area reference point. The ITI sectors contain the start sync and track information. The subcode sector contains the subcode data.

Edit gaps between all sectors accommodate timing errors during editing. Figure 5 shows the arrangement of the ITI sectors, the video and audio sectors, and the subcode sector on the tape.



Sector		Bits as recorded	Bits from Program area reference point at beginning of sector
OM		900	-2,300
ITI 0	Preamble	1400	-1,400
	SSA + TIA	1920	0
	Postamble	280	1,920
Gap 1		4150	2,200
Video 0		114,700	6,350
Gap 2		4,650	121,050
ITI 1		3,600	125,700
Gap 3		4,150	129,300
Subcode		3,700	133,450
Gap 4		4,200	137,150
Audio 0		13,450	141,350
Gap 5		4,250	154,800
Audio 1		13,450	159,050
Gap 6		4,350	172,500
Video 1		114,700	176,850
Gap 7		4,850	291,550
ITI 2		3,600	296,400
OM		900	300,000
Total		303,200	

Figure 5 – Sector arrangement on single helical track (525/60 and 625/50 systems)

7.1.2 Labeling convention

The most significant bit is written on the left and first recorded to tape. The lowest numbered byte is shown at the left/top and is the first encountered in the input data stream. Byte values are expressed in hexadecimal notation unless otherwise noted. An h subscript indicates hexadecimal value.

7.2 Signal processing

7.2.1 General

The data to be recorded on the program track shall be processed through the following operations:

– Randomization (except for sync patterns)
– Modulation (except for sync patterns and IDO)
– Precoding (except for sync patterns)

All preambles, postambles, edit gaps, overwrite margins, and ITI sectors are defined as the bit streams after those processed in this specification.

7.2.2 Randomization

Bit stream data (except for sync patterns) shall be randomized. The randomizing is equivalent to performing the exclusive-or operation between the serial data stream and the serial stream generated by the polynomial function below:

$$X^7 + X^3 + 1$$

where X^i are place-keeping variables in GF(2), the binary field. The first term is the most significant and the first to enter the division computation. Randomization limits the run length of similar binary values.

7.2.3 24-25 modulation

As shown in figure 6, bit streams of randomized data shall be processed through 24-25 modulation by adding an extra bit at the beginning of previously randomized three consecutive bytes. A total of 25 bits of data is referred to as a codeword. The extra bit shall satisfy three restrictions in a precoded bit stream as follows:

Priority 1 – Avoid duplicating the sync pattern as shown in 8.2.3.1 and 8.4.3.1.

Priority 2 – Both the run length of zeros and ones shall be less than ten. If the maximum run length is greater than nine for the extra bit = 0 and the extra bit = 1, the value of the extra bit shall be chosen to make the maximum run length shorter.

Priority 3 – If priority 2 is satisfied in a precoded bit stream, the value of the extra bit shall be chosen to make the frequency characteristics of the precoded bit stream nearer to being DC free.

7.2.4 Precoding

Precoding of the 24-25 modulated data stream shall be performed by converting it to interleaved NRZI as shown in figure 7.

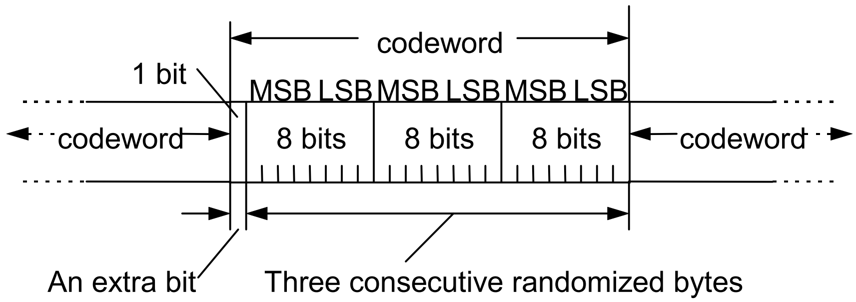


Figure 6 – Bit stream before interleaved NRZI modulation

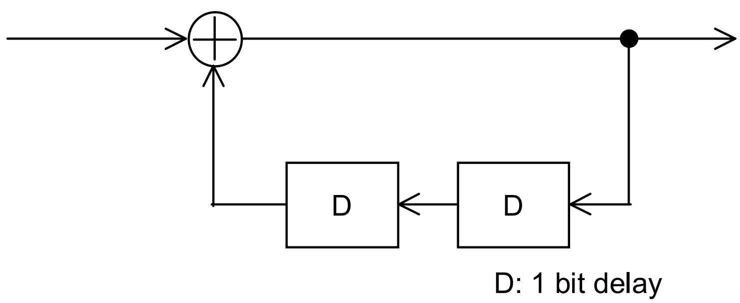


Figure 7 – Precoding

7.3 Magnetization

7.3.1 Polarity

The recorder shall reproduce signals without regard to the polarity of the recorded flux on the helical tracks.

7.3.2 Record equalization

The record current should generate a record head gap flux which is constant within ± 1 dB between 0.55 MHz and 24.75 MHz.

7.3.3 Record level

The optimum recording current that flows through either of the heads should be higher by 3 dB ± 1 dB than the level necessary to obtain maximum signal output level at 24.75 MHz.

7.3.4 Overwrite margin

In an original recording, the overwrite margin shall be recorded with concatenations of run pattern A and run pattern B defined as follows:

– Run pattern A:

MSB LSB
0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 1 1 1 0 0 0 1 1

– Run pattern B:

MSB LSB
1 1 1 0 0 0 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 1 1 0 0

In overwriting whole sectors including ITI, an overwrite margin (OM) shall be recorded so as to erase old ITI 2 data.

However, the overwrite margin (OM) need not be recorded when insert editing by using the start sync area (SSA). Since the overwrite margin (OM) has no data, it need not be recorded or produced outside the effective area.

8 Program track data

8.1 ITI sector

8.1.1 Structure

The ITI sector contains the following elements:

- ITI preamble
- Start sync area (SSA)
- Track information area (TIA)
- ITI postamble

The ITI sector is not overwritten during insert editing. Figure 8 shows the structure of the ITI sector.

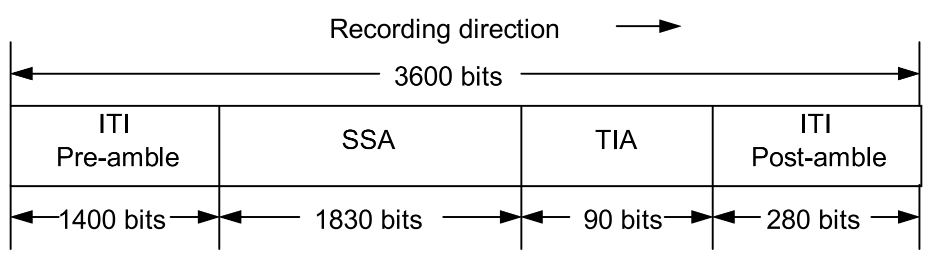


Figure 8 – Structure of ITI sector

8.1.2 ITI preamble

Codeword 1000101110 shall be recorded for 140 words as the ITI preamble.

8.1.3 SSA

The bit stream shown in table 5 shall be recorded as SSA. The bit stream shown in table 5 serves only as the sync start-up pattern and does not carry information.

8.1.4 TIA (track information area)

The bit stream specified in table 6 shall be recorded as TIA. Within each frame, the entire TIA bit stream pattern shall follow either that of table 6a or 6b (but not both).

Table 5 – Bit stream of SSA

Order of recording	Code word MSB LSB	Order of recording	Code word MSB LSB	Order of recording	Code word MSB LSB	Order of recording	Code word MSB LSB
0	0010011101	50	0101010101	100	0110101001	150	0010011101
1	0101010101	51	0010011101	101	0101011001	151	0110010101
2	0101010101	52	0101101001	102	0010011101	152	0101101001
3	0010011101	53	0101011001	103	0110101001	153	0010011101
4	0101010101	54	0010011101	104	0101101001	154	0110010101
5	0101011001	55	0101101001	105	0010011101	155	0101100101
6	0010011101	56	0101101001	106	0110101001	156	0010011101
7	0101010101	57	0010011101	107	0101100101	157	0110010101
8	0101101001	58	0101101001	108	0010011101	158	0110101001
9	0010011101	59	0101100101	109	0110101001	159	0010011101
10	0101010101	60	0010011101	110	0110101001	160	0110010101
11	0101100101	61	0101101001	111	0010011101	161	0110100101
12	0010011101	62	0110101001	112	0110101001	162	0010011101
13	0101010101	63	0010011101	113	0110100101	163	0110010101
14	0110101001	64	0101101001	114	0010011101	164	0110010101
15	0010011101	65	0110100101	115	0110101001	165	0010011101
16	0101010101	66	0010011101	116	0110010101	166	0110010101
17	0110100101	67	0101101001	117	0010011101	167	0110011001
18	0010011101	68	0110010101	118	0110101001	168	0010011101
19	0101010101	69	0010011101	119	0110011001	169	0110011001
20	0110010101	70	0101101001	120	0010011101	170	0101010101
21	0010011101	71	0110011001	121	0110100101	171	0010011101
22	0101010101	72	0010011101	122	0101010101	172	0110011001
23	0110011001	73	0101100101	123	0010011101	173	0101011001
24	0010011101	74	0101010101	124	0110100101	174	0010011101
25	0101011001	75	0010011101	125	0101011001	175	0110011001
26	0101010101	76	0101100101	126	0010011101	176	0101101001
27	0010011101	77	0101011001	127	0110100101	177	0010011101
28	0101011001	78	0010011101	128	0101101001	178	0110011001
29	0101011001	79	0101100101	129	0010011101	179	0101100101
30	0010011101	80	0101101001	130	0110100101	180	0010011101
31	0101011001	81	0010011101	131	0101100101	181	0110011001
32	0101101001	82	0101100101	132	0010011101	182	0110101001
33	0010011101	83	0101100101	133	0110100101		
34	0101011001	84	0010011101	134	0110101001		
35	0101100101	85	0101100101	135	0010011101		
36	0010011101	86	0110101001	136	0110100101		
37	0101011001	87	0010011101	137	0110100101		
38	0110101001	88	0101100101	138	0010011101		
39	0010011101	89	0110100101	139	0110100101		
40	0101011001	90	0010011101	140	0110010101		
41	0110100101	91	0101100101	141	0010011101		
42	0010011101	92	0110010101	142	0110100101		
43	0101011001	93	0010011101	143	0110011001		
44	0110010101	94	0101100101	144	0010011101		
45	0010011101	95	0110011001	145	0110010101		
46	0101011001	96	0010011101	146	0101010101		
47	0110011001	97	0110101001	147	0010011101		
48	0010011101	98	0101010101	148	0110010101		
49	0101101001	99	0010011101	149	0101011001		

Table 6 – Bit stream of TIA

Table 6a

Order of recording	Code word MSB LSB
0	0010011101
1	0101010101
2	0110010101
3	0010011101
4	0101010101
5	0110010101
6	0010011101
7	0101010101
8	0110010101

Table 6b

Order of recording	Code word MSB LSB
0	0010011101
1	0101010101
2	0110011001
3	0010011101
4	0101010101
5	0110011001
6	0010011101
7	0101010101
8	0110011001

8.1.5 ITI postamble

Codeword 1000101110 shall be recorded 28 times as the ITI postamble.

8.2 Audio sector

8.2.1 Structure

The audio sector contains the following elements:

- Audio preamble
- Audio sync block
- Audio postamble

An audio sync block contains the following elements:

- Presync block
- Data sync block
- Postsync block

Figure 9 shows the structure of an audio sector.

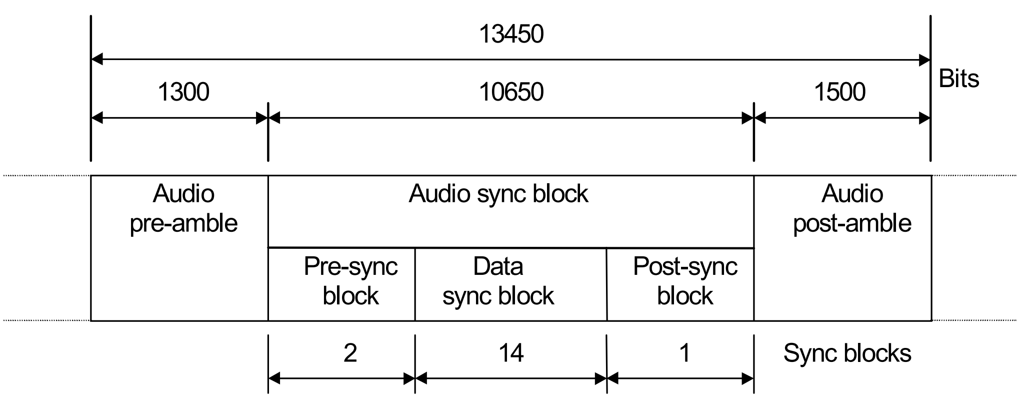


Figure 9 – Structure of audio sector after 24-25 modulation

8.2.2 Audio preamble

The two types of audio preamble patterns are defined as shown below:

– Run pattern A:

MSB LSB
0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 1 1 1 0 0 0 1 1

– Run pattern B:

MSB LSB
1 1 1 0 0 0 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 1 1 0 0

The pattern to be recorded shall be chosen from the above two patterns according to the restrictions described in 7.2.3. The length of the audio preamble shall be 1300 bits as recorded on tape.

8.2.3 Audio sync block

An audio sync block contains 2 presync blocks followed by 14 data sync blocks, followed by one postsync block. Each sync block contains 2 sync bytes, 3 ID bytes (ID0, ID1, IDP), and/or an area that can be composed either of 85 audio data bytes or an ID2 or ID3 byte. Byte position number 5 of presync and postsync are additional ID bytes (ID2, ID3). Figure 10 shows the structure of an audio sync block.

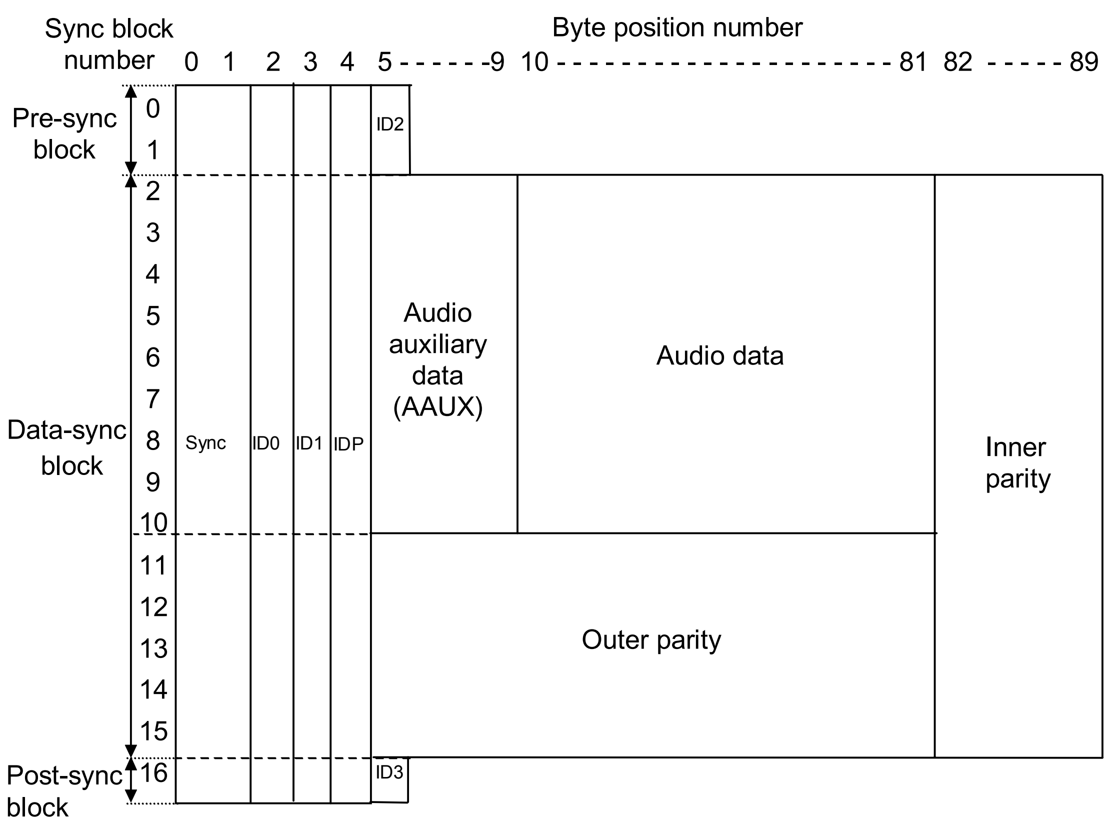


Figure 10 – Structure of sync blocks in audio sector

8.2.3.1 Sync

The two types of sync patterns after precoding are defined as follows:

	MSB LSB
Sync pattern F :	0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 1
Sync pattern G :	1 1 1 0 0 0 0 0 0 0 0 0 0 1 1 1 0

A sync pattern to be recorded shall be chosen from the above two patterns according to the priority 2 and priority 3 restrictions in 7.2.3. The length of the recorded sync shall be 17 bits.

8.2.3.2 ID

The ID sections consist of 2 ID data bytes (ID0, ID1), and 1 ID parity byte (IDP). ID data consist of application ID (AP12, AP11, AP10), sequence number (Seq3, Seq2, Seq1, Seq0), upper/lower flag (U/L), track pair number (Trp2, Trp1, Trp0), and sync block number (Syb7, Syb6, Syb5, Syb4, Syb3, Syb2, Syb1, Syb0) (see tables 7, 8, and 9).

– ID0

ID0 contains the information defined in table 10.

Table 7 – Audio application ID

Audio application ID			Format type
$AP1_2$	$AP1_1$	$AP1_0$	
0	0	0	D-9 use
0	0	1	Res
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 8 – Track pair number

			Track pair number	
Trp_2	Trp_1	Trp_0	525/60 system	625/50 system
0	0	0	Tracks 0 and 1	Tracks 0 and 1
0	0	1	Tracks 2 and 3	Tracks 2 and 3
0	1	0	Tracks 4 and 5	Tracks 4 and 5
0	1	1	Tracks 6 and 7	Tracks 6 and 7
1	0	0	Tracks 8 and 9	Tracks 8 and 9
1	0	1	Res	Tracks 10 and 11
1	1	0	Res	Res
1	1	1	Res	Res

Table 9 – Sequence number (525/60 and 625/50 system)

Seq_3	Seq_2	Seq_1	Seq_0	Meaning
0	0	0	0	Sequence 0
0	0	0	1	Sequence 1
0	0	1	0	Sequence 2
0	0	1	1	Sequence 3
0	1	0	0	Sequence 4
0	1	0	1	Sequence 5
0	1	1	0	Sequence 6
0	1	1	1	Sequence 7
1	0	0	0	Sequence 8
1	0	0	1	Sequence 9
1	0	1	0	Sequence 10
1	0	1	1	Sequence 11
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	No information

Table 10 – ID0 in audio sector

	Sync block number 0,1,11 to 16	Sync block number 2 to 10
Bit 7	$AP1_2$	Seq_3
Bit 6	$AP1_1$	Seq_2
Bit 5	$AP1_0$	Seq_1
Bit 4	Seq_0	Seq_0
Bit 3	U/L	U/L
Bit 2	Trp_2	Trp_2
Bit 1	Trp_1	Trp_1
Bit 0	Trp_0	Trp_0

The track pair number shall be defined as given in table 8.

The sequence number shall be kept at the same value during one video frame and is numbered from 0 to 11 sequentially. Table 9 shows the sequence number.

– ID1

ID1 contains the sync block number defined as follows:

MSB							LSB
Syb_7	Syb_6	Syb_5	Syb_4	Syb_3	Syb_2	Syb_1	Syb_0

Sync blocks are numbered 0 to 16 and stored in ID1 in binary notation. Sync block number = FFh means no information.

The length of ID1 shall be 8 bits before modulation.

– IDP

IDP is the parity byte of ID0 and ID1. The length of the IDP shall be 8 bits before modulation.

IDP is defined as (12, 8, 3) BCH code for which the generator polynomial is $X^4 + X + 1$. ID code is divided into two ID codewords (ID - CW0, ID - CW1) as follows:

ID – CW0: C14, C12, C10, C8, C6, C4, C2, C0, P6, P4, P2, P0

ID – CW1: C15, C13, C11, C9, C7, C5, C3, C1, P7, P5, P3, P1

The bit assignment of ID codewords is shown in table 11.

Parity bits P0 to P7 are given by the following equations:

P6 = C14 + C10 + C6 + C4
P4 = C14 + C12 + C8 + C4 + C2
P2 = C14 + C12 + C10 + C6 + C2 + C0
P0 = C12 + C8 + C6 + C0
P7 = C15 + C11 + C7 + C5
P5 = C15 + C13 + C9 + C5 + C3
P3 = C15 + C13 + C11 + C7 + C3 + C1
P1 = C13 + C9 + C7 + C1

where + is the symbol of an exclusive-or.

Modulation shall be applied together with ID1, IDP, ID2, or ID3, or first audio data.

Table 11 – Bit assignment of ID code words

Byte position number		
2 ID0	3 ID1	4 IDP
C15	C7	P7
C14	C6	P6
C13	C5	P5
C12	C4	P4
C11	C3	P3
C10	C2	P2
C9	C1	P1
C8	C0	P0

8.2.3.3 Additional ID (ID2, ID3)

Byte position number 5 of presync block (ID2) shall be set to F0h before modulation. Byte position number 5 of postsync block (ID3) shall be set to FFh before modulation. Modulation shall be applied to three-byte sequences to include: ID1, IDP, ID2, and ID1, IDP, ID3.

8.2.3.4 Composed audio data

Composed audio data containing the audio data, audio auxiliary data, inner error code, and outer error code are shown in figure 10.

The length of the composed audio data shall be 85 bytes prior to 24-25 modulation. By including the last two bytes of the ID, the length of the composed audio data shall be 87 bytes, divisible into three-byte length sections for 24-25 modulation.

8.2.4 Audio postamble

Audio postamble shall be the same as the audio preamble described in 8.2.2 (except in length). The recorded length of the audio postamble shall be 1500 bits.

8.3 Video sector

8.3.1 Structure

A video sector contains the following elements:

- Video preamble
- Video sync block
- Video postamble

A video sync block contains the following elements:

- Presync block
- Data sync block
- Postsync block

Figure 11 shows the structure of the video sector.

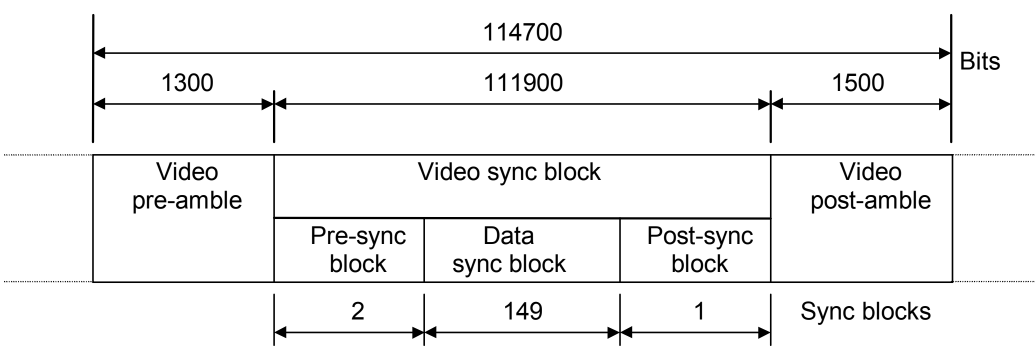


Figure 11 – Structure of video sector after 24-25 modulation

8.3.2 Video preamble

The video preamble pattern shall be the same as the audio preamble described in 8.2.2. The recorded length of the video preamble shall be 1300 bits.

8.3.3 Video sync block

The video sync block contains 2 presync blocks followed by 149 data sync blocks, followed by 1 postsync block. Each sync block contains sync of 2 bytes, ID of 3 bytes, and compressed video data of 77 bytes. Figure 12 shows the structure of a video sync block. Byte position number 5 of presync and postsync is the additional ID (ID2, ID3).

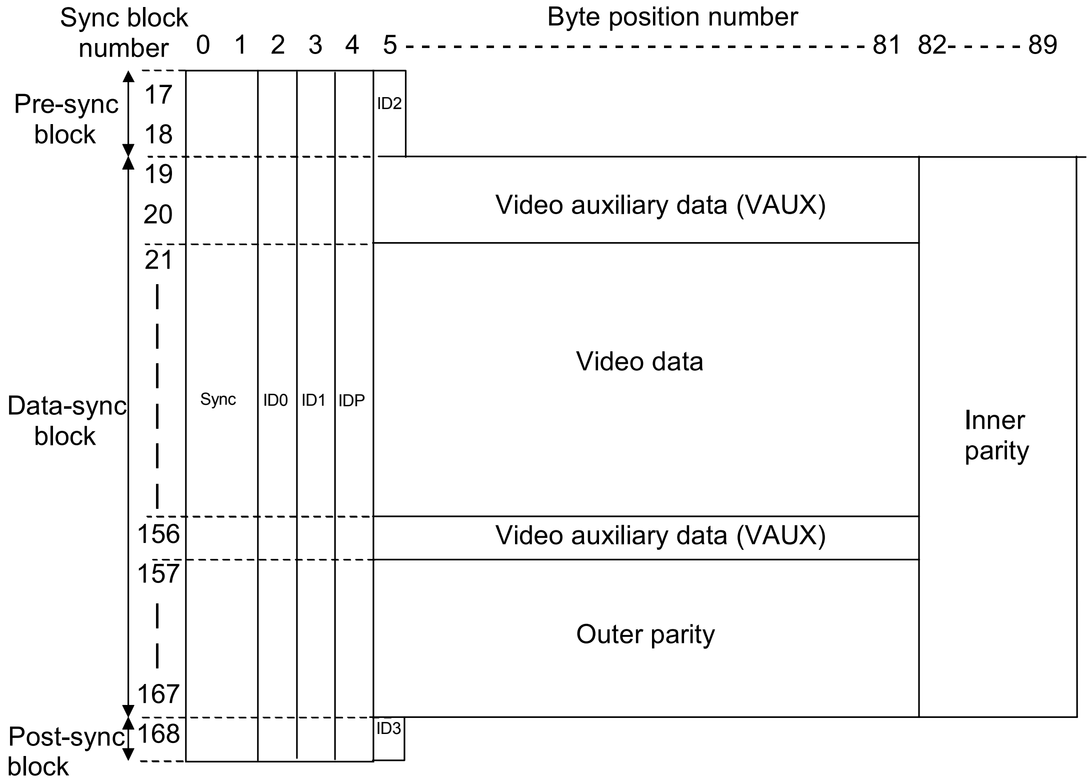


Figure 12 – Structure of sync blocks in video sector

8.3.3.1 Sync

Sync shall be the same as the audio sync described in 8.2.3.1. The recorded length of the sync shall be 17 bits.

The ID consists of 2 data bytes (ID0, ID1), and 1 ID parity byte (IDP). ID data consists of the video application ID (AP22, AP21, AP20), sequence number (Seq3, Seq2, Seq1, Seq0), track pair number (Trp3, Trp2, Trp1, Trp0), and sync block number (Syb7, Syb6, Syb5, ..., Syb0).

– ID0

ID0 contains the information defined in table 12.

The video application ID is defined in table 13. The track pair number shall be the same as in table 8. The sequence number is defined in table 9.

– ID1

ID1 contains the sync block number defined as follows:

MSB							LSB
Syb_7	Syb_6	Syb_5	Syb_4	Syb_3	Syb_2	Syb_1	Syb_0

Sync blocks are numbered 17 to 168 and are stored in ID1 in binary notation. Sync block = FFh means no information.

– IDP

IDP shall be the same as that in 8.2.3.2.

Table 12 – ID data in video sector

Bit position	Sync block number 17 to 18 and 157 to 168		Sync block number 19 to 156	
	ID0	ID1	ID0	ID1
b7	$AP2_2$	Syb_7	Seq_3	Syb_7
b6	$AP2_1$	Syb_6	Seq_2	Syb_6
b5	$AP2_0$	Syb_5	Seq_1	Syb_5
b4	Seq_0	Syb_4	Seq_0	Syb_4
b3	U / L	Syb_3	U / L	Syb_3
b2	Trp_2	Syb_2	Trp_2	Syb_2
b1	Trp_1	Syb_1	Trp_1	Syb_1
b0	Trp_0	Syb_0	Trp_0	Syb_0

Table 13 – Video application ID

Video application ID $AP2_2$	$AP2_1$	$AP2_0$	Format type
0	0	0	D9 use
0	0	1	Res
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

8.3.3.3 Additional ID (ID2, ID3)

Byte position number 5 of presync block (ID2) shall be set to $F0_h$ before modulation. Byte position number 5 of postsync block (ID3) shall be set to FF_h before modulation.

8.3.3.4 Composed video data

Composed video data containing the video data, video auxiliary data, inner error code, and outer error code are shown in figure 12. The length of the composed video data shall be 85 bytes before modulation.

8.3.3.5 Video postamble

Video postamble shall be the same as the audio postamble described in 8.2.4. The recorded length of the video postamble shall be 1500 bits.

8.4 Subcode sector

8.4.1 Structure

The subcode sector contains the following elements:

– Subcode preamble
– Subcode sync block
– Subcode postamble

Figure 13 shows the structure of the subcode sector.

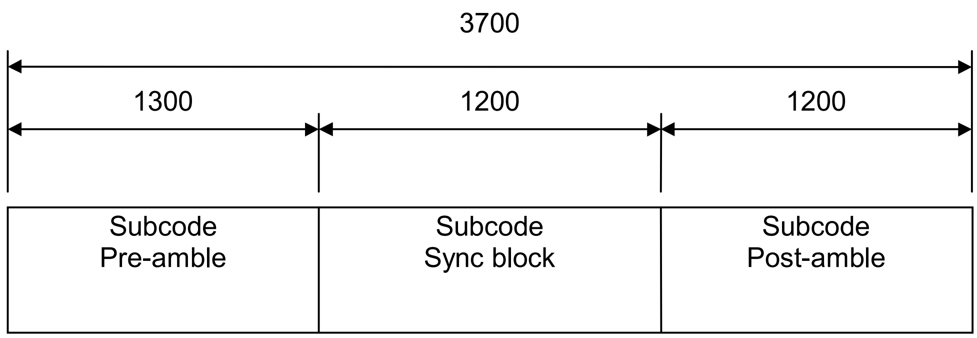


Figure 13 – Structure of subcode sector after 24-25 modulation

8.4.2 Subcode preamble

The subcode preamble pattern shall be the same as the audio preamble described in 8.2.2. The recorded length of the subcode preamble shall be 1300 bits.

8.4.3 Subcode sync block

The subcode sync block contains 12 sync blocks. Each sync block consists of a 2 byte sync word, 3 ID bytes, 5 bytes of subcode data, followed by 2 parity bytes. Figure 14 shows the structure of the subcode sync block.

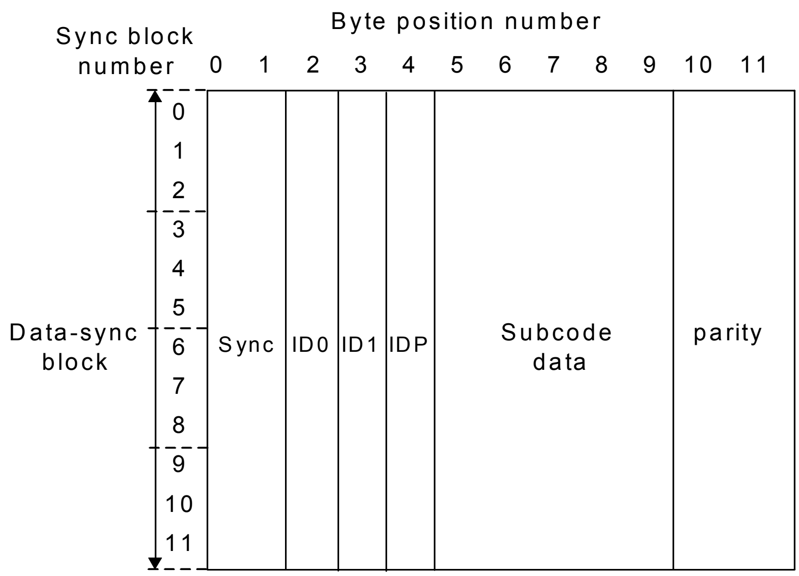


Figure 14 – Structure of sync blocks in subcode sector

8.4.3.1 Sync

The two types of sync patterns after precoding are defined as follows:

	MSB	LSB
Sync pattern D :	0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 0 1	
Sync pattern E :	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 1 0	

A sync pattern to be recorded shall be chosen from the above two patterns according to the restrictions of priority 2 and 3 described in 7.2.3. The length of the recorded sync shall be 17 bits.

8.4.3.2 ID

The ID consists of 2 data bytes (ID0, ID1), and 1 ID parity byte (IDP). They are placed in sync block byte positions 2, 3, and 4. ID parity is the same as for the audio and video sectors. ID data consist of the subcode application ID (AP32, AP31, AP30), application ID for track (APT2, APT1, APT0), first half ID (FR ID), and sync block number (Syb3, Syb2, Syb1, Syb0).

Figure 15 shows the structure of the ID data.

Sync block number	IDO								ID1							
	MSB							LSB	MSB							LSB
0	FR	$AP3_2$	$AP3_1$	$AP3_0$	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
1	FR	0	0	0	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
2	FR	0	0	0	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
3	FR	0	0	0	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
4	FR	0	0	0	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
5	FR	0	0	0	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
6	FR	$AP3_2$	$AP3_1$	$AP3_0$	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
7	FR	0	0	0	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
8	FR	0	0	0	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
9	FR	0	0	0	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
10	FR	0	0	0	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0
11	FR	APT_2	APT_1	APT_0	0	0	0	0	0	0	0	0	Syb_3	Syb_2	Syb_1	Syb_0

Where AP3: Subcode application
Syb: Sync block number
APT: Application ID for track

Figure 15 – Structure of ID data

8.4.3.2.1 ID0

FR ID (first half ID)

FR ID is an identification for the first half or the second half of the video frame data:

– FR = 1: The first half of the video frame data
– FR = 0: The second half of the video frame data

AP3: Subcode application ID

The subcode application ID is defined in table 14.

APTn: Application ID for track

APTn shall be defined in table 15. If the signal source is unknown, all bits for these data shall be set to 1. AP1, AP2, and AP3 shall be identical with APT.

8.4.3.2.2 ID1

Sync block number (Syb): The sync blocks are numbered 0 to 11, and stored in Syb in binary notation. A sync block number = Fh means no information.

8.4.3.2.3 IDP

IDP shall be the same as in 8.2.3.2.

Table 14 – Application ID of area 3

Area 3 application ID			Format type
$AP3_2$	$AP3_1$	$AP3_0$	
0	0	0	D9 use
0	0	1	Res
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	No information

Table 15 – Application ID for track

Application ID for track			Format type
APT_2	APT_1	APT_0	
0	0	0	D-9 use
0	0	1	Res
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	No information

8.4.4 Subcode postamble

The subcode postamble shall be the same as the audio postamble described in 8.2.4. The recorded length of the subcode postamble shall be 1200 bits.

8.5 Edit gap

The space between areas on a track, reserved for accommodation of timing errors during editing, is referred to as the edit gap. In an original recording, the edit gap records concatenations of run pattern A and run pattern B defined as follows:

– Run pattern A:

MSB LSB
0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 1 1 1 0 0 0 1 1

– Run pattern B:

MSB LSB
1 1 1 0 0 0 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 1 1 0 0

During an edit, the edit gap may be partially rewritten with the above concatenations. The preamble and postamble of adjacent unedited areas shall not be overwritten.

The choice of a run pattern between run patterns A and B depends only on the minimization of DC constants.

9 Longitudinal tracks

9.1 Control track

9.1.1 Method of recording

The control track shall be recorded using the hysteresis (direct recording) method.

9.1.2 Flux polarity and control pulse reference edge

The polarities of the flux shall be as shown in figure 16.

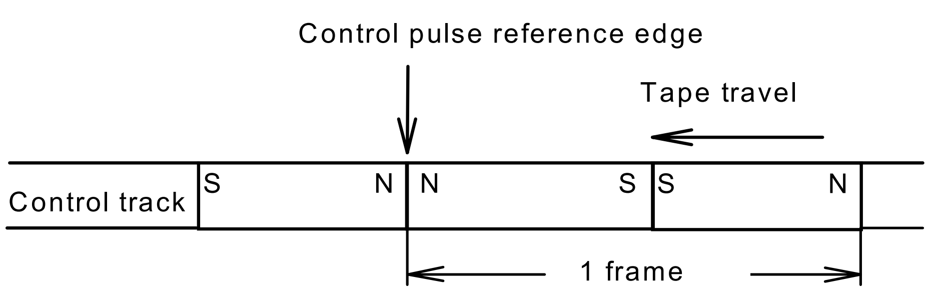
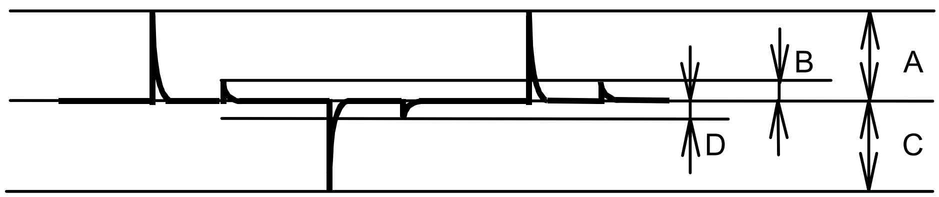


Figure 16 – Flux polarity of control track

9.1.3 Flux level

The control signal shall be recorded on the control track with sufficient current for saturation. The playback circuit shall not be impaired when the residual control signal is up to –10 dB compared with the new (overwritten) control signal, as shown in figure 17.



A or C: Newly recorded control signal
B or D: Remaining control signal after overwrite

Figure 17 – Flux levels

9.1.4 Pulse width

The period of the whole cycle of the recorded pulse shall be 33.37 ms (nominal) for the 525/60 system and 40 ms (nominal) for the 625/50 system. The rise time (10%, 90%) shall be less than 200 μs.

9.1.5 Color frame indication by nonsymmetrical duty factor

525/60 system

When color frame indication is required, the control track pulse duty factor shall be modified as indicated below:

- Color frame A – 67.5% ± 0.5%
- Color frame B – 52.5% ± 0.5%

When color frame indication is not required, the control track pulse duty factor shall be 62.5% ± 0.5% or 57.5% ± 0.5%. A pulse with a duty factor of 20% ± 0.5% can be used as the 0 frame pulse, indicating the last frame of a recorded cut.

625/50 system

When color frame indication is required, the control track pulse duty factor shall be modified as indicated below:

- Fields 1 and 2 – 70% ± 0.5%
- Fields 3 and 4 – 50% ± 0.5%
- Fields 5 and 6 – 65% ± 0.5%
- Fields 7 and 8 – 55% ± 0.5%

When color frame indication is not required, the control track pulse duty factor shall be 60% ± 0.5%. A pulse with a duty factor of 20% ± 0.5% can be used as the 0 frame pulse, indicating the last frame of a recorded cut.

9.1.6 Servo reference pulse timing

The control pulse reference edge and the program area reference point shall have the relation shown in figure 1.

9.2 Cue track

9.2.1 Method of recording

The signals shall be recorded using the nonhysteresis (AC bias) method.

9.2.2 Flux level

The recorded reference audio level shall correspond to an rms magnetic short circuit flux level of 70 nWb/m (± 20 nWb/m) of track width at 1000 Hz.

9.2.3 Relative timing

Cue information shall be recorded on the tape at a point referenced to the program area reference point as defined by dimension P2 of figure 1 and table 1.

10 Audio processing

10.1 Introduction

Four channels of audio data, each of which corresponds to one video frame period, are recorded in four audio blocks respectively. Each audio block is processed identically but independently. The audio block is composed of five audio sectors in five consecutive tracks for the 525/60 system, and six audio sectors in six consecutive tracks for the 625/50 system.

Each audio sector consists of audio data, audio auxiliary data (AAUX), and inner and outer parity data as shown in figure 10. Each audio sector is processed in a product block of 77 columns by 9 rows. Audio data are shuffled prior to the addition of AAUX and after the addition of AAUX data, error correction data are added to the product block.

10.2 Encoding mode

One channel of audio signal shall be recorded in an audio block with a sampling frequency of 48 kHz. The encoded data are expressed by twos complement representation with 16 linear bits.

10.2.1 Emphasis

Audio encoding is carried out with linear frequency characteristics or with first-order preemphasis of 50/15 µs.

NOTE – For analog-input recording, emphasis should be off in the default state.

10.2.2 Audio error code

In audio encoded data, 8000_h shall be assigned as the error code to indicate an invalid audio sample. This code corresponds to negative full-scale value in ordinary twos complement representation. When the encoded data includes 8000_h, 8000_h shall be converted to 8001_h.

10.2.3 Sample to data-byte conversion

Samples of 16 bits are defined as Dn (n = 0, 1, 2, ...) and are shuffled by each Dn unit. The 16 bit encoded data are divided into two bytes as shown in figure 18.

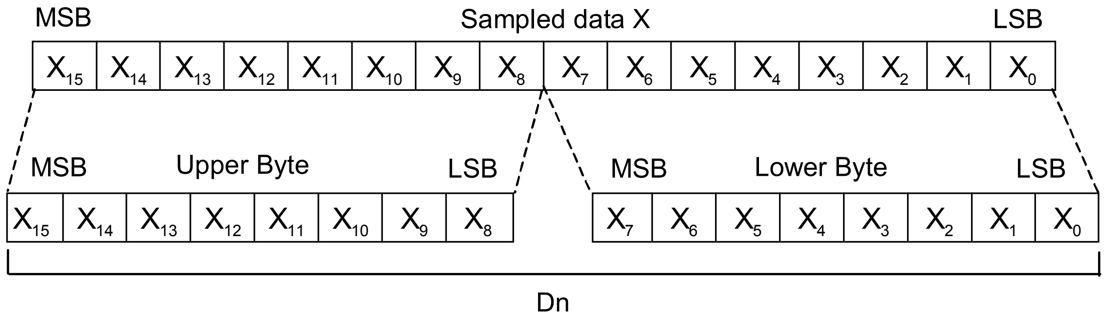


Figure 18 – Sample to data byte conversion for 16 bits

10.3 Audio channel allocation

10.3.1 Audio block

The audio block is the physical recording channel for the audio signal on tape. Four audio blocks named CH1, CH2, CH3, and CH4 are provided. The construction of these audio blocks is shown in table 16.

Table 16 – Construction of audio block

Audio block		CH1	CH4	CH3	CH2
Sector position		Sector 0	Sector 0	Sector 1	Sector 1
Track position	525/60 system	Track 0 to 4	Track 5 to 9	Track 0 to 4	Track 5 to 9
	625/50 system	Track 0 to 5	Track 6 to 11	Track 0 to 5	Track 6 to 11
Encoding mode	4ch audio	48k mode			

10.3.2 Channel allocation rule

Audio channels are defined such that all channels of audio blocks shall be recorded simultaneously. Encoded data for CH1, CH2, CH3, and CH4 correspond to encoded data X in figure 18.

10.4 Frame structure

10.4.1 Relative audio-video timing

The audio duration corresponding to one video frame duration is defined as one audio frame. The timing edge of the first preequalizing pulse of each video frame shall coincide with the audio frame within the tolerance of – 0 to + 50 audio samples. The first preequalizing pulse timing edge is located at the beginning of line 1 in the 525/60 system, and at the middle of line 623 in the 625/50 system.

10.4.2 Audio frame processing

This standard provides two types of audio frame processing modes: sequence locked mode and average locked mode. In the sequence locked mode, each video frame within the five video frame duration is assigned with a fixed number of audio samples. In the average locked mode, the number of audio samples per video frame may vary, although the long-term average samples per video frame are kept constant. The machine shall be so designed as to accept both modes. The audio sampling frequency, fs, is locked to the video horizontal scan frequency, fh, as shown below:

– fs = fh x 1144 / 375 for the 525/60 system
– fs = fh x 384 / 125 for the 625/50 system

10.4.2.1 Sequence locked mode

The number of audio samples per frame keeps a regular sequence (525/60) or fixed value (625/50) as shown in table 17.

Table 17 – Number of samples per frame (Sequence locked mode)

Mode	Samples (byte) / frame	
525/60 system	1st frame :	1,600 (3,200)
	2nd to 5th frame :	1,602 (3,204)
625/50 system	All frames:	1,920 (3,840)

NOTES

1 Each audio sample per frame in CH1, CH2, CH3, and CH4 should have the same value.

2 For postrecording, if the prerecording channel is recorded by the sequence locked mode, the postrecording channel should be recorded by the sequence locked mode too.

3 For postrecording, if the postrecording channel is recorded by the average locked mode in spite of the prerecording channel's being recorded by the sequence locked mode, the notes of the average locked mode (table 18) shall be observed.

10.4.2.2 Average locked mode

The number of audio samples per frame is variable within the range between the maximum and the minimum as shown in table 18. The average number of audio samples per frame shall be the number shown in table 18.

Table 18 – Number of samples per frame (Average locked mode)

Mode	Samples (byte) / frame		
	Maximum	Minimum	Average
525/60 system	1,620 (3,240)	1,580 (3,160)	1,601.60 (3,203.20)
625/50 system	1,944 (3,888)	1,896 (3,792)	1,920 (3,840)

NOTES

1 Each audio sample per frame in CH1, CH2, CH3, and CH4 should have the same value.

2 Even if the number of audio samples per frame is different in each audio block, the average value of the numbers shall be the same in CH1, CH2, CH3, and CH4. Therefore, the sampling frequency of the post-recording channel shall be synchronized to that of the prerecording channel.

3 The accumulated difference of values between the number of audio samples per frame in CH1, CH2, CH3, and CH4 shall not exceed the range as shown in table 19.

Table 19 – Allowance range of the accumulated difference of values between the numbers of audio samples per frame in CH1, CH2, CH3 and CH4

Mode	Allowance
525/60 system	20
625/50 system	24

In the average locked mode, the number of audio samples per frame is rounded to the nearest integer. Because of the lack of samples for filling the audio block, arbitrary values 1 or 0 shall be recorded.

10.5 Audio shuffling

Audio samples are shuffled across tracks and data sync blocks within a frame. Audio shuffling is accomplished by shuffling Dn data, a two-byte word, across sync blocks and tracks within the frame boundary.

Dn data (that is, samples at nth order [n = 0, 1, 2, ...]) within a frame are located at the position derived from the following equations:

525/60 system

Track, sector number:

Sector 0 of track number (INT(n / 3) + 2 x (n mod 3)) mod 5 for CH1
Sector 1 of track number (INT(n / 3) + 2 x (n mod 3)) mod 5 + 5 for CH2
Sector 1 of track number (INT(n / 3) + 2 x (n mod 3)) mod 5 for CH3
Sector 0 of track number (INT(n / 3) + 2 x (n mod 3)) mod 5 + 5 for CH4

Sync block number:

2 + 3 x (n mod 3) + INT ((n mod 45) / 15)

Byte position number:

10 + 2 x INT (n / 45) for the upper byte
11 + 2 x INT (n / 45) for the lower byte

where n = 0 to 1619

625/50 system

Track, sector number:

Sector 0 of (INT(n / 3) + 2 x (n mod 3)) mod 6 for CH1
Sector 1 of (INT(n / 3) + 2 x (n mod 3)) mod 6 + 6 for CH2
Sector 1 of (INT(n / 3) + 2 x (n mod 3)) mod 6 for CH3
Sector 0 of (INT(n / 3) + 2 x (n mod 3)) mod 6 + 6 for CH4

Sync block number:

2 + 3 x (n mod 3) + INT ((n mod 54) / 18)

Byte position number:

10 + 2 x INT (n / 54) for the upper byte
11 + 2 x INT (n / 54) for the lower byte

where n = 0 to 1943

Audio shuffling patterns are shown in figure 19 for the 525/60 system and figure 20 for the 625/50 system.

	j =	10, 11	12, 13	14, 15		78, 79	80, 81
	i = 2	D0	D45	D90	•••	D1530	D1575
	3	D15	D60	D105	•••	D1545	D1590
	4	D30	D75	D120	•••	D1560	D1605
Track 0	5	D10	D55	D100	•••	D1540	D1585
or	6	D25	D70	D115	•••	D1555	D1600
Track 5	7	D40	D85	D130	•••	D1570	D1615
	8	D5	D50	D95	•••	D1535	D1580
	9	D20	D65	D110	•••	D1550	D1595
	10	D35	D80	D125	•••	D1565	D1610
	2	D3	D48	D93	•••	D1533	D1578
	3	D18	D63	D108	•••	D1548	D1593
	4	D33	D78	D123	•••	D1563	D1608
Track 1	5	D13	D58	D103	•••	D1543	D1588
or	6	D28	D73	D118	•••	D1558	D1603
Track 6	7	D43	D88	D133	•••	D1573	D1618
	8	D8	D53	D98	•••	D1538	D1583
	9	D23	D68	D113	•••	D1553	D1598
	10	D38	D83	D128	•••	D1568	D1613
	2	D6	D51	D96	•••	D1536	D1581
	3	D21	D66	D111	•••	D1551	D1596
	4	D36	D81	D126	•••	D1566	D1611
Track 2	5	D1	D46	D91	•••	D1531	D1576
or	6	D16	D61	D106	•••	D1546	D1591
Track 7	7	D31	D76	D121	•••	D1561	D1606
	8	D11	D56	D101	•••	D1541	D1586
	9	D26	D71	D116	•••	D1556	D1601
	10	D41	D86	D131	•••	D1571	D1616
	2	D9	D54	D99	•••	D1539	D1584
	3	D24	D69	D114	•••	D1554	D1599
	4	D39	D84	D129	•••	D1569	D1614
Track 3	5	D4	D49	D94	•••	D1534	D1579
or	6	D19	D64	D109	•••	D1549	D1594
Track 8	7	D34	D79	D124	•••	D1564	D1609
	8	D14	D59	D104	•••	D1544	D1589
	9	D29	D74	D119	•••	D1559	D1604
	10	D44	D89	D134	•••	D1574	D1619
	2	D12	D57	D102	•••	D1542	D1587
	3	D27	D72	D117	•••	D1557	D1602
	4	D42	D87	D132	•••	D1572	D1617
Track 4	5	D7	D52	D97	•••	D1537	D1582
or	6	D22	D67	D112	•••	D1552	D1597
Track 9	7	D37	D82	D127	•••	D1567	D1612
	8	D2	D47	D92	•••	D1532	D1577
	9	D17	D62	D107	•••	D1547	D1592
	10	D32	D77	D122	•••	D1562	D1607

Where i: Sync block number
j: Byte position number

Figure 19 – Audi shuffling pattern for 525/60 system

	j =	10, 11	12, 13	14, 15		78, 79	80, 81
	i = 2	D0	D54	D108	•••	D1836	D1890
	3	D18	D72	D126	•••	D1854	D1908
	4	D36	D90	D144	•••	D1872	D1926
Track 0	5	D13	D67	D121	•••	D1849	D1903
or	6	D31	D85	D139	•••	D1857	D1921
Track 6	7	D49	D103	D157	•••	D1885	D1939
	8	D8	D62	D116	•••	D1844	D1898
	9	D26	D80	D134	•••	D1862	D1916
	10	D44	D98	D152	•••	D1880	D1934
	2	D3	D57	D111	•••	D1839	D1893
	3	D21	D75	D129	•••	D1857	D1911
	4	D39	D93	D147	•••	D1875	D1929
Track 1	5	D16	D70	D124	•••	D1852	D1906
or	6	D34	D88	D142	•••	D1870	D1924
Track 7	7	D52	D106	D160	•••	D1888	D1942
	8	D11	D65	D119	•••	D1847	D1901
	9	D29	D83	D137	•••	D1865	D1919
	10	D47	D101	D155	•••	D1883	D1937
	2	D6	D60	D114	•••	D1842	D1896
	3	D24	D78	D132	•••	D1860	D1914
	4	D42	D96	D150	•••	D1878	D1932
Track 2	5	D1	D55	D109	•••	D1837	D1891
or	6	D19	D73	D127	•••	D1855	D1909
Track 8	7	D37	D91	D145	•••	D1873	D1927
	8	D14	D68	D122	•••	D1850	D1904
	9	D32	D86	D140	•••	D1968	D1922
	10	D50	D104	D158	•••	D1886	D1940
	2	D9	D63	D117	•••	D1845	D1899
	3	D27	D81	D135	•••	D1863	D1917
	4	D45	D99	D153	•••	D1881	D1935
Track 3	5	D4	D58	D112	•••	D1840	D1894
or	6	D22	D76	D130	•••	D1858	D1912
Track 9	7	D40	D94	D148	•••	D1876	D1930
	8	D17	D71	D125	•••	D1853	D1907
	9	D35	D89	D143	•••	D1871	D1925
	10	D53	D107	D161	•••	D1889	D1943
	2	D12	D66	D120	•••	D1848	D1902
	3	D30	D84	D138	•••	D1866	D1920
	4	D48	D102	D156	•••	D1884	D1938
Track 4	5	D7	D61	D115	•••	D1843	D1897
or	6	D25	D79	D133	•••	D1861	D1915
Track 10	7	D43	D97	D151	•••	D1879	D1933
	8	D2	D56	D110	•••	D1838	D1892
	9	D20	D74	D128	•••	D1856	D1910
	10	D38	D92	D146	•••	D1974	D1928
	2	D15	D69	D123	•••	D1851	D1905
	3	D33	D87	D141	•••	D1869	D1923
	4	D51	D105	D159	•••	D1887	D1941
Track 5	5	D10	D64	D118	•••	D1846	D1900
or	6	D28	D82	D136	•••	D1864	D1918

Track 11	7	D46	D100	D154	•••	D1882	D1936
	8	D5	D59	D113	•••	D1841	D1895
	9	D23	D77	D131	•••	D1859	D1913
	10	D41	D95	D149	•••	D1877	D1931

Where i: Sync block number
j: Byte position number

Figure 20 – Audio shuffling pattern for 625/50 system

10.6 Audio auxiliary data (AAUX)

AAUX shall be added into each audio sync block, which has previously been loaded with the shuffled audio data, as shown in figure 10. Each AAUX packet of 5-byte length consists of a 1-byte packet header, followed by a 4-byte packet data containing AAUX source pack (AS) and AAUX source control pack (ASC). (See tables 20-22.) As shown in figure 21, AAUX data for one audio sector consists of nine packs, audio pack numbers 0 through 8, located in audio sync blocks 2 through 10.

AAUX data in CH1, CH2, CH3, and CH4 are defined independently. All data shall be set as correct values.

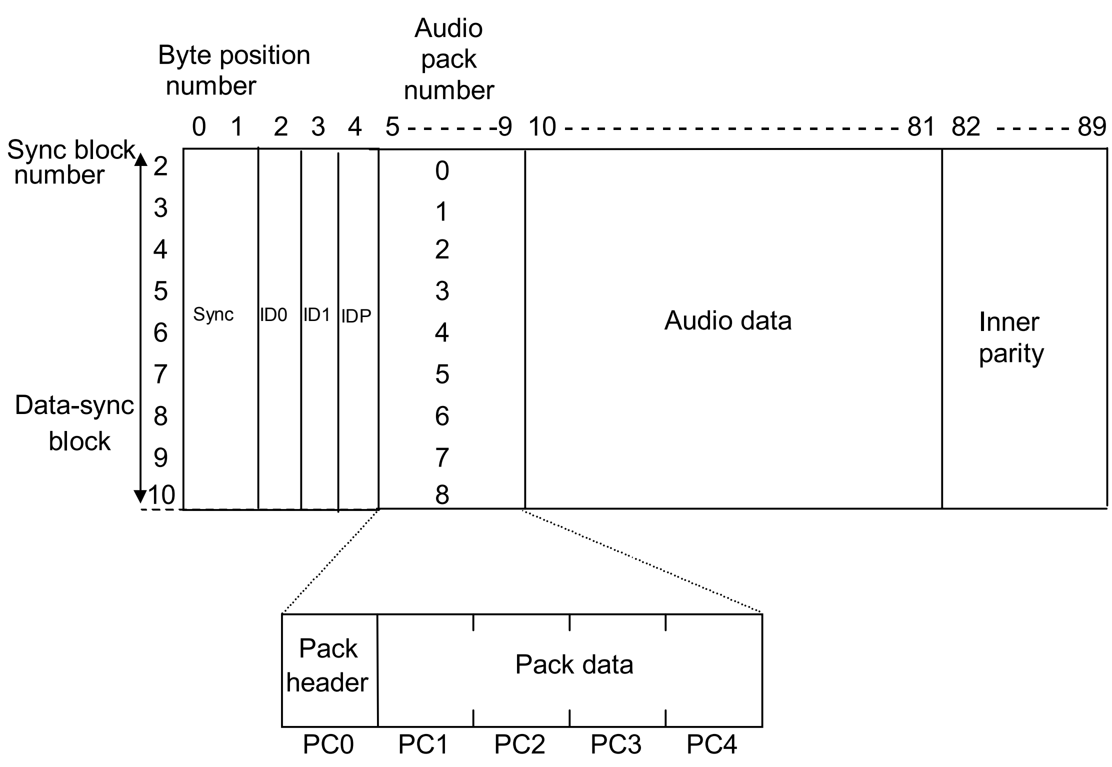


Figure 21 – Arrangement of AAUX packs in audio sector

Table 20 – AAUX data of the main area

Audio pack number		AAUX data of a video frame
Even track	Odd track	
3	0	AS
4	1	ASC

NOTE
AS: AAUX source pack (pack header = 50h)
ASC: AAUX source control pack (pack header = 51h)

Even track: Track number 0, 2, 4, 6, 8 for 525/60 system
Track number 0, 2, 4, 6, 8, 10 for 625/50 system

Odd track: Track number 1, 3, 5, 7, 9 for 525/60 system
Track number 1, 3, 5, 7, 9, 11 for 625/50 system

10.6.1 AAUX source pack (AS)

Table 21 – Mapping of AAUX source pack

	MSB							LSB
PC0	0	1	0	1	0	0	0	0
PC1	LF	Res	AF SIZE					
PC2	Res	CHN		Res	AUDIO MODE			
PC3	Res	Res	50/60	STYPE				
PC4	EF	Res	SMP			QU		

LF: Locked mode flag
Locking condition of audio sampling frequency with video signal
0: Sequence locked mode
1: Average locked mode

AF SIZE: Audio frame size
The number of audio samples per frame

	525/60 system
000000	1580
|	|
|	|
|	|
101000	1620
|	Res
|	|
111111	Res

	625/50 system
000000	1896
|	|
|	|
|	|
110000	1944
|	Res
|	|
111111	Res

CHN: The number of audio channels within an audio block
00b: One channel per audio block
Others: Reserved

AUDIO MODE: The contents of the audio signal on each sector

AUDIO MODE	CHN	
	00	01
0000	CH1(CH3)	Res
0001	CH2(CH4)	Res
0010 | 1110	Res	
1111	No information	

50/60:

0: 60 field system
1: 50 field system

STYPE: STYPE defines audio blocks per video frame

STYPE	audio blocks / frame
00000	4
00001 | 11111	Res | Res

EF: Emphasis flag

0: On
1: Off

SMP: Sampling frequency

000b: 48 kHz
Others: Reserved

QU: Quantization

000b: 16 bits linear
Others: Reserved

10.6.2 AAUX source control pack (ASC)

Table 22 – AAUX source control pack

	MSB							LSB
PC0	0	1	0	1	0	0	0	1
PC1	CGMS		Res	Res	Res	IRF	REC ST	REC END
PC2	Res	Res	0	0	Res	Res	Res	Res
PC3	DRF	0	Res	0	0	0	0	0
PC4	Res	Res	Res	Res	Res	Res	Res	Res

CGMS: Copy generation management system

CGMS	Possible Copy generations
00	Free to Copy
01	TBA
10	
11	

IRF: Invalid recording flag

For CH1, CH2

0: Invalid recording

1: Valid recording

For CH3, CH4

0: Valid recording

1: Invalid recording

REC ST: Recording start frame flag

1: Recording start frame

0: Not recording start frame

The duration of recording start flag shall be one audio block period for each recording channel.

REC END: Recording end frame flag

1: Recording end frame

0: Not recording end frame

The duration of recording end frame shall be one audio block period for each recording channel.

DRF: Direction flag

0: Reverse direction

1: Forward direction

10.6.2 AAUX NO INFO pack

All AAUX packs that have no information shall be recorded with NO INFO packs as shown in table 23.

Table 23 – Mapping of AAUX NO INFO pack

	MSB							LSB
PC0	1	1	1	1	1	1	1	1
PC1	1	1	1	1	1	1	1	1
PC2	1	1	1	1	1	1	1	1
PC3	1	1	1	1	1	1	1	1
PC4	1	1	1	1	1	1	1	1

10.7 Error correction code addition

Audio data are protected by an inner error correction code and an outer error correction code.

10.7.1 Inner error correction code

The inner parity as shown in figure 10 is defined as a codeword of an inner error correction code.

The inner error correction code is a (85, 77) Reed-Solomon code in GF(256) of which the field generator polynomial is

$$X^8 + X^4 + X^3 + X^2 + 1$$

where Xi are place-keeping variables in GF(256), the binary field.

The generator polynomial of the code in GF(256) is

$$gin(X) = (X + 1)(X + \alpha)(X + \alpha^2)(X + \alpha^3)(X + \alpha^4)(X + \alpha^5)(X + \alpha^6)(X + \alpha^7)$$

where α is given by 02_h in GF(256).

Parities $K_7, K_6, K_5, K_4, K_3, K_2, K_1, K_0$ are given by the equation:

$$K_7X^7 + K_6X^6 + K_5X^5 + K_4X^4 + K_3X^3 + K_2X^2 + K_1X + K_0,$$

which is the residue of $X^8D(X)$ divided by gin(X), where the data polynomial D(X) is defined as follows:

$$D(X) = D_{76}X^{76} + D_{75} X^{75} + ... + D_2X_2 + D_1X + D_0$$

and the codeword polynomial is given by the following equation:

$$D_{76}X^{84} + D_{75}X^{83} + ... + D_1X^9 + D_0X^8 + K_7X^7 + K_6X^6 + ... + K_1X + K_0$$

where D_{76} through D_0 correspond to the data of byte position number 5 through 81, and K_7 through K_0 to inner parity of byte position number 82 through 89, respectively.

10.7.2 Outer error correction code

The outer parity as shown in figure 10 is defined as a codeword of an outer error correction code.

The outer error correction code is a (14, 9) Reed-Solomon code in GF(256) of which the field generator polynomial is

$$X^8 + X^4 + X^3 + X^2 + 1$$

where Xi are place-keeping variables in GF(256), the binary field.

The generator polynomial of the code in GF(256) is

$$Gaout(X) = (X + 1)(X + \alpha)(X + \alpha^2)(X + \alpha^3)(X + \alpha^4)$$

where α is given by 2_h in GF(256).

Parities K_4, K_3, K_2, K_1, K_0 are given by the equation:

$$K_4X^4 + K_3X^3 + K_2X^2 + K_1X + K_0,$$

which is the residue of $X^5D(X)$ divided by gaout(X) , where the data polynomial D(X) is defined as follows:

$$D(X) = D_8X^8 + D_7X^7 + ... + D_2X^2 + D_1X + D_0$$

and the codeword polynomial is given by the equation:

$$D_8X^{13} + D_7X^{12} + ... + D_1X^6 + D_0X^5 + K_4X^4 + K_3X^3 + ... + K_1X + K_0$$

where D_8 through D_0 correspond to the data of sync block number 2 through 10, and K_4 through K_0 to outer parity of sync block number 11 through 15, respectively.

11 Video processing

11.1 Introduction

Analog video component signals are sampled at 13.5 MHz for luminance (Y) and 6.75 MHz for color-difference (C_R, C_B) signals. The sampled data in the vertical blanking area and the horizontal blanking area are discarded.

The active video samples, mapped as a video frame of active horizontal samples by active vertical lines, are divided into DCT blocks. One DCT block contains 8 samples from 8 consecutive horizontal lines respectively. Two luminance DCT blocks and two color-difference DCT blocks form a macro block. Five macro blocks, which are gathered from various areas in a frame by the rule shown in 11.2.6, form a video segment. A video segment is compressed to five compressed macro blocks by DCT and VLC processing.

The compressed macro blocks are reordered with the order defined in 11.8 when data sync blocks are formed.

Video auxiliary data (VAUX) are multiplexed with the compressed video data, and the multiplexed data are processed in a product block of 77 columns by 138 rows. The data in the product block are protected with error correction data added to the product block. Prior to recording, 24-25 modulation is applied .

11.2 Video structure

11.2.1 Sampling structure

The sampling structure is the same as the sampling structure of 4:2:2 component television signals described in ITU-R BT.601. Sampling structures of luminance (Y) and two color-difference signals (C_R, C_B) in the 4:2:2 method are described in table 24.

– Pixel structure in one frame

For the 525/60 and 625/50 systems, 720 pixels of luminance per line shall be transmitted as shown in figures 22 and 23. For the 525/60 and 625/50 systems, 360 pixels of color-difference signal per line shall be transmitted as shown in figures 22 and 23.

The sampling starting point in the active period of C_R and C_B signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel has a value from –127 to 126, which is obtained by subtracting 128 from the input video signal level.

– Line structure in one frame

For the 525/60 system, 240 lines shall be transmitted for Y, C_R, and C_B signals from each field. For the 625/50 system, 288 lines shall be transmitted for Y, C_R, and C_B signals from each field. The transmitted lines in two fields are described in table 24.

Table 24 – Construction of video signal sampling

<table>
<tr><td colspan="2"></td><td>525/60 system</td><td colspan="2">625/50 system</td></tr>
<tr><td rowspan="2">Sampling frequency</td><td>Y</td><td colspan="3">13.5MHz</td></tr>
<tr><td>C_R,C_B</td><td colspan="3">6.75MHz</td></tr>
<tr><td rowspan="2">Total number of pixels per line</td><td>Y</td><td>858</td><td colspan="2">864</td></tr>
<tr><td>C_R,C_B</td><td>429</td><td colspan="2">432</td></tr>
<tr><td>The number of active pixels per line</td><td>Y</td><td colspan="3">720</td></tr>
<tr><td></td><td>C_R,C_B</td><td colspan="3">360</td></tr>
<tr><td colspan="2">Total number of line per frame</td><td>525</td><td colspan="2">625</td></tr>
<tr><td colspan="2">The number of active line per frame</td><td>480</td><td colspan="2">576</td></tr>
<tr><td>The active line numbers</td><td>Field 1</td><td>23 to 262</td><td colspan="2">23 to 310</td></tr>
<tr><td></td><td>Field 2</td><td>285 to 524</td><td colspan="2">335 to 622</td></tr>
<tr><td>Quantization</td><td></td><td colspan="3">Each sample is linearly quantized to 8 bits for Y, C_R and C_B.</td></tr>
<tr><td rowspan="4">The relation between video signal level and quantized level</td><td>Scale</td><td colspan="3">1 to 254</td></tr>
<tr><td rowspan="2">Y</td><td colspan="2">Video signal level of white: 235</td><td rowspan="2">Quantized level 220</td></tr>
<tr><td colspan="2">Video signal level of black: 16</td></tr>
<tr><td>C_R, C_B</td><td colspan="2">Zero signal level: 128</td><td>Quantized level 225</td></tr>
<tr><td colspan="5">NOTE – The sampling frequency shall synchronize with the horizontal sync signal.
Y: Luminance
C_R, C_B: Color difference</td></tr>
</table>

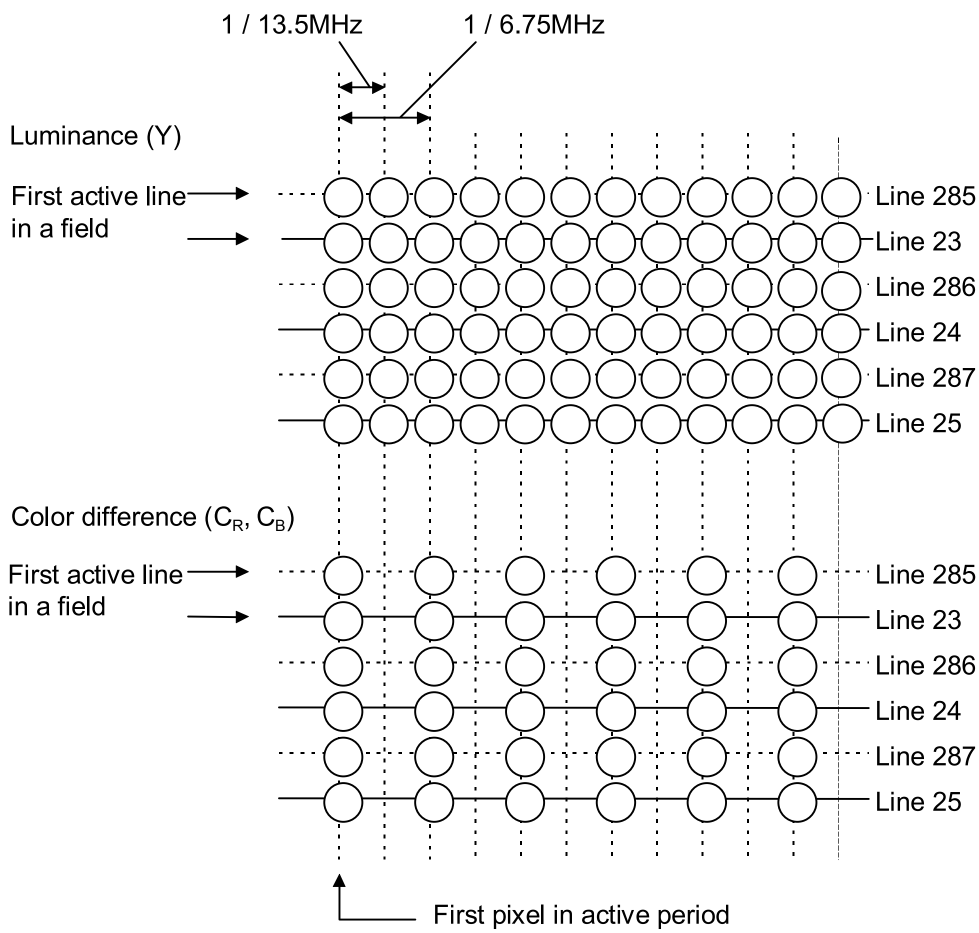


Figure 22 – Transmitting samples for 525/60 systems

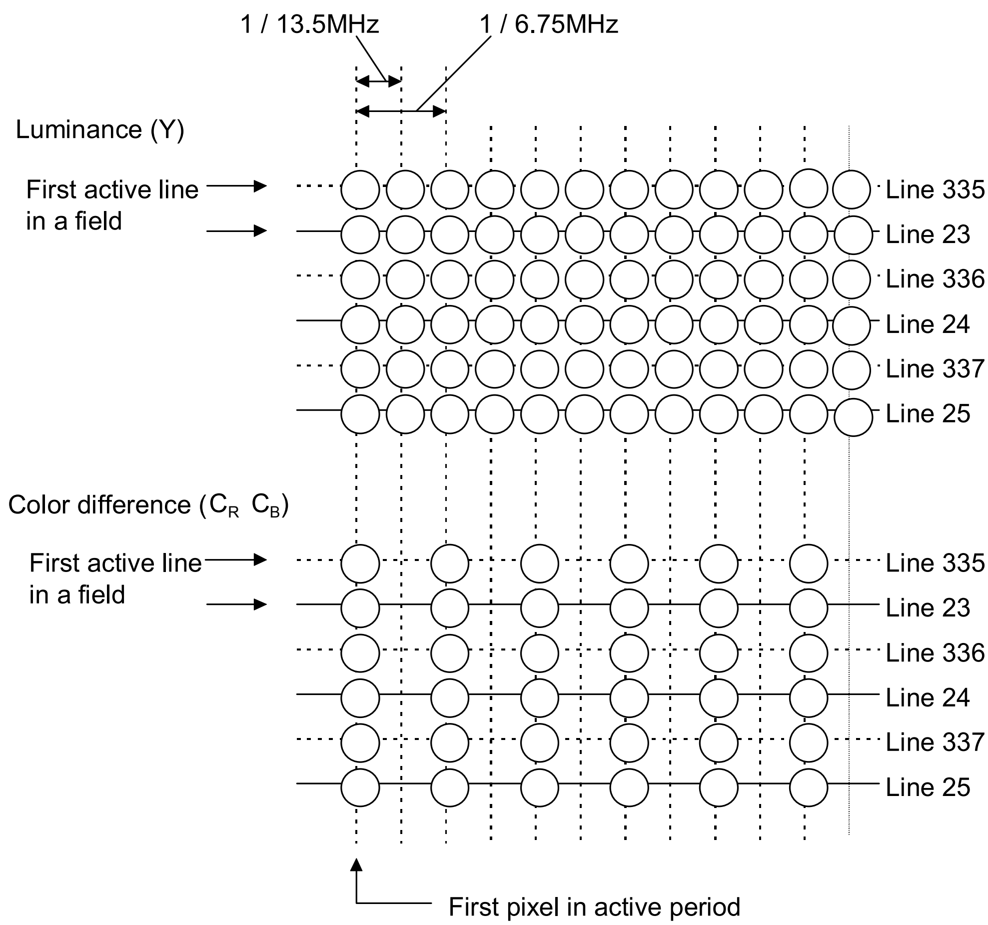


Figure 23 – Transmitting samples for 625/50 system

11.2.2 DCT block

The Y, C_R, and C_B pixels within a frame shall be divided into DCT blocks. As shown in figure 24, all DCT blocks are structured with a rectangular area of eight consecutive horizontal lines, and eight adjacent samples along a horizontal line, within a frame. The value of x shows the horizontal coordinate from the left. The value of y shows the vertical coordinate from the top. Odd lines of y = 1, 3, 5, 7 are the horizontal lines of field one, and even lines of y = 0, 2, 4, 6 are those of field two.

– DCT block arrangement in one frame for 525/60system

The arrangement of horizontal DCT blocks in one frame is shown in figure 25. The same horizontal arrangement is repeated with 60 DCT blocks in the vertical direction. Pixels in one frame are divided into 10,800 DCT blocks.

Y: 60 vertical DCT blocks × 90 horizontal DCT blocks = 5400 DCT blocks

C_R: 60 vertical DCT blocks × 45 horizontal DCT blocks = 2700 DCT blocks

C_B: 60 vertical DCT blocks × 45 horizontal DCT blocks = 2700 DCT blocks

– DCT block arrangement in one frame for 625/50 system

The arrangement of horizontal DCT blocks in one frame is shown in figure 25. The same horizontal arrangement is repeated to 72 DCT blocks in the vertical direction. Pixels in one frame are divided into 12,960 DCT blocks.

Y: 72 vertical DCT blocks × 90 horizontal DCT blocks = 6480 DCT blocks

C_R: 72 vertical DCT blocks × 45 horizontal DCT blocks = 3240 DCT blocks

C_B: 72 vertical DCT blocks × 45 horizontal DCT blocks = 3240 DCT blocks

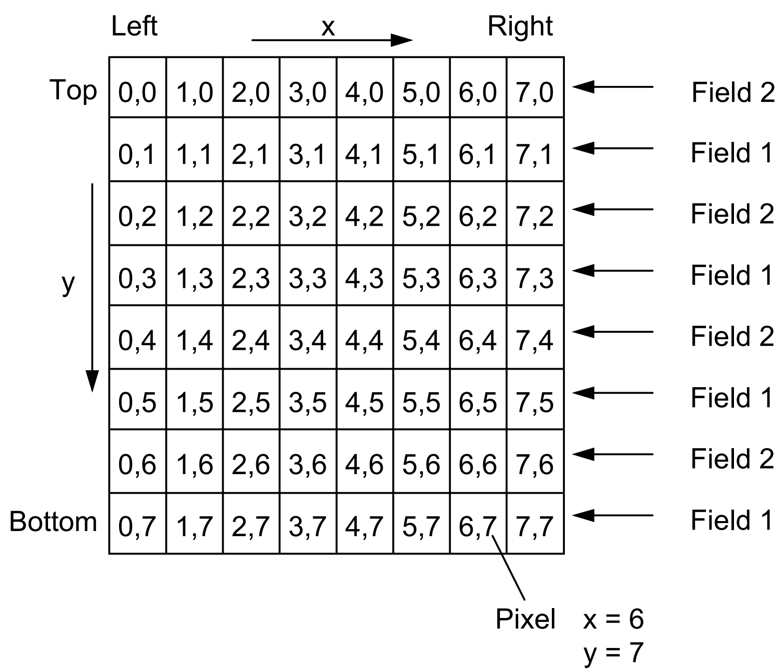


Figure 24 – DCT block and the pixel coordinate

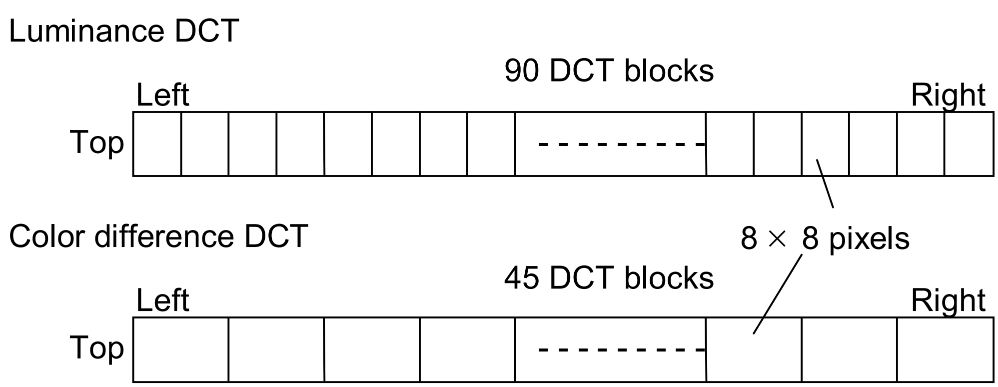


Figure 25 – DCT block arrangement

11.2.3 Macro block

Four DCT blocks form a macro block. Figure 26 shows the relationship between the macro block and the DCT blocks.

Each macro block consists of two luminance DCT blocks which are next to each other horizontally in the picture frame, and two chrominance DCT blocks for CR and CB respectively. Each chrominance block covers the same spatial area as the two luminance DCT blocks combined.

– Macro block arrangement in one frame for 525/60 system

The arrangement of macro blocks in one frame is shown in figure 27. The small rectangle shows a macro block. Pixels in one frame are divided into 2700 macro blocks.

60 vertical macro blocks × 45 horizontal macro blocks = 2700 macro blocks

– Macro block arrangement in one frame for 625/50 system

The arrangement of macro blocks in one frame is shown in figure 28. The small rectangle shows a macro block. Pixels in one frame are divided into 3240 macro blocks.

72 vertical macro blocks × 45 horizontal macro blocks = 3240 macro blocks

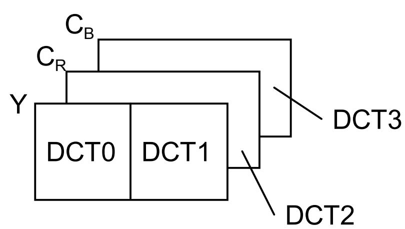


Figure 26 – Macro block and DCT blocks

11.2.4 Super block

Each super block consists of 27 macro blocks .

– Super block arrangement in one frame for 525/60 system

The arrangement of super blocks in one frame is shown in figure 27. Each super block is structured with 27 adjacent macro blocks enclosed by a thick line. The pixels in one frame are divided into 100 super blocks.

20 vertical super blocks × 5 horizontal super blocks = 100 super blocks

– Super block arrangement in one frame for 625/50 system

The arrangement of super blocks in one frame is shown in figure 28. Each super block is structured with 27 adjacent macro blocks enclosed by a thick line. The pixels in one frame are divided into 120 super blocks.

24 vertical super blocks × 5 horizontal super blocks = 120 super blocks.

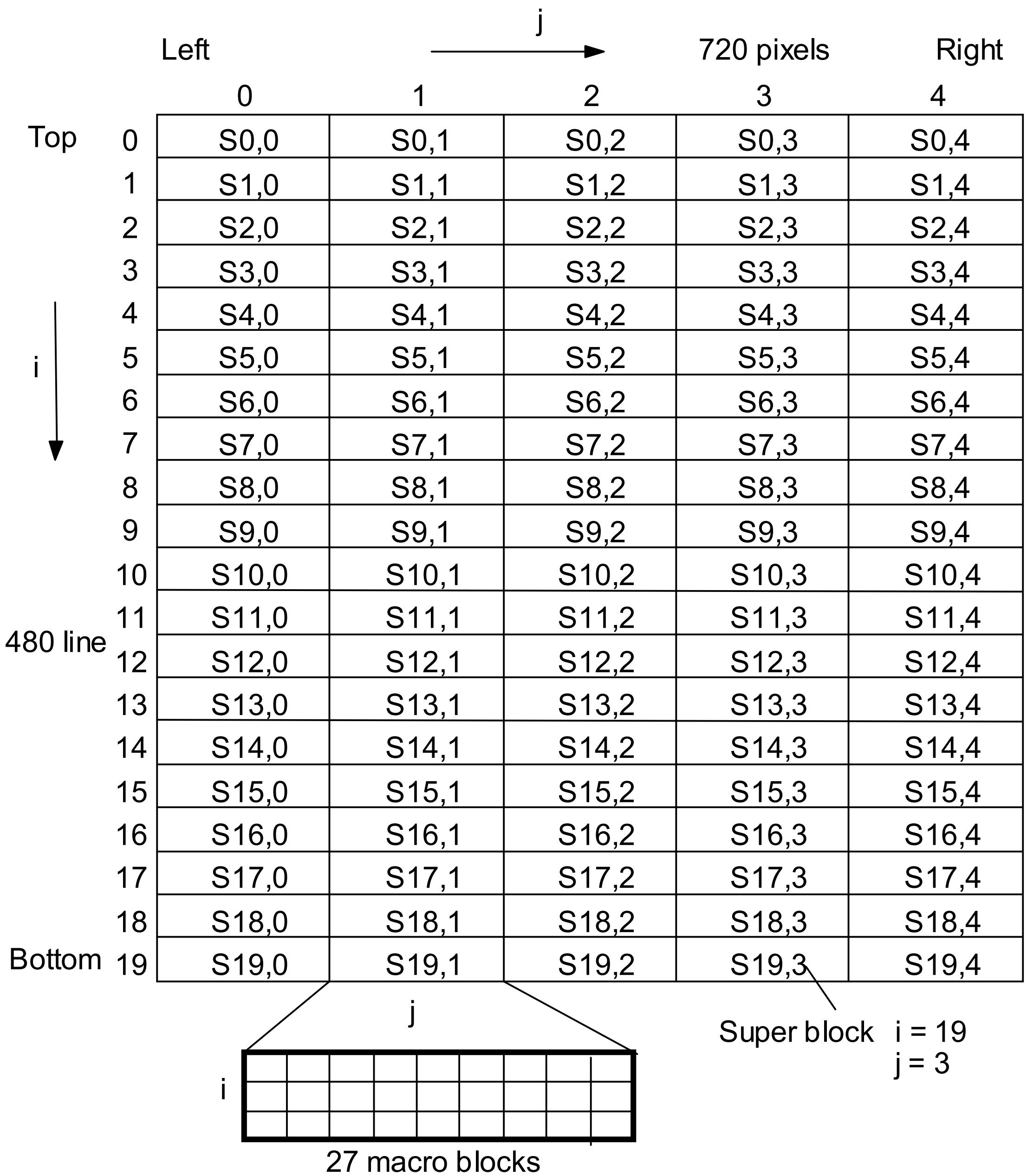


Figure 27 – Super blocks and macro blocks in a video frame for 525/60 system

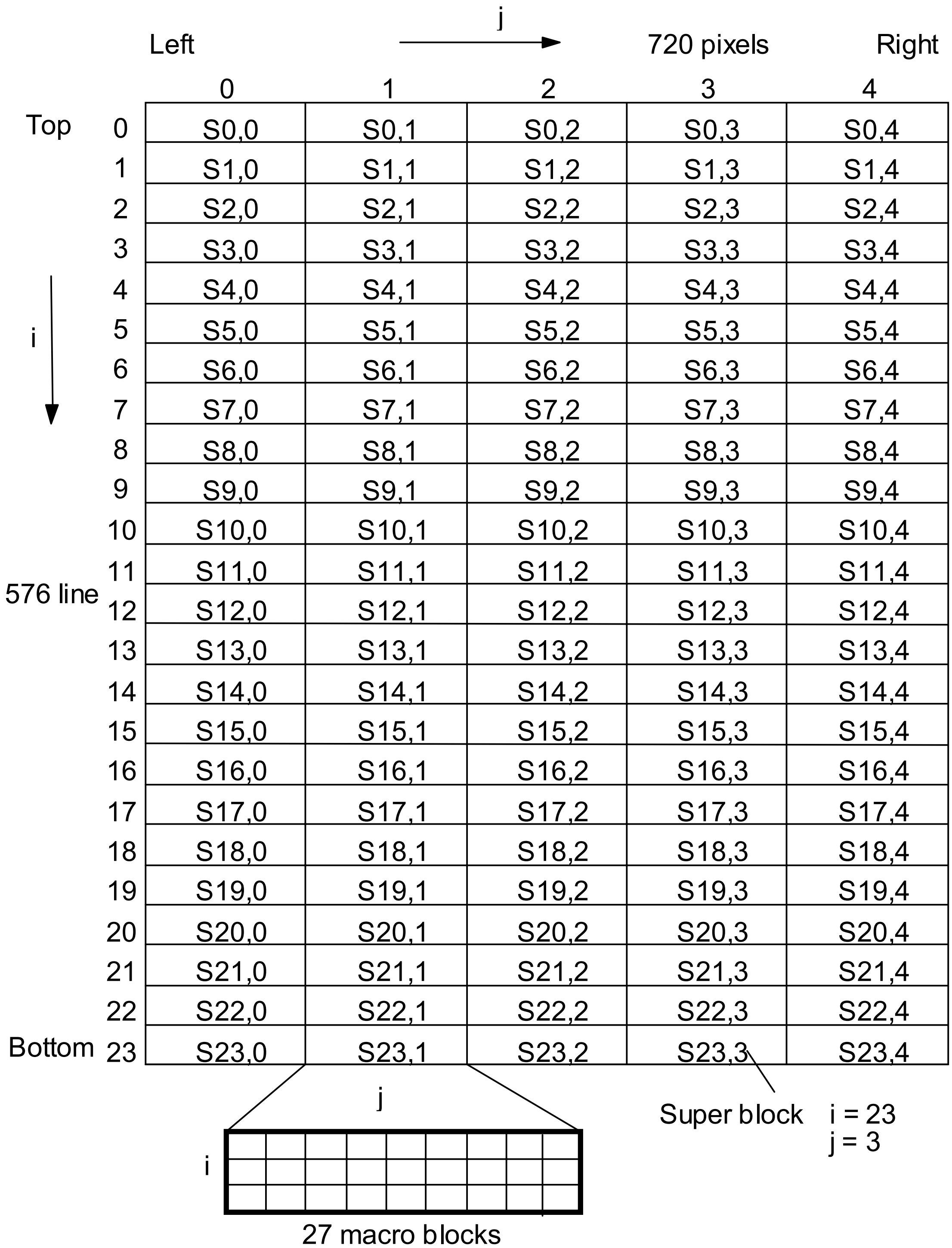


Figure 28 – Super blocks and macro blocks in a video frame for 625/50 system

11.2.5 Definition of super block number, macro block number and value of the pixel

– Super block number

The super block number in a frame is expressed as Si,j as shown in figures 27 and 28.

S i,j where i: the vertical order of the super block
i = 0, ..., 19 for 525/60 system
i = 0, ..., 23 for 625/50 system

j: the horizontal order of the super block
j = 0, ..., 4

– Macro block number

The macro block number is expressed as Mi,j,k. The symbol k is the macro block order in the super block as shown in figure 29. The small rectangle in the figure shows a macro block, and the number in the small rectangle indicates k.

Mi,j,k where i, j: the super block number
k: the macro block order in the super block
k = 0, ..., 26

– Pixel location

The value of the pixel is expressed as Pi,j,k,l(x,y). The pixel is indicated by the suffixes i,j,k,l(x,y). The symbol l is the DCT block order in a macro block as shown in figure 24. The rectangle in the figure shows a DCT block. The DCT number in the rectangle expresses l. Symbols x and y are the pixel coordinates in the DCT block as described in figure 24.

Pi,j,k,l(x,y) where i,j,k: the macro block number
l: the DCT block order in the macroblock
(x,y): the pixel coordinate in the DCT block
x = 0, ..., 7
y = 0, ..., 7

Super block $S_{i,j}$

0	5	6	11	12	17	18	23	24
1	4	7	10	13	16	19	22	25
2	3	8	9	14	15	20	21	26

Where i: vertical order of the super block
i = 0,• • •, 19 for 525-60 system
i = 0,• • •, 23 for 625-50 system
j: the horizontal order of the super block
j = 0,• • •, 4

Figure 29 – Macro block order in a super block

11.2.6 Definition of video segment and compressed macro block

A video segment consists of five macro blocks which are gathered from various areas. Each video segment before bit-rate reduction is expressed as Vi,k which consists of Ma,2,k, Mb,1,k, Mc,3,k, Md,0,k, and Me,4,k.

where a = (i + 4) mod n
where b = (i + 12) mod n
where c = (i + 16) mod n
where d = (i + 0) mod n
where e = (i + 8) mod n

i: the vertical order of the super block
i = 0, ..., n-1
n: the number of vertical super blocks in a video frame
n = 20 for the 525/60 system
n = 24 for the 625/50 system
k: the macro block order in the super block
k = 0, ..., 26

The bit-rate reduction is executed from Ma,2,k to Me,4,k. The data in a video segment are compressed so that the total data are 385 bytes. One set of compressed video data consists of five compressed macro blocks. Each compressed macro block consists of 77 bytes and is expressed as CM. Each video segment after bit-rate reduction is expressed as CVi,k which consists of CMa,2,k, CMb,1,k, CMc,3,k, CMd,0,k, and CMe,4,k as shown below (see also 11.7.1):

CMa,2,k : This block includes all parts or most parts of the compressed data from macro block Ma,2,k and may include the compressed data from macro block Mb,1,k or Mc,3,k or Md,0,k or Me,4,k.

CMb,1,k : This block includes all parts or most parts of the compressed data from macro block Mb,1,k and may include the compressed data from macro block Ma,2,k or Mc,3,k or Md,0,k or Me,4,k.

CMc,3,k: This block includes all parts or most parts (depending on the algorithm defined in 11.7.1) of the compressed data from macro block Mc,3,k and may include the compressed data from macro block Ma,2,k or Mb,1,k or Md,0,k or Me,4,k.

CMd,0,k: This block includes all parts or most parts of the compressed data from macro block Md,0,k and may include the compressed data from macro block Ma,2,k or Mb,1,k or Mc,3,k or Me,4,k.

CMe,4,k: This block includes all parts or most parts of the compressed data from macro block Me,4,k and may include the compressed data from macro block Ma,2,k or Mb,1,k or Mc,3,k or Md,0,k.

11.3 DCT processing

The DCT block is made up of pixels from two fields. It has a structure consisting of 4 horizontal lines and 8 pixels per line per field. This clause describes the transformation of a DCT block from 64 pixels with numbers i,j,k,**l**(x,y) to 64 coefficients with numbers i,j,k,**l**(h,v).

The value of the pixel is Pi,j,k,l(x,y) and the value of the coefficient is Ci,j,k,l(h,v). When h = 0 and v = 0, the coefficient is called a DC coefficient. Other coefficients are called AC coefficients.

11.3.1 DCT mode

There are two DCT modes to improve the picture quality after the bit-rate reduction called 8-8-DCT mode and 2-4-8-DCT mode. The 8-8-DCT mode should be selected when the difference between two fields is small. The 2-4-8-DCT mode should be selected when the difference between two fields is significant.

The two DCT modes are defined as follows:

11.3.1.1 8-8-DCT mode

DCT:

$$C_{i,j,k,l}(h,v) = C(v)C(h)\sum_{y=0}^{7}\sum_{x=0}^{7}(P_{i,j,k,l}(x,y)Cos(\pi v(2y+1)/16)Cos(\pi h(2x+1)/16))$$

Inverse DCT:

$$P_{i,j,k,l}(x,y) = \sum_{v=0}^{7}\sum_{h=0}^{7}(C(v)C(h)C_{i,j,k,l}(h,v)Cos(\pi v(2y+1)/16)Cos(\pi h(2x+1)/16))$$

where

$C(h) = 0.5/\sqrt{2}$	for h = 0
$C(h) = 0.5$	for h = 1 to 7
$C(v) = 0.5/\sqrt{2}$	for v = 0
$C(v) = 0.5$	for v = 1 to 7

11.3.1.2 2-4-8 DCT mode

DCT:

$$C_{i,j,k,l}(h,u) = C(u)C(h)\sum_{y=0}^{3}\sum_{x=0}^{7}\left((P_{i,j,k,l}(x,2z) + P_{i,j,k,l}(x,2z+1))KC \right)$$

$$C_{i,j,k,l}(h,u+4) = C(u)C(h)\sum_{y=0}^{3}\sum_{x=0}^{7}\left((P_{i,j,k,l}(x,2z) - P_{i,j,k,l}(x,2z+1))KC \right)$$

Inverse DCT:

$$P_{i,j,k,l}(x,2z) = \sum_{u=0}^{3}\sum_{h=0}^{7}\left((C(u)C(h)C_{i,j,k,l}(h,u) + C_{i,j,k,l}(h,u+4))KC \right)$$

$$P_{i,j,k,l}(x,2z+1) = \sum_{u=0}^{3}\sum_{h=0}^{7}\left((C(u)C(h)C_{i,j,k,l}(h,u) - C_{i,j,k,l}(h,u+4))KC \right)$$

where

u = 0, ..., 3
z = INT(y / 2)

$$KC = Cos(\pi u(2z+1)/8)Cos(\pi h(2x+1)/16)$$

$C(h) = 0.5/\sqrt{2}$	for h = 0
$C(h) = 0.5$	for h = 1 to 7
$C(u) = 0.5/\sqrt{2}$	for v = 0
$C(u) = 0.5$	for v = 1 to 7

11.3.2 Weighting

DCT coefficients shall be weighted by the process described below. W(h,v) expresses the weighting factor for Ci,j,k,l (h,v) of the DCT coefficient.

8-8-DCT mode

For h = 0 and v = 0 $\quad$ W(h,v) = 1 / 4
For others $\quad$ W(h,v) = W(h)W(v) / 2

2-4-8- DCT mode

For h = 0 and v = 0 $\quad$ W(h,v) = 1 / 4
For v< 4 $\quad$ W(h,v) = W(h)W(2 v) / 2
For others $\quad$ W(h,v) = W(h)W(2 (v-4)) / 2

where

W(0) =1
W(1) = CS4 / (4 × CS7 × CS2)
W(2) = CS4 / (2 × CS6)
W(3) = 1 / (2 × CS5)
W(4) = 7 / 8
W(5) = CS4 / CS3
W(6) = CS4 / CS2
W(7) = CS4 / CS1

where

CSm = Cos (mπ / 16) m = 1 to 7

11.3.3 Output order

Figure 30 shows the output order of the weighted coefficients.

8-8-DCT

horizontal →, vertical ↓

	0	1	2	3	4	5	6	7
0	1	2	6	7	15	16	28	29
1	3	5	8	14	17	27	30	43
2	4	9	13	18	26	31	42	44
3	10	12	19	25	32	41	45	54
4	11	20	24	33	40	46	53	55
5	21	23	34	39	47	52	56	61
6	22	35	38	48	51	57	60	62
7	36	37	49	50	58	59	63	64

2-4-8-DCT

horizontal →, vertical ↓ (sum) / (difference)

	0	1	2	3	4	5	6	7
0	1	3	7	19	21	35	37	51
1	5	9	17	23	33	39	49	53
2	11	15	25	31	41	47	55	61
3	13	27	29	43	45	57	59	63
4	2	4	8	20	22	36	38	52
5	6	10	18	24	34	40	50	54
6	12	16	26	32	42	48	56	62
7	14	28	30	44	46	58	60	64

Figure 30 – Output order of a weighted DCT block

11.3.4 Tolerance of DCT with weighting

Output error between the reference DCT and the tested DCT (see figure 31) should satisfy tolerance specifications for the following cases:

– Probability of occurrence of error
– Mean square errors for all coefficients
– Maximum value of mean square error for each DCT block
– When all input pixel values of a DCT block are the same

The error calculated with the method above should satisfy the following four tolerances:

1) Probability of occurrence of error Pr which is greater than one is less than or equal to 1×10^{-5}.

$$Pr(|Y\,ti(h,v)| - Y\,ri(h,v)| > 1) \leq 1 \times 10^{-5}$$

where i = 0, ..., 9999
h = 0, ..., 7
v = 0, ..., 7

2) Mean square errors for all coefficients are less than or equal to 0.125.

$$\sum_{i=0}^{9999}\sum_{h=0}^{7}\sum_{v=0}^{7}(Yti(h,v)-Yri(h,v))^2 / (64 \times 1000) \leq 0.125$$

3) The maximum value of mean square errors for each DCT block is less than or equal to 0.33.

$$\sum_{h=0}^{7}\sum_{v=0}^{7}(Yti(h,v)-Yri(h,v))^2 / 64 \leq 0.33$$

where l = 0, ..., 9999

4) If all input pixel values of a DCT block are the same, all AC coefficients of the DCT block should be zero.

The IDCT operation should be executed using a circuit with the same precision as the DCT that satisfies the above tolerances.

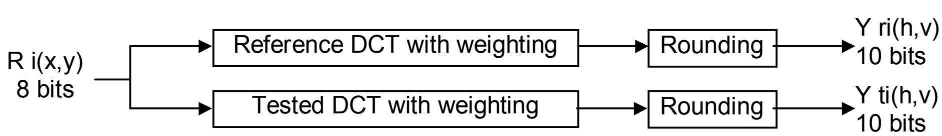


Figure 31 – Measurement method of DCT operation precision

11.4 Quantization

11.4.1 Introduction

Weighted DCT coefficients are transformed into 9 bits. Then the 9-bit transformed data are divided by quantization step in order to limit the amount of data in one video segment after bit-rate reduction.

11.4.2 Bit assignment for quantization

Weighted DCT coefficients are represented as follows:

DC coefficient value (9 bits):
b8 b7 b6 b5 b4 b3 b2 b1 b0
twos complement (–255 to 255)

AC coefficient value (10 bits):
s b8 b7 b6 b5 b4 b3 b2 b1 b0
1 sign bit + 9 bits of absolute value (–511 to 511)

11.4.3 Class number

Each DCT block shall be defined by four classes as defined in table 25. The class number is used for selecting quantization steps. Both c1 and c0 express the class number and are stored in the DC coefficient of the compressed DCT blocks as described in 11.6. For reference, table 26 shows an example of classification.

Table 25 – Class number and the DCT block

Class number			DCT block	
	c1	c0	Quantization noises	Maximum absolute value of AC coefficients
0	0	0	Visible	Less than or equal to 255
1	0	1	Lower than class 0	
2	1	0	Lower than class 1	
3	1	1	Lower than class 2	
			———	Greater than 255

Table 26 – An example of the classification for reference

	Maximum absolute value of AC coefficients			
	0 to 11	12 to 23	24 to 35	> 35
Y	0	1	2	3
C_R	1	2	3	3
C_B	2	3	3	3

11.4.4 Initial scaling

Initial scaling is an operation to transform AC coefficients from 10 bits to 9 bits. Initial scaling shall be done as follows:

For class number = 0, 1, 2:
input data s b8 b7 b6 b5 b4 b3 b2 b1 b0
output data s b7 b6 b5 b4 b3 b2 b1 b0

For class number = 3:
input data s b8 b7 b6 b5 b4 b3 b2 b1 b0
output data s b8 b7 b6 b5 b4 b3 b2 b1 b0

11.4.5 Area number

The area number is used for selection of quantization step. AC coefficients within a DCT block shall be classified into four areas with an area number as shown in figure 32.

8-8-DCT

horizontal →

vertical ↓

	0	1	2	3	4	5	6	7
0	DC	0	0	1	1	1	2	2
1	0	0	1	1	1	2	2	2
2	0	1	1	1	2	2	2	3
3	1	1	1	2	2	2	3	3
4	1	1	2	2	2	3	3	3
5	1	2	2	2	3	3	3	3
6	2	2	2	3	3	3	3	3
7	2	2	3	3	3	3	3	3

2-4-8-DCT

horizontal →

vertical ↓

		0	1	2	3	4	5	6	7
(sum)	0	DC	0	1	1	1	2	2	3
	1	0	1	1	2	2	2	3	3
	2	1	1	2	2	2	3	3	3
	3	1	2	2	2	3	3	3	3
(difference)	4	0	0	1	1	2	2	2	3
	5	0	1	1	2	2	2	3	3
	6	1	1	2	2	2	3	3	3
	7	1	2	2	3	3	3	3	3

Figure 32 – Area number

11.4.6 Quantization step

The quantization step shall be decided by the class number, area number, and quantization number (QNO) as specified in table 27. The QNO is selected for each macro block in order to limit the amount of data in one video segment.

Table 27 – Quantization step

	Class number				Area number				
	0	1	2	3	0	1	2	3	
Quantization number (QNO)	15				1	1	1	1	Quantization Step
	14				1	1	1	1	
	13				1	1	1	1	
	12	15			1	1	1	1	
	11	14			1	1	1	1	
	10	13		15	1	1	1	1	
	9	12	15	14	1	1	1	1	
	8	11	14	13	1	1	1	2	
	7	10	13	12	1	1	2	2	
	6	9	12	11	1	1	2	2	
	5	8	11	10	1	2	2	4	
	4	7	10	9	1	2	2	4	
	3	6	9	8	2	2	4	4	
	2	5	8	7	2	2	4	4	
	1	4	7	6	2	4	4	8	
	0	3	6	5	2	4	4	8	
		2	5	4	4	4	8	8	
		1	4	3	4	4	8	8	
		0	3	2	4	8	8	16	
			2	1	4	8	8	16	
			1	0	8	8	16	16	
			0		8	8	16	16	

11.5 Variable length coding (VLC)

Variable length coding is an operation for transforming quantized AC coefficients to variable length codes. One or several successive AC coefficients within a DCT block are coded into one variable length code according to the order as shown in figure 30.

Run length and amplitude are defined as follows:

Run length: The number of successive AC coefficients quantized to 0 (run = 0, ..., 61)

Amplitude: Absolute value just after successive AC coefficients quantized to 0 (amp = 0, ..., 255)

(run, amp): The pair of run length and amplitude

Table 28 shows the length of codewords corresponding to (run, amp). In the table, the sign bit is not included in the length of codewords. When the amplitude is not zero, the code length shall be plus 1 because the sign bit is needed. For an empty column, the length of codewords of (run, amp) equals that of (run – 1, 0) plus that of (0, amp). The code of variable length coding shall be as shown in table 29; the leftmost bit of codewords in MSB and the rightmost bit of codewords in LSB. The MSB of the subsequent codeword is next to the LSB of the codeword just before. Sign bit s shall be as follows:

When the quantized AC coefficients are greater than zero: s = 0

When the quantized AC coefficients are less than zero: s = 1

When the values of all the remaining quantized coefficients are zero within a DCT block, the coding process is ended by adding the EOB (end of block) codeword of 0110b just after the last codeword.

Table 28 – Length of code word

	Amplitude																									
Run length	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	- - - -	255
0	11	2	3	4	4	5	5	6	6	7	7	7	8	8	8	8	8	8	9	9	9	9	9	15	- - - -	15
1	11	4	5	7	7	8	8	8	9	10	10	10	11	11	11	12	12	12								
2	12	5	7	8	9	9	10	12	12	12	12	12														
3	12	6	8	9	10	10	11	12																		
4	12	6	8	9	11	12																				
5	12	7	9	10																						
6	13	7	9	11																						
7	13	8	12	12																						
8	13	8	12	12																						
9	13	8	12																							
10	13	8	12																							
11	13	9																								
12	13	9																								
13	13	9																								
14	13	9																								
15	13																									
• •	• •																									
61	13																									

NOTE
1) The sign bit is not included.
2) The length of EOB = 4

Table 29 – Code words of variable length coding

(run,amp)		Code	Length
0	1	0 0 s	2+1
0	2	0 1 0 s	3+1
EOB		0 1 1 0	4
1	1	0 1 1 1 s	4+1
0	3	1 0 0 0 s	
0	4	1 0 0 1 s	
2	1	1 0 1 0 0 s	5+1
1	2	1 0 1 0 1 s	
0	5	1 0 1 1 0 s	
0	6	1 0 1 1 1 s	
3	1	1 1 0 0 0 0 s	6+1
4	1	1 1 0 0 0 1 s	
0	7	1 1 0 0 1 0 s	
0	8	1 1 0 0 1 1 s	
5	1	1 1 0 1 0 0 0 s	7+1
6	1	1 1 0 1 0 0 1 s	
2	2	1 1 0 1 0 1 0 s	
1	3	1 1 0 1 0 1 1 s	
1	4	1 1 0 1 1 0 0 s	
0	9	1 1 0 1 1 0 1 s	
0	10	1 1 0 1 1 1 0 s	
0	11	1 1 0 1 1 1 1 s	
7	1	1 1 1 0 0 0 0 0 s	8+1
8	1	1 1 1 0 0 0 0 1 s	
9	1	1 1 1 0 0 0 1 0 s	
10	1	1 1 1 0 0 0 1 1 s	
3	2	1 1 1 0 0 1 0 0 s	
4	2	1 1 1 0 0 1 0 1 s	
2	3	1 1 1 0 0 1 1 0 s	
1	5	1 1 1 0 0 1 1 1 s	
1	6	1 1 1 0 1 0 0 0 s	
1	7	1 1 1 0 1 0 0 1 s	
0	12	1 1 1 0 1 0 1 0 s	
0	13	1 1 1 0 1 0 1 1 s	
0	14	1 1 1 0 1 1 0 0 s	
0	15	1 1 1 0 1 1 0 1 s	
0	16	1 1 1 0 1 1 1 0 s	
0	17	1 1 1 0 1 1 1 1 s	
11	1	1 1 1 1 0 0 0 0 0 s	9+1
12	1	1 1 1 1 0 0 0 0 1 s	
12	1	1 1 1 1 0 0 0 1 0 s	
14	1	1 1 1 1 0 0 0 1 1 s	
5	2	1 1 1 1 0 0 1 0 0 s	
6	2	1 1 1 1 0 0 1 0 1 s	
3	3	1 1 1 1 0 0 1 1 0 s	
4	3	1 1 1 1 0 0 1 1 1 s	
2	4	1 1 1 1 0 1 0 0 0 s	
2	5	1 1 1 1 0 1 0 0 1 s	
1	8	1 1 1 1 0 1 0 1 0 s	
0	18	1 1 1 1 0 1 0 1 1 s	
0	19	1 1 1 1 0 1 1 0 0 s	
0	20	1 1 1 1 0 1 1 0 1 s	
0	21	1 1 1 1 0 1 1 1 0 s	
0	22	1 1 1 1 0 1 1 1 1 s	

(run,amp)		Code	Length
5	3	1 1 1 1 1 0 0 0 0 0 s	10+1
3	4	1 1 1 1 1 0 0 0 0 1 s	
3	5	1 1 1 1 1 0 0 0 1 0 s	
2	6	1 1 1 1 1 0 0 0 1 1 s	
1	9	1 1 1 1 1 0 0 1 0 0 s	
1	10	1 1 1 1 1 0 0 1 0 1 s	
1	11	1 1 1 1 1 0 0 1 1 0 s	
0	0	1 1 1 1 1 0 0 1 1 1 0	11
1	0	1 1 1 1 1 0 0 1 1 1 1	
6	3	1 1 1 1 1 0 1 0 0 0 0 s	11+1
4	4	1 1 1 1 1 0 1 0 0 0 1 s	
3	6	1 1 1 1 1 0 1 0 0 1 0 s	
1	12	1 1 1 1 1 0 1 0 0 1 1 s	
1	13	1 1 1 1 1 0 1 0 1 0 0 s	
1	14	1 1 1 1 1 0 1 0 1 0 1 s	
2	0	1 1 1 1 1 0 1 0 1 1 0 0	12
3	0	1 1 1 1 1 0 1 0 1 1 0 1	
4	0	1 1 1 1 1 0 1 0 1 1 1 0	
5	0	1 1 1 1 1 0 1 0 1 1 1 1	
7	2	1 1 1 1 1 0 1 1 0 0 0 0 s	12+1
8	2	1 1 1 1 1 0 1 1 0 0 0 1 s	
9	2	1 1 1 1 1 0 1 1 0 0 1 0 s	
10	2	1 1 1 1 1 0 1 1 0 0 1 1 s	
7	3	1 1 1 1 1 0 1 1 0 1 0 0 s	
8	3	1 1 1 1 1 0 1 1 0 1 0 1 s	
4	5	1 1 1 1 1 0 1 1 0 1 1 0 s	
3	7	1 1 1 1 1 0 1 1 0 1 1 1 s	
2	7	1 1 1 1 1 0 1 1 1 0 0 0 s	
2	8	1 1 1 1 1 0 1 1 1 0 0 1 s	
2	9	1 1 1 1 1 0 1 1 1 0 1 0 s	
2	10	1 1 1 1 1 0 1 1 1 0 1 1 s	
2	11	1 1 1 1 1 0 1 1 1 1 0 0 s	
1	15	1 1 1 1 1 0 1 1 1 1 0 1 s	
1	16	1 1 1 1 1 0 1 1 1 1 1 0 s	
1	17	1 1 1 1 1 0 1 1 1 1 1 1 s	
6	0	1 1 1 1 1 1 0 0 0 0 1 1 0	
7	0	1 1 1 1 1 1 0 0 0 0 1 1 1	
• R •	• 0 •	Binary notation 1 1 1 1 1 1 0 of R R=6 to 61	13
61	0	1 1 1 1 1 0 0 0 1 1 s	
0	23	1 1 1 1 1 1 1 0 0 0 1 0 1 1 1 s	15+1
0	24	1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 s	
• 0 •	• A •	Binary notation 1 1 1 1 1 1 1 of A A = 23 to 255	
0	255	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 s	

NOTES
1 (R, 0): 1 1 1 1 1 1 0 r5 r4 r3 r2 r1 r0, where 32r5 + 16r4 + 8r3 + 4r2 + 2r1 + r0 = R.
2 (0, A): 1 1 1 1 1 1 0 a7 a6 a5 a4 a3 a2 a1 a0, where 128a7 + 64a6 + 32a5 + 16a4 + 8a3 + 4a2 + 2a1 + a0 = A.
3 Sign bit is s and end of block is EOB.

11.6 Arrangement of a compressed macro block

A compressed video segment consists of five compressed macro blocks. Each compressed macro block has 77 bytes of data. The arrangement of the compressed macro block shall be as shown in figure 33.

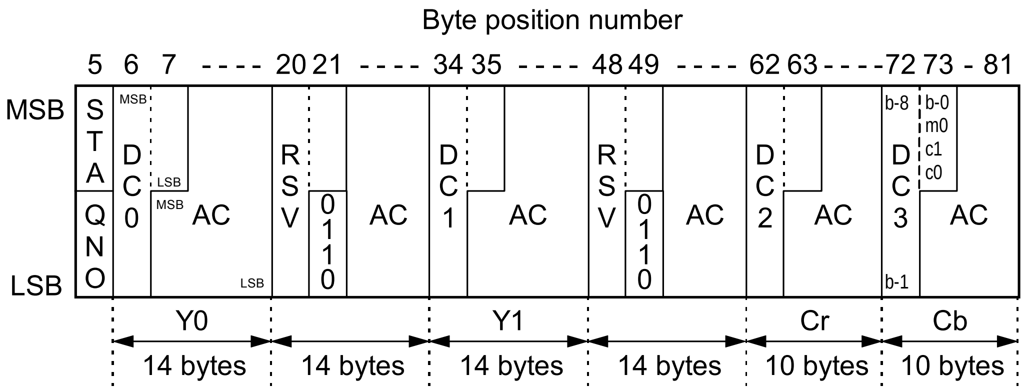


Figure 33 – Arrangement of compressed macro block

– STA (status of the compressed macro block)

STA expresses the error and concealment of the compressed macro block and consists of four bits, s3 s2 s1 s0. Table 30 shows the definition of STA.

Table 30 – Definition of STA

MSB	STA		LSB	Information of the compressed macro block		
s3	s2	s1	s0	Error	Error concealment	Continuity
0	0	0	0	No error	Not proceeded	----------
0	0	1	0	No error	Type A	Type a
0	1	0	0	No error	Type B	Type a
0	1	1	0	No error	Type C	Type a
0	1	1	1	Error exists	——	——
1	0	1	0	No error	Type A	Type b
1	1	0	0	No error	Type B	Type b
1	1	1	0	No error	Type C	Type b
1	1	1	1	Error exists	——	——
others				Res		

NOTES
1 Type A: Replaced with a compressed macro block of the same compressed macro block number in the immediate previous frame.
2 Type B: Replaced with a compressed macro block of the same compressed macro block number in the next immediate frame.
3 Type C: This compressed macro block is concealed, but the concealment method is not specified.
4 Type a: The continuity of data processing sequence with other compressed macro block whose s0 = 0 and s 3 = 0 in the same video segment is guaranteed.
5 Type b: The continuity of data processing sequence with other compressed macro block is not guaranteed.
6 For STA = 0111b, the error code is inserted in the compressed macro block. This is an option.
7 For STA = 1111b, the error position is unidentified.

– QNO (quantizaton number)

The QNO is the quantization number applied to the macro block, which consists of four bits: q3, q2, q1, q0. Codewords of the QNO shall be as shown in table 31.

Table 31 – Code words of QNO

MSB			LSB	
q3	q2	q1	q0	QNO
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

– DC

DCI (where the DCT block order in the macro block is, I = 0, ..., 3) consists of a DC coefficient, the DCT mode, and the class number of the DCT block.

MSB LSB
DCI: b8 b7 b6 b5 b4 b3 b2 b1 b0 m0 c1 c0

where:

b8 to b0: DC coefficient value
m0: DCT mode
m0 = 0 for 8-8-DCT mode
m0 = 1 for 2-4-8-DCT mode
c1 c0: class number

– AC

AC is a generic term referring to variable length coded AC coefficients within video segment Vi,k.

The areas of Y0, Y1, C_R, and C_B are defined as compressed data areas. Both Y0 and Y1 consist of 112 bits and both C_R and C_B consist of 80 bits, as shown in figure 33.

In figure 33, the variable length codeword is located starting from MSB which is shown on the upper-left side to LSB which is shown on the lower-right side. Therefore, AC data are distributed from the upper-left corner to the lower-right corner.

11.7 Arrangement of a video segment

11.7.1 Arrangement

This clause describes the distribution method of quantized AC coefficients.

Figure 34 shows the arrangement of a video segment CV i,k after bit-rate reduction. The column shows a compressed macro block. Symbol F i,j,k,l expresses the compressed data area for a DCT block whose DCT block number is i,j,k,l. Symbol E i,j,k,l represents areas to be used for recording of overflow data generated through compression processes.

In the bit sequence which shall be concatenated, the DC coefficient, the information of DCT mode, the class number, and the codewords for AC coefficients of the DCT block (for which the DCT block number is i,j,k,l) are defined as B i,j,k,l.

Codewords for AC coefficients of B i,j,k,l shall be concatenated according to the order as shown in figure 30. The last codeword shall be EOB. The MSB of subsequent codewords shall be next to the LSB of the codeword just before.

The arrangement algorithm of a video segment shall be composed of three passes:

- Pass 1: The distribution to the compressed data area of B i,j,k,l.

- Pass 2: The distribution in the same compressed macro block of overflowed B i,j,k,l (which is the remainder after pass 1).

- Pass 3: The distribution in the same video segment of overflowed B i,j,k,l (which is the remainder after pass 2).

The remaining data shall be ignored when the data are not completely distributed. Consequently, if error concealment is performed for a compressed macro block, the data distributed by pass 3 may not be reproduced.

– Arrangement algorithm of a video segment

```
if (525/60 system) n = 20 else n = 24;
for (i = 0; i<n ; i++){
        a = (i + 4) mod n;
        b = (i + 12) mod n;
        c = (i + 16) mod n;
        d = (i + 0) mod n;
        e = (i + 8) mod n;
        for (k = 0; k<27; k++){
                q = 2;
                p = a;
                VR = 0
                /* VR is the bit sequence for the data which are not distributed to video segment CV i,k by
                  pass 2. */
/* pass 1 */
        for (j = 0; j <5; j++) {
                MRq = 0;
        /* MRq is the bit sequence for the data which are not distributed to macro block M i,q,k by pass 1. */
                for (l = 0, l< 4; l ++) {
                        remain = distribute (Bp,q,k,l,Fp,q,k,l);
                        MRq = connect (MRq, remain);
                }
```

```
                        if (q == 2) {q = 1; p = b;}
                    else if (q == 1) {q = 3; p = c;}
                    else if (q == 3) {q = 0; p = d;}
                    else if (q == 0) {q = 4; p = e;}
                    else if (q == 4) {q = 2; p = a;}
        }
/* pass 2 */
        for (j = 0; j< 5; j++) {
                for (l = 0; l<6; l ++) {
                    MRq = distribute (MRq, Fp,q,k,l);
                        if ((l == 0) || (l == 1))
                            MRq = distribute (MRq, Ep,q,k,l)
                    }
                    VR = connect (VR, MRq);
                        if (q == 2) {q = 1; p = b;}
                    else if (q == 1) {q = 3; p = c;}
                    else if (q == 3) {q = 0; p = d;}
                    else if (q == 0) {q = 4; p = e;}
                    else if (q == 4) {q = 2; p = a;}
/* pass 3 */
        for (j = 0; j<5; j++) {
                for (l = 0; l<6; l ++) {
                    VR = distribute (VR, Fp,q,k,l);
                    if ((l == 0) || (l == 1))
                        VR = distribute (VR,Ep,q,k,l);
                }
                        if (q == 2) {q = 1; p = b;}
                    else if (q == 1) {q = 3; p = c;}
                    else if (q == 3) {q = 0; p = d;}
                    else if (q == 0) {q = 4; p = e;}
                    else if (q == 4) {q = 2; p = a;}
                }
        }
}
distribute (data0, area0)       /* Area0 is filled starting from the MSB. */
                                /* Distribute data0 from MSB into empty area of area0. */
remain = (remaining_data);      /* Remaining data are data; which are not distributed. */
        return (return)
}
connect (data1, data2) {         /* Connect the MSB of data2 with the LSB of data1. */
        data3 =(connecting_data);       /* Connecting data are data which consist of data2 connected with
                                        data1. */
        return (data3);
}
```

Byte position number

Compressed macro block number	5	6 ------- 20	20 ------- 34	34 ------- 48	48 ------- 62	62 ------- 72	72 ----- 81
CM a, 2, k	STAa QNOa	F a, 2, k, 0	E a, 2, k, 0	F a, 2, k, 1	E a, 2, k, 1	F a, 2, k, 2	F a, 2, k, 3
CM b, 1, k	STAb QNOb	F b, 1, k, 0	E b, 1, k, 0	F b, 1, k, 1	E b, 1, k, 1	F b, 1, k, 2	F b, 1, k, 3
CM c, 3, k	STAc QNOc	F c, 3, k, 0	E c, 3, k, 0	F c, 3, k, 1	E c, 3, k, 1	F c, 3, k, 2	F c, 3, k, 3
CM d, 0, k	STAd QNOd	F d, 0, k, 0	E d, 0, k, 0	F d, 0, k, 1	E d, 0, k, 1	F d, 0, k, 2	F d, 0, k, 3
CM e, 4, k	STAe QNOe	F e, 4, k, 0	E e, 4, k, 0	F e, 4, k, 1	E e, 4, k, 1	F e, 4, k, 2	F e, 4, k, 3
		Y0		Y1		Cr	Cb
		14 bytes	14 bytes	14 bytes	14 bytes	10 bytes	10 bytes

NOTES

a = (i + 4) mod n
b = (i + 12) mod n
c = (i + 16) mod n
d = (i + 0) mod n
e = (i + 8) mod n

i : the vertical order of the super block
i = 0, • • •, n - 1
n : the number of vertical super blocks in a video frame
n = 20 for 525-60 system
n = 24 for 625-50 system
k : the macro block order in the super block
k = 0,• • •, 26

Figure 34 – Arrangement of video segment after bit rate reduction

11.7.2 Video error code processing

If errors are detected in a compressed macro block which is reproduced and processed with error correction, the compressed data area containing these errors should be replaced with the video error code.

This process replaces the first two data bytes of the compressed data area with a code as follows:

MSB LSB
1000000000000110b

The first 9 bits are the DC error code, the next 3 bits are information of the DCT mode and class number, and the last 4 bits are the EOB as shown in figure 35. After error code processing, when the compressed macro blocks are input to a decoder which does not operate with video error code, all data in this compressed macro block should be processed as invalid.

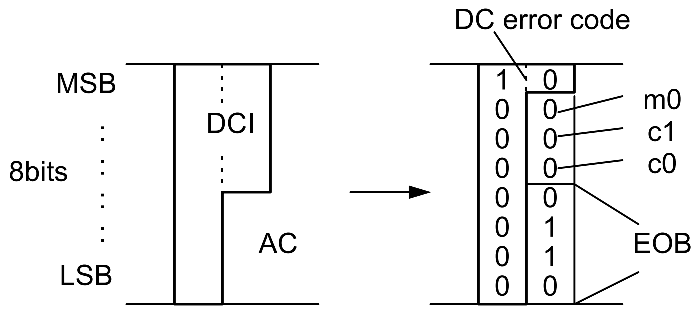


Figure 35 – Video error code

11.8 Relationship between compressed macro block and data sync block

A compressed macro block has an identification number. This is signified by CMi,j,k. The suffixes i,j,k are defined in 11.2.5.

A compressed macro block is distributed to a data sync block with a sync block number as follows:

27j + k + 21 in sector (INT(i / 2) mod 2) of track (INT(i / 4) x 2 + mod 2)

where
the vertical order of the super block
i = 0, ..., n-1
the horizontal order of the super block
j = 0, ..., 4
the macro block order in the super block
k = 0, ..., 26
n =10 for the 525/60 system
n =12 for the 625/50 system

Figures 36 and 37 show the relationship between the macro block number and the data sync number.

Sync block number	Track number 0	1	2	3	- - - - - - - -	n - 2	n - 1
156	VAUX	VAUX	VAUX	VAUX	- - - - - - - -	VAUX	VAUX
155	$CM_{0,4,26}$	$CM_{1,4,26}$	$CM_{4,4,26}$	$CM_{5,4,26}$	- - - - - - - -	$CM_{2n-4,4,26}$	$CM_{2n-3,4,26}$
154	$CM_{0,4,25}$	$CM_{1,4,25}$	$CM_{4,4,25}$	$CM_{5,4,25}$	- - - - - - - -	$CM_{2n-4,4,25}$	$CM_{2n-3,4,25}$
•	•	•	•	•		•	•
•	•	•	•	•		•	•
•	•	•	•	•		•	•
129	$CM_{0,4,0}$	$CM_{1,4,0}$	$CM_{4,4,0}$	$CM_{5,4,0}$	- - - - - - - -	$CM_{2n-4,4,0}$	$CM_{2n-3,4,0}$
128	$CM_{03,26}$	$CM_{1,3,26}$	$CM_{4,3,26}$	$CM_{5,3,26}$	- - - - - - - -	$CM_{2n-4,3,26}$	$CM_{2n-3,3,26}$
127	$CM_{0,3,25}$	$CM_{1,3,25}$	$CM_{4,3,25}$	$CM_{5,3,25}$	- - - - - - - -	$CM_{2n-4,3,25}$	$CM_{2n-3,3,25}$
•	•	•	•	•		•	•
•	•	•	•	•		•	•
•	•	•	•	•		•	•
102	$CM_{0,3,0}$	$CM_{1,3,0}$	$CM_{4,3,0}$	$CM_{5,3,0}$	- - - - - - - -	$CM_{2n-4,3,0}$	$CM_{2n-3,3,0}$
101	$CM_{0,2,26}$	$CM_{1,2,26}$	$CM_{4,2,26}$	$CM_{5,2,26}$	- - - - - - - -	$CM_{2n-4,2,26}$	$CM_{2n-3,2,26}$
100	$CM_{0,2,25}$	$CM_{1,2,25}$	$CM_{4,2,25}$	$CM_{5,2,25}$	- - - - - - - -	$CM_{2n-4,2,25}$	$CM_{2n-3,2,25}$
•	•	•	•	•		•	•
•	•	•	•	•		•	•
•	•	•	•	•		•	•
75	$CM_{0,2,0}$	$CM_{1,2,0}$	$CM_{4,2,0}$	$CM_{5,2,0}$	- - - - - - - -	$CM_{2n-4,2,0}$	$CM_{2n-3,2,0}$
74	$CM_{0,1,26}$	$CM_{1,1,26}$	$CM_{4,1,26}$	$CM_{5,1,26}$	- - - - - - - -	$CM_{2n-4,1,26}$	$CM_{2n-3,1,26}$
73	$CM_{0,1,25}$	$CM_{1,1,25}$	$CM_{4,1,25}$	$CM_{5,1,25}$	- - - - - - - -	$CM_{2n-4,1,25}$	$CM_{2n-3,1,25}$
•	•	•	•	•		•	•
•	•	•	•	•		•	•
•	•	•	•	•		•	•
48	$CM_{0,1,0}$	$CM_{1,1,0}$	$CM_{4,1,0}$	$CM_{5,1,0}$	- - - - - - - -	$CM_{2n-4,1,0}$	$CM_{2n-3,1,0}$
47	$CM_{0,0,26}$	$CM_{1,0,26}$	$CM_{4,0,26}$	$CM_{5,0,26}$	- - - - - - - -	$CM_{2n-4,0,26}$	$CM_{2n-3,0,26}$
46	$CM_{0,0,25}$	$CM_{1,0,25}$	$CM_{4,0,25}$	$CM_{5,0,25}$	- - - - - - - -	$CM_{2n-4,0,25}$	$CM_{2n-3,0,25}$
•	•	•	•	•		•	•
•	•	•	•	•		•	•
•	•	•	•	•		•	•
21	$CM_{0,0,0}$	$CM_{1,0,0}$	$CM_{4,0,0}$	$CM_{5,0,0}$	- - - - - - - -	$CM_{2n-4,0,0}$	$CM_{2n-3,0,0}$
20	VAUX	VAUX	VAUX	VAUX	- - - - - - - -	VAUX	VAUX
19	VAUX	VAUX	VAUX	VAUX	- - - - - - - -	VAUX	VAUX

Where n = 10 for 525/60 system
n = 12 for 625/50 system

Figure 36 – Relation between the macro block number and the data sync block for sector 0

sync block number	Track number 0	1	2	3	- - - - - - - -	n - 2	n - 1
156	VAUX	VAUX	VAUX	VAUX	- - - - - - - -	VAUX	VAUX
155	$CM_{2,4,26}$	$CM_{3,4,26}$	$CM_{6,4,26}$	$CM_{7,4,26}$	- - - - - - - -	$CM_{2n-2,4,26}$	$CM_{2n-1,4,26}$
154	$CM_{2,4,25}$	$CM_{3,4,25}$	$CM_{6,4,25}$	$CM_{7,4,25}$	- - - - - - - -	$CM_{2n-2,4,25}$	$CM_{2n-1,4,25}$
•	•	•	•	•		•	•
•	•	•	•	•		•	•
•	•	•	•	•		•	•
129	$CM_{2,4,0}$	$CM_{3,4,0}$	$CM_{6,4,0}$	$CM_{7,4,0}$	- - - - - - - -	$CM_{2n-2,4,0}$	$CM_{2n-1,4,0}$
128	$CM_{2,3,26}$	$CM_{3,3,26}$	$CM_{6,3,26}$	$CM_{7,3,26}$	- - - - - - - -	$CM_{2n-2,3,26}$	$CM_{2n-1,3,26}$
127	$CM_{2,3,25}$	$CM_{3,3,25}$	$CM_{6,3,25}$	$CM_{7,3,25}$	- - - - - - - -	$CM_{2n-2,3,25}$	$CM_{2n-1,3,25}$
•	•	•	•	•		•	•
•	•	•	•	•		•	•
•	•	•	•	•		•	•
102	$CM_{2,3,0}$	$CM_{3,3,0}$	$CM_{6,3,0}$	$CM_{7,3,0}$	- - - - - - - -	$CM_{2n-2,3,0}$	$CM_{2n-1,3,0}$
101	$CM_{2,2,26}$	$CM_{3,2,26}$	$CM_{6,2,26}$	$CM_{7,2,26}$	- - - - - - - -	$CM_{2n-2,2,26}$	$CM_{2n-1,2,26}$
100	$CM_{2,2,25}$	$CM_{3,2,25}$	$CM_{6,2,25}$	$CM_{7,2,25}$	- - - - - - - -	$CM_{2n-2,2,25}$	$CM_{2n-1,2,25}$
•	•	•	•	•		•	•
•	•	•	•	•		•	•
•	•	•	•	•		•	•
75	$CM_{2,2,0}$	$CM_{3,2,0}$	$CM_{6,2,0}$	$CM_{7,2,0}$	- - - - - - - -	$CM_{2n-2,2,0}$	$CM_{2n-1,2,0}$
74	$CM_{2,1,26}$	$CM_{3,1,26}$	$CM_{6,1,26}$	$CM_{7,1,26}$	- - - - - - - -	$CM_{2n-2,1,26}$	$CM_{2n-1,1,26}$
73	$CM_{2,1,25}$	$CM_{3,1,25}$	$CM_{6,1,25}$	$CM_{7,1,25}$	- - - - - - - -	$CM_{2n-2,1,25}$	$CM_{2n-1,1,25}$
•	•	•	•	•		•	•
•	•	•	•	•		•	•
•	•	•	•	•		•	•
48	$CM_{2,1,0}$	$CM_{3,1,0}$	$CM_{6,1,0}$	$CM_{7,1,0}$	- - - - - - - -	$CM_{2n-2,1,0}$	$CM_{2n-1,1,0}$
47	$CM_{2,0,26}$	$CM_{3,0,26}$	$CM_{6,0,26}$	$CM_{7,0,26}$	- - - - - - - -	$CM_{2n-2,0,26}$	$CM_{2n-1,0,26}$
46	$CM_{2,0,25}$	$CM_{3,0,25}$	$CM_{6,0,25}$	$CM_{7,0,25}$	- - - - - - - -	$CM_{2n-2,0,25}$	$CM_{2n-1,0,25}$
•	•	•	•	•		•	•
•	•	•	•	•		•	•
•	•	•	•	•		•	•
21	$CM_{2,0,0}$	$CM_{3,0,0}$	$CM_{6,0,0}$	$CM_{7,0,0}$	- - - - - - - -	$CM_{2n-2,0,0}$	$CM_{2n-1,0,0}$
20	VAUX	VAUX	VAUX	VAUX	- - - - - - - -	VAUX	VAUX
19	VAUX	VAUX	VAUX	VAUX	- - - - - - - -	VAUX	VAUX

Where n=10 for 525/60 system
n=12 for 625/50 system

Figure 37 – Relation between the macro block number and the data sync block for sector 1

11.9 Reordering of compressed macro blocks

Compressed macro blocks are reordered with the order defined in 11.8 when data sync blocks are formed. This permits maximum data recovery at nonstandard playback speeds.

11.10 Video auxiliary data (VAUX)

Video auxiliary data (VAUX) shall be added to the compressed video data as shown in figure 12. VAUX is formed using both a standard length pack and long length pack structures.

Figure 38 shows the VAUX pack arrangement of each track. Sync blocks 19, 20, and 156 each contain 15 standard length packs following the ID code. These sync blocks also contain two arbitrary bytes following the last VAUX pack.

VAUX packs are numbered 0 to 44 from the entrance side of the video sector in order as shown in figure 38.

This number is called the video pack number. The main area of VAUX consists of seven packs. Table 32 shows the VAUX data of the main area. The VAUX SOURCE pack, VAUX SOURCE CONTROL pack, and FORMAT pack include mandatory data for playback video signals that must be recorded.

VIDEO EXTRA LINE is recorded with a long length pack. The structure of such a long length pack is described in 11.10.4.

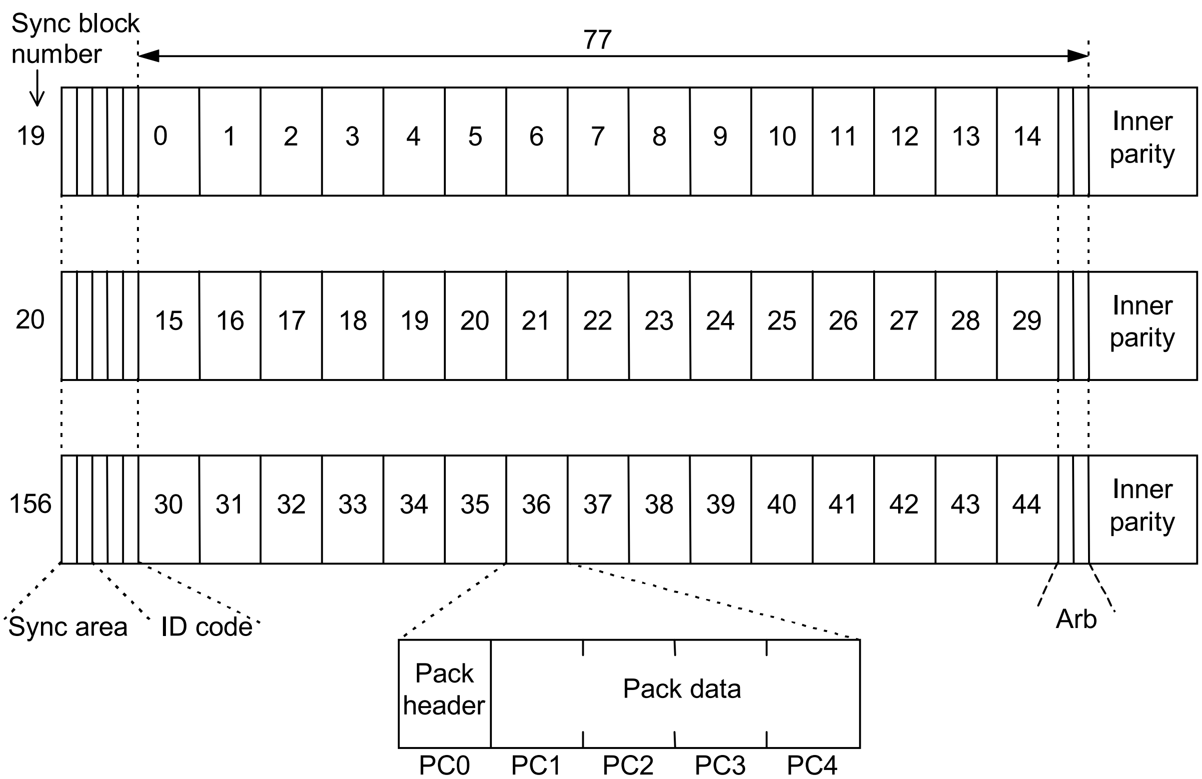


Figure 38 – Arrangement of VAUX packs in VAUX sync blocks

The reserved area of VAUX is as follows:

Table 32 – VAUX data of the reserved area

Video pack number		VAUX data of a video frame
Video 0 sector	Video 1 sector	
39	0	VS.
40	1	VSC
30	14	FMT

where

VS: VAUX SOURCE pack (pack header = 60_h)
VSC: VAUX SOURCE CONTROL pack (pack header = 61_h)
FMT: FORMAT pack (pack header = 81_h)

11.10.1 VAUX SOURCE pack (VS)

Table 33 shows a mapping of the VAUX source pack.

Table 33 – Mapping of VAUX source pack

	MSB							LSB
PC0	0	1	1	0	0	0	0	0
PC1	Res	Res	Res	Res	Res	Res	Res	Res
PC2	B/W	EN	CLF		Res	Res	Res	Res
PC3	Res	Res	50/60	STYPE				
PC4	Res	Res	Res	Res	Res	Res	Res	Res

B/W: Black-and-white flag
- 0: Black and white
- 1: Color

EN: Color frame enable flag
- 0: CLF is valid.
- 1: CLF is invalid.

CLF: Color frame identification code (refer to ITU-R BT.470)

50/60	CLF	Form	CLF Identification
0	0 0 0 1 Others	525/60 system	Color frame A Color frame B Res
1	0 0 0 1 1 0 1 1	625/50 system	1st, 2nd fields 3rd, 4th fields 5th, 6th fields 7th, 8th fields

50/60:
- 0: 525/60
- 1: 625/50

STYPE: STYPE defines the video signal system type in combination with 50/60 as follows:

STYPE	50 / 60	
	0	1
00000 : 11110	Reserved	Reserved
11111	525/60 system	625/50 system

According to the video signal:

50/60: 50 or 60 field system
STYPE: Video signal type

11.10.2 VAUX source control pack (VSC)

Table 34 shows a mapping of the VAUX source control pack.

Table 34 – Mapping of VAUX source control pack

	MSB							LSB
PC0	0	1	1	0	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	Res	RECST
PC2	Res	Res	0	0	Res	DISP		
PC3	FF	FS	FC	IL	1	1	Res	Res
PC4	Res	Res	Res	Res	Res	Res	Res	Res

This pack shall be recorded at least in the VAUX main area.

CGMS: Copy generation management system

CGMS	Possible copy generations
00	Free to copy
01	TBA
10	
11	

REC ST: Recording start point
- 0: Recording start point
- 1: Not recording start point

Recording start point flag shall be recorded during the first frame of the new recording.

DISP: Display select mode

DISP	Aspect ratio and format	Position
000	4:3 full format	not applicable
001	Res	---
010	16:9 full format (squeeze)	not applicable
011 | 111	Res	

FF: Frame/field flag

FF indicates whether the frame is produced from two sequential fields, or by repeating one field twice.
- 0: Field repeated twice
- 1: Frame

FS: First/second flag

FS indicates which field is repeated twice to produce the frame.
- 0: Field 2 used
- 1: Field 1 used

FF	FS	Output field
0	0	Field 2 is repeated twice
0	1	Field 1 is repeated twice
1	0	Field 2 and field 1 are processed in that order
1	1	Field 1 and field 2 are processed in that order

FC: Frame change flag

FC indicates whether the picture of the current frame is the same picture as that of the immediate previous frame.

0: Same picture as the immediate previous frame
1: Different picture from the immediate previous frame

IL: Interlace flag

IL indicates whether the data of the field which is repeated twice to produce the frame is interlaced or noninterlaced.

0: Noninterlaced
1: Interlaced

11.10.3 VAUX format pack

Table 35 shows a mapping of the VAUX format pack.

Table 35 – Mapping of VAUX format pack

	MSB							LSB
PC0	1	0	0	0	0	0	0	1
PC1	CH			PA	VIDEO MODE			
PC2	SCANNING			IR	Res		EX MODE	
PC3	VISC							
PC4	Res							

CH: 000: 50 Mb/s
Others: Reserved

PA: Pair channel flag
0: One of pair channel
1: Not one of pair channel

VIDEO MODE: 0000: SD 4:2:2
Others: Reserved

SCANNING:
000: 60/1.001
001: 60
010: 50
011: 30/1.001
100: 30
101: 25
110: 24
111: Reserved

IR: 0: Interlaced
1: Noninterlaced

VISC: The phase difference between decoded chrominance subcarrier phase of composite video input signal and ScH

01111000:	180°
:	:
00000010:	3.0°
00000001:	1.5°
00000000:	0°
11111111:	–1.5°
:	:
10001000:	–180°
01111111:	No information
Others:	Reserved

11.10.4 VAUX extra line pack

Except for the vertical sync signal or active video lines shown in table 24, any other two lines may optionally

be recorded in the VAUX extra line pack. Encoded data is expressed by straight binary code with 8 linear bits. VAUX extra line packs are recorded in sync blocks 19 and 20 of the video 0 sector and sync blocks 20 and 156 of the video 1 sector.

Figure 39 shows the arrangement of VAUX extra line packs in the VAUX sync block. Table 36 shows a mapping of the VAUX extra line packs. Figures 40 and 41 show the data allocation of the VAUX extra line pack.

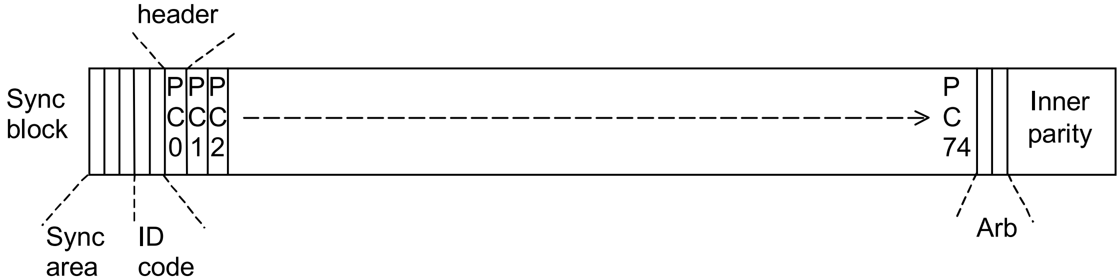


Figure 39 – Arrangement of VAUX extra line packs in VAUX sync blocks

Table 36 – Mapping of VAUX extra line pack

	MSB							LSB
PC0	1	1	1	0	1	0	1	1
PC1	Res		DATA TYPE			Res	LINE #[9:8]	
PC2	LINE #[7:0]							
PC3	LINE DATA 0							
PC4	LINE DATA 1							
PC5	LINE DATA 2							
PC6 | PC74	LINE DATA 3 | LINE DATA 71							

DATA TYPE: 000b: Y
001b: C

LINE#(9:0): 1~525: 525/60
1~625: 625/50

LINE DATA: 1~254

Res: Reserved bit for future use Default value shall be set to 1.

		Video 0 sector Extra line A	Video 1 sector Extra line B
	VAUX0	Y0, Y2, ···, Y142	
trk0	VAUX1	C_R0, C_B0, C_R2, C_B2, ···, C_R70, C_B70	C_R0, C_B0, C_R2, C_B2, ···, C_R70, C_B70
	VAUX2		Y0, Y2, ···, Y142
	VAUX0	C_R1, C_B1, C_R3, C_B3, ···, C_R71, C_B71	
trk1	VAUX1	Y1, Y3, ···, Y143	Y1, Y3, ···, Y143
	VAUX2		C_R1, C_B1, C_R3, C_B3, ···, C_R71, C_B71
	VAUX0	Y144,Y146, ···,Y286	
trk2	VAUX1	C_R72, C_B72, C_R74, C_B74, ···, C_R142, C_B142	C_R72, C_B72, C_R74, C_B74, ···, C_R142, C_B142
	VAUX2		Y144, Y146, ···, Y286
	VAUX0	C_R73, C_B73,C_R75, C_B75, ···, C_R143, C_B143	
trk3	VAUX1	Y145, Y147, ···, Y287	Y145, Y147, ···, Y287
	VAUX2		C_R73, C_B73, C_R75, C_B75, ···, C_R143, C_B143
	VAUX0	Y288, Y290, ···, Y430	
trk4	VAUX1	C_R144, C_B144, C_R146, C_B146, ···, C_R214, C_B214	C_R144, C_B144, C_R146, C_B146, ···, C_R214, C_B214
	VAUX2		Y288, Y290, ···, Y430
	VAUX0	C_R145, C_B145, C_R147, C_B147, ···, C_R215, C_B215	
trk5	VAUX1	Y289, Y291, ···, Y431	Y289, Y291, ···, Y431
	VAUX2		C_R145, C_B145, C_R147, C_B147, ···, C_R215, C_B215
	VAUX0	Y432, Y434, ···, Y574	
trk6	VAUX1	C_R216, C_B216, C_R218, C_B218, ···, C_R286, C_B286	C_R216, C_B216, C_R218, C_B218, ···, C_R286, C_B286
	VAUX2		Y432, Y434, ···, Y574
	VAUX0	C_R217, C_B217, C_R219, C_B219, ···, C_R287, C_B287	
trk7	VAUX1	Y433, Y435, ···, Y575	Y433, Y435, ···, Y575
	VAUX2		C_R217, C_B217, C_R219, C_B219, ···, C_R287, C_B287
	VAUX0	Y576, Y578, ···, Y718	
trk8	VAUX1	C_R288, C_B288, C_R290, C_B290, ···, C_R358, C_B358	C_R288, C_B288, C_R290, C_B290, ···, C_R358, C_B358
	VAUX2		Y576, Y578, ···, Y718
	VAUX0	C_R289, C_B289, C_R291, C_B291, ···, C_R359, C_B359	
trk9	VAUX1	Y577, Y579, ···, Y719	Y577, Y579, ···, Y719
	VAUX2		C_R289, C_B289, C_R291, C_B291, ···, C_R359, C_B359

Figure 40 – Data allocation of VAUX extra line pack for 525/60 system

Track		Video 0 sector Extra line A	Video 1 sector Extra line B
trk0	VAUX0	Y0, Y2, ···, Y142	
	VAUX1	C_R0, C_B0, C_R2, C_B2, ···, C_R70, C_B70	C_R0, C_B0, C_R2, C_B2, ···, C_R70, C_B70
	VAUX2		Y0, Y2, ···, Y142
trk1	VAUX0	C_R1, C_B1, C_R3, C_B3, ···, C_R71, C_B71	
	VAUX1	Y1, Y3, ···, Y143	Y1, Y3, ···, Y143
	VAUX2		C_R1, C_B1, C_R3, C_B3, ···, C_R71, C_B71
trk2	VAUX0	Y144,Y146, ···,Y286	
	VAUX1	C_R72, C_B72, C_R74, C_B74, ···, C_R142, C_B142	C_R72, C_B72, C_R74, C_B74, ···, C_R142, C_B142
	VAUX2		Y144, Y146, ···, Y286
trk3	VAUX0	C_R73, C_B73,C_R75, C_B75, ···, C_R143, C_B143	
	VAUX1	Y145, Y147, ···, Y287	Y145, Y147, ···, Y287
	VAUX2		C_R73, C_B73, C_R75, C_B75, ···, C_R143, C_B143
trk4	VAUX0	Y288, Y290, ···, Y430	
	VAUX1	C_R144, C_B144, C_R146, C_B146, ···, C_R214, C_B214	C_R144, C_B144, C_R146, C_B146, ···, C_R214, C_B214
	VAUX2		Y288, Y290, ···, Y430
trk5	VAUX0	C_R145, C_B145, C_R147, C_B147, ···, C_R215, C_B215	
	VAUX1	Y289, Y291, ···, Y431	Y289, Y291, ···, Y431
	VAUX2		C_R145, C_B145, C_R147, C_B147, ···, C_R215, C_B215
trk6	VAUX0	Y432, Y434, ···, Y574	
	VAUX1	C_R216, C_B216, C_R218, C_B218, ···, C_R286, C_B286	C_R216, C_B216, C_R218, C_B218, ···, C_R286, C_B286
	VAUX2		Y432, Y434, ···, Y574
trk7	VAUX0	C_R217, C_B217, C_R219, C_B219, ···, C_R287, C_B287	
	VAUX1	Y433, Y435, ···, Y575	Y433, Y435, ···, Y575
	VAUX2		C_R217, C_B217, C_R219, C_B219, ···, C_R287, C_B287
trk8	VAUX0	Y576, Y578, ···, Y718	
	VAUX1	C_R288, C_B288, C_R290, C_B290, ···, C_R358, C_B358	C_R288, C_B288, C_R290, C_B290, ···, C_R358, C_B358
	VAUX2		Y576, Y578, ···, Y718
trk9	VAUX0	C_R289, C_B289, C_R291, C_B291, ···, C_R359, C_B359	
	VAUX1	Y577, Y579, ···, Y719	Y577, Y579, ···, Y719
	VAUX2		C_R289, C_B289, C_R291, C_B291, ···, C_R359, C_B359
trk10	VAUX0		
	VAUX1		
	VAUX2		
trk11	VAUX0		
	VAUX1		
	VAUX2		

Figure 41 – Data allocation of VAUX extra line pack for 625/50 system

11.10.5 VAUX NO INFO pack

All VAUX packs that have no information shall be recorded with NO INFO packs. Table 37 shows a mapping of the NO INFO pack.

Table 37 – Mapping of NO INFO pack

	MSB							LSB
PC0	1	1	1	1	1	1	1	1
PC1	1	1	1	1	1	1	1	1
PC2	1	1	1	1	1	1	1	1
PC3	1	1	1	1	1	1	1	1
PC4	1	1	1	1	1	1	1	1

11.11 Error correction code addition

An inner error correction code and an outer error correction code are used to protect the video data.

11.11.1 Inner error correction code

The inner parity as shown in figure 10 is defined as a codeword of an inner error correction code.

The inner error correction code is a (85, 77) Reed-Solomon code in GF(256) of which the field generator polynomial is:

$$X^8 + X^4 + X^3 + X^2 + 1$$

where Xi are place-keeping variables in GF(256), the binary field.

The generator polynomial of the code in GF(256) is

$$gin(X) = (X +1)(X + \alpha)(X + \alpha^2)(X + \alpha^3)(X + \alpha^4)(X + \alpha^5)(X + \alpha^6)(X + \alpha^7)$$

where α is given in GF(256).

Parities $K_7, K_6, K_5, K_4, K_3, K_2, K_1, K_0$ are given by the equation:

$$K_7X^7+ K_6X^6 + K_5X^5 + K_4X^4 + K_3X^3 + K_2X^2 + K_1X + K_0,$$

which is the residue of $X^8D(X)$ divided by gin(X), where the data polynomial D(X) is defined as follows:

$$D(X) = D_{76}X^{76} + D_{75} X^{75} + ... + D_2X_2 + D_1X + D_0$$

and the codeword polynomial is given by the following equation:

$$D_{76}X^{84} + D_{75}X^{83} + ... + D_1X^9 + D_0X^8 + K_7X^7 + K_6X^6 + ... + K_1X + K_0$$

where D_{76} through D_0 correspond to the data of byte position number 5 through 81, and K_7 through K_0 to inner parity of byte position number 82 through 89, respectively.

11.11.2 Outer error correction code

The outer parity as shown in figure 12 is defined as a codeword of an outer error correction code. The outer error correction code is a (149, 138) Reed-Solomon code in GF(256) for which the field generator polynomial is

$$X^8 + X^4 + X^3 + X^2 + 1$$

where X^i are place-keeping variables in GF(256), the binary field.

The generator polynomial of the code in GF(256) is

$$Gvout(X) = (X + 1)(X + \alpha)(X + \alpha^2)(X + \alpha^3) \ldots (X + \alpha^9)(X + \alpha^{10})$$

where α is given by 2h in GF(256).

Parities K_{10}, K_9, K_8, K_7, K_6, K_5,K_4, K_3, K_2, K_1, K_0 are given by the equation:

$$K_{10}X^{10} + K_9X^9 + K_8X^8 + K_7X^7 + K_6X^6 + K_5X^5 + K_4X^4 + K_3X^3 + K_2X^2 + K_1X + K_0$$

which is the residue of $X^{11}D(X)$ divided by Gvout(X), where the data polynomial D(X) is defined as:

$$D(X) = D_{137}X^{137} + D_{136}X^{136} + \ldots + D_1X + D_0$$

and the codeword polynomial is given by the equation:

$$D_{137}X^{148} + D_{136}X^{147} + D_{135}X^{146} + \ldots + D_1X^{12} + D_0X^{11} + K_{10}X^{10} + K_9X^9 + \ldots + K_1X + K_0$$

where D137 through D0 correspond to the data bytes of sync block number 19 through 156, and K10 through K0 to outer parity of sync block number 157 through 167, respectively.

12 Subcode processing

12.1 Introduction

Subcode data are processed with every video frame. The subcode data shall be recorded for 10 consecutive tracks in a frame for the 525/60 system and 12 consecutive tracks in a frame for the 625/50 system. Each subcode sector is a block of 5 columns by 12 rows as shown in figure 14. Error correction code (ECC) parity bytes are added to subcode data prior to 24-25 modulation. There are several purposes for the subcode sector. The main purpose of the sector is to locate a certain point within the tape while in the high-speed shuttle mode.

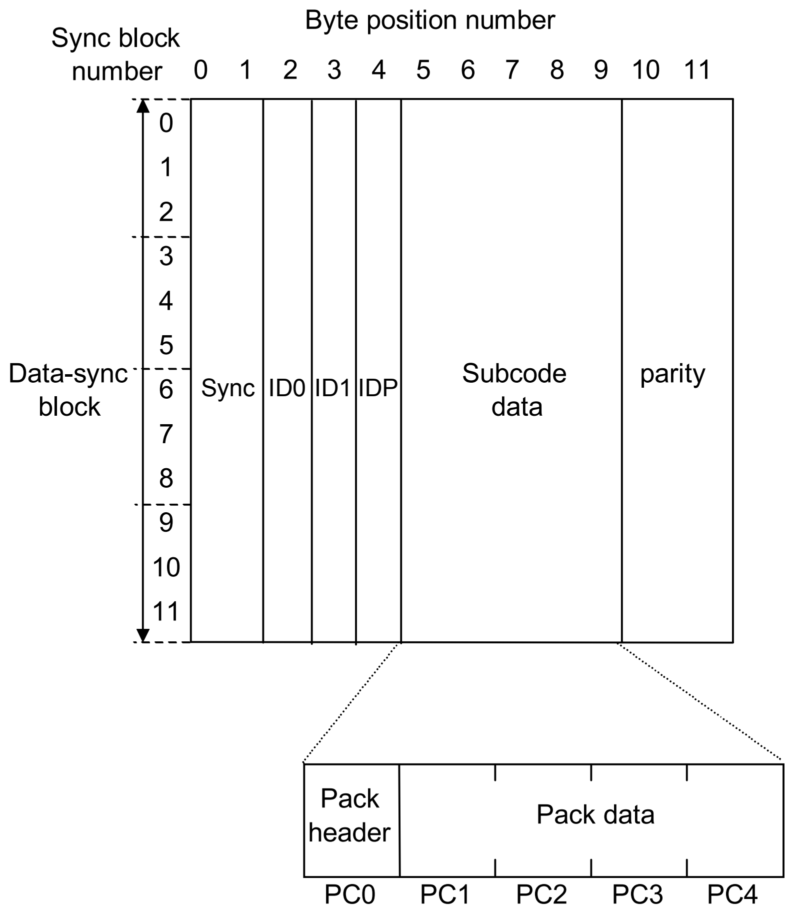


Figure 42 – Arrangement of subcode data packs in subcode sector

12.2 Subcode data

12.2.1 Subcode data pack

Subcode data in a subcode sync block consist of 5 bytes. Those bytes form a subcode data pack as shown in figure 42. A subcode data pack shall consist of a pack header byte and four bytes of pack data.

12.2.2 Mapping of subcode data

Table 38 shows the mapping of the subcode data.

Table 38 – Mapping of subcode data

Sync block number	Subcode data	
	The first half of a video frame	The second half of a video frame
0	Res	Res
1	Res	Res
2	Res	Res
3	MTC	MTC
4	STC	STC
5	MUB	SUB
6	Res	Res
7	Res	Res
8	Res	Res
9	MTC	MTC
10	STC	STC
11	MUB	SUB

MTC: MAIN TIME CODE pack (pack header = 13h)
STC: SUB TIME CODE pack (pack header = 23h)
MUB: MAIN USER's BINARY group pack (pack header = 33h)
SUB: SUB USER's BINARY group pack (pack header = 43h)

The first half of a video frame:
Track number 0 1 2 3 4 for the 525/60 system
Track number 0 1 2 3 4 5 for the 625/50 system
The second half of a video frame:
Track number 5 6 7 8 9 for the 525/60 system
Track number 6 7 8 9 10 11 for the 625/50 system

12.2.3 Time code pack (TC)

12.2.3.1 Main time code pack (MTC)

This pack contains linear time code (LTC). (See table 39.)

Table 39 – Mapping of MTC

	MSB							LSB
PC0	0	0	0	1	0	0	1	1
PC1	S2	S1	TENS of FRAMES		UNITS of FRAMES			
PC2	S3	TENS of SECONDS			UNITS of SECONDS			
PC3	S4	TENS of MINUTES			UNITS of MINUTES			
PC4	S6	S5	TENS of HOURS		UNITS of HOURS			

NOTE S1 to S6 flags shall be recorded with bit numbers based on SMPTE 12M

	Bit number (LTC)
S1:	10
S2:	11
S3:	27
S4:	43
S5:	58
S6	59

12.2.3.2 Sub time code pack (STC)

This pack contains vertical interval time code (VITC). (See table 40.)

Table 40 – Mapping of the STC

	MSB							LSB
PC0	0	0	1	0	0	0	1	1
PC1	S2	S1	TENS of FRAMES		UNITS of FRAMES			
PC2	S3	TENS of SECONDS			UNITS of SECONDS			
PC3	S4	TENS of MINUTES			UNITS of MINUTES			
PC4	S6	S5	TENS of HOURS		UNITS of HOURS			

NOTE S1 to S6 flags shall be recorded with bit numbers based on SMPTE 12M

	Bit number (LTC)
S1:	14
S2:	15
S3:	35
S4:	55
S5:	74
S6	75

12.2.3.3 Subcode NO INFO pack

All subcode data packs that have no information and are defined for reserved shall be recorded with NO INFO packs as shown in table 41.

Table 41 – Mapping of Subcode NO INFO pack

	MSB							LSB
PC0	1	1	1	1	1	1	1	1
PC1	1	1	1	1	1	1	1	1
PC2	1	1	1	1	1	1	1	1
PC3	1	1	1	1	1	1	1	1
PC4	1	1	1	1	1	1	1	1

12.2.4 Binary group pack (BG)

12.2.4.1 Main user's binary group pack (MUB)

Table 42 shows a mapping of MUB.

Table 42 – Mapping of MUB

	MSB							LSB
PC0	0	0	1	1	0	0	1	1
PC1	BINARY GROUP 2				BINARY GROUP 1			
PC2	BINARY GROUP 4				BINARY GROUP 3			
PC3	BINARY GROUP 6				BINARY GROUP 5			
PC4	BINARY GROUP 8				BINARY GROUP 7			

12.2.4.2 Sub user's binary group pack (SUB)

Table 43 shows a mapping of SUB.

Table 43 – Mapping of SUB

	MSB							LSB
PC0	0	1	0	0	0	0	1	1
PC1	BINARY GROUP 2				BINARY GROUP 1			
PC2	BINARY GROUP 4				BINARY GROUP 3			
PC3	BINARY GROUP 6				BINARY GROUP 5			
PC4	BINARY GROUP 8				BINARY GROUP 7			

12.3 Error correction code addition

Since AP3 = 001b, subcode data consist of 5 bytes and subcode parity consists of 2 bytes which are defined as a codeword of a subcode error correction code.

The subcode error correction code is a (14, 10) Reed-Solomon code in GF(16) of which the field generator polynomial is shown as follows:

$$X^4 + X + 1$$

where X^i are place-keeping variables in GF(2), the binary field.

The generator polynomial of the code in GF(16) is

$$gsub(X) = (X + 1)(X + \alpha)(X + \alpha^2)(X + \alpha^3)$$

where α is given by 2h in GF(16).

Parities, K_3, K_2, K_1, K_0, as shown in figure 43, are given by the equation

$$K_3X^3 + K_2X^2 + K_1X + K_0$$

which is the residue of $X^4D(X)$ divided by gsub(X), where the data polynomial D(X) is defined as

$$D(X) = D_9X^9 + D_8X^8 + ... + D_2X^2 + D_1X + D_0$$

and the codeword polynomial is given by the equation

$$D_9X^{13} + D_8X^{12} + ... + D_1X^5 + D_0X^4 + K_3X^3 + K_2X^2 + K_1X + K_0$$

Byte position number

	5	6	7	8	9	10	11
MSB	$d_{9,3}$	$d_{7,3}$	$d_{5,3}$	$d_{3,3}$	$d_{1,3}$	$k_{3,3}$	$k_{1,3}$
	$d_{9,2}$	$d_{7,2}$	$d_{5,2}$	$d_{3,2}$	$d_{1,2}$	$k_{3,2}$	$k_{1,2}$
	$d_{9,1}$	$d_{7,1}$	$d_{5,1}$	$d_{3,1}$	$d_{1,1}$	$k_{3,1}$	$k_{1,1}$
	$d_{9,0}$	$d_{7,0}$	$d_{5,0}$	$d_{3,0}$	$d_{1,0}$	$k_{3,0}$	$k_{1,0}$
	$d_{8,3}$	$d_{6,3}$	$d_{4,3}$	$d_{2,3}$	$d_{0,3}$	$k_{2,3}$	$k_{0,3}$
	$d_{8,2}$	$d_{6,2}$	$d_{4,2}$	$d_{2,2}$	$d_{0,2}$	$k_{2,2}$	$k_{0,2}$
	$d_{8,1}$	$d_{6,1}$	$d_{4,1}$	$d_{2,1}$	$d_{0,1}$	$k_{2,1}$	$k_{0,1}$
LSB	$d_{8,0}$	$d_{6,0}$	$d_{4,0}$	$d_{2,0}$	$d_{0,0}$	$k_{2,0}$	$k_{0,0}$
	Subcode data					Subcode parity	

Where $Dn = (dn,3\ dn,2\ dn,1\ dn,0)\ 9 \geq n \geq 0$
$Kn = (kn,3\ kn,2\ kn,1\ kn,0)\ 3 \geq n \geq 0$

Figure 43 – Bit assignment for the subcode data and subcode parity

13 Interface

13.1 Introduction

Figure 44 shows the configuration of the digital interface in the D-9 VTR. This clause describes only the data structure on the digital interface.

The applied data is as follows:

AP1, sequence numbers, AAUX, and audio data in the audio sector;
AP2, sequence numbers, VAUX, and video data in the video sector;
AP3, APT, ID data, and subcode data in the subcode sector.

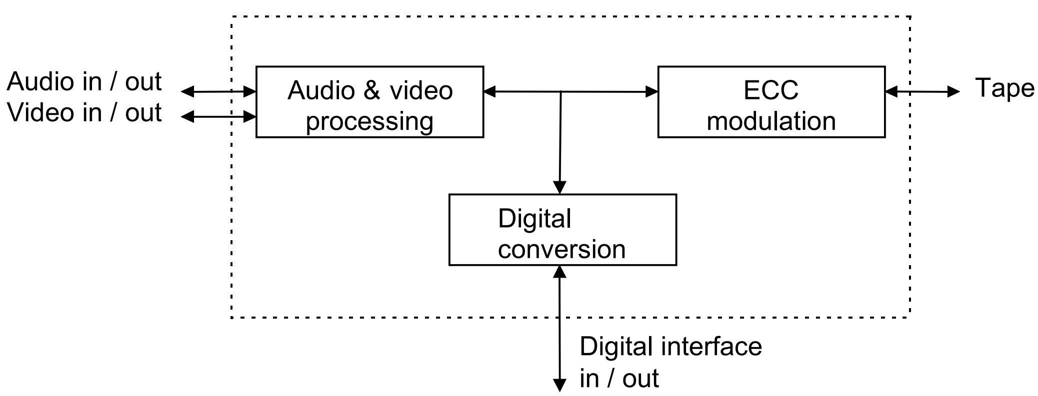


Figure 44 – Block diagram of digital interface

13.2 Data structure

The data structure of the digital interface is shown in figure 45.

The data for one video frame period, including video frame data, audio data accompanying the video frame, and all ancillary data are divided into two channels. Each channel is divided into 10 DIF sequences for the 525/60 system and 12 DIF sequences for the 625/50 system. Each DIF sequence has a header section, a subcode section, a VAUX section, and an audio and video section, in that order, and consists of 300 DIF blocks.

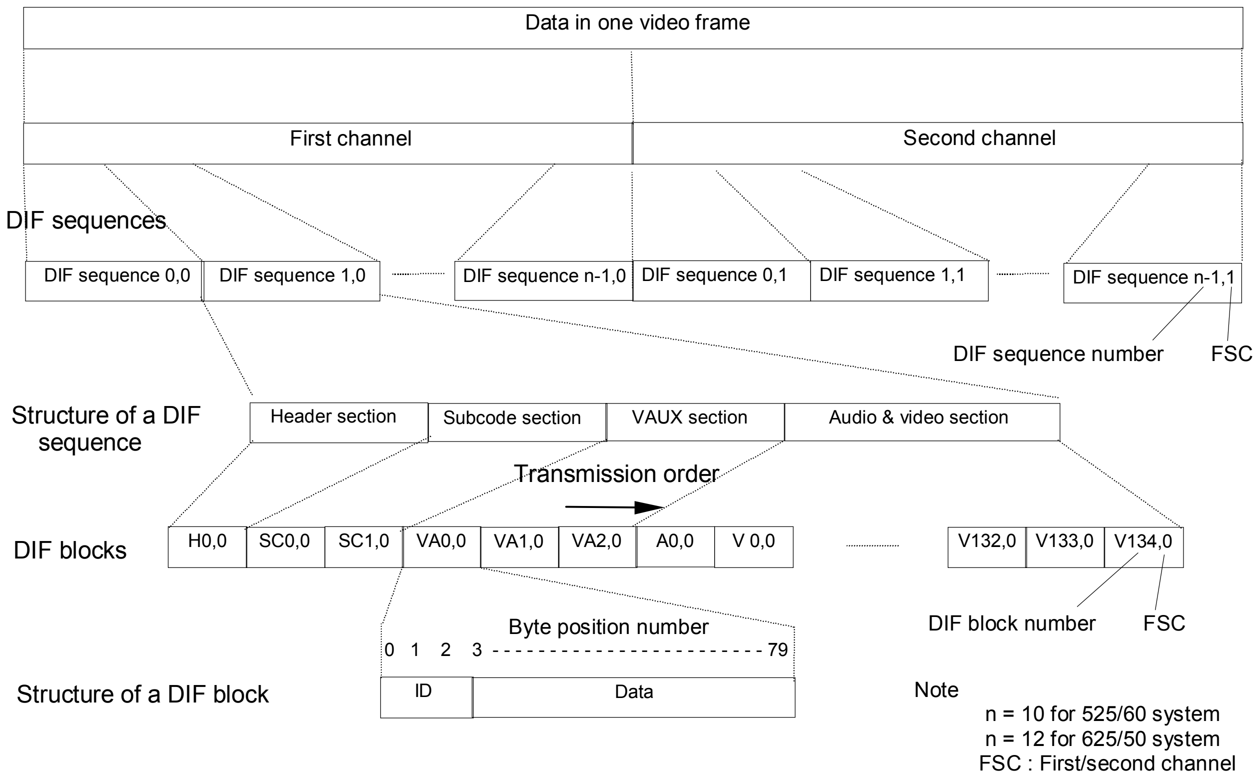


Figure 45 – Data structure for transmission

13.2.1 ID

The ID part consists of ID data (ID0, ID1, ID2) consisting of 3 bytes. Figure 46 shows the ID data in a DIF block.

ID data consists of section type (SCT2, SCT1, SCT0, [see table 44]), DIF sequence number (Dseq3, Dseq2, Dseq1, Dseq0 [see tables 45 and 46]), DIF block set number (FSC), and DIF block number (DBN7, DBN6, DBN5, DBN4, DBN3, DBN2, DBN1, DBN0).

- FSC indicates the order of DIF block set.
- FSC = 0: First block.
- FSC = 1: Second block.
- Arb is an arbitrary bit.

	Byte position number 0	1	2
	ID0	ID1	ID2
MSB	SCT_2	$Dseq_3$	DBN_7
	SCT_1	$Dseq_2$	DBN_6
	SCT_0	$Dseq_1$	DBN_5
	Res	$Dseq_0$	DBN_4
	Arb	FSC	DBN_3
	Arb	Res	DBN_2
	Arb	Res	DBN_1
LSB	Arb	Res	DBN_0

Figure 46 – ID data in a DIF block

Table 44 – DIF block type

SCT_2	SCT_1	SCT_0	Section type
0	0	0	Header
0	0	1	Subcode
0	1	0	VAUX
0	1	1	Audio
1	0	0	Video
1	0	1	Res
1	1	0	
1	1	1	

Table 45 – DIF sequence number (525/60 system)

$Dseq_3$	$Dseq_2$	$Dseq_1$	$Dseq_0$	Meaning
0	0	0	0	DIF sequence number 0
0	0	0	1	DIF sequence number 1
0	0	1	0	DIF sequence number 2
0	0	1	1	DIF sequence number 3
0	1	0	0	DIF sequence number 4
0	1	0	1	DIF sequence number 5
0	1	1	0	DIF sequence number 6
0	1	1	1	DIF sequence number 7
1	0	0	0	DIF sequence number 8
1	0	0	1	DIF sequence number 9
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

Table 46 – DIF sequence number (625/50 system)

$Dseq_3$	$Dseq_2$	$Dseq_1$	$Dseq_0$	Meaning
0	0	0	0	DIF sequence number 0
0	0	0	1	DIF sequence number 1
0	0	1	0	DIF sequence number 2
0	0	1	1	DIF sequence number 3
0	1	0	0	DIF sequence number 4
0	1	0	1	DIF sequence number 5
0	1	1	0	DIF sequence number 6
0	1	1	1	DIF sequence number 7
1	0	0	0	DIF sequence number 8
1	0	0	1	DIF sequence number 9
1	0	1	0	DIF sequence number 10
1	0	1	1	DIF sequence number 11
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

13.2.2 Data

13.2.2.1 Header section

The header section consists of two DIF blocks (H0,0 and H0,1). The data part of the header section is shown in figure 47. Byte positions number 3 to 7 are used and the rest of the data are reserved. The header section includes the data about the DIF sequence and the ITI sector.

- Res: A reserved bit for future use, and the value is 1.
- DSF: DIF sequence flag.
- DSF = 0: 10 DIF sequences included in a block (525/60 system)
- DSF = 1: 12 DIF sequences included in a block (625/50 system)

These data shall be kept the same value in a frame. When no ITI data are transmitted, "no information" shall be transmitted.

APT, AP1, AP2, AP3: Application IDs (see 8.2.3.2, 8.3.3.2, and 8.4.3.2). When not transmitting these data, "no information" shall be transmitted.

APTn: Application ID for track. APTn is shown in table 47. If the signal source is unknown, all bits for these data shall be set to 1. AP1, AP2, and AP3 shall be identical with APT.

TF1, TF2, TF3: Transmitting flag of area n (where n = 1, 2, 3).

TFn = 0: DIF blocks of area n are transmitted in the current DIF sequence.

TFn = 1: DIF blocks of area n are not transmitted in the current DIF sequence.

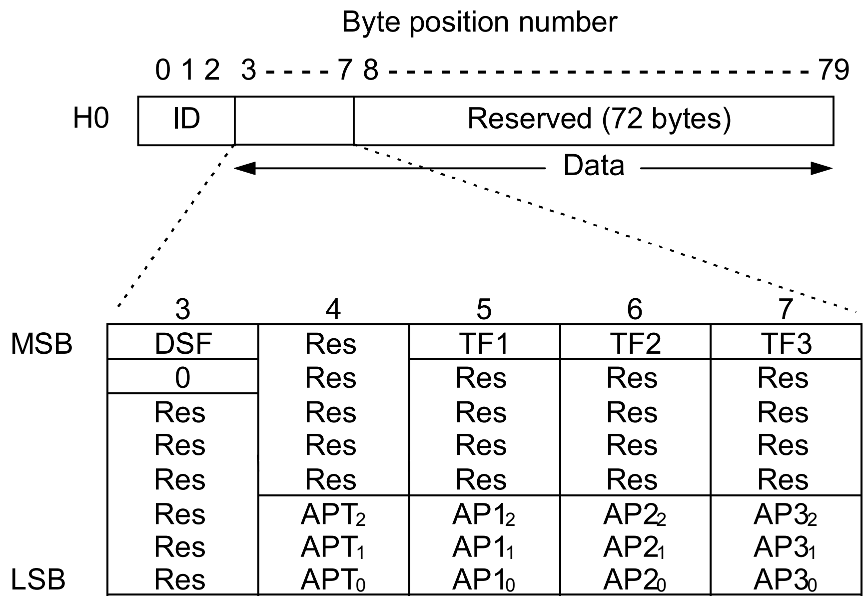


Figure 47 – Data in the header section

Table 47 – Application ID for track

Application ID for track			Format type
APT_2	APT_1	APT_0	
0	0	0	Res
0	0	1	D-9 use
0	1	0	Res
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

13.2.2.2 Subcode section

The data part of the subcode section is shown in figure 48. Subcode ID data and subcode data whose byte position number is 2 to 9 are distributed in the subcode section. Since subcode ID parity is not necessary, a reserved byte is transmitted instead of it. The data of 24 subcode sync blocks in a track are transmitted by four DIF blocks (SC0,0, SC0,1, SC1,0, SC1,1) in a subcode section.

When not transmitting subcode ID, Syb3, Syb2, Syb1, and Syb0 shall be 111b. When not transmitting subcode data, a NO INFO pack shall be transmitted. Correspondence between DIF blocks and subcode sync blocks is shown in table 48.

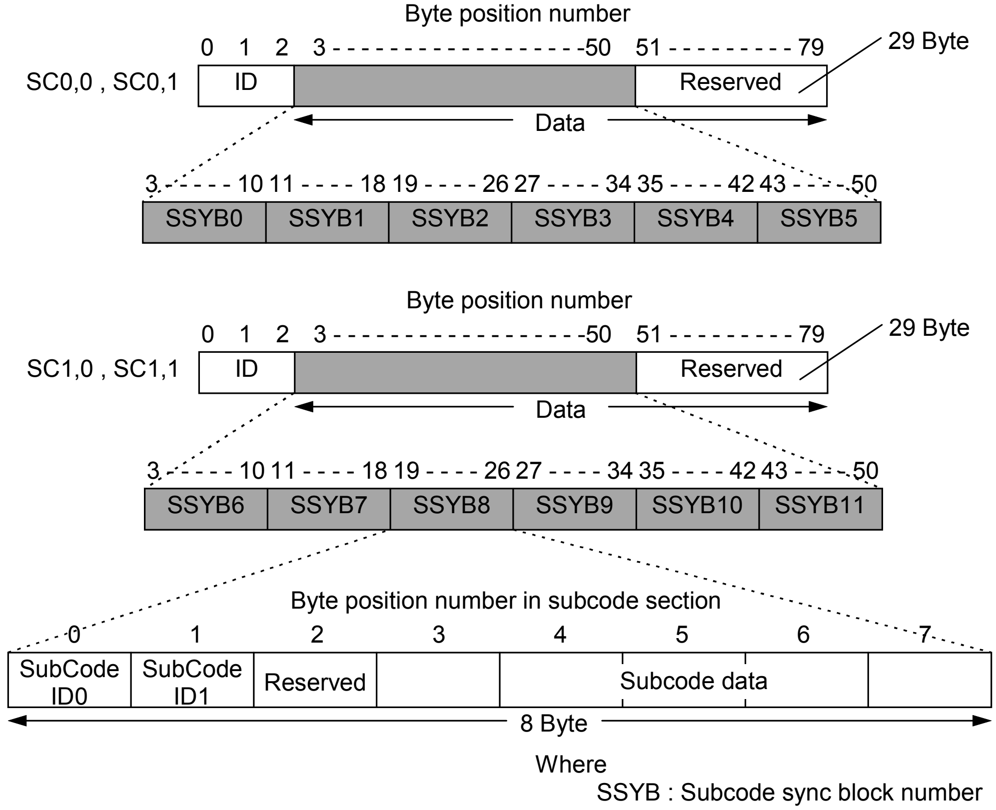


Figure 48 – Data in the subcode section

Table 48 – DIF blocks and subcode sync blocks

DIF sequence number	DIF block	Track number	SSYB
0	SC0,0	0	0 to 5
	SC0,1		
	SC1,0	0	6 to 11
	SC1,1		
1	SC0,0	1	0 to 5
	SC0,1		
	SC1,0	1	6 to 11
	SC1,1		
2	SC0,0	2	0 to 5
	SC0,1		
	SC1,0	2	6 to 11
	SC1,1		
. . .	. . .	. . .	. . .
n-1	SC0,0	n-1	0 to 5
	SC0,1		
	SC1,0	n-1	6 to 11
	SC1,1		

NOTES
1 SSYB: Subcode sync block number
2 n = 10 for 525/60 system
3 n = 12 for 625/50 system

13.2.2.3 VAUX section

The data part of the VAUX section is shown in figure 49. VAUX data whose byte position number is 5 to 81 are distributed in the VAUX section. The VAUX data of two sector 0 blocks in two tracks are transmitted by six DIF blocks (VA0,0, VA0,1, VA1,0, VA1,1, VA2,0, VA2,1) in a VAUX section. Correspondence between DIF blocks and VAUX data sync blocks is shown in table 49.

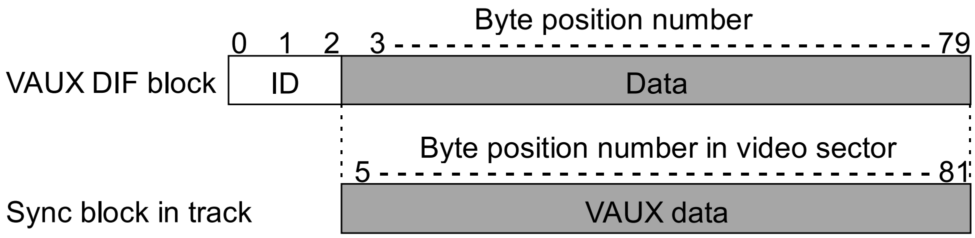


Figure 49 – Data in the VAUX section

Table 49 – DIF blocks and VAUX data sync blocks

DIF sequence number	DIF block	Sector number	Track number	SYB
0	VA0,0	0	0	19
	VA0,1		1	
	VA1,0	0	0	20
	VA1,1		1	
	VA2,0	0	0	156
	VA2,1		1	
1	VA0,0	1	0	19
	VA0,1		1	
	VA1,0	1	0	20
	VA1,1		1	
	VA2,0	1	0	156
	VA2,1		1	
2	VA0,0	0	2	19
	VA0,1		3	
	VA1,0	0	2	20
	VA1,1		3	
	VA2,0	0	2	156
	VA2,1		3	
:	:	:	:	:
n-1	VA0,0	1	n-2	19
	VA0,1		n-1	
	VA1,0	1	n-2	20
	VA1,1		n-1	
	VA2,0	1	n-2	156
	VA2,1		n-1	

NOTES
1 SYB: Sync block number
2 PN: Packet number
3 n = 10 for 525/60 system
4 n = 12 for 625/50 system

When VAUX data are not transmitted or errors are detected in any pack of VAUX, the VAUX pack shall be replaced by the NO INFO pack. VAUX SOURCE and VAUX SOURCE CONTROL packs shall keep the same value within each video frame.

– VAUX source pack

Table 50 shows a mapping of the VAUX source pack.

Table 50 – Mapping of VAUX source pack for interface

	MSB							LSB
PC0	0	1	1	0	0	0	0	0
PC1	Res	Res	Res	Res	Res	Res	Res	Res
PC2	B/W	EN	CLF		Res	Res	Res	Res
PC3	SOURCE CODE		50/60	STYPE				
PC4	VISC							

B/W: Black-and-white flag
- 0: Black and white
- 1: Color

EN: Color frame enable flag
- 0: CLF is valid
- 1: CLF is invalid

CLF: Color frame identification code (refer to ITU-R BT.470).

50/60	CLF	Form	CLF Identification
0	00	525/60 system	Color frame A
	01		Color frame B
	Others		Res
1	00	625/50 system	1st, 2nd fields
	01		3rd, 4th fields
	10		5th, 6th fields
	11		7th, 8th fields

SOURCE CODE: SOURCE CODE defines the input source of the video signal.
- 00b: Camera input
- 01b: Reserved
- 10b: Reserved
- 11b: No information

50/60:
- 0: 525/60
- 1: 625/50

STYPE: STYPE defines a video signal type in combination with the 50/60 flag as follows:

STYPE	50/60	
	0	1
00000	Reserved	Reserved
:		
00011		
00100	525/60 system 480 line (4:2:2 50M)	625/50 system 576 line (4:2:2 50M)
00101	Reserved	Reserved
:		
11111		

VISC:

01111000:	180°
:	:
00000010:	3.0°
00000001:	1.5°
00000000:	0°
11111111:	–1.5°
:	:
10001000:	–180°
01111111:	No information
Others:	Reserved

– VAUX source control pack

Table 51 shows a mapping of the VAUX source control pack.

Table 51 – Mapping of VAUX source control pack for interface

	MSB							LSB
PC0	0	1	1	0	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	Res	Res
PC2	RECST	Res	0	0	Res	DISP		
PC3	FF	FS	FC	IL	Res	Res	0	0
PC4	Res	Res	Res	Res	Res	Res	Res	Res

CGMS: Copy generation management system

CGMS	Copy possible
00	Copy free
01	Res
10	Res
11	Res

REC ST: Recording start point

0: Recording start point

1: Not recording start point

Recording start point flag shall be recorded during the first frame of the new recording.

DISP: Display select mode

DISP	Aspect ratio and format	Position
000 001 010	4:3 full format Res 16:9 full format (squeeze)	not applicable ---- not applicable
011 | 111	Res	

FF: Frame/field flag

FF indicates whether the frame is produced from two sequential fields, or by repeating one field twice.

0: Field repeated twice
1: Frame

FS: First/second flag

FS indicates which field is repeated twice to produce the frame.

0: Field 2 used
1: Field 1 used

FF	FS	Output field
0	0	Field 2 is repeated twice
0	1	Field 1 is repeated twice
1	0	Field 2 and field 1 are processed in that order
1	1	Field 1 and field 2 are processed in that order

FC: Frame change flag

FC indicates whether the picture of the current frame is the same picture as that in the immediate previous frame.

0: Same picture as the immediate previous frame
1: Different picture from the immediate previous frame.

IL: Interlace flag

IL indicates whether the data of the field which is to produce the frame are interlaced or noninterlaced.

0: Noninterlaced
1: Interlaced

13.2.2.4 Audio section

The data part of the audio section is shown in figure 50. Audio and AAUX data whose byte position number is 5 to 81 are distributed in the audio section. The audio and AAUX data of 18 data sync blocks in a track are transmitted by 18 DIF blocks (A0,0, A0,1, to A8,0, A8,1) in an audio section. Correspondence between DIF blocks and audio data sync blocks is shown in table 52.

If errors are detected in the audio data, these error samples should be replaced an with audio error code as described in 10.7. When not transmitting AAUX data, a NO INFO pack shall be transmitted. If errors are detected in any pack of AAUX, a NO INFO pack should be transmitted. AAUX SOURCE and AAUX SOURCE CONTROL packs shall keep the same value in each audio block.

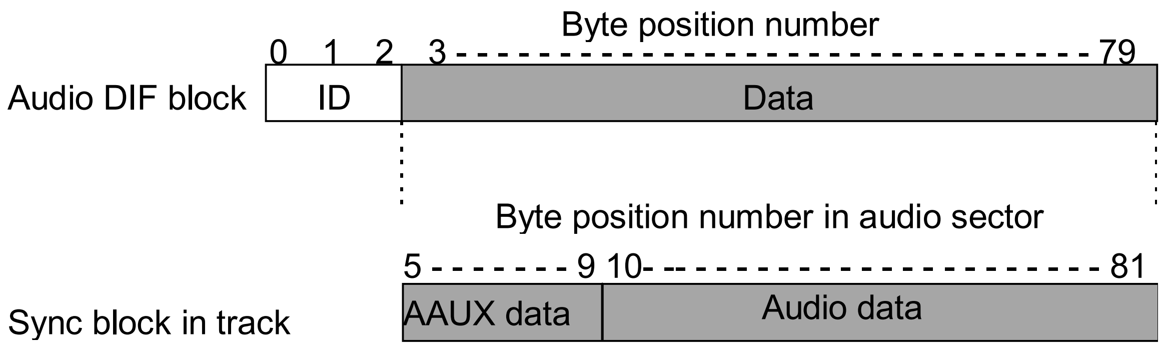


Figure 50 – Data in the audio section

Table 52 – DIF blocks and audio data sync blocks

DIF sequence number	DIF block	Track number	Sector number	SYB
0	A0,0	0	0	2
	A0,1		1	
	A1,0	0	0	3
	A1,1		1	
	⋮	⋮	⋮	⋮
	A8,0	0	0	10
	A8,1		1	
1	A0,0	1	0	2
	A0,1		1	
	A1,0	1	0	3
	A1,1		1	
	⋮	⋮	⋮	⋮
	A8,0	1	0	10
	A8,1		1	
⋮	⋮	⋮	⋮	⋮
n/2-1	A0,0	n/2-1	0	2
	A0,1		1	
	A1,0	n/2-1	0	3
	A1,1		1	
	⋮	⋮	⋮	⋮
	A8,0	n/2-1	0	10
	A8,1		1	
n/2	A0,0	n/2	1	2
	A0,1		0	
	A1,0	n/2	1	3
	A1,1		0	
	⋮	⋮	⋮	⋮
	A8,0	n/2	1	10
	A8,1		0	
⋮	⋮	⋮	⋮	⋮
n-1	A0,0	n-1	1	2
	A0,1		0	
	A1,0	n-1	1	3
	A1,1		0	
	⋮	⋮	⋮	⋮

– AAUX source pack

The data in the AAUX source pack are the same as those in 10.6.1 except that table 21 shall be read as table 53.

Table 53 – Mapping of AAUX source pack for interface

	MSB							LSB
PC0	0	1	0	1	0	0	0	0
PC1	LF	1	AF SIZE					
PC2	0	CHN		1	AUDIO MODE			
PC3	1	1	50/60	STYPE				
PC4	EF	1	SMP			QU		

LF: Locked mode flag

Locking condition of audio sampling frequency with video signal

0: Sequence locked mode
1: Reserved

AF SIZE: Audio frame size

The number of audio samples per frame (sampling frequency: 48 kHz)

	525/60 system
000000	1580
|	|
|	|
|	|
101000	1620
|	Res
|	|
111111	Res

	625/50 system
000000	1896
|	|
|	|
|	|
110000	1944
|	Res
|	|
111111	Res

CHN: The number of audio channels within an audio block

00b: One channel per audio block
Others: Reserved

AUDIO MODE: The contents of the audio signal on each sector.

AUDIO MODE	CHN	
	00	01
0000	CH1(CH3)	Res
0001	CH2(CH4)	Res
0010 | 1110	Res	
1111	No information	

50/60:

0: 60 field system
1: 50 field system

STYPE: STYPE defines audio blocks per video frame

STYPE	audio blocks / frame
00000	2
00001	1
00010	4
00011	Res

EF: Emphasis flag
0: On
1: Off

SMP: Sampling frequency
000b: 48 kHz
Others: Reserved

QU: Quantization
000b: 16 bits linear
Others: Reserved

– AAUX source control pack

Table 54 shows a mapping of the AAUX source control pack

Table 54 – Mapping of AAUX source control pack for interface

	MSB							LSB
PC0	0	1	0	1	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	EMPHASIS	
PC2	REC ST	REC END	FADE ST	FADE END	Res	Res	Res	Res
PC3	DRF	SPEED						
PC4	Res	Res	Res	Res	Res	Res	Res	Res

CGMS: Copy generation management system

CGMS	Copy possible
0 0	Copy free
0 1	Res
1 0	Res
1 1	Res

EMPHASIS: Emphasis flag

EMPAHSIS	CHN=00	CHN=01	
	CH1 or CH2 or CH3 or CH4	Cha or CHc or CHe or CHg	CHb or CHd or CHf or CHh
00	off	off	off
01	on	on	off
10	Res	off	on
11		on	on

REC ST: Recording start frame of CH1, CH2, CH3, CH4, CHa, CHc, CHe, or CHg

The duration of the recording start frame shall be one audio block period for each recording channel.

REC ST	CHN=00	CHN=01
	CH1 or CH2 or CH3 or CH4	CHa or CHc or Che or CHg
0	Recording start frame	
1	Not recording start frame	

REC END: Recording end frame of CH1, CH2, CH3, CH4, CHa, CHc, CHe, or CHg

The duration of the recording end frame shall be one audio block period for each recording channel.

REC ST	CHN=00	CHN=01
	CH1 or CH2 or CH3 or CH4	CHa or CHc or Che or CHg
0	Recording end frame	
1	Not recording end frame	

FADE ST: Editing start point reproduction of CH1, CH2, CH3, CH4, CHa, CHc, CHe, or CHg

The duration of the editing start point shall be one audio block period for each recording channel.

FADE ST	CHN=00	CHN=01
	CH1 or CH2 or CH3 or CH4	CHa or CHc or CHe or CHg
0	Direct cut	
1	Fade_out_in	

FADE END: Editing end point reproduction of CH1, CH2, CH3, CH4, CHa, CHc, CHe, or CHg

The duration of the editing end point shall be one audio block period for each recording channel.

FADE END	CHN=00	CHN=01
	CH1 or CH2 or CH3 or CH4	CHa or CHc or CHe or CHg
0	Direct cut	
1	Fade_out_in	

DRF: Direction flag:

0: Reverse direction
1: Forward direction

SPEED: Playback speed

Playback speed is defined by coarse value plus fine value. Playback speed = 1 indicates normal speed. SPEED constants of 7 bits.

SPEED	Playback speed of VCR	
	525/60 system	625/50 system
0000000	0/120 (=0)	0/100 (=0)
0000001	1/120	1/100
0000010	2/120	2/100
•	•	•
•	•	•
1100100	100/120	100/100 (=1)
•	•	Res
•	•	Res
1111000	120/120 (=1)	Res
• •	Res Res	Res Res
1111110	Res	Res
1111111	Data Invalid	Data Invalid
Note – Res: Reserved bits for future use. Default value shall be set to 1.		

13.2.2.5 Video section

The data part of the video section is shown in figure 51. Video data whose byte position number is 5 to 81 are distributed in the video section. The video data of the 270 data sync blocks which are gathered from the various tracks are transmitted by 270 DIF blocks (V0,0, V0,1 to V134,0, V134,1) in a video section.

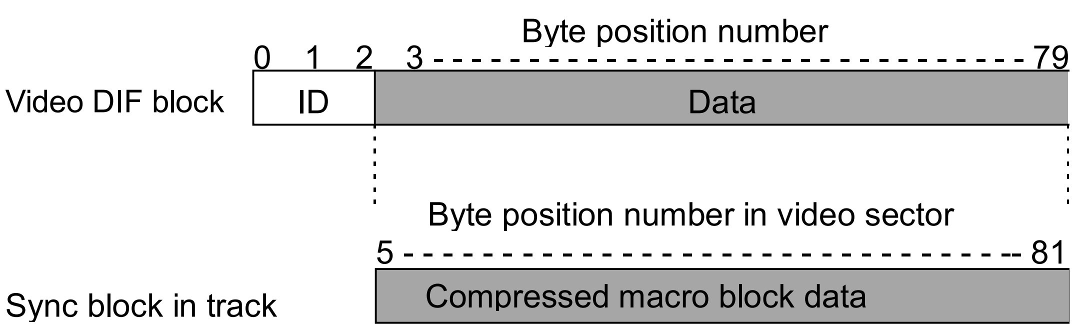


Figure 51 – Data in the video section

Correspondence between the DIF blocks and the video compressed macro blocks is shown in table 55.

The corresponding rule is as follows:

```
if (525/60 system) n = 10 else n = 12;
for (i = 0; i<n; i++) {
        a = i;
        b = (i - 6) mod n;
        c = (i - 2) mod n;
        d = (i - 8) mod n;
        e = (i - 4) mod n;
        p = a;
        q = 3;
```

```
    for (j = 0; j<5; j++) {
        for (k = 0; k<27; k++) {
            V(5 x k + q), 0 of DSNp = CM2i,j,ki;
            V(5 x k + q), 1 of DSNp = CM2i+1,j,ki;
        }
              if (q == 3) {p = b; q = 1;}
        else if (q == 1) {p = c; q = 0;}
        else if (q == 0) {p = d; q = 2;}
        else if (q == 2) {p = e; q = 4;}
    }
}
```

If a compressed macro block is replaced by another compressed macro block for error concealment or for fast playback mode, the STA data of the compressed macro block should be changed. For example, STA of 4 bits at fast playback mode is changed to 1110b.

Table 55 – DIF blocks and compressed macro blocks

DIF sequence number	DIF block	Compressed macro block
0	V0,0	$CM_{4,2,0}$
	V0,1	$CM_{5,2,0}$
	V1,0	$CM_{12,1,0}$
	V1,1	$CM_{13,1,0}$
	V2,0	$CM_{16,3,0}$
	V2,1	$CM_{17,3,0}$
	• •	• •
	V134,0	$CM_{8,4,26}$
	V134,1	$CM_{9,4,26}$
1	V0,0	$CM_{6,2,0}$
	V0,1	$CM_{7,2,0}$
	V1,0	$CM_{14,1,0}$
	V1,1	$CM_{15,1,0}$
	V2,0	$CM_{18,3,0}$
	V2,1	$CM_{19,3,0}$
	• •	• •
	V134,0	$CM_{10,4,26}$
	V134,1	$CM_{11,4,26}$
• •	• •	• •
n-1	V0,0	$CM_{2,2,0}$
	V0,1	$CM_{3,2,0}$
	V1,0	$CM_{10,1,0}$
	V1,1	$CM_{11,1,0}$
	V2,0	$CM_{14,3,0}$
	V2,1	$CM_{15,3,0}$
	• •	• •
	V134,0	$CM_{6,4,26}$
	V134,1	$CM_{7,4,26}$

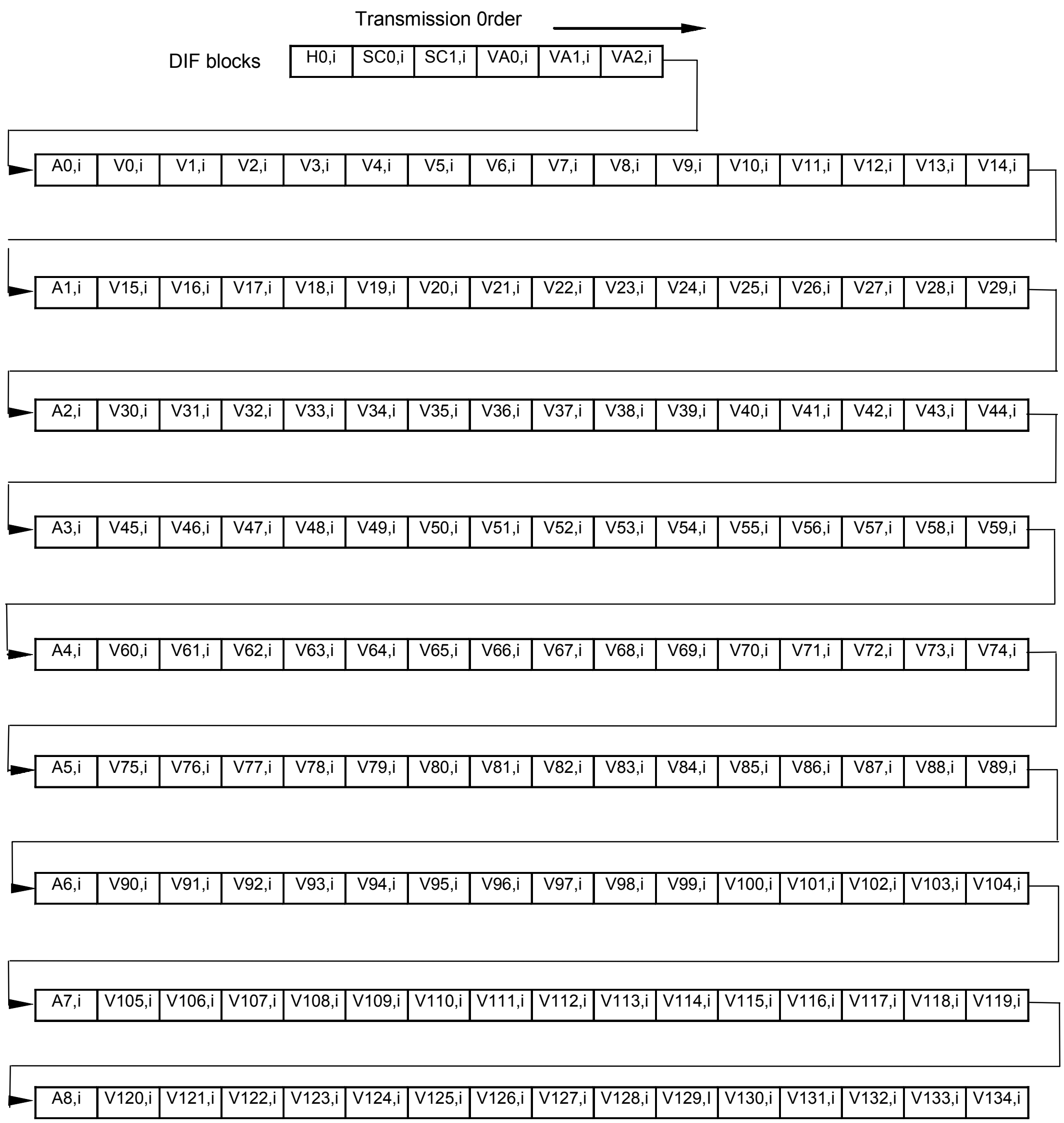
NOTES
1 n = 10 for 525/60 system
2 n = 12 for 625/50 system

13.3 Transmission order

The transmission order of the DIF blocks shall be as defined in figure 52.

13.4 Frame period

Deviation of a frame duration during transmission should be within +1% to –1% for every frame except for transient states. Therefore, a frame duration should be within 33,033 ms to 33,700 ms for the 525/60 system and 39,600 ms to 40,400 ms for the 625/50 system.



NOTES

1	i:	FSC i = 0,1 for 50 Mb/s structure
2	H0,i:	DIF block in header section
3	SC0,i to SC1,i :	DIF blocks in subcode section
4	VA0,i to VA2,i	DIF blocks in VAUX section
5	A0,i to A8,I:	DIF blocks in audio section
6	V0,i to V134,i:	DIF blocks in video section

Figure 52 – Transmission order of DIF blocks in a DIF sequence

13.5 Playback speed

Instead of the SPEED flag which is recorded during recording, playback speed shall be transmitted as SPEED in the AAUX SOURCE CONTROL pack when the machine is in playback mode. The SPEED consists of 7 bits and 1111111b is indicative of no information or an unknown speed.

For normal playback, the SPEED flag recorded on the tape shall be transmitted as it is.

When the machine is playing back in a non-normal mode and the speed flag recorded on tape is normal, the actual playback speed shall be transmitted.

When the machine is playing back in a no-normal mode and the speed flag recorded on tape is not normal, 1111111b shall be transmitted.

Annex A (informative)
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