PROPOSED SMPTE STANDARD

for Television —
Mapping of Vertical Ancillary Data Packets (VANC) into VAUX DIF Blocks of DV-Based 100 Mb/s DIF Stream Format

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1 Scope

This standard specifies the mapping of vertical ancillary data packets (VANC) into the payload area of the DV-based 100 Mb/s digital interface format (DIF) structure VAUX DIF blocks as defined in SMPTE 370M. Metadata and data essence may be contained in VANC packets present in vertical blanking interval (VBI) of the uncompressed high-fefinition serial digital interface (HD-SDI). The purpose of this standard is to define how such data is mapped into the video auxiliary (VAUX) DIF blocks of the 100 Mb/s DV-based compressed signal stream format. This mapping is applicable to the 1080/60i, 1080/50i, and 720/60p signal formats present on the HD-SDI.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

SMPTE 291M-1997, Television – Ancillary Data Packet and Space Formatting

SMPTE 292M-1998, Television – Bit-Serial Digital Interface for High-Definition Television Systems

SMPTE 370M—2002, Television – Data Structure for DV Based Audio, Data and Compressed Video at 100 Mb/s 1080/60i, 1080/50i, 720/60p

SMPTE RP 168-2002, Definition of Vertical Switching Point for Synchronous Video Switching

3 General description

Metadata and Data Essence can be carried in the Ancillary space of the HD-SDI stream structure. These data that are formatted according SMPTE 291M as VANC packets are located in a VBI space. The VANC packets can be converted/transformed and subsequently mapped into an available data space of the 100 Mb/s DV-based DIF stream. The space that is used for the mapping of these VANC packets is located in multiple VAUX DIF blocks of a DIF frame. Multiple DIF blocks (each 80 bytes long) form a DIF Sequence. Several DIF Sequences form a DIF frame, all defined in the SMPTE 370M (see figure 1).

The conversion process converts VANC packets into DIF ancillary data packet (DANC). Every VANC packet is converted into a DANC packet of an identical length, as is the originating VANC packet. The resulting DANC packets are then assembled into a string of DANC packets and this string is then mapped into the available space of the VAUX DIF blocks.

Due to the limited total VAUX DIF block space, and to achieve maximum benefit of the available space for the user, management of the data space by the user should be established (see note 1). A specific data management method is beyond the scope of this standard.

NOTE 1: Designers should be aware that the size of VANC data can exceed the capacity of the VAUX packs. It is the responsibility of the application to manage the mapping of VANC data into VAUX packs such that only complete VANC packets are mapped into VAUX DIF blocks. Where the VAUX capacity is exceeded, it is the responsibility of the application to manage this mapping in such a way as to minimize the effect on system performance, of not mapping all of the VANC data

The ancillary packet conversion to DANC packet is a direct conversion technique, fully transparent for the data content, and is defined in this standard.

3.1 Data capacity of the mapped space (VAUX DIF block space) and its structure

Figure 1 shows the typical organization of a DIF frame and DIF Sequence for a DV-based 100 Mb/s stream structure as described in SMPTE 370M.

The basic VAUX DIF block space that is used for mapped VANC packets consists of three VAUX DIF blocks VA 0,i; VA 1,i; and VA 2,i located in multiple DIF sequences. These DIF sequences form a DIF frame. The payload space of these three VAUX DIF blocks is subdivided into smaller entities called VAUX packs. These VAUX packs exist in 5-byte, 45-byte, and 75-byte long form (see figure 3a, 3b, and 3c).

i) 5-byte long VAUX pack —
The 5-byte long VAUX pack is defined in the SMPTE 370M. These 5-byte long VAUX packs (see figure 3a) may be used in any of the VAUX DIF blocks, regardless of odd or even DIF sequence.

ii) 45-byte or 75-byte long VAUX pack —
Additionally, this standard defines a different payload structure of the VAUX DIF block that is not defined in SMPTE 370M (see figures 3b and 3c). These new structures are based on a 45-byte or 75-byte long VAUX pack. The reason for these additional structures is to increase payload efficiency. However, the structure of a used VAUX pack is determined by the actual structure of a VAUX DIF block and if this block is located in an odd or even DIF sequence (see figure 2).

The user available payload capacity of all VAUX DIF blocks in a single DIF frame using different VAUX pack structures is shown below:

In the case of a VAUX DIF block that uses the 5-byte VAUX pack structure:

1080/60i system: 4 bytes x (15 + 15 + 9) packs x 40 DIF sequences = 6240 bytes/frame
1080/50i system: 4 bytes x (15 + 15 + 9) packs x 48 DIF sequences = 7488 bytes/frame
720/60p system: 4 bytes x (15 + 15 + 9) packs x 40 DIF sequences = 6240 bytes/2frames

In the case of a VAUX DIF block that uses the 45-byte or 75-byte VAUX pack structure:

1080/60i system:	(72 x 2+ 42) bytes x 40 DIF sequences = 7440 bytes/frame
1080/50i system:	(72 x 2 + 42) bytes x 48 DIF sequences = 8928 bytes/frame
720/60p system:	(72 x 2+ 42) bytes x 40 DIF sequences = 7440 bytes/2frames

4 VAUX DIF block space structure and payload format (VAUX packs)

The format of the VAUX DIF block space available for data mapping is shown in figure 2. Each DIF sequence of a DIF frame contains 3 VAUX DIF blocks, but depending on if the VAUX DIF block is located in the odd or even DIF sequence, the formatting of the data payload is slightly different for one of the three VAUX DIF blocks (see figure 2).

The differently formatted VAUX DIF block in a DIF sequence contains control information called VS (VAUX source pack) and VSC (VAUX source control pack) which contains essential information for identification of the DIF frame signal parameters. The control information is carried in the 5-byte long VAUX packs form and is defined SMPTE 370M.

The size of the available mapping space in 3 VAUX DIF blocks is identical for both DIF sequences, odd or even.

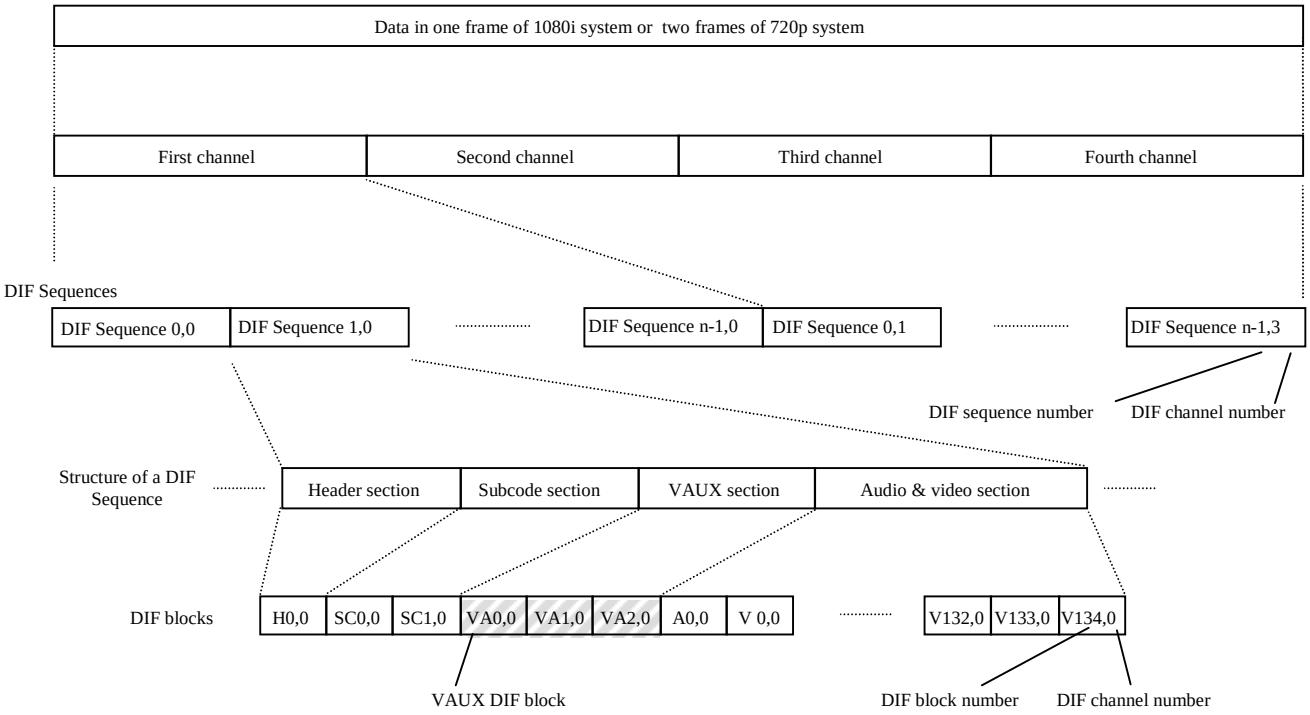


Figure 1 – Structure of a DIF frame for DV-based 100 Mb/s stream

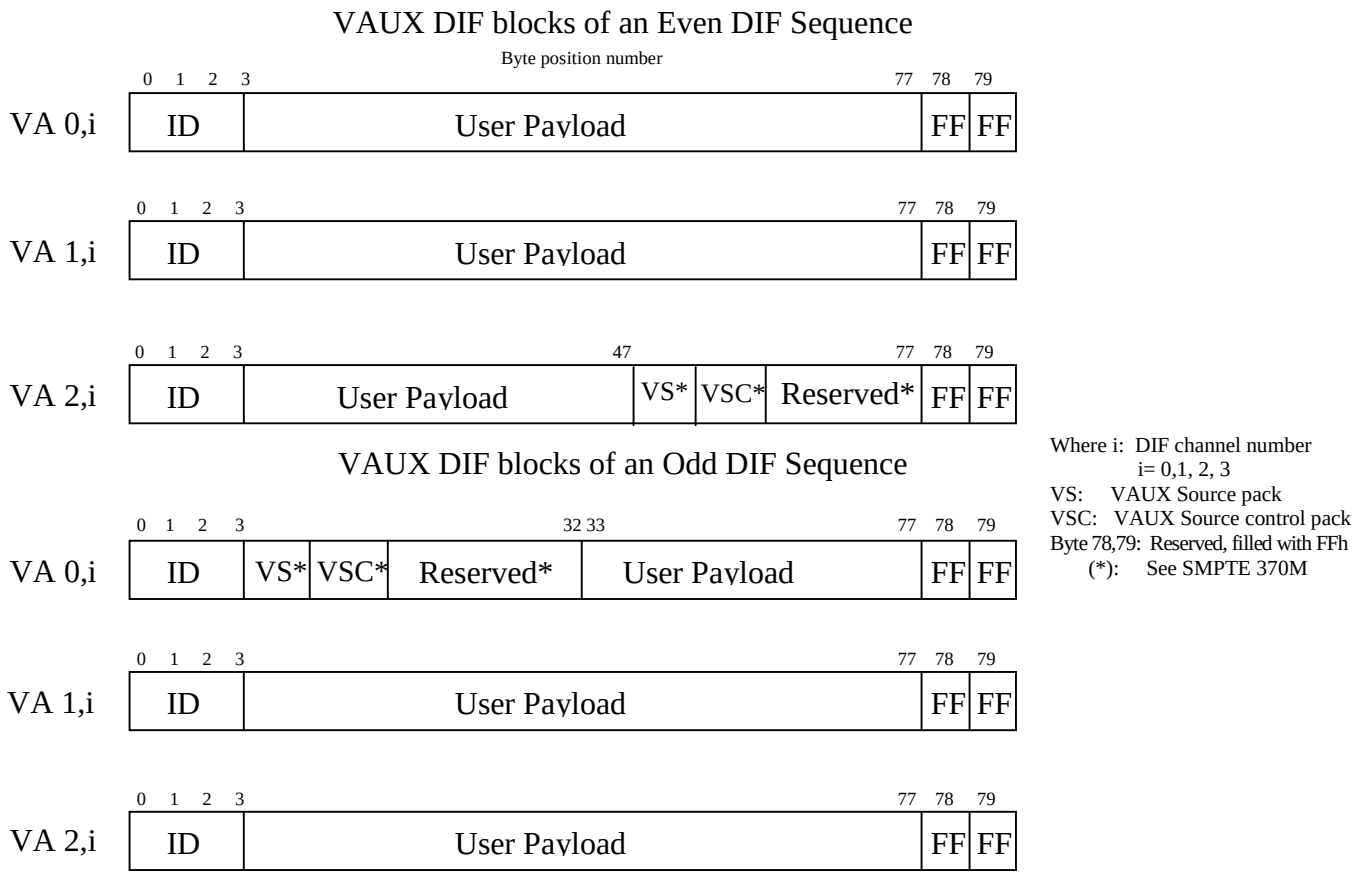


Figure 2 – Payload structure of VAUX DIF blocks of DV-based 100Mb/s DIF frame

For higher payload efficiency of the VAUX DIF block space, two additional VAUX pack structures are defined in this standard. In these two VAUX pack structures, (45-byte, 75-byte) the header of the VAUX pack is repeated only once per VAUX DIF block, therefore providing more space for data mapping.

The formats of all three of VAUX packs are shown in figure 3.

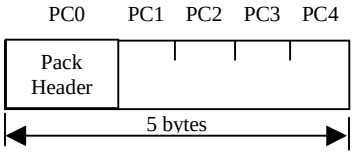


Figure 3a – 5-byte VAUX pack structure

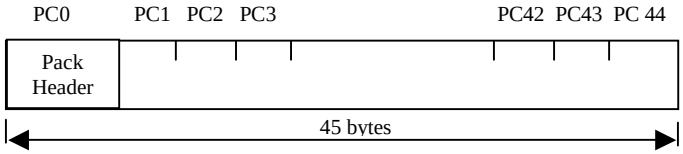


Figure 3b – 45-byte VAUX pack structure

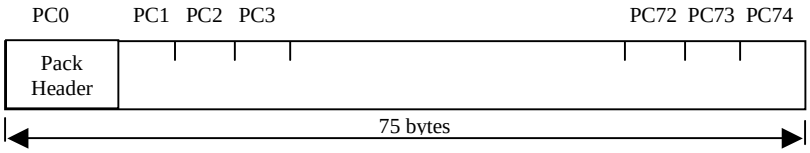


Figure 3c – 75-byte VAUX pack structure

4.1 VAUX packs structure definitions

4.1.1 5-byte long VAUX packs type 1 and type 2

The 5-byte long VAUX pack is defined in two basic structures, type 1 and type 2. Both types are 5-byte long VAUX packs, however they differ from each other by different VAUX pack header value and intended functionality. The 5-byte long VAUX packs type 1 or 2 can be used with any of the VAUX DIF blocks from any DIF sequence. For data mapping purpose, the type 1 VAUX pack is used as a “starter” VAUX pack indicating a start of a DANC packet, while the type 2 VAUX pack is used only as a DANC packet data carrier (see figure 4).

The mapping of a DANC string into the VAUX DIF blocks is based on mapping of individual DANC packets, so the start of all DANC packets is always marked by use of the VAUX pack type 1 (see figure 7).

4.1.1.1 Type 1 VAUX pack definitions (see table 1)

The VAUX pack header (PC0) of type 1 is set to E1h. The second byte (PC1) contains “Reserved” bits that are intended for future use. Their default value is set to 1. The subsequent bytes of the VAUX pack type 1 are used for mapping of the DANC string data B0; B1; B2.

Table 1 – VAUX pack type 1

	MSB							LSB
PC0	1	1	1	0	0	0	0	1
PC1	Res	Res	Res	Res	Res	Res	Res	Res
PC2	B0							
PC3	B1							
PC4	B2							

4.1.1.2 Type 2 VAUX pack definitions (see table 2)

The VAUX pack header (PC0) for type 2 is set to E2h. The subsequent bytes of the VAUX pack type 2 are used for mapping of the DANC string data B j, B j+1; B j+2; B j+3 and are in a same order as bytes of the DANC packet.

The unused bytes of the last VAUX pack type 2 containing mapped data of a DANC packet, shall be filed with FFh (see figure 4).

Table 2 – VAUX pack type 2

	MSB							LSB
PC0	1	1	1	0	0	0	1	0
PC1	B j							
PC2	B j+1							
PC3	B j+2							
PC4	B j+3							

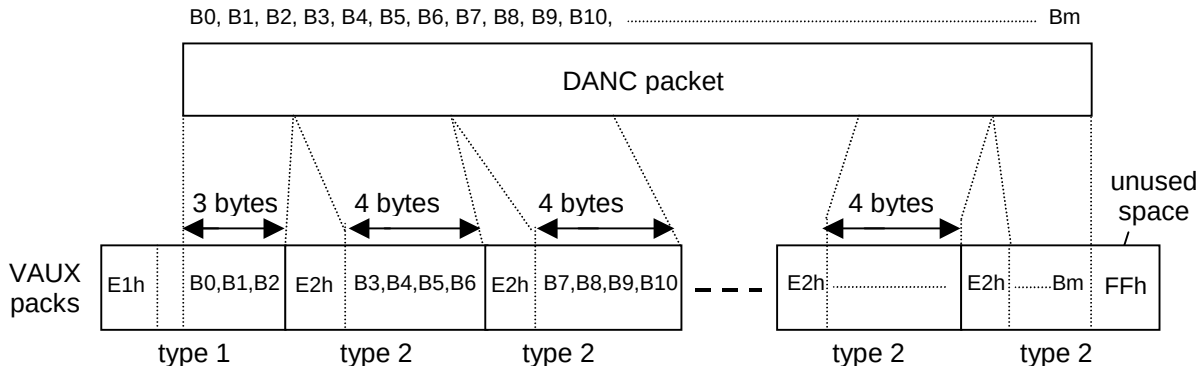


Figure 4 – Mapping a DANC packet into type 1 and type 2 VAUX packs

4.1.2 45-byte and 75-byte long VAUX packs type 3a and 3b

These VAUX packs are used for greater payload efficiency. Both packs use the same pack header, which is set to E3h. During the mapping process these packs are selected such that a chosen specific pack length depends on the payload size of the VAUX DIF block from either the odd or even DIF sequence.

4.1.2.1 Type 3a VAUX pack definition

This type of a VAUX pack is 45 bytes long. The type 3a VAUX pack is used with VAUX DIF block VA 2,i from the even DIF sequence and VAUX DIF block VA 0,i from the odd DIF sequence (see figure 2).

The VAUX pack header (PC0) for type 3a is set to E3h. The second byte (PC1) contains “Reserved” bits with the exception of the LSB bit. The LSB bit is called the END bit, and if this bit is set to 0, it indicates that the particular VAUX pack contains the last byte of the mapped DANC string (see figure 5). The third byte (PC2) of the VAUX pack type 3a contains only “Reserved” bits for future applications. The “Reserved” bits default value is set to 1. The remaining bytes PC3 thru PC44 shall contain the mapped data of a DANC string (see table 3a).

Table 3a – VAUX pack type 3a

	MSB							LSB
PC0	1	1	1	0	0	0	1	1
PC1	Res	Res	Res	Res	Res	Res	Res	END
PC2	Res	Res	Res	Res	Res	Res	Res	Res
PC3	B k							
PC4	B k+1							
PC5	B k+2							
:	:							
PC44	B k+41							

4.1.2.2 Type 3b VAUX pack definition

This type of a VAUX pack is 75 bytes long. The type 3b VAUX pack is used with VAUX DIF blocks VA 0,i; VA 1,i from the even DIF sequence and VAUX DIF blocks VA 1,i; VA 2,i from the odd DIF sequence (see figure 2).

The definition of the VAUX pack type 3b is the same as the definition of a VAUX pack type 3a (section 4.1.2.1) with the exception that the mapped data of the DANC string is loaded into bytes PC3 through PC74 due to its longer length (see table 3b). The unused space of the last VAUX pack type 3a or 3b shall be filled with FFh (see figure 5).

Table 3b – VAUX pack type 3b

	MSB							LSB
PC0	1	1	1	0	0	0	1	1
PC1	Res	Res	Res	Res	Res	Res	Res	END
PC2	Res	Res	Res	Res	Res	Res	Res	Res
PC3	B k							
PC4	B k+1							
PC5	B k+2							
:	:							
PC74	B k+71							

If END = 0 then the VAUX pack and the used VAUX DIF block contains the last byte of the DANC string

If END = 1 then the VAUX pack and the used VAUX DIF block does not contain the last byte of the DANC string

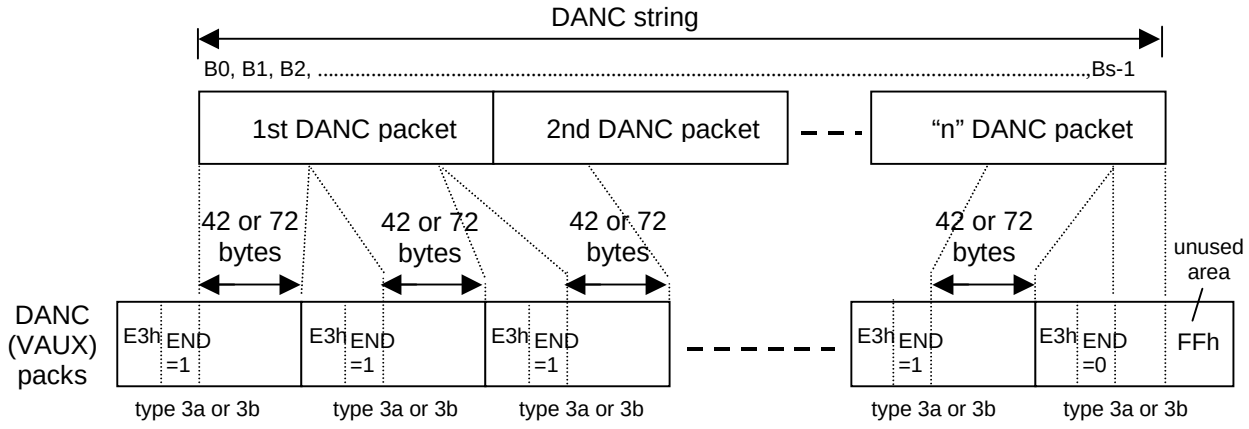


Figure 5 – Mapping of a DANC string into VAUX packs type 3a or 3b

5 Conversion and mapping process of VANC data packets

SMPTE 291M VANC data packets present on the 10-bit HD-SDI interface (SMPTE 292M) are converted into DIF ancillary data packets, DANC packets. Figure 6 shows the relationship between a VANC and a DANC packet.

A converted DANC packet is of identical length as the originating VANC packet (figure 6.) Of the DID, SDID/(DBN), DC, UDW, and CS, only the lower 8 bits of the 10-bit SMPTE 291M ancillary data packet words are processed. For definitions of ADF, DID, SDID, DBN, UDW, and CS of anaAncillary packet see SMPTE 291M.

During the conversion process, the three ADF data bytes are replaced by new information consisting of one LE bit (line enable flag), 11 LN bits (line number), FI bit (frame indication flag), YCF bit (YC flag) and “Res” bits. “Res” bits are reserved for future use and default value is set to 1. The LE bit defines validity of the present LN bits, and these LN bits indicate the HD-SDI line number on which the originating VANC packet resides at the start of the conversion process. The FI flag is used to identify either one of the two frames in the 720/60p system. The YCF flag is used to identify where the originating VANC ancillary packet was located on the Y signal or C signal in the VBI. The ADF bytes are discarded during this process.

All of the VANC packets present in the VBI of the HD-SDI interface are converted into the DANC packets and these are assembled to form a string of DANC packets of total length S bytes. This string of DANC packets is then mapped into multiple VAUX DIF blocks shown in figure 2.

The LN bits, the FI bit and the YCF bit are used to identify the location of the originating VANC packet on the HD-SDI interface and are used during a reverse mapping process. During that process, the DANC packets are converted back into VANC packets and relocated back into the VBI space of the HD-SDI interface. Use of the LN bits and FI flag bit assures that a temporal skew of the VANC packets (based on field/frame location) is not possible.

When the data from a DANC packet are converted back to a VANC packet, the upper 2 bits are generated from the lower 8 bits.

This conversion process is applied only to VANC data located in a single frame of the relevant high-definition television signal and the available space for the VANC packets is indicated in 3.1.

SMPTE 291M ancillary data packet (VANC packet)

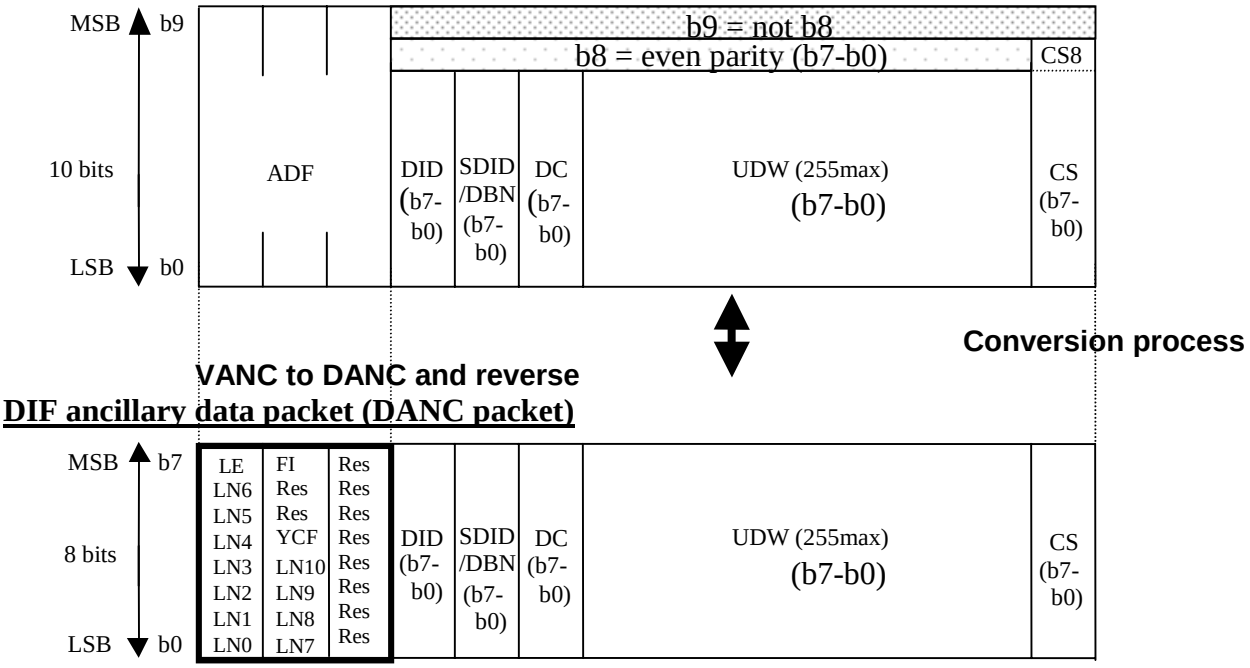


Figure 6 - SMPTE 291M ancillary data packet (VANC) & DIF ancillary data packet (DANC)

LE: Line number enable flag (see note 2)
LE = 0 then LN bits are invalid
LE = 1 then LN bits are valid

NOTE 2 – In the case of originally generated information to be placed in a DANC packet (e.g., ancillary time code or UMID), LE may be set to 0 or 1, depending if any specific line is preferred for the mapped data location on the interface

LN: Line number – a line number identifying where the originating VANC ancillary packet was located in the VBI. This number is equal to the binary code of the line number provided by the HD-SDI interface defined in SMPTE 292M

1080/60i and 1080/50i system	LN0 -- LN10 = 1, ⋯ , 1125
720/60p system	LN0 -- LN10 = 1, ⋯ , 750

FI: Frame indication flag – identification of the two frames present in the 720/60p system

1080/60i and 1080/50i system	FI = 1
720/60p system	FI = 1: video frame 1 (refer to SMPTE 370M)
	FI = 0: video frame 2

YCF: YC flag – identifies where the originating VANC ancillary packet was located on the HD-SDI interface in the VBI (Y or C signal channel space) YCF = 1: Y signal
YCF = 0: C signal

Res: Reserved bit for future use, default value set to 1.

The total size of the VANC packets in a single frame that are converted into a DANC packet string cannot exceed the available space defined in clause 3 and 3.1 (see note 1).

6 Mapping DANC packets into VAUX DIF blocks

The VANC packets converted into relevant DANC packets are mapped into the VAUX DIF blocks payload. This mapping depends on the structure of the VAUX pack. When the type 1 or type 2 VAUX packs are used, the DANC packets are mapped on an individual basis. When the type 3a or 3b VAUX packs are used, the mapping process maps a DANC packet string that consists of all DANC packets assembled together and left justified.

6.1 Mapping DANC packets using VAUX packs type 1 and type 2.

When the VAUX pack type 1 and 2 are used for mapping, each DANC packet is mapped separately. These VAUX packs containing data of a DANC packet from B0 to Bm are contiguous and left justified as shown in figure 7. It is permissible to overflow data contained in a DANC packet into the next VAUX DIF block. When multiple DANC packets are mapped, each DANC packet is mapped independently of other DANC packets.

The last type 2 VAUX pack of the mapped DANC packet in a VAUX DIF block shall be followed either by a VAUX pack type 1, signifying a start of the next mapped DANC packet, or all of the unused bytes of the VAUX DIF block are filled with FFh.

An example of multiple DANC packets mapping within different VAUX DIF blocks is shown in figure 7. Regarding mapping of different types of data see note 3. The structure and sequence of all VAUX DIF blocks in a DIF frame is shown in table 4.

NOTE 3 – In the case that VAUX packs type 1 and 2 are jointly mapped with other data, the other data types shall be placed in different VAUX DIF blocks than the VAUX DIF blocks occupied by VAUX packs type 1 and 2. The identification of the data type is achieved by use of a different VAUX pack header value located in byte position 3 or 33 of the particular VAUX DIF block. Designers should be aware that other applications may map data into the VAUX packs with pack header values other than those defined in this standard. Applications that do not recognize a VAUX pack header value should ignore this VAUX pack. In case that byte position 3 or 33 of the VAUX DIF block is occupied by an already mapped DANC packet, an additional DANC packet may be placed after the last VAUX pack of the previous DANC packet, if there is available space.

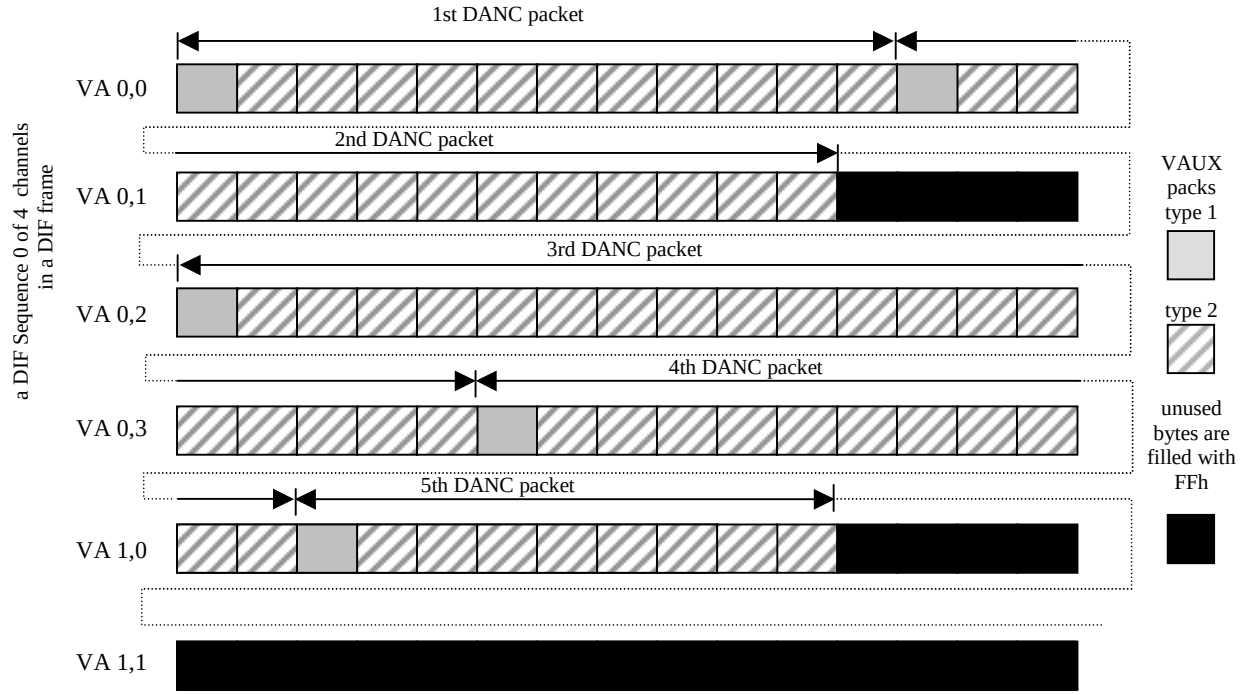


Figure 7 – Example of mapping DANC packets using VAUX packets type 1 and 2 into VAUX DIF blocks

6.2 Mapping DANC packet string using VAUX packs type 3a and 3b

Maximum mapping space is available when the mapping process uses VAUX packs type 3a and 3b.(see 4.1.2). This type of mapping uses combination of 45-byte and 75-byte long VAUX packs, so minimum space in the VAUX DIF blocks is dedicated to VAUX pack headers.

All of the DANC packets (essentially the VANC data) are assembled into a DANC string, where all DANC packets are contiguous and left justified. The DANC string contains data from byte B0 to byte B s-1. The type of VAUX packs (type 3a or 3b) are selected such that they fit the relevant VAUX DIF blocks that are used for mapping.

All of the VAUX packs have set their END bit = 1 with the exception of the last VAUX pack that contains the last byte of the DANC string B s-1. In this particular VAUX pack the END bit = 0 signifies that the end of the DANC string is located there, and there are no more VAUX packs type 3a or 3b following. The unused space of the last VAUX pack type 3a or 3b is filled with FFh. Figure 8 shows an example of such mapping using VAUX packs type 3a and 3b. In this particular example, the total byte "s" of the DANC packet string is 300. Regarding mapping different types of data see note 4.

The structure and sequence of all VAUX DIF blocks in a DIF frame is shown in table 4.

NOTE 4 – In the case that VAUX packs type 3a and 3b are jointly mapped with other data in VAUX DIF blocks, other data types shall be placed in different VAUX DIF blocks than the VAUX DIF blocks occupied by these 3a and 3b VAUX packs. The identification of the data type is achieved by use of a different VAUX pack header value located in byte position 3 or 33 of a particular VAUX DIF block.

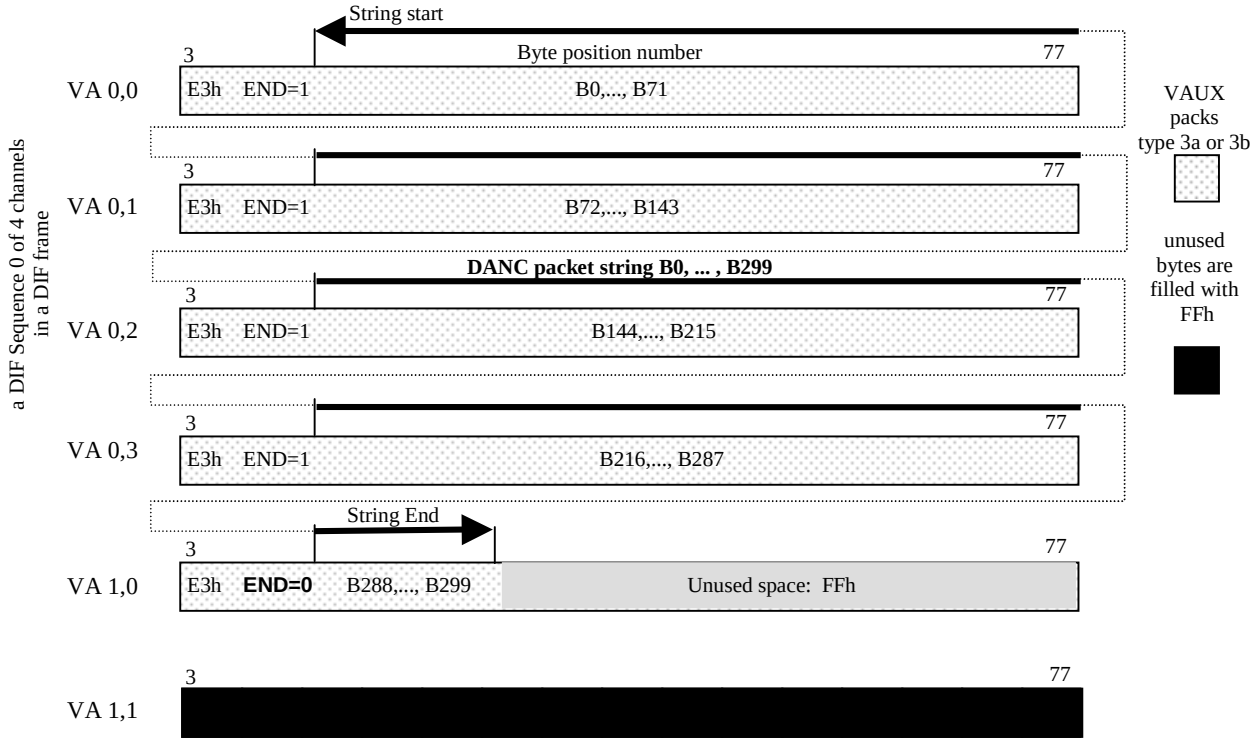


Figure - 8 An example of mapping DANC packets using VAUX packs type 3a and 3b into VAUX DIF blocks

6.3 Data retrieval from a mapped VAUX DIF space.

VANC packets recovered during the inverse DANC to VANC process shall be placed into the VBI space of an HD-SDI interface. The placement of VANC packets into the VBI space may be accomplished by the following means:

a) If LE is set to zero –
The placement of the VANC packets into the VBI ancillary space starts on the second line after the vertical switching point line as defined in SMPTE RP 168. The insertion of VANC packets continues to the last line of the VBI before the start of an active video line in a field. The placement of packets shall conform to SMPTE 291M rules requiring that ancillary packets are contiguous and left justified. A single video line in VBI space can carry multiple VANC packets as long as space is available.

Note: In this case the recovered VANC data packets are not located at the same place on the interface where they were originally located.

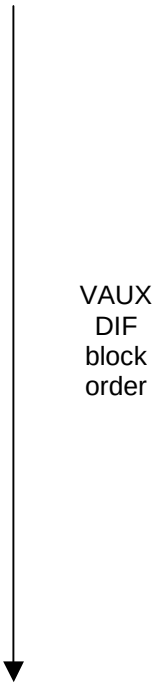
b) If LE is set to one –
The placement of the packets into the VBI ancillary space shall be determined by the Line Number LN and the frame indication FI indicted in the header of the DANC packet. Recovered VANC data packets are located on the same horizontal line on the interface where they were originally found. The packets shall be carried in the Y stream within the SMPTE 292M signal. The placement of packets shall conform to SMPTE 291M rules requiring that ancillary packets are contiguous and left justified.

7 Mapping in a DIF frame

Multiple VAUX DIF blocks are distributed throughout the DIF frame. The organization of the VAUX DIF block space is shown in table 4 and shows how the VAUX DIF blocks are interleaved on basis of different DIF channels in a frame (see figure 1 or SMPTE 370M). The different VAUX packs (type 1, 2, 3a and 3b) are used for mapping of DANC packet data. The data of all DANC (VANC) packets of a single frame are mapped into a single DIF frame and overflow of DANC (VANC) data from frame to frame is not possible.

Table 4 – VAUX DIF block order of a DV-based 100 Mb/s DIF frame

DIF sequence number	DIF block
0	VA 0,0
	VA 0,1
	VA 0,2
	VA 0,3
	VA 1,0
	VA 1,1
	VA 1,2
	VA 1,3
	VA 2,0
	VA 2,1
	VA 2,2
	VA 2,3
:	:
9	:
	VA 2,2
	VA 2,3
(10)	:
	(VA 2,2)
	(VA 2,3)
(11)	:
	(VA 2,2)
	(VA 2,3)



NOTE – Data from the VAUX DIF blocks are interleaved between four DIF channels that form a DIF frame. Values shown in parenthesis are only for a 50-Hz system

Annex A (informative)
Abbreviations

ANC:	Ancillary data packet located in ancillary space.
Bm:	A byte name (B) and a byte number (m) of a DANC packet.
DANC packet:	A VANC packet converted into DANC space of a same length as the originating VANC packet.
DANC packet string:	A string of DANC packets that are contiguous and left justified.
DIF:	Digital interface format.
DIF sequence:	A sequence of 150 DIF blocks that form a DIF sequence. Several DIF sequences form a compressed DIF stream frame.
END:	END flag.
FI:	Frame indication flag.
HD-SDI:	High-definition serial digital interface.
LE:	Line number enable flag.
LN:	Line number.
Res:	Reserved bit for future use.
S:	Size of a DANC/ (VANC) packet string.
VA :	A VAUX DIF block.
VANC:	A vertical ancillary data packet located in the vertical blanking interval of the HD-SDI interface.
VAUX DIF block:	A DIF block carrying VAUX data.
VAUX pack:	A pack that subdivides the payload space of a DIF VAUX block. A VAUX pack may be 5-byte, 45-byte, or 75-byte long.
VBI:	Vertical blanking interval where VANC packets are located.
VS:	VAUX source pack.
VSC :	VAUX source control pack.

Annex B (informative)
Bits from SDI VANC

This standard only maps the eight least significant bits from the SDI VANC data words, bits b7 through b0, into the DIF blocks of the DV-based stream. For the reverse process, conversion of DIF blocks into VANC packets, the two most significant bits b8 and b9 are derived. Bit b8 is calculated as the even parity of bits b7 through b0 and bit b9 is the inverse of bit b8. This reverse conversion process is correct for the VANC DID, SDID, DBN and DC bytes. For most applications this will be correct for the UDW bytes because most applications use this same technique to avoid generating prohibited byte values. Bit b8 of the CS byte can be calculated to create a valid checksum value.

NOTE – Designers should be aware of the above limitation and should take precautions to avoid using this technique for mapping VANC packets that do not use this technique, into DIF blocks.

Annex C (nformative)
Structure of the mapping process

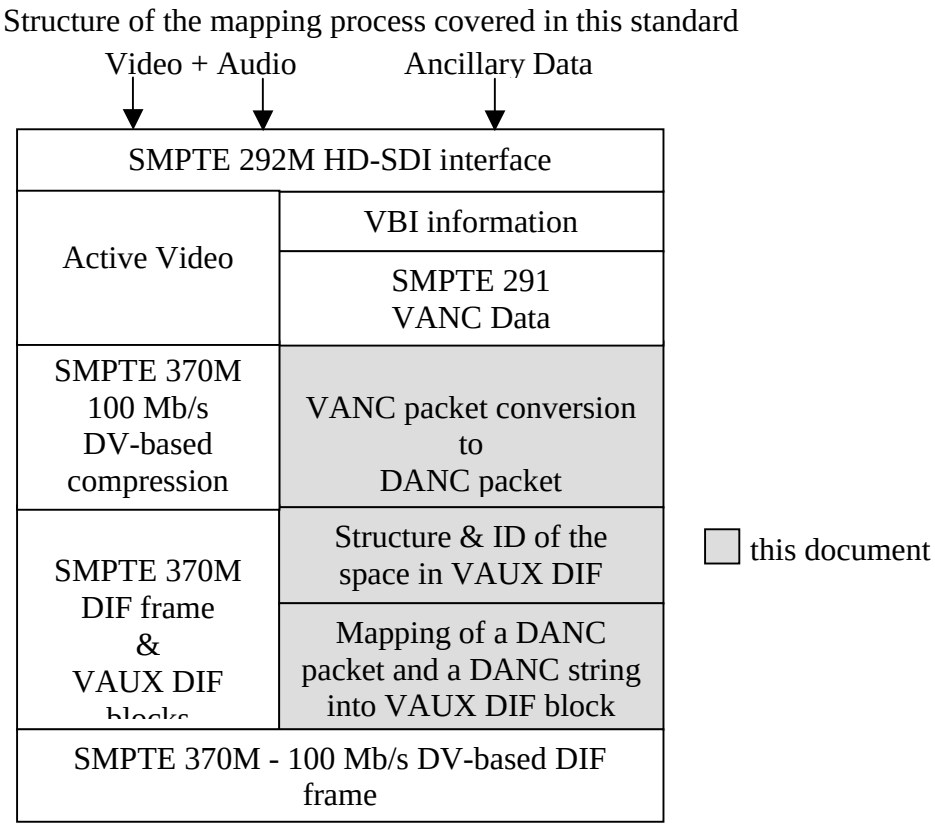


Figure C.1 – Structure of the mapping process