PROPOSED SMPTE STANDARD

SMPTE 399M

for Digital Television Recording — 1/2-in Type D-15 High-Definition Compressed Video Data Format

Table of contents

1 Scope

This standard specifies the content, format, and recording method of the data blocks containing compressed video data, AES3 audio data, and associated data which form the helical records on 12.65-mm (0.5-in) tape. In addition, this standard specifies the content, format, and recording method of the longitudinal record containing tracking information for the scanning head associated with the helical records, and also the longitudinal cue audio, and time and control code.

One video channel of high definition compressed video data and eight independent AES3 audio data channels are recorded in the digital format. Each of these channels is designed to be capable of independent editing.

The HD video compressed data are derived from the following HD video signals:

– 1080 line / 59.94 Hz field frequency interlace system (1080/59.94i)
– 720 line / 59.94 Hz frame frequency progressive system (720/59.94p)
– 1080 line / 50 Hz field frequency interlace system (1080/50i)
– 1080 line / 25 Hz frame frequency progressive system (1080/25p)
– 1080 line / 24 Hz frame frequency progressive system (1080/24p)
– 1080 line / 23.98 Hz frame frequency progressive system (1080/23.98p)

Through out the text of this standard, the expression “AES3 audio data” may be abbreviated to “audio data” and represents digitized audio and data in AES-3 format. The tape format also supports a recording of AES-3 data payload streams with some limitation (see 6.3.3 d).

Figures 1 and 2 show block diagrams of typical recording and playback circuits. The compression part in the dotted line rectangle in figure 1 refers to SMPTE 342M.

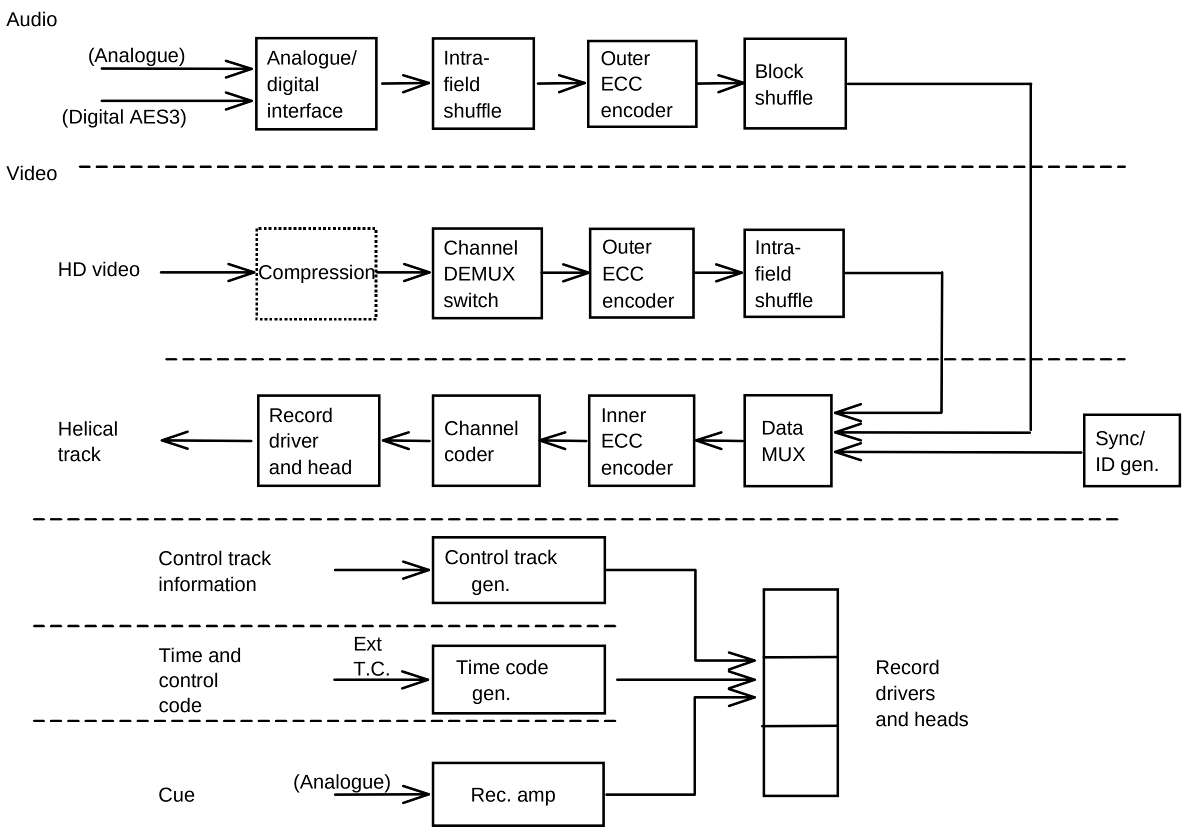


Figure 1 – Record block diagram

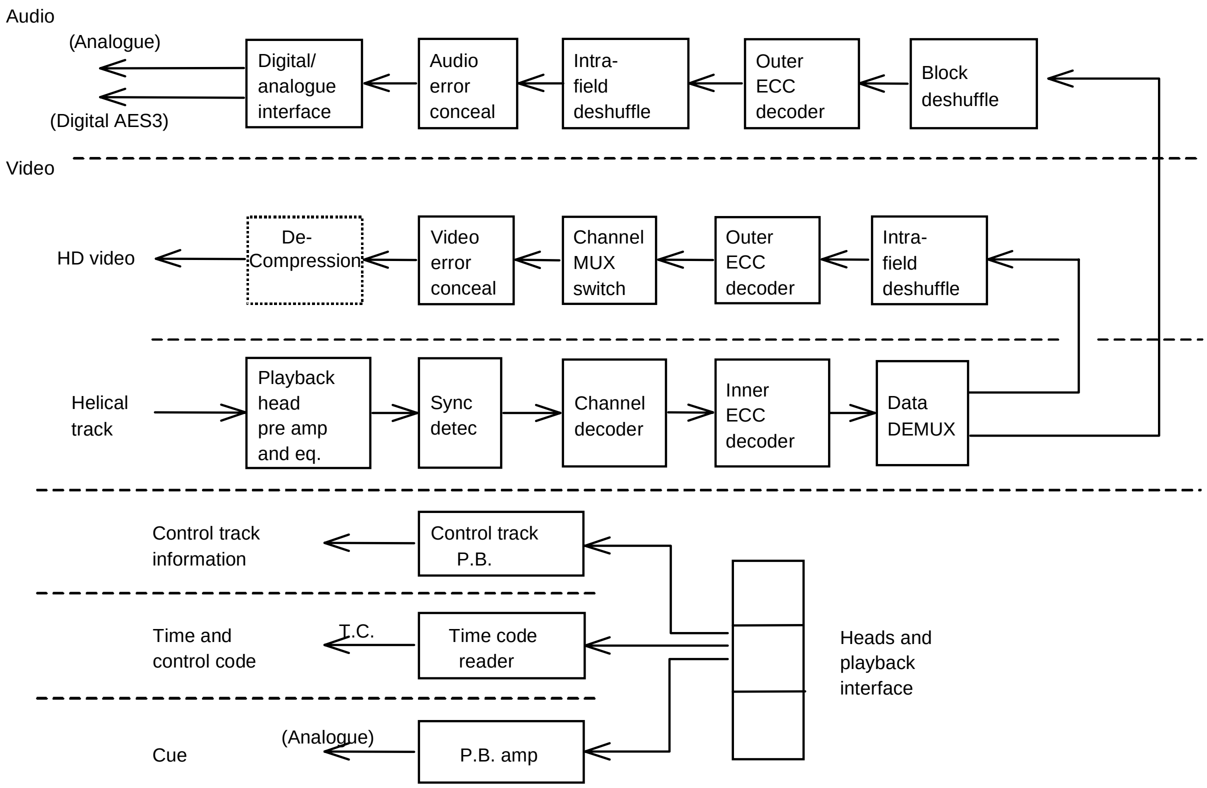


Figure 2 – Playback block diagram (including decompression)

2 Normative references

The following standards contain provisions, which through reference in this text constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this Standard are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

ANSI/SMPTE 299M-1997 24-Bit Digital Audio Format of HDTV Bit-Serial Interface

SMPTE 12M-1999, Television, Audio and Film — Time and Control Code

SMPTE 342M-2003, Television — HD-D5 Compressed Video 1080i and 720p Systems — Encoding Process and Data Format

SMPTE RP 155-1997, Audio levels for Digital Audio Records on Digital Television Tape Recorders

AES3-1992 (R1997), Serial Transmission Format for two Channel Linearly Represented Digital Audio Data

3 Environment and test conditions

3.1 Environment

Tests and measurements made on the system to check the requirements of this standard shall be carried out under the following conditions:

- Temperature 20 °C ± 1 °C
- Relative humidity (50 ± 2) %
- Barometric pressure from 86 kPa to 106 kPa
- Tape conditioning not less than 24 h
- Center tape tension 0.31 N ± 0.05 N (see annex A)

4 Magnetic tape

4.1 Base

The base material shall be polyester or equivalent.

4.2 Width

The tape width shall be 12.650 mm ± 0.008 mm. The tape, covered with glass, is measured without tension at a minimum of five different positions along the tape using a calibrated comparator having an accuracy of 0.001 mm (1 µm). The tape width is defined as the average of the five readings.

4.3 Width fluctuation

Tape width fluctuation shall not exceed 5 µm peak to peak. Measurement of tape width fluctuation shall be taken over a tape length of 900 mm. The value of tape width fluctuation shall be evaluated by measuring the tape width at 10 points, each separated by a distance of 100 mm.

4.4 Tape thickness

Two types of tape thickness shall be permitted by this standard. The first tape thickness shall be 10.2 µm to 11.0 µm (referred to as 11 µm); the second tape thickness shall be 13.0 µm to 14.0 µm (referred to as 14 µm).

4.5 Transmissivity

Transmissivity shall be less than 5%, measured over the range of wavelengths 800 nm to 900 nm.

4.6 Offset yield strength

The offset yield strength shall be greater than 9 N for 11-µm tape and 10 N for 14-µm tape. The force required to produce 0.2 % elongation of a 1000 mm test sample with a pull rate of a 10 mm per minute shall be used to confirm the offset yield strength. The line beginning at 0.2 % elongation parallel to the initial tangential slope is drawn and then read at the point of intersection of the line and the stress-strain curve.

4.7 Magnetic coating

The magnetic layer of the tape shall consist of a coating of metal particles or equivalent.

4.8 Coating coercivity

The coating coercivity shall be a class 1800 (144000 A/m) with an applied field of 400000 A/m (5000 Oe) as measured by a 50-Hz or 60-Hz B-H meter or vibrating sample magnetometer (VSM).

4.9 Particle orientation

The metal particles shall be longitudinally oriented.

5 Helical recordings

5.1 Tape speed

The tape speed shall be 167.228 mm/s for the 1080/59.94i and 720/59.94p systems, 139.496 mm/s for the 1080/50i and 1080/25p system, 133.782 mm/s for the 1080/24p and 1080/23.98p system respectively. The tolerance shall be ± 0.2 %.

5.2 Record location and dimensions

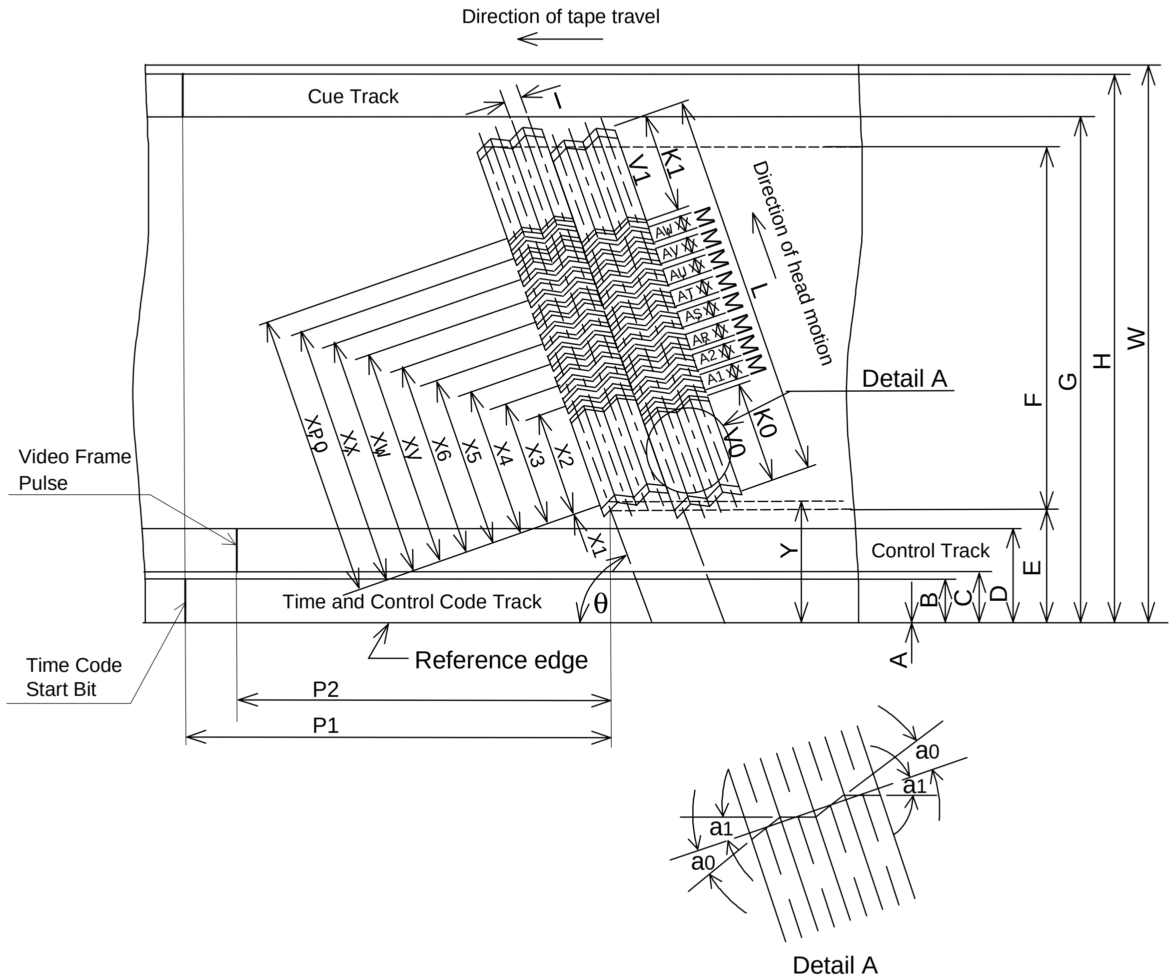
5.2.1 The format requires full track width erasure for continuous recording and flying erasure for insert editing.

5.2.2 Record location and dimensions for continuous recording shall be as specified in figures 3 and 4 and table 1. In recording, sector locations on each helical track shall be contained within the tolerances specified in figure 3 and table 1.

5.2.3 The reference edge of the tape for record location dimensions specified in this standard shall be the lower edge as shown in figure 3. The magnetic coating, with the direction of tape travel as shown in figure 3, is on the side facing the observer (measuring techniques are shown in annex B).

5.2.4 As indicated in figure 3, this standard anticipates a zero guard band between recorded tracks, and the record head width should be equivalent to the track pitch of 20 µm. The scanner head configuration should be chosen such that the recorded track widths are contained within the limits of 18 µm to 22 µm.

5.2.5 In insert editing, this standard provides a guard band of 2 µm (nominal) between the previously recorded track and the inserted track at editing points only. A typical track pattern for insert editing is shown in figure C.1 of annex C.



NOTES

1 A1 to A8 are audio data sectors.
2 V0 and V1 are compressed video data sectors.
3 Tape viewed from magnetic coating side.
4 Dimensions X1 to X10 are determined by the program reference point as defined in figure 4.

Figure 3 – Location and dimensions* of recorded tracks
(*See table 1)

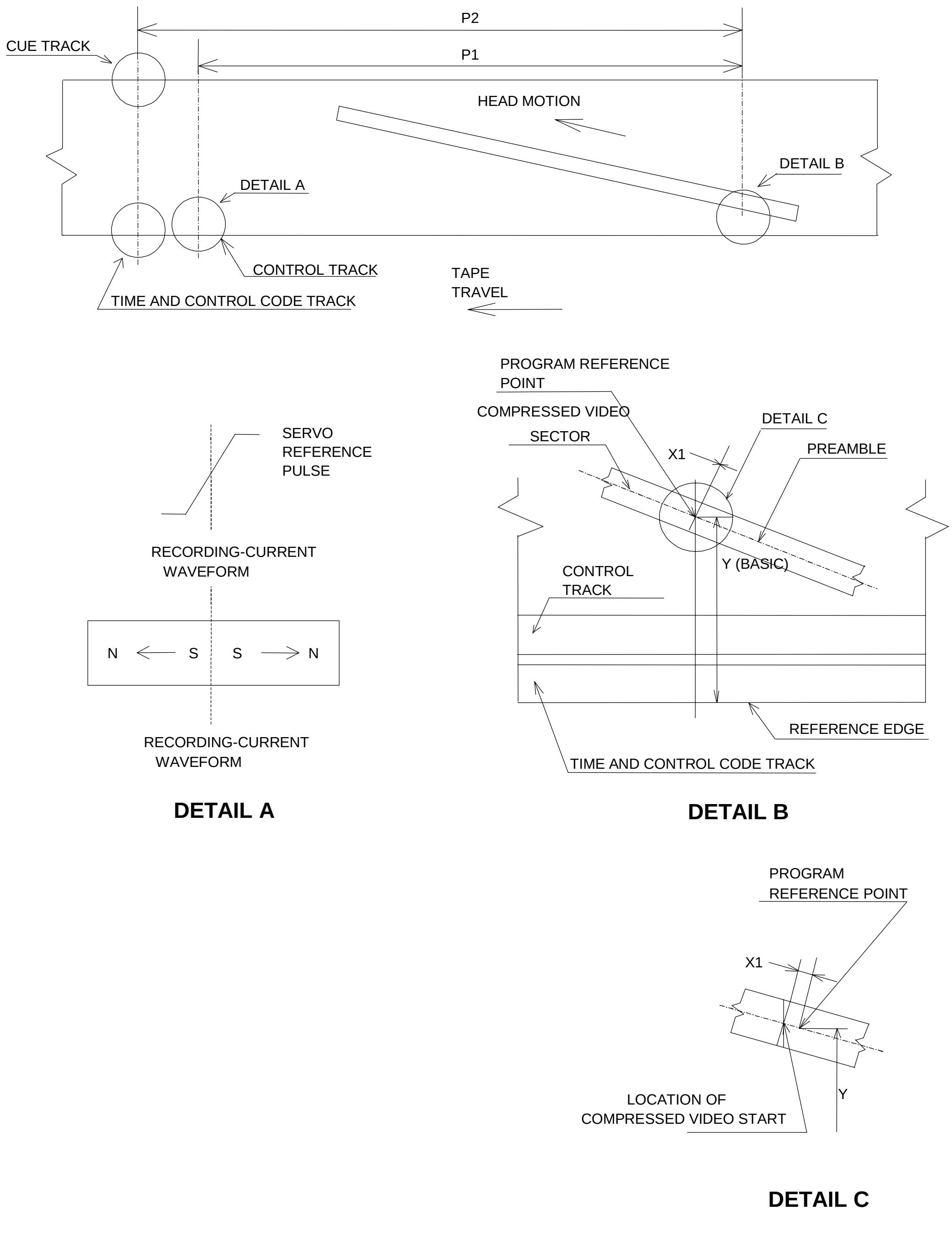


Figure 4 – Location of cue and time and control code track records

Table 1 – Record location and dimensions

	Dimensions	59.94i 50i 25p 23.98p	24p	Tolerance
A	Time and control code track lower edge	0	0	Basic
B	Time and control code track upper edge	0.450	0.450	± 0.050
C	Control track lower edge	0.900	0.900	± 0.050
D	Control track upper edge	1.300	1.300	± 0.050
E	Program area lower edge	1.629	1.624	Derived
F	Program area width	10.020	10.030	Derived
G	Cue audio track lower edge	11.950	11.950	± 0.050
H	Cue audio track upper edge	12.550	12.550	± 0.050
I	Helical track pitch	0.0200	0.0200	Ref
K0	Compressed video data sector 0 length	51.624	51.676	Derived
K1	Compressed video data sector 1 length	51.562	51.614	Derived
L	Helical track total length	116.397	116.514	Derived
M	Audio data sector length	1.273	1.275	Derived
P1	Control track reference pulse to program reference point (see figure 4)	180.556	180.614	± 0.050
P2	Cue/time and control code signal, start of code word, to program reference point (see figure 4)	183.407	183.465	± 0.100
X1	Location of start of compressed video data sector V0	0	0	± 0.050
X2	Location of start of audio data sector A1	51.898	51.950	± 0.050
X3	Location of start of audio data sector A2	53.507	53.561	± 0.050
X4	Location of start of audio data sector A3	55.117	55.172	± 0.050
X5	Location of start of audio data sector A4	56.726	56.783	± 0.050
X6	Location of start of audio data sector A5	58.335	58.394	± 0.050
X7	Location of start of audio data sector A6	59.944	60.005	± 0.050
X8	Location of start of audio data sector A7	61.554	61.616	± 0.050
X9	Location of start of audio data sector A8	63.163	63.227	± 0.050
X10	Location of start of compressed video data sector V1	64.772	64.837	± 0.050
Y	Program reference point	1.639	1.634	Basic
θ	Track angle	4.9384 °	4.9384 °	Basic
a0	Azimuth angle (track 0)	- 20.038 °	- 20.038 °	± 0.150 °
a1	Azimuth angle (track 1)	19.962 °	19.962 °	± 0.150 °

NOTES

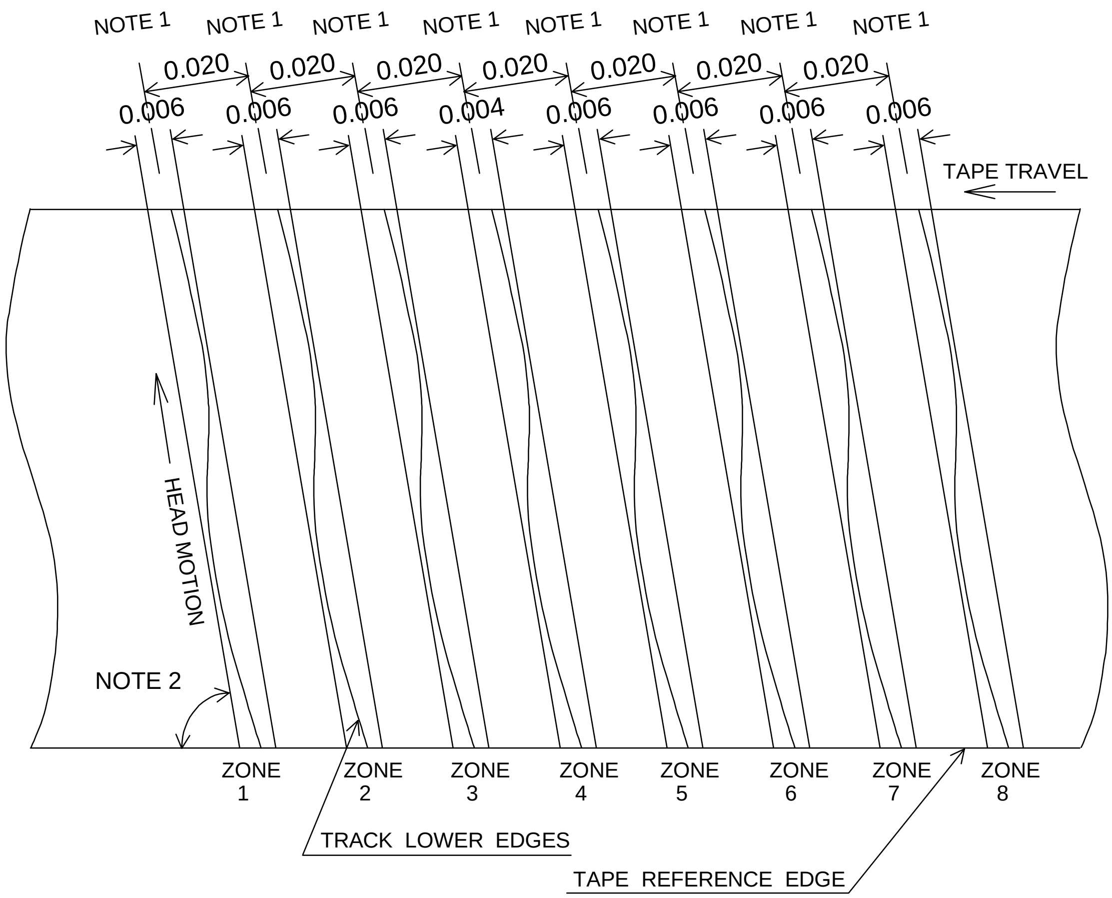
1 Measurements shall be made under the conditions specified in 3.1. The measurements shall be corrected to account for actual tape speed (see figures B.1 and B.2 of Annex B).

2 All dimensions in millimeters.

5.3 Helical track record tolerance zones

The lower edges of any eight consecutive tracks starting at the first track in each compressed video data frame shall be contained within the pattern of the eight tolerance zones established in figure 5. Each zone is defined by two parallel lines, which are inclined with respect to the tape reference edge at an angle of 4.9384° (basic).

The centerlines of all zones shall be spaced apart 0.0200 mm (basic). The width of zones 1 to 3 and 5 to 8 shall be 0.006 mm (basic). The width of zone 4 shall be 0.004 mm (basic). These zones are established to contain track angle errors, track straightness errors, and vertical head offset tolerance (measuring technique is shown in annex B).



NOTES

1 Tolerance zone centerlines.
2 4.9384°
3 All dimensions in millimeters.

Figure 5 – Location and dimensions of tolerance zones of helical track record

5.4 Relative positions of recorded information

5.4.1 Relative positions of longitudinal tracks

Audio data, compressed video data, control track, time and control code, and cue track with information intended to be time coincident shall be positioned as shown in figures 3 and 4.

5.4.2 Program area reference point

The program area reference point is determined by the intersection of a line parallel to the reference edge of the tape at a distance Y from the reference edge and the centerline of the first track in each compressed video data field (segment 0, track 0) (see figures 3 and 4 and 6.1). The end of the preamble and start of the compressed video data sector are located at the program area reference point, and the tolerance is dimension X1. The locations are shown in figures 3 and 4; dimensions X1 and Y are in table 1. The relationship between sectors and contents of each sector is specified in clause 6.

5.5 Gap azimuth

5.5.1 Cue track, control track, time code track

The azimuth angle of the cue, control track, and time and control code head gaps used to produce longitudinal track records shall be perpendicular to the track record.

5.5.2 Helical track

The azimuth of the head gaps used for the helical track shall be inclined at angles a_0 and a_1 as specified in table 1, with respect to a line perpendicular to the helical track. The azimuth of the first track of every field (segment 0, track 0) shall be oriented in the counterclockwise direction with respect to a line perpendicular to the helical track direction when viewed from the side of tape containing the magnetic record.

5.6 Transport and scanner (informative)

The effective drum diameter, tape tension, helix angle, and tape speed taken together determine the track angle. Different methods of design and/or variations in drum diameter and tape tension can produce equivalent recordings for interchange purposes.

One possible configuration of the transport uses a scanner with an effective diameter of 76.000 mm. Scanner rotation is in the same direction as tape motion during normal playback mode. Data is recorded by two groups of four heads mounted 180° apart. Figure 6 shows one possible mechanical configuration of the scanner, and table 2 shows the corresponding mechanical parameters. Figures 7 and 8 shows the relationship between the longitudinal heads and the scanner.

Other mechanical configurations are allowable provided the same footprint of recorded information is produced on tape.

Erase heads are illustrated in annex C.

6 Program track data

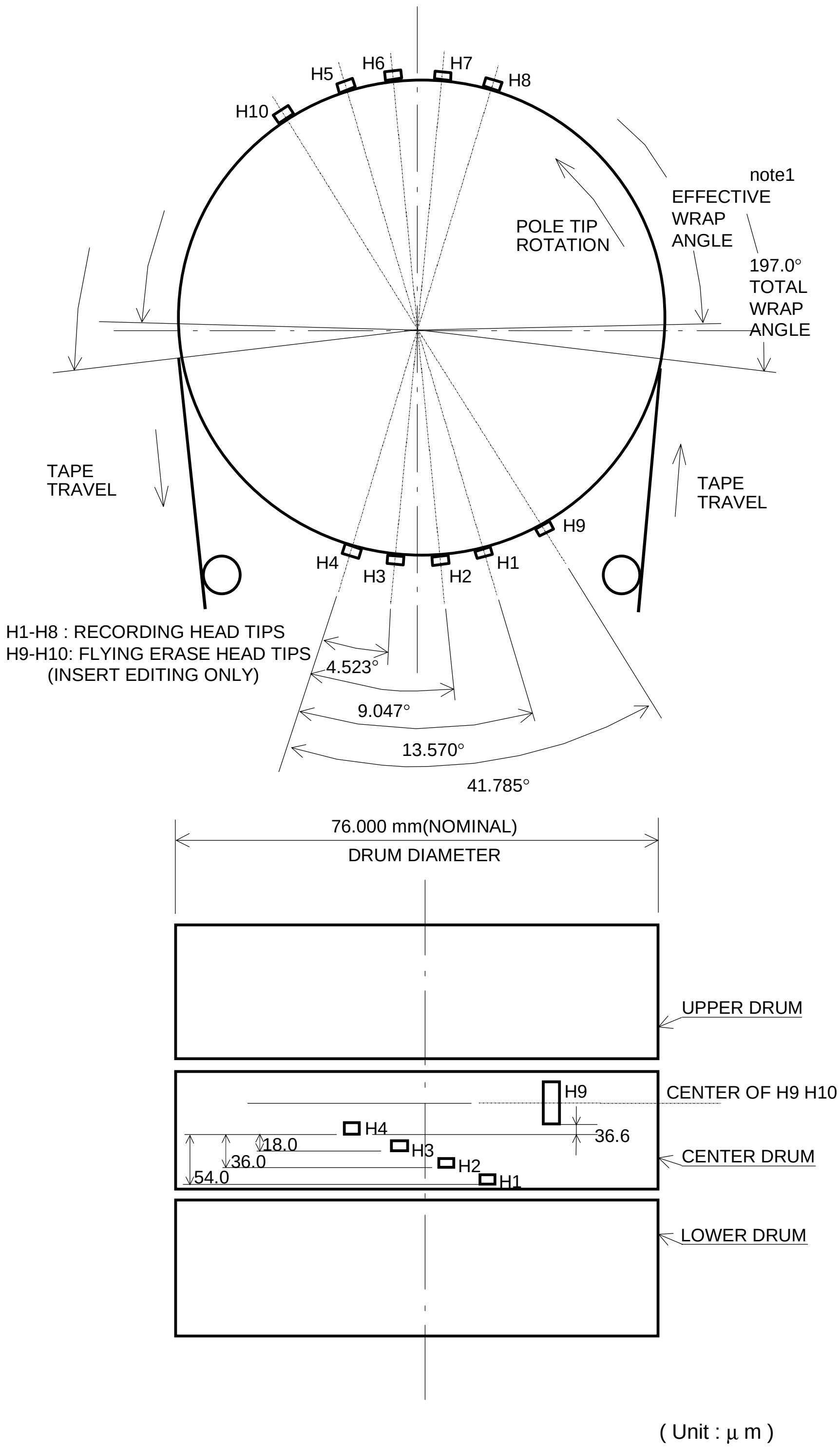
6.1 Introduction

Each television field is recorded on 12 tracks. This standard describes a recorder that processes data every "field". In the case of progressive scan compressed video data based on the 720/59.94p system, consecutive frames 1 and 2 are mapped into a space corresponding to fields 1 and 2 of an interlace system. In the case of a 1080/23.98p, 1080/24p and 1080/25p system a single frame is mapped into a space corresponding to both fields of an interlace system. (See figure 16). Therefore a recorded "field" of progressive compressed video conveys information contained in a whole frame of the progressive video source.

The helical tracks contain digital data from the compressed video channel compressed video data sector, recorded in that order. An edit gap between sectors accommodates timing errors during editing. Figure 9 shows the arrangement of the sectors on helical track. Figure 12 shows the arrangement of compressed video data and audio data sectors on the tape.

Each frame of time code shows a frame number that corresponds to each compressed video frame in an interlace system, and to a pair of two consecutive compressed video frames in progressive 720 system. Therefore the time codes of these equivalent periods of time in the interlaced 59.94i and progressive 59.94p systems are the same.

INFORMATIVE NOTE – SMPTE 12M does not provide for differentiation between the two identical time codes assigned to two consecutive frames in the 720 system.

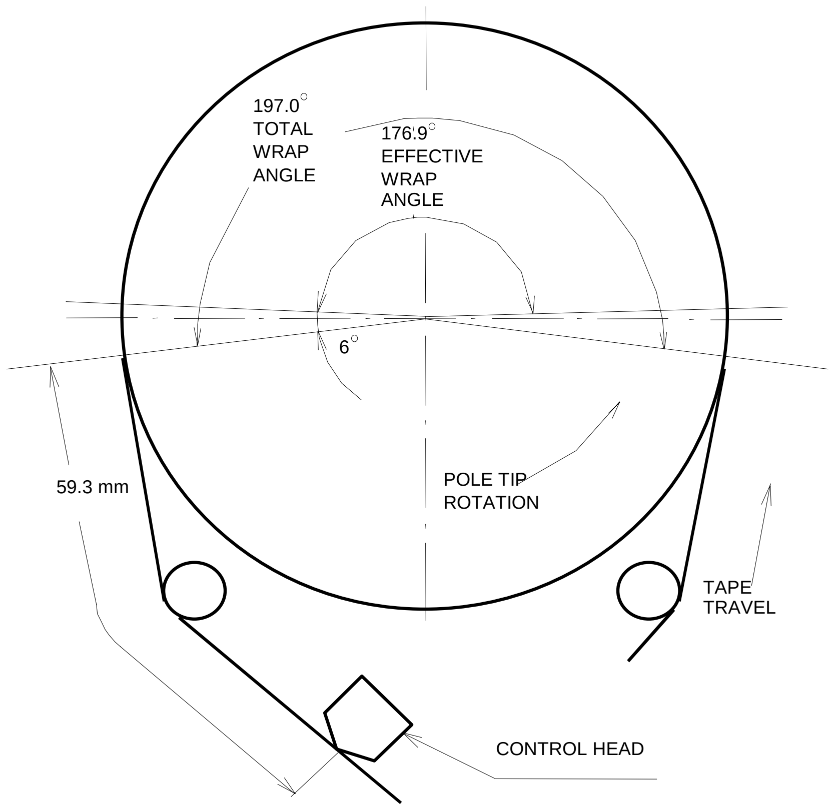


NOTE – 176.9° for 1080/59.94i, 720/59.94p, 1080/50i, 1080/25p and 1080/23.98p system;
177.1° for 1080/24p system

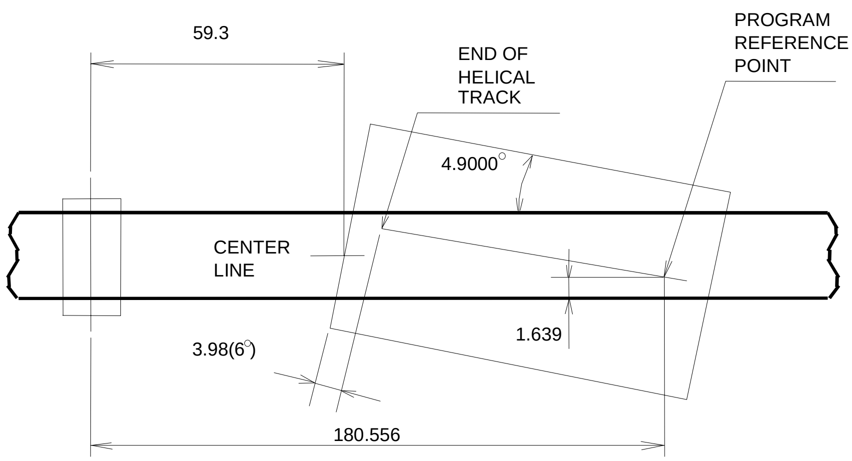
Figure 6 – Possible scanner configuration

Table 2 – Parameters for a possible scanner design

Parameters		1080/59.94i 720/59.94p system	1080/50i 1080/25p system	1080/24p system	1080/23.98p system
Scanner rotation speed (rps)		90/1.001	75	72	72/1.001
Number of tracks per rotation		8	8	8	8
Drum diameter (mm)		76.000	76.000	76.000	76.000
Centre span tension (N)		0.31	0.31	0.31	0.31
Helix angle (degrees)		4.9000	4.9000	4.9000	4.9000
Effective wrap angle (degrees)		176.9	176.9	177.1	176.9
Scanner circumferential speed (m/s)		21.5	17.9	17.2	17.2
H1,H5 over wrap head entrance (degrees)		14.1	14.1	14.0	14.1
H1,H5 over wrap head exit (degrees)		6	6	5.9	6
Angular relationship (degrees)	H1 - H4 :	13.570	13.570	13.570	13.570
	H2 - H4 :	9.047	9.047	9.047	9.047
	H3 - H4 :	4.523	4.523	4.523	4.523
	H5 - H8 :	13.570	13.570	13.570	13.570
	H6 - H8 :	9.047	9.047	9.047	9.047
	H7 - H8 :	4.523	4.523	4.523	4.523
	H4 - H8 :	180.000	180.000	180.000	180.000
Vertical displacement (mm)	H1 - H4 :	0.054	0.054	0.054	0.054
	H2 - H4 :	0.036	0.036	0.036	0.036
	H3 - H4 :	0.018	0.018	0.018	0.018
	H5 - H8 :	0.054	0.054	0.054	0.054
	H6 - H8 :	0.036	0.036	0.036	0.036
	H7 - H8 :	0.018	0.018	0.018	0.018
Maximum tip projection (µm) Note: Head projection from a drum surface		42.0	42.0	42.0	42.0
Record head track width (µm) Note: Track edit points are excepted		20	20	20	20

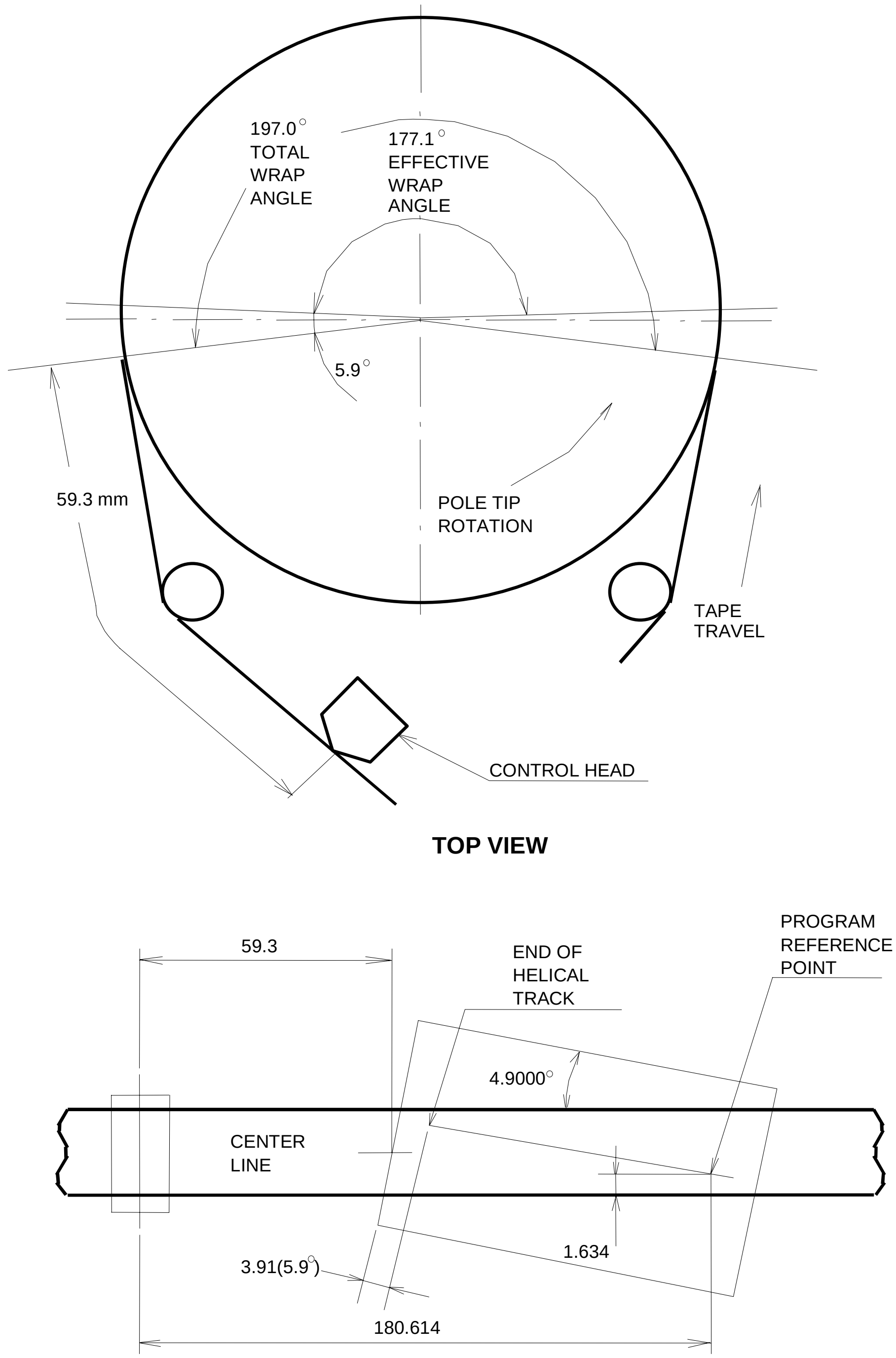


TOP VIEW



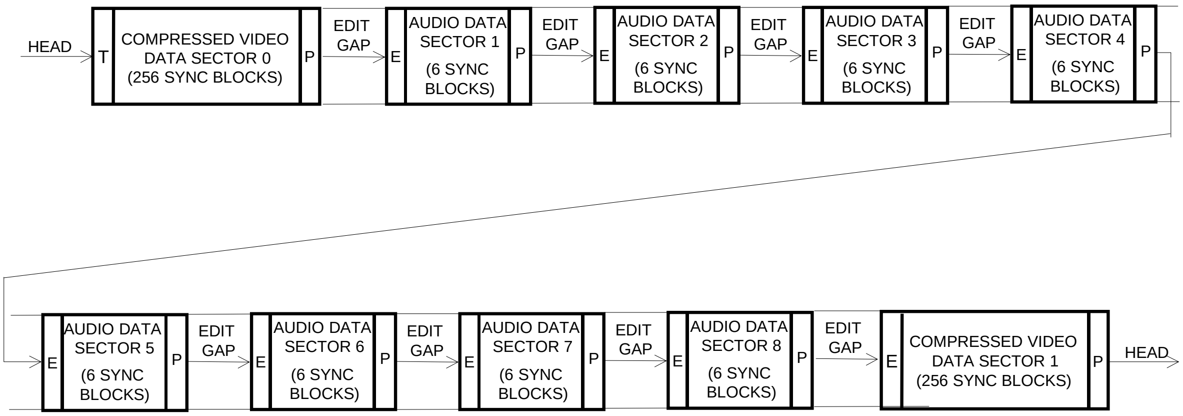
NOTE - Unwrapped, viewed magnetic coating side.

Figure 7 – Possible longitudinal head location and tape wrap (1080/59.94i, 720/59.94p, 1080/50i, 1080/25p and 1080/23.98p systems)



NOTE - Unwrapped, viewed magnetic coating side.

Figure 8 – Possible longitudinal head location and tape wrap (1080/24p system)



NOTES
1 T = Track preamble (58 bytes).
2 E = In-track preamble (28 bytes).
3 P = Postamble (4 bytes).
4 Sync block: 97 bytes.
5 Edit gap: 162 bytes nominal.

Figure 9 – Sector arrangement on helical track

6.2 Labeling convention

The least significant bit is written on the left and first is the recorded to tape.

The lowest numbered byte is shown at the left/top and is the first encountered in the input data stream.
Byte values are expressed in hexadecimal notation unless otherwise noted. An h subscript indicates a hexadecimal value.

6.3 Sector details

Each sector (audio data or compressed video data) is divided into the following elements:

– Preamble containing clock run-up sequence, sync pattern, identification pattern and fill pattern;

– Sync blocks containing sync pattern and identification pattern, followed by a fixed length data block with error control;

– Postamble containing sync pattern and identification pattern.

6.3.1 Sync block

The sync block format is common to both audio data and compressed video data sectors. Each sync block contains a sync pattern (2 bytes) and an inner code block. Each inner block contains an identification pattern (2 bytes) and 85 data bytes of compressed video data, audio data, or outer check bytes followed by 8 inner check bytes.

The inner code block contains the two bytes of the identification pattern together with 85 data bytes. Figure 10 shows the sync block format.

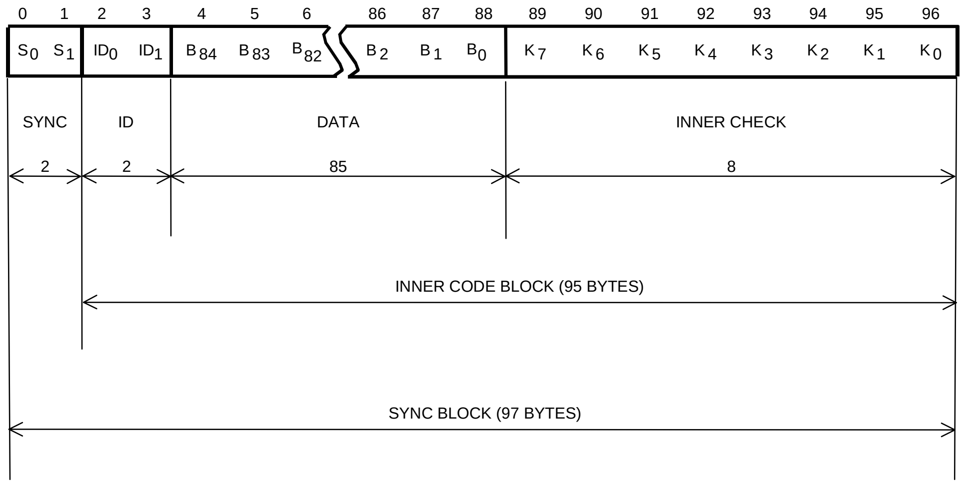


Figure 10 – Sync block format

6.3.2 Sync pattern

a) Length: 16 bits (2 bytes).

b) Pattern: 97F1 (in hexadecimal notation).

	LSB							MSB
Byte 0 -	1	1	1	0	1	0	0	1
Byte 1 -	1	0	0	0	1	1	1	1

c) Protection: None.

d) Randomization: None.

6.3.3 Identification Pattern

As illustrated in figure 11, the first two bytes of each inner block are used for identification of sync block, segment (group of helical tracks scanned simultaneously), helical track number, television field, and sector (portion of a track). While a progressive scan signal format contains only frames, each progressive frame is split into two fields as is indicated in figure 16.. Bits 1 to 6 of the second byte (byte 3 of sync block) of the identification pattern identify the track. Bit 7 of the second byte (byte 3) identifies a sector on the helical track (see figure 12).

a) Length: 16 bits (2 bytes).

b) Arrangement: The sync block number (byte 2 and the bit 0 of byte 3) follows a coded sequence along the track. Figure 13 shows the sequence of the sync block numbers.

The sector ID (bits 1-7 of byte 3) identifies a particular sector.

The segment number is modulo 3. For the 1080/59.94i and 720/59.94p system, the field number for compressed video data sectors is modulo 4 (VF_2 = 0 in byte 3). The field number for audio data sectors is modulo 4 (for AF_0 and AF_1 in byte 3) and AF_2 (in byte 3) is used for the identification of the five field sequences. For the 1080/50i, 1080/25p, 1080/24p and 1080/23.98p systems, the field number for compressed video data sectors is modulo 8 and the field number for audio data sectors is modulo 4 (AF_2 = 0).

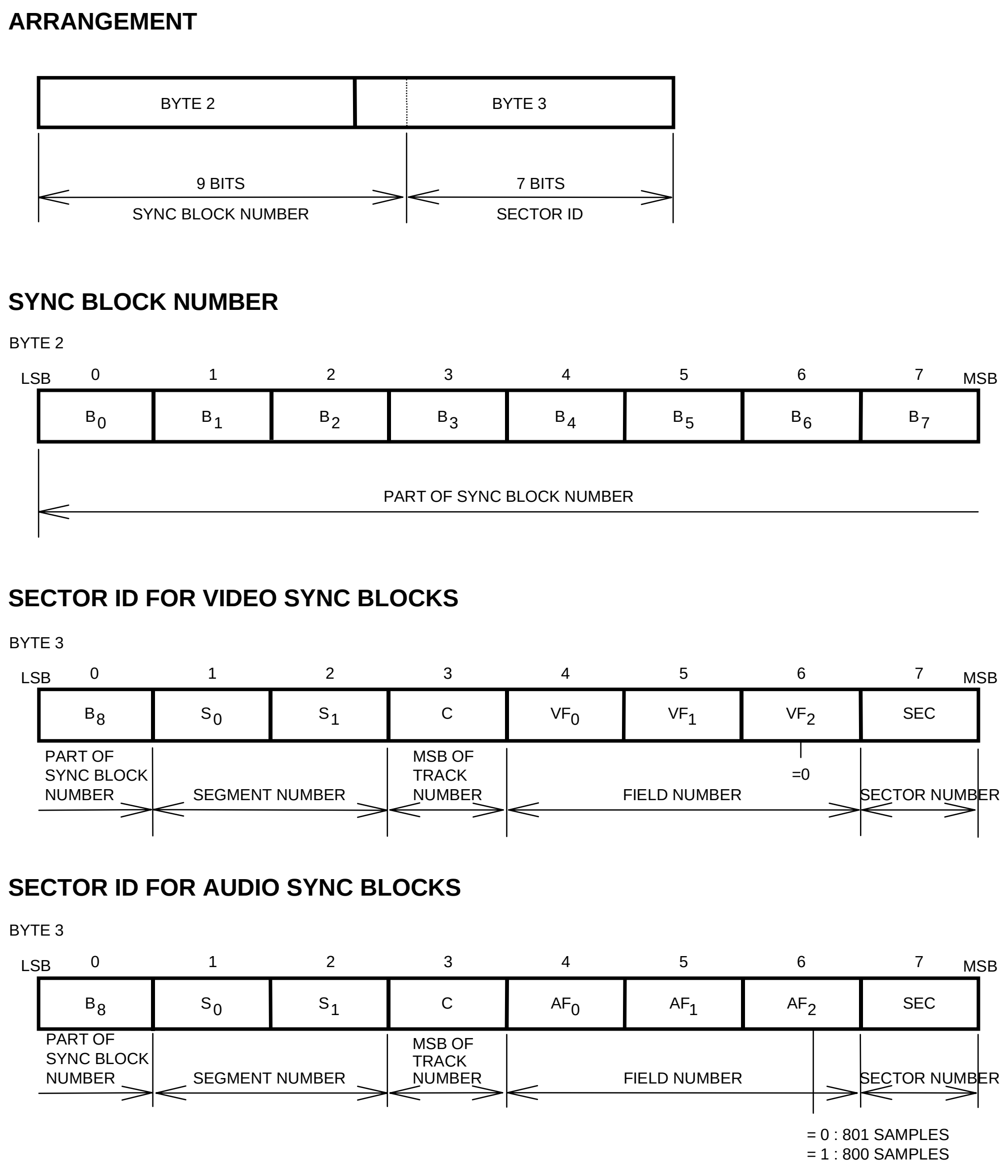
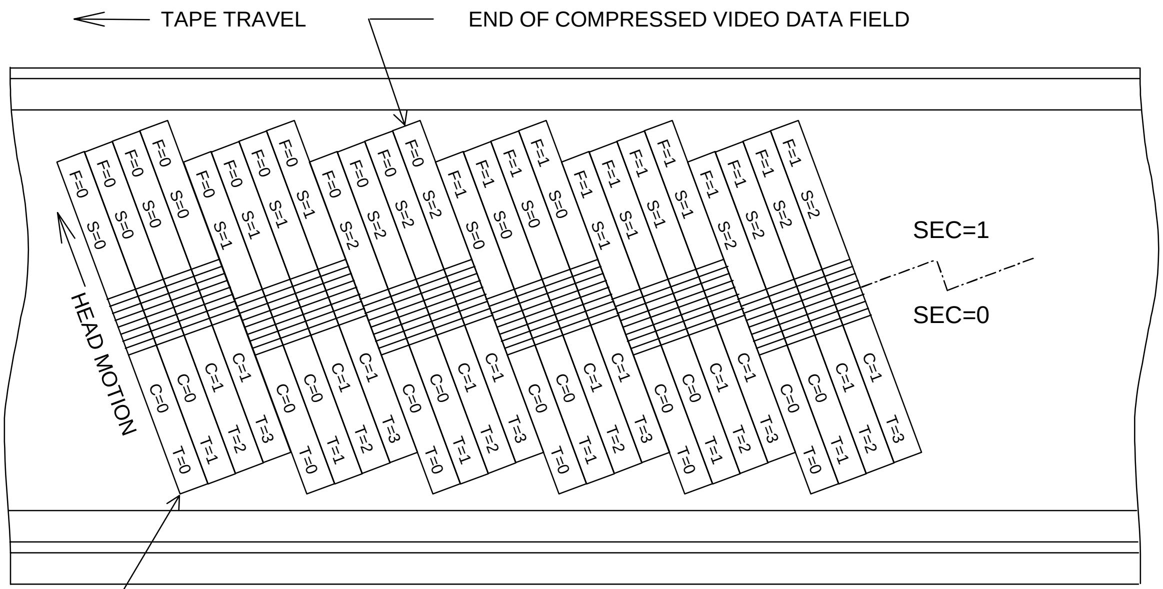


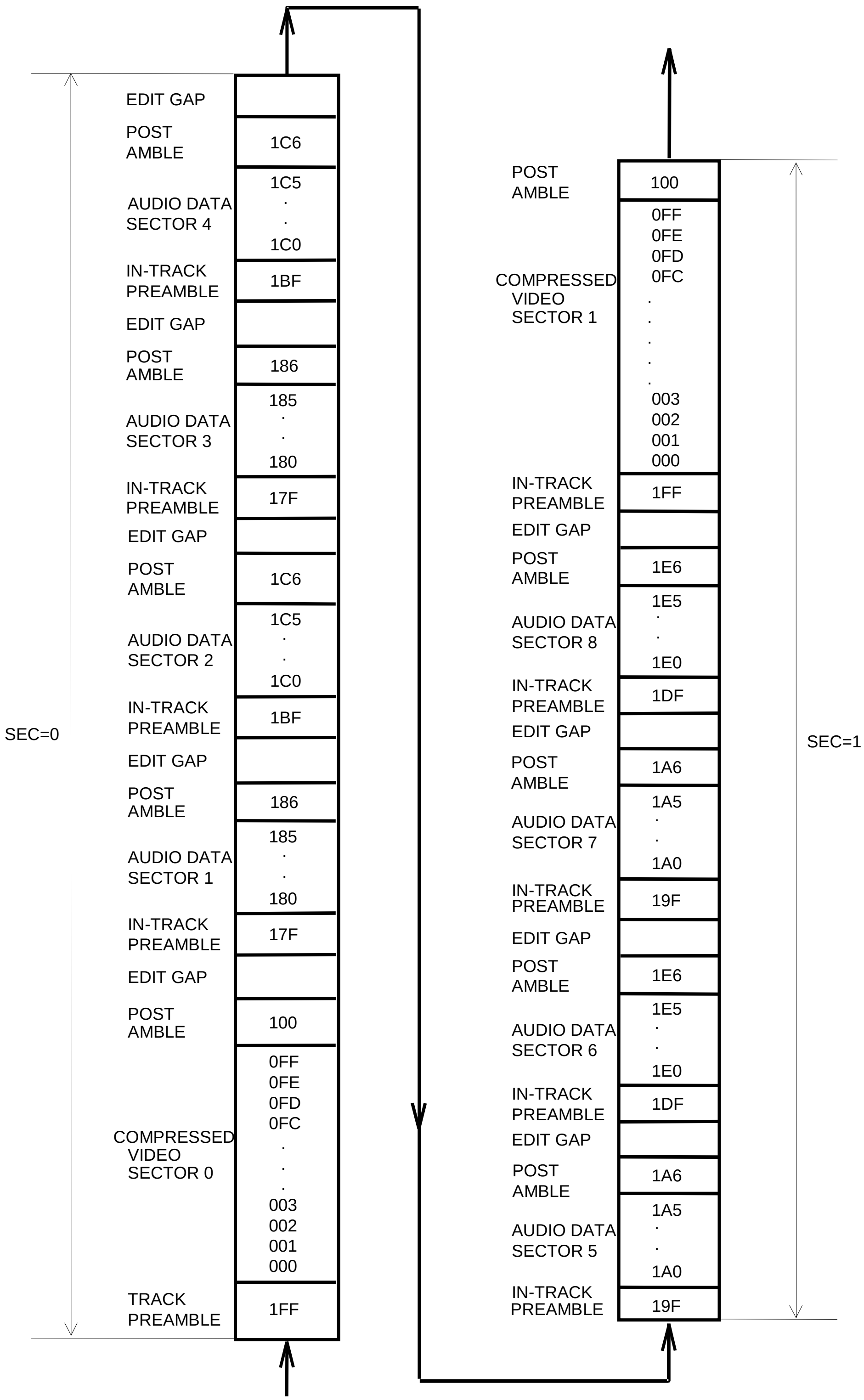
Figure 11 – Sync block identification format



NOTES

1 F = field number (0, 1, 2, 3).
2 S = segment number (0, 1, 2).
3 SEC = sector number; C = MSB of track number (0, 1).
4 T = track number (0, 1, 2, 3). LSB of track number is identified by the azimuth angle.
5 Audio data sectors are not shown.

Figure 12 – Track, segment and field numbers



NOTE – Sync block number shows in hexadecimal notation.

Figure 13 – Sync block number

c) Compressed video data field identification: The field address VF_0, VF_1, VF_2 (bits 4, 5, and 6 of the byte 3) for compressed video sync blocks shall identify the field sequence as shown below:

1080/59.94i and 720/59.94p systems:

	VF_0	VF_1	VF_2
Field 1 / Frame	0	0	0
Field 2 / Frame	1	0	0
Field 1 / Frame	0	1	0
Field 2 / Frame	1	1	0

1080/50i, 1080/25p, 1080/24p and 1080/23.98p systems:

	VF_0	VF_1	VF_2
Field 1 / Frame	0	0	0
Field 2 / Frame	1	0	0
Field 1 / Frame	0	1	0
Field 2 / Frame	1	1	0
Field 1 / Frame	0	0	1
Field 2 / Frame	1	0	1
Field 1 / Frame	0	1	1
Field 2 / Frame	1	1	1

d) Audio data field identification: The field address AF_0 and AF_1 of the audio data sync block (bits 4 and 5 of byte 3) shall identify a four-field sequence as shown below. When audio data sectors are edited, the four-field sequence shall be maintained.

Field/Frame	AF_0	AF_1
m	0	0
m+1	1	0
m+2	0	1
m+3	1	1

For 1080/59.94i and 720/59.94p systems, the field address AF_2 of the audio data sync block (bit 6 of byte 3) shall identify a five-field sequence for the number of audio data samples in the current field as shown below. When audio data sectors are edited, the five-field sequence shall be maintained (see 10.3.6 d)).

For 1080/50i, 1080/25p, 1080/24p and 1080/23.98p systems, the field address AF_2 of the audio data sync block (bit 6 of byte 3) shall be set always to 0.

	1080/59.94i 720/59.94p		1080/50i 1080/25p		1080/24p [1)] 1080/23.98p	
Field/frame	AF_2	Number of audio data samples	AF_2	Number of audio data samples	AF_2	Number of audio data samples
n	0	801	0	960	0	1001
n+1	0	801	0	960	0	1001
n+2	0	801	0	960	0	1001
n+3	0	801	0	960	0	1001
n+4	1	800	0	960	0	1001

[1)] The format supports recording of AES3 audio and data payload stream for all frame rates with the exception of the 1080/24p. The 1000 samples of the AES3 audio data payload for the 1080/24p frame rate is made common to the 1080/23.98p by use of a sample rate converter (see figure 15). However use of the sample rate converter in the 1080/24p mode limits the AES streams only to AES3 audio.

e) Protection: The identification pattern is protected by an inner code block.

f) Randomization: The identification pattern is randomized before being channel coded. The randomizing is equivalent to performing the exclusive-OR operation between the serial data stream and serial stream generated by the polynomial function

$$x^8 + x^4 + x^3 + x^2 + 1 \text{ (in GF(2))}$$

The first term is the most significant and the first to enter the division computation. The polynomial generator noted above is preset to 15_h at the first byte of the identification pattern and continues to cycle until the end of the sync block.

6.3.4 Data field

This block is used for all compressed video data and audio data and the associated error correction data.

a) Length: 1 inner code block. The inner code block contains 95 bytes consisting of two identification pattern bytes, 85 data bytes (outer ECC check bytes are considered data), plus 8 inner ECC check bytes.

b) Arrangement: See figure 10.

c) Interleaving: None

d) Protection: Inner ECC code

Type: Reed-Solomon.

Galois Field: GF(256).

Field generator polynomial: $x^8 + x^4 + x^3 + x^2 + 1$,

where x^i are place keeping variables in GF(2), the binary field.

Order of use: Left-most term is most significant, "oldest" in time computationally, and written to tape first.

Code generator polynomial in GF(256) is:

$$G(x) = (x+1)(x+a)(x+a^2)(x+a^3)(x+a^4)(x+a^5)(x+a^6)(x+a^7),$$

where a is given by 02_h in GF(256).

Check characters : $K_7, K_6, K_5, K_4, K_3, K_2, K_1, K_0$ in $K_7x^7 + K_6x^6 + K_5x^5 + K_4x^4 + K_3x^3 + K_2x^2 + K_1x + K_0$ obtained as the remainder after dividing $x^8D(x)$ by $G(x)$, where

$$D(x) = ID_0x^{86} + ID_1x^{85} + B_{84}x^{84} + \ldots + B_2x^2 + B_1x + B_0 .$$

Polynomial of full code :

$$ID_0x^{94} + ID_1x^{93} + B_{84}x^{92} + B_{83}x^{91} + \ldots + B_1x^9 + B_0x^8 + K_7x^7 + K_6x^6 + \ldots + K_2x^2 + K_1x + K_0 .$$

e) Randomization: All data and error correction check characters are randomized before being channel coded. The randomization is equivalent to randomization as defined in 6.3.3 e).

6.3.5 Sector preamble

All sectors are preceded by a preamble consisting of a clock run-up sequence, sync pattern (2 bytes), identification pattern (2 bytes), and fill pattern (4 bytes). The clock run-up sequence varies in length depending on the sector. The remaining elements of the preamble have the same format for all sectors. When a sector is edited, the appropriate preamble, including run-up sequence, shall be recorded.

6.3.5.1 Track preamble (T)

The track preamble precedes the first sector of every track. The total length of track preamble is 58 bytes and contains 50 bytes of run-up pattern "$2C_h$" which is followed by two bytes of sync pattern, two bytes of identification pattern, and four bytes of fill pattern "00_h".

LSB							MSB
0	0	1	1	0	1	0	0

a) Arrangement: See figure 14 (a).

b) Total length: 58 bytes.

c) Run-up pattern: $2C_h$.

d) Sync pattern: See 6.3.2.

e) Identification pattern: See 6.3.3.

f) Fill pattern: 00_h.

g) Protection: None.

h) Randomization: Only the identification pattern and fill pattern are randomized before being channel coded. The randomization is equivalent to randomization as defined in 6.3.3 e).

6.3.5.2 In-track preamble (E)

An in-track preamble precedes every sector except the first sector of a track. The total length is 28 bytes long and contains 20 bytes of run-up pattern "$2C_h$" followed by two bytes of sync pattern, two bytes of identification pattern, and four bytes of fill pattern "00_h".

a) Arrangement: See figure 14 (b).

b) Total length: 28 bytes.

c) Run-up pattern: $2C_h$.

LSB							MSB
0	0	1	1	0	1	0	0

d) Sync pattern: See 6.3.2.

e) Identification pattern: See 6.3.3.

f) Fill pattern: 00_h.

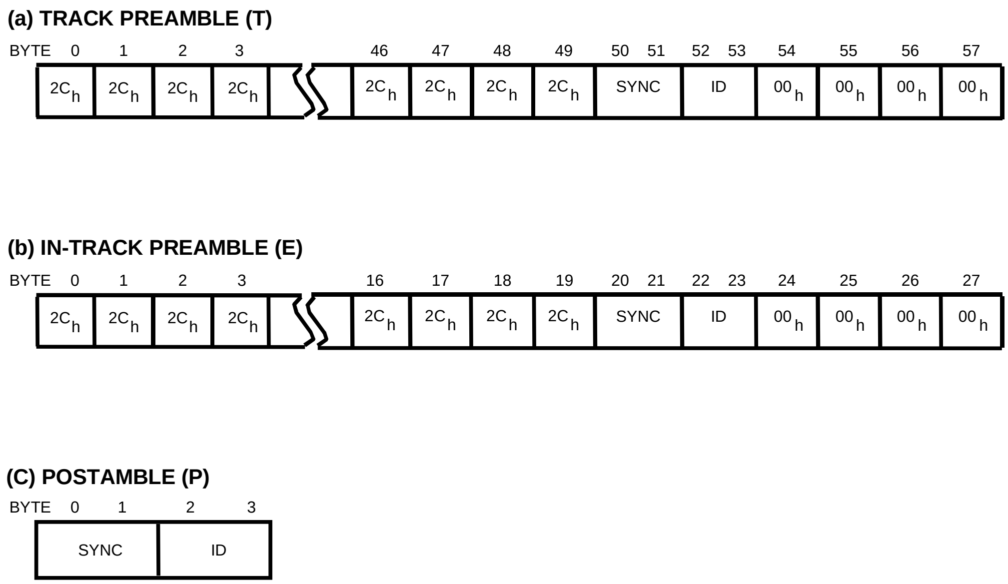


Figure 14 – Sector preamble and postamble

g) Protection: None.

h) Randomization: Only the identification pattern and fill pattern are randomized before being channel coded. The randomization is equivalent to randomization as defined in 6.3.3 f).

6.3.6 Sector postamble (P)

All sectors are followed by a postamble. The total length is four bytes and contains two bytes of sync pattern and two bytes of identification pattern.

a) Arrangement: See figure 14 (c).

b) Total length: 4 bytes.

c) Sync pattern: See 6.3.2.

d) Identification pattern: See 6.3.3.

e) Protection: None.

f) Randomization: Only the identification pattern is randomized before being channel coded. The randomization is equivalent to randomization as defined in 6.3.3 f).

6.4 Edit gaps

The spaces between individual sectors of a track, exclusive of preamble and postamble, are nominally 162 bytes long.

The edit gap is used to accommodate timing errors during editing. In an original recording, the edit gap shall contain the pattern $2C_h$. During an edit, the edit gap may be partially overwritten with $2C_h$ code provided that the preamble and/or postamble of the adjacent unedited track sectors are not overwritten.

a) Protection: None.

b) Randomization: None.

6.5 Channel code

The channel code shall be an 8-14 modulation code which is defined by the following code rules.

NOTES

1 DSV is an abbreviation for digital sum variation and indicates the integral value which is counted from the beginning of the 8-14 modulated wave form, taking high level as 1 and low level as -1.

2 CDS is an abbreviation for code word digital sum and indicates the DSV of one symbol modulation code.

3 8-bit data entries in tables 3 and 4 are in hexadecimal notation.

Selecting the current 14-bit code, the following steps shall be taken:

1) Select a 14-bit code satisfying the following conditions of (A) and (B) from tables 3 and 4:

a) The number of consecutive identical bits at the joint portion with the preceding 14-bit code is two to seven.

b) The absolute value of the DSV at the end of the code (called end DSV hereafter) is equal to or less than two.

2) When two or more 14-bit codes are selected at step (1), choose a 14-bit code that gives the smallest absolute value of the end DSV.

3) When two or more 14-bit codes are still chosen in step (2), select a 14-bit code by calculating the DSV for each bit of the code (called bit DSV hereafter), determining the bit DSV the absolute value of which is minimum for each code, and choosing the code with the bit DSV whose minimum absolute value is smallest.

4) When two or more 14-bit codes are further found in step (3), select a 14-bit code by finding the maximum absolute value of the bit DSV of each code, and choosing a code with the bit DSV whose maximum absolute value is equal to or less than six.

5) When two or more codes are still found in step (4), select a 14-bit code satisfying the condition that the number of consecutive identical bits at the joint portion with the preceding 14-bit code is equal to or less than six.

6) When any codes selected in step (4) do not satisfy step (5), or two or more modulation codes satisfy step (5), select a 14-bit code satisfying the condition that the number of consecutive identical bits in that code is equal to or less than six.

7) When any codes selected in step (4) do not satisfy step (5) and step (6), or when any codes selected in step (5) do not satisfy step (6), or when two or more codes are further found in step (6), the following two steps shall be taken:

a) When the end DSV of the code is -2, select a code of higher priority (corresponding to a smaller number in table 5) according to table 5. Likewise, when the end DSV of the code is

+2, select a code of higher priority (corresponding to smaller number in table 6) according to table 6.

b) When two or more codes belonging to the equal highest priority are found in step (a), select all of them temporarily. When the end DSV is zero, select a code satisfying the last six bits except when 111111 or 000000 are in the code.

8) When any codes selected in step (4) do not satisfy steps (5), (6), and (7), or when any codes selected in step (5) do not satisfy step (6) and step (7), or when any codes selected in step (6) do not satisfy step (7), or when two or more codes are further found in step (7), select a code with the bit DSV whose maximum absolute value is smallest.

9) When two or more codes are still found in step (8), select a 14-bit code with the bit DSV whose minimum absolute value appears earliest in the bit string of the code.

10) When two or more codes are further found in step (9), select a 14-bit code whose bit will be reversed earliest after the joint portion with the preceding code.

Table 3 – 8-14 modulation (CDS≥0)

Class	8-bit data	Modulation codes beginning with "0"	CDS	Class	8-bit data	Modulation codes beginning with "1"	CDS
	00	01111110000001	0		00	10000001111110	0
	01	01111100110000	0		01	10000011001111	0
	02	01111100011000	0		02	10000011100111	0
	03	01111100001100	0		03	10000011110011	0
	04	01111100000110	0		04	10000011111001	0
	05	01111100000011	0		05	10000011111100	0
	06	01111001110000	0		06	10000110001111	0
	07	01111001100001	0		07	10000110011110	0
	08	01111000111000	0		08	10000111000111	0
	09	01111000110001	0		09	10000111001110	0
	0A	01111000011100	0		0A	10000111100011	0
	0B	01111000011001	0		0B	10000111100110	0
	0C	01111000001110	0		0C	10000111110001	0
	0D	01111000000111	0		0D	10000111111000	0
	0E	01110011110000	0		0E	10001100001111	0
	0F	01110011100001	0		0F	10001100011110	0
	10	01110011001100	0		10	10001100110011	0
	11	01110011000110	0		11	10001100111001	0
	12	01110011000011	0		12	10001100111100	0
	13	01110001111000	0		13	10001110000111	0
	14	01110001110001	0		14	10001110001110	0
	15	01110001100110	0		15	10001110011001	0
	16	01110001100011	0		16	10001110011100	0
	17	01110000111100	0		17	10001111000011	0
	18	01110000111001	0		18	10001111000110	0
	19	01110000110011	0		19	10001111001100	0
	1A	01110000011110	0		1A	10001111100001	0
	1B	01110000001111	0	1(B)	1B	10001111110000	0
1(A)	1C	01100111110000	0		1C	10011000001111	0
	1D	01100111100001	0		1D	10011000011110	0
	1E	01100111001100	0		1E	10011000110011	0
	1F	01100111000110	0		1F	10011000111001	0
	20	01100111000011	0		20	10011000111100	0
	21	01100110011100	0		21	10011001100011	0
	22	01100110011001	0		22	10011001100110	0
	23	01100110001110	0		23	10011001110001	0
	24	01100110000111	0		24	10011001111000	0
	25	01100011111000	0		25	10011100000111	0
	26	01100011110001	0		26	10011100001110	0
	27	01100011100110	0		27	10011100011001	0
	28	01100011100011	0		28	10011100011100	0
	29	01100011001110	0		29	10011100110001	0
	2A	01100011000111	0		2A	10011100111000	0
	2B	01100001111100	0		2B	10011110000011	0
	2C	01100001111001	0		2C	10011110000110	0
	2D	01100001110011	0		2D	10011110001100	0
	2E	01100001100111	0		2E	10011110011000	0
	2F	01100000111110	0		2F	10011111000001	0
	30	01100000011111	0		30	10011111100000	0
	31	01111111001100	4		31	10000011111110	2
	32	01111111000110	4		32	10000110011111	2
	33	01111111000011	4		33	10000111001111	2
	34	01111110011100	4		34	10000111100111	2
	35	01111110011001	4		35	10000111110011	2
	36	01111110001110	4		36	10000111111001	2
	37	01111110000111	4		37	10000111111100	2
	38	01111100111100	4		38	10001100011111	2

(continued)

Table 3 – 8-14 modulation (CDS≥0) (continued)

Class	8-bit data	Modulation codes beginning with "0"	CDS	Class	8-bit data	Modulation codes beginning with "1"	CDS
	39	01111100111001	4		39	10001100111110	2
	3A	01111100110011	4		3A	10001110001111	2
	3B	01111100011110	4		3B	10001110011110	2
	3C	01111100001111	4		3C	10001111000111	2
	3D	01111001111100	4		3D	10001111001110	2
	3E	01111001111001	4		3E	10001111100011	2
	3F	01111001110011	4		3F	10001111100110	2
	40	01111001100111	4		40	10001111110001	2
	41	01111000111110	4		41	10001111111000	2
	42	01111000011111	4		42	10011000011111	2
	43	01110011111100	4		43	10011000111110	2
	44	01110011111001	4		44	10011001100111	2
	45	01110011110011	4		45	10011001110011	2
	46	01110011100111	4		46	10011001111001	2
	47	01110011001111	4		47	10011001111100	2
	48	01110001111110	4		48	10011100001111	2
	49	01110000111111	4		49	10011100011110	2
	4A	01100111111100	4		4A	10011100110011	2
	4B	01100111111001	4		4B	10011100111001	2
	4C	01100111110011	4	1(B)	4C	10011100111100	2
	4D	01100111100111	4		4D	10011110000111	2
	4E	01100111001111	4		4E	10011110001110	2
	4F	01100110011111	4		4F	10011110011001	2
	50	01100011111110	4		50	10011110011100	2
	51	01111111000001	2		51	10011111000011	2
	52	01111110011000	2		52	10011111000110	2
	53	01111110001100	2		53	10011111001100	2
1(A)	54	01111110000110	2		54	10011111100001	2
	55	01111110000011	2		55	10011111110000	2
	56	01111100111000	2		56	10001111001111	4
	57	01111100110001	2		57	10001111100111	4
	58	01111100011100	2		58	10001111110011	4
	59	01111100011001	2		59	10011001111110	4
	5A	01111100001110	2		5A	10011100111110	4
	5B	01111100000111	2		5B	10011110001111	4
	5C	01111001111000	2		5C	10011110011110	4
	5D	01111001110001	2		5D	10011111000111	4
	5E	01111001100110	2		5E	10011111001110	4
	5F	01111001100011	2		5F	10011111100011	4
	60	01111000111100	2		60	10011111100110	4
	61	01111000111001	2		61	11000111100111	4
	62	01111000110011	2		62	11000111110011	4
	63	01111000011110	2		63	11000000111111	2
	64	01111000001111	2		64	11000001111110	2
	65	01110011111000	2		65	11000011001111	2
	66	01110011110001	2		66	11000011100111	2
	67	01110011100110	2		67	11000011110011	2
	68	01110011100011	2		68	11000011111001	2
	69	01110011001110	2	2(B)	69	11000011111100	2
	6A	01110011000111	2		6A	11000110001111	2
	6B	01110001111100	2		6B	11000110011110	2
	6C	01110001111001	2		6C	11000111000111	2
	6D	01110001110011	2		6D	11000111001110	2
	6E	01110001100111	2		6E	11000111100011	2
	6F	01110000111110	2		6F	11000111100110	2
	70	01110000011111	2		70	11000111110001	2

(continued)

Table 3 – 8-14 modulation (CDS≥0) (continued)

Class	8-bit data	Modulation codes beginning with "0"	CDS	Class	8-bit data	Modulation codes beginning with "1"	CDS
1(A)	71	01100111111000	2	2(B)	71	11000111111000	2
	72	01100111110001	2		72	11001100001111	2
	73	01100111100110	2		73	11001100011110	2
	74	01100111100011	2		74	11001100110011	2
	75	01100111001110	2		75	11001100111001	2
	76	01100111000111	2		76	11001100111100	2
	77	01100110011110	2		77	11001110000111	2
	78	01100110001111	2		78	11001110001110	2
	79	01100011111100	2		79	11001110011001	2
	7A	01100011111001	2		7A	11001110011100	2
	7B	01100011110011	2		7B	11001111000011	2
	7C	01100011100111	2		7C	11001111000110	2
	7D	01100011001111	2		7D	11001111001100	2
	7E	01100001111110	2		7E	11001111100001	2
	7F	01100000111111	2		7F	11001111110000	2
2(A)	80	00111111100000	0		80	11000000011111	0
	81	00111111000001	0		81	11000000111110	0
	82	00111110011000	0		82	11000001100111	0
	83	00111110001100	0		83	11000001110011	0
	84	00111110000110	0		84	11000001111001	0
	85	00111110000011	0		85	11000001111100	0
	86	00111100111000	0		86	11000011000111	0
	87	00111100110001	0		87	11000011001110	0
	88	00111100011100	0		88	11000011100011	0
	89	00111100011001	0		89	11000011100110	0
	8A	00111100001110	0		8A	11000011110001	0
	8B	00111100000111	0		8B	11000011111000	0
	8C	00111001111000	0		8C	11000110000111	0
	8D	00111001110001	0		8D	11000110001110	0
	8E	00111001100110	0		8E	11000110011001	0
	8F	00111001100011	0		8F	11000110011100	0
	90	00111000111100	0		90	11000111000011	0
	91	00111000111001	0		91	11000111000110	0
	92	00111000110011	0		92	11000111001100	0
	93	00111000011110	0		93	11000111100001	0
	94	00111000001111	0		94	11000111110000	0
	95	00110011111000	0		95	11001100000111	0
	96	00110011110001	0		96	11001100001110	0
	97	00110011100110	0		97	11001100011001	0
	98	00110011100011	0		98	11001100011100	0
	99	00110011001110	0		99	11001100110001	0
	9A	00110011000111	0		9A	11001100111000	0
	9B	00110001111100	0		9B	11001110000011	0
	9C	00110001111001	0		9C	11001110000110	0
	9D	00110001110011	0		9D	11001110001100	0
	9E	00110001100111	0		9E	11001110011000	0
	9F	00110000111110	0		9F	11001111000001	0
	A0	00110000011111	0		A0	11001111100000	0
	A1	00111111100001	2		A1	11001100111110	4
	A2	00111111001100	2		A2	11001110011110	4
	A3	00111111000110	2		A3	11001111000111	4
	A4	00111111000011	2		A4	11001111001110	4
	A5	00111110011100	2		A5	11001111100011	4
	A6	00111110011001	2		A6	11001111100110	4

(continued)

Table 3 – 8-14 modulation (CDS≥0) (continued)

Class	8-bit data	Modulation codes beginning with "0"	CDS	Class	8-bit data	Modulation codes beginning with "1"	CDS
	A7	00111110001110	2		A7	11100001111110	4
	A8	00111110000111	2		A8	11100011100111	4
	A9	00111100111100	2		A9	11100011110011	4
	AA	00111100111001	2		AA	11100011111100	4
	AB	00111100110011	2		AB	11100110011110	4
	AC	00111100011110	2		AC	11100111000111	4
	AD	00111100001111	2		AD	11100111001110	4
	AE	00111001111100	2		AE	11100111100011	4
	AF	00111001111001	2		AF	11100111100110	4
	B0	00111001110011	2		B0	11100111111000	4
	B1	00111001100111	2		B1	11100000011111	2
	B2	00111000111110	2		B2	11100000111110	2
	B3	00111000011111	2		B3	11100001100111	2
	B4	00110011111100	2		B4	11100001110011	2
	B5	00110011111001	2		B5	11100001111001	2
2(A)	B6	00110011110011	2		B6	11100001111100	2
	B7	00110011100111	2		B7	11100011000111	2
	B8	00110011001111	2		B8	11100011001110	2
	B9	00110001111110	2		B9	11100011100011	2
	BA	00110000111111	2		BA	11100011100110	2
	BB	00111111100110	4		BB	11100011110001	2
	BC	00111111100011	4		BC	11100011111000	2
	BD	00111111001110	4		BD	11100110000111	2
	BE	00111111000111	4	3(B)	BE	11100110001110	2
	BF	00111110011110	4		BF	11100110011001	2
	C0	00111110001111	4		C0	11100110011100	2
	C1	00111100111110	4		C1	11100111000011	2
	C2	00111100011111	4		C2	11100111000110	2
	C3	00111001111110	4		C3	11100111001100	2
	C4	00111000111111	4		C4	11100111100001	2
	C5	00110011111110	4		C5	11100111110000	2
	C6	00011111110000	0		C6	11100000001111	0
	C7	00011111100001	0		C7	11100000011110	0
	C8	00011111001100	0		C8	11100000110011	0
	C9	00011111000110	0		C9	11100000111001	0
	CA	00011111000011	0		CA	11100000111100	0
	CB	00011110011100	0		CB	11100001100011	0
	CC	00011110011001	0		CC	11100001100110	0
	CD	00011110001110	0		CD	11100001110001	0
	CE	00011110000111	0		CE	11100001111000	0
	CF	00011100111100	0		CF	11100011000011	0
	D0	00011100111001	0		D0	11100011000110	0
	D1	00011100110011	0		D1	11100011001100	0
	D2	00011100011110	0		D2	11100011100001	0
3(A)	D3	00011100001111	0		D3	11100011110000	0
	D4	00011001111100	0		D4	11100110000011	0
	D5	00011001111001	0		D5	11100110000110	0
	D6	00011001110011	0		D6	11100110001100	0
	D7	00011001100111	0		D7	11100110011000	0
	D8	00011000111110	0		D8	11100111000001	0
	D9	00011000011111	0		D9	11100111100000	0
	DA	00011111110001	2		DA	11110001111100	4
	DB	00011111100110	2	4(B)	DB	11110011111000	4
	DC	00011111100011	2		DC	11110000001111	2
	DD	00011111001110	2		DD	11110000011110	2

(continued)

Table 3 – 8-14 modulation (CDS≥0) (concluded)

Class	8-bit data	Modulation codes beginning with "0"	CDS	Class	8-bit data	Modulation codes beginning with "1"	CDS
3(A)	DE	00011111000111	2	4(B)	DE	11110000110011	2
	DF	00011110011110	2		DF	11110000111001	2
	E0	00011110001111	2		E0	11110000111100	2
	E1	00011100111110	2		E1	11110001100011	2
	E2	00011100011111	2		E2	11110001100110	2
	E3	00011001111110	2		E3	11110001110001	2
	E4	00011000111111	2		E4	11110001111000	2
	E5	00011111110011	4		E5	11110011000011	2
	E6	00011111100111	4		E6	11110011000110	2
	E7	00011111001111	4		E7	11110011001100	2
	E8	00011110011111	4		E8	11110011100001	2
	E9	00011100111111	4		E9	11110011110000	2
4(A)	EA	00001111111000	0		EA	11110000000111	0
	EB	00001111110001	0		EB	11110000001110	0
	EC	00001111100110	0		EC	11110000011001	0
	ED	00001111100011	0		ED	11110000011100	0
	EE	00001111001110	0		EE	11110000110001	0
	EF	00001111000111	0		EF	11110000111000	0
	F0	00001110011110	0		F0	11110001100001	0
	F1	00001110001111	0		F1	11110001110000	0
	F2	00001100111110	0		F2	11110011000001	0
	F3	00001100011111	0		F3	11110011100000	0
	F4	00001111111001	2	5(B)	F4	11111000000111	2
	F5	00001111110011	2		F5	11111000001110	2
	F6	00001111100111	2		F6	11111000011001	2
	F7	00001111001111	2		F7	11111000011100	2
	F8	00001110011111	2		F8	11111000110001	2
	F9	00001100111111	2		F9	11111000111000	2
5(A)	FA	00000111111100	0		FA	11111001100001	2
	FB	00000111111001	0		FB	11111001110000	2
	FC	00000111110011	0		FC	11111000001100	0
	FD	00000111100111	0		FD	11111000011000	0
	FE	00000111001111	0		FE	11111000110000	0
	FF	00000110011111	0		FF	11111001100000	0

Table 4 – 8-14 modulation (CDS≤0)

Class	8-bit data	Modulation codes beginning with "0"	CDS	Class	8-bit data	Modulation codes beginning with "1"	CDS
	00	01111110000001	0		00	10000001111110	0
	01	01111100110000	0		01	10000011001111	0
	02	01111100011000	0		02	10000011100111	0
	03	01111100001100	0		03	10000011110011	0
	04	01111100000110	0		04	10000011111001	0
	05	01111100000011	0		05	10000011111100	0
	06	01111001110000	0		06	10000110001111	0
	07	01111001100001	0		07	10000110011110	0
	08	01111000111000	0		08	10000111000111	0
	09	01111000110001	0		09	10000111001110	0
	0A	01111000011100	0		0A	10000111100011	0
	0B	01111000011001	0		0B	10000111100110	0
	0C	01111000001110	0		0C	10000111110001	0
	0D	01111000000111	0		0D	10000111111000	0
	0E	01110011110000	0		0E	10001100001111	0
	0F	01110011100001	0		0F	10001100011110	0
	10	01110011001100	0		10	10001100110011	0
	11	01110011000110	0		11	10001100111001	0
	12	01110011000011	0		12	10001100111100	0
	13	01110001111000	0		13	10001110000111	0
	14	01110001110001	0		14	10001110001110	0
	15	01110001100110	0		15	10001110011001	0
	16	01110001100011	0		16	10001110011100	0
	17	01110000111100	0		17	10001111000011	0
	18	01110000111001	0		18	10001111000110	0
	19	01110000110011	0		19	10001111001100	0
	1A	01110000011110	0		1A	10001111100001	0
	1B	01110000001111	0		1B	10001111110000	0
1(C)	1C	01100111110000	0	1(D)	1C	10011000001111	0
	1D	01100111100001	0		1D	10011000011110	0
	1E	01100111001100	0		1E	10011000110011	0
	1F	01100111000110	0		1F	10011000111001	0
	20	01100111000011	0		20	10011000111100	0
	21	01100110011100	0		21	10011001100011	0
	22	01100110011001	0		22	10011001100110	0
	23	01100110001110	0		23	10011001110001	0
	24	01100110000111	0		24	10011001111000	0
	25	01100011111000	0		25	10011100000111	0
	26	01100011110001	0		26	10011100001110	0
	27	01100011100110	0		27	10011100011001	0
	28	01100011100011	0		28	10011100011100	0
	29	01100011001110	0		29	10011100110001	0
	2A	01100011000111	0		2A	10011100111000	0
	2B	01100001111100	0		2B	10011110000011	0
	2C	01100001111001	0		2C	10011110000110	0
	2D	01100001110011	0		2D	10011110001100	0
	2E	01100001100111	0		2E	10011110011000	0
	2F	01100000111110	0		2F	10011111000001	0
	30	01100000011111	0		30	10011111100000	0
	31	01111100000001	-2		31	10000000110011	-4
	32	01111001100000	-2		32	10000000111001	-4
	33	01111000110000	-2		33	10000000111100	-4
	34	01111000011000	-2		34	10000001100011	-4
	35	01111000001100	-2		35	10000001100110	-4
	36	01111000000110	-2		36	10000001110001	-4
	37	01111000000011	-2		37	10000001111000	-4
	38	01110011100000	-2		38	10000011000011	-4

(continued)

Table 4 – 8-14 modulation (CDS≤0) (continued)

Class	8-bit data	Modulation codes beginning with "0"	CDS	Class	8-bit data	Modulation codes beginning with "1"	CDS
1(C)	39	01110011000001	-2	1(D)	39	10000011000110	-4
	3A	01110001110000	-2		3A	10000011001100	-4
	3B	01110001100001	-2		3B	10000011100001	-4
	3C	01110000111000	-2		3C	10000011110000	-4
	3D	01110000110001	-2		3D	10000110000011	-4
	3E	01110000011100	-2		3E	10000110000110	-4
	3F	01110000011001	-2		3F	10000110001100	-4
	40	01110000001110	-2		40	10000110011000	-4
	41	01110000000111	-2		41	10000111000001	-4
	42	01100111100000	-2		42	10000111100000	-4
	43	01100111000001	-2		43	10001100000011	-4
	44	01100110011000	-2		44	10001100000110	-4
	45	01100110001100	-2		45	10001100001100	-4
	46	01100110000110	-2		46	10001100011000	-4
	47	01100110000011	-2		47	10001100110000	-4
	48	01100011110000	-2		48	10001110000001	-4
	49	01100011100001	-2		49	10001111000000	-4
	4A	01100011001100	-2		4A	10011000000011	-4
	4B	01100011000110	-2		4B	10011000000110	-4
	4C	01100011000011	-2		4C	10011000001100	-4
	4D	01100001111000	-2		4D	10011000011000	-4
	4E	01100001110001	-2		4E	10011000110000	-4
	4F	01100001100110	-2		4F	10011001100000	-4
	50	01100001100011	-2		50	10011100000001	-4
	51	01100000111100	-2		51	10000000111110	-2
	52	01100000111001	-2		52	10000001100111	-2
	53	01100000110011	-2		53	10000001110011	-2
	54	01100000011110	-2		54	10000001111001	-2
	55	01100000001111	-2		55	10000001111100	-2
	56	01110000110000	-4		56	10000011000111	-2
	57	01110000011000	-4		57	10000011001110	-2
	58	01110000001100	-4		58	10000011100011	-2
	59	01100110000001	-4		59	10000011100110	-2
	5A	01100011000001	-4		5A	10000011110001	-2
	5B	01100001110000	-4		5B	10000011111000	-2
	5C	01100001100001	-4		5C	10000110000111	-2
	5D	01100000111000	-4		5D	10000110001110	-2
	5E	01100000110001	-4		5E	10000110011001	-2
	5F	01100000011100	-4		5F	10000110011100	-2
	60	01100000011001	-4		60	10000111000011	-2
	61	00111000011000	-4		61	10000111000110	-2
2(C)	62	00111000001100	-4		62	10000111001100	-2
	63	00111111000000	-2		63	10000111100001	-2
	64	00111110000001	-2		64	10000111110000	-2
	65	00111100110000	-2		65	10001100000111	-2
	66	00111100011000	-2		66	10001100001110	-2
	67	00111100001100	-2		67	10001100011001	-2
	68	00111100000110	-2		68	10001100011100	-2
	69	00111100000011	-2		69	10001100110001	-2
	6A	00111001110000	-2		6A	10001100111000	-2
	6B	00111001100001	-2		6B	10001110000011	-2
	6C	00111000111000	-2		6C	10001110000110	-2
	6D	00111000110001	-2		6D	10001110001100	-2
	6E	00111000011100	-2		6E	10001110011000	-2
	6F	00111000011001	-2		6F	10001111000001	-2
	70	00111000001110	-2		70	10001111100000	-2

(continued)

Table 4 – 8-14 modulation (CDS≤0) (continued)

Class	8-bit data	Modulation codes beginning with "0"	CDS	Class	8-bit data	Modulation codes beginning with "1"	CDS
	71	00111000000111	-2		71	10011000000111	-2
	72	00110011110000	-2		72	10011000001110	-2
	73	00110011100001	-2		73	10011000011001	-2
	74	00110011001100	-2		74	10011000011100	-2
	75	00110011000110	-2		75	10011000110001	-2
	76	00110011000011	-2		76	10011000111000	-2
	77	00110001111000	-2	1(D)	77	10011001100001	-2
	78	00110001110001	-2		78	10011001110000	-2
	79	00110001100110	-2		79	10011100000011	-2
	7A	00110001100011	-2		7A	10011100000110	-2
	7B	00110000111100	-2		7B	10011100001100	-2
	7C	00110000111001	-2		7C	10011100011000	-2
	7D	00110000110011	-2		7D	10011100110000	-2
	7E	00110000011110	-2		7E	10011110000001	-2
	7F	00110000001111	-2		7F	10011111000000	-2
	80	00111111100000	0		80	11000000011111	0
	81	00111111000001	0		81	11000000111110	0
	82	00111110011000	0		82	11000001100111	0
	83	00111110001100	0		83	11000001110011	0
	84	00111110000110	0		84	11000001111001	0
	85	00111110000011	0		85	11000001111100	0
	86	00111100111000	0		86	11000011000111	0
	87	00111100110001	0		87	11000011001110	0
	88	00111100011100	0		88	11000011100011	0
	89	00111100011001	0		89	11000011100110	0
2(C)	8A	00111100001110	0		8A	11000011110001	0
	8B	00111100000111	0		8B	11000011111000	0
	8C	00111001111000	0		8C	11000110000111	0
	8D	00111001110001	0		8D	11000110001110	0
	8E	00111001100110	0		8E	11000110011001	0
	8F	00111001100011	0		8F	11000110011100	0
	90	00111000111100	0		90	11000111000011	0
	91	00111000111001	0		91	11000111000110	0
	92	00111000110011	0		92	11000111001100	0
	93	00111000011110	0		93	11000111100001	0
	94	00111000001111	0	2(D)	94	11000111110000	0
	95	00110011111000	0		95	11001100000111	0
	96	00110011110001	0		96	11001100001110	0
	97	00110011100110	0		97	11001100011001	0
	98	00110011100011	0		98	11001100011100	0
	99	00110011001110	0		99	11001100110001	0
	9A	00110011000111	0		9A	11001100111000	0
	9B	00110001111100	0		9B	11001110000011	0
	9C	00110001111001	0		9C	11001110000110	0
	9D	00110001110011	0		9D	11001110001100	0
	9E	00110001100111	0		9E	11001110011000	0
	9F	00110000111110	0		9F	11001111000001	0
	A0	00110000011111	0		A0	11001111100000	0
	A1	00110011000001	-4		A1	11000000011110	-2
	A2	00110001100001	-4		A2	11000000110011	-2
	A3	00110000111000	-4		A3	11000000111001	-2
	A4	00110000110001	-4		A4	11000000111100	-2
	A5	00110000011100	-4		A5	11000001100011	-2
	A6	00110000011001	-4		A6	11000001100110	-2

(continued)

Table 4 – 8-14 modulation (CDS≤0) (continued)

Class	8-bit data	Modulation codes beginning with "0"	CDS	Class	8-bit data	Modulation codes beginning with "1"	CDS
	A7	00011110000001	-4		A7	11000001110001	-2
	A8	00011100011000	-4		A8	11000001111000	-2
	A9	00011100001100	-4		A9	11000011000011	-2
	AA	00011100000011	-4		AA	11000011000110	-2
	AB	00011001100001	-4		AB	11000011001100	-2
	AC	00011000111000	-4		AC	11000011100001	-2
	AD	00011000110001	-4		AD	11000011110000	-2
	AE	00011000011100	-4		AE	11000110000011	-2
	AF	00011000011001	-4		AF	11000110000110	-2
	B0	00011000000111	-4		B0	11000110001100	-2
	B1	00011111100000	-2		B1	11000110011000	-2
	B2	00011111000001	-2		B2	11000111000001	-2
	B3	00011110011000	-2		B3	11000111100000	-2
	B4	00011110001100	-2		B4	11001100000011	-2
	B5	00011110000110	-2	2(D)	B5	11001100000110	-2
	B6	00011110000011	-2		B6	11001100001100	-2
	B7	00011100111000	-2		B7	11001100011000	-2
	B8	00011100110001	-2		B8	11001100110000	-2
	B9	00011100011100	-2		B9	11001110000001	-2
	BA	00011100011001	-2		BA	11001111000000	-2
	BB	00011100001110	-2		BB	11000000011001	-4
	BC	00011100000111	-2		BC	11000000011100	-4
	BD	00011001111000	-2		BD	11000000110001	-4
3(C)	BE	00011001110001	-2		BE	11000000111000	-4
	BF	00011001100110	-2		BF	11000001100001	-4
	C0	00011001100011	-2		C0	11000001110000	-4
	C1	00011000111100	-2		C1	11000011000001	-4
	C2	00011000111001	-2		C2	11000011100000	-4
	C3	00011000110011	-2		C3	11000110000001	-4
	C4	00011000011110	-2		C4	11000111000000	-4
	C5	00011000001111	-2		C5	11001100000001	-4
	C6	00011111110000	0		C6	11100000001111	0
	C7	00011111100001	0		C7	11100000011110	0
	C8	00011111001100	0		C8	11100000110011	0
	C9	00011111000110	0		C9	11100000111001	0
	CA	00011111000011	0		CA	11100000111100	0
	CB	00011110011100	0		CB	11100001100011	0
	CC	00011110011001	0		CC	11100001100110	0
	CD	00011110001110	0		CD	11100001110001	0
	CE	00011110000111	0		CE	11100001111000	0
	CF	00011100111100	0		CF	11100011000011	0
	D0	00011100111001	0		D0	11100011000110	0
	D1	00011100110011	0		D1	11100011001100	0
	D2	00011100011110	0	3(D)	D2	11100011100001	0
	D3	00011100001111	0		D3	11100011110000	0
	D4	00011001111100	0		D4	11100110000011	0
	D5	00011001111001	0		D5	11100110000110	0
	D6	00011001110011	0		D6	11100110001100	0
	D7	00011001100111	0		D7	11100110011000	0
	D8	00011000111110	0		D8	11100111000001	0
	D9	00011000011111	0		D9	11100111100000	0
	DA	00001110000011	-4		DA	11100000001110	-2
	DB	00001100000111	-4		DB	11100000011001	-2
4(C)	DC	00001111110000	-2		DC	11100000011100	-2
	DD	00001111100001	-2		DD	11100000110001	-2

(continued)

Table 4 – 8-14 modulation (CDS≤0) (concluded)

Class	8-bit data	Modulation codes beginning with "0"	CDS	Class	8-bit data	Modulation codes beginning with "1"	CDS
4(C)	DE	00001111001100	-2	3(D)	DE	11100000111000	-2
	DF	00001111000110	-2		DF	11100001100001	-2
	E0	00001111000011	-2		E0	11100001110000	-2
	E1	00001110011100	-2		E1	11100011000001	-2
	E2	00001110011001	-2		E2	11100011100000	-2
	E3	00001110001110	-2		E3	11100110000001	-2
	E4	00001110000111	-2		E4	11100111000000	-2
	E5	00001100111100	-2		E5	11100000001100	-4
	E6	00001100111001	-2		E6	11100000011000	-4
	E7	00001100110011	-2		E7	11100000110000	-4
	E8	00001100011110	-2		E8	11100001100000	-4
	E9	00001100001111	-2		E9	11100011000000	-4
	EA	00001111111000	0	4(D)	EA	11110000000111	0
	EB	00001111110001	0		EB	11110000001110	0
	EC	00001111100110	0		EC	11110000011001	0
	ED	00001111100011	0		ED	11110000011100	0
	EE	00001111001110	0		EE	11110000110001	0
	EF	00001111000111	0		EF	11110000111000	0
	F0	00001110011110	0		F0	11110001100001	0
	F1	00001110001111	0		F1	11110001110000	0
	F2	00001100111110	0		F2	11110011000001	0
	F3	00001100011111	0		F3	11110011100000	0
5(C)	F4	00000111111000	-2		F4	11110000000110	-2
	F5	00000111110001	-2		F5	11110000001100	-2
	F6	00000111100110	-2		F6	11110000011000	-2
	F7	00000111100011	-2		F7	11110000110000	-2
	F8	00000111001110	-2		F8	11110001100000	-2
	F9	00000111000111	-2		F9	11110011000000	-2
	FA	00000110011110	-2	5(D)	FA	11111000000011	0
	FB	00000110001111	-2		FB	11111000000110	0
	FC	00000111110011	0		FC	11111000001100	0
	FD	00000111100111	0		FD	11111000011000	0
	FE	00000111001111	0		FE	11111000110000	0
	FF	00000110011111	0		FF	11111001100000	0

Table 5 – Priority of modulation code selection (end DSV = –2)

Modulation codes	Priority
x x x x x x x x x x x 0 0 1	4
x x x x x x x x x x 0 0 1 1	1
x x x x x x x x x 0 0 1 1 1	2
x x x x x x x x 0 0 1 1 1 1	3
x x x x x x x 0 0 1 1 1 1 1	8
x x x x x x x x x x x 1 1 0	10
x x x x x x x x x x 1 1 0 0	5
x x x x x x x x x 1 1 0 0 0	6
x x x x x x x x 1 1 0 0 0 0	7
x x x x x x x 1 1 0 0 0 0 0	9
x x x x x x 1 1 0 0 0 0 0 0	11

NOTES
1 "x" is a don't-care bit. (default value is meaningless)
2 This table shall be used in the case where DSV at the end of modulation code is –2

Table 6 – Priority of modulation code selection (end DSV = +2)

Modulation codes	Priority
x x x x x x x x x x x 1 1 0	4
x x x x x x x x x x 1 1 0 0	1
x x x x x x x x x 1 1 0 0 0	2
x x x x x x x x 1 1 0 0 0 0	3
x x x x x x x 1 1 0 0 0 0 0	8
x x x x x x x x x x x 0 0 1	10
x x x x x x x x x x 0 0 1 1	5
x x x x x x x x x 0 0 1 1 1	6
x x x x x x x x 0 0 1 1 1 1	7
x x x x x x x 0 0 1 1 1 1 1	9
x x x x x x 0 0 1 1 1 1 1 1	11

NOTES
1 "x" is a don't-care bit. (default value is meaningless).
2 This table shall be used in the case where DSV at the end of modulation code is +2.

The recorded data rate (for the scanner configuration defined in 5.6) and shortest recorded wavelength are given in table 7, provided for reference only.

Table 7 – Data rate and wavelength

Parameter	1080/59.94i 720/59.94p system	1080/50i 1080/25p system	1080/24p system	1080/23.98p system
Total average data rate	322.97 Mb/s	269.41 Mb/s	258.64 Mb/s	258.38 Mb/s
Instantaneous channel data rate	82.2 Mb/s	68.5 Mb/s	65.7 Mb/s	65.7 Mb/s
Shortest recorded wavelength	0.59 µm	0.59 µm	0.59 µm	0.59 µm

6.6 Magnetization

6.6.1 Polarity

Reproduction of the tape record shall be without regard to the polarity of the recorded flux on the helical tracks.

6.6.2 Recorded equalization

The record head current applied to a head should generate a constant magnetic flux level within a gap from the lowest recorded frequency (i.e. approximately one-third the Nyquist frequency) to the Nyquist frequency.

6.6.3 Record level

The level of the record head current applied to a head with a gap should be optimized for best reproduced signal-to-noise ratio at the highest constant recorded frequency (i.e. the Nyquist frequency of the channel). Other methods of setting the record level are permitted, providing they achieve the same results.

7 Video interface (informative)

The video signal is compressed in compliance with SMPTE 342M and formatted into the recording stream. Figure D.1 shows the relationship between the recording format (this document) and other format on the recorder. Annex D describes the video interface.

8 Audio data interface (informative)

The audio data interface for serial digital input shall conform to AES3 and for embedded AES3 audio data shall conform to SMPTE 299M.

8.1 Encoding parameters

Figure 15 shows the data flow of sampled audio data for each field rate and data structure for encoded audio data and auxiliary data. Signal processing of the standard is based on the field as shown in figure 16 and the audio data flow shown in figure 15 is classified by the field for convenience.

The digital audio data signal is encoded according to the following parameters:

8.1.1 Sampling

a) The audio sampling frequency is 48.000 kHz and shall be related to the video horizontal frequency as follows:

48 kHz = F_H X 8008 / 5625 (1080/59.94i system);
48 kHz = F_H X 2002 / 1875 (720/59.94p system);
48 kHz = F_H X 128 / 75 (1080/50i system);
48kHz = F_H X 128 / 75 (1080/25p system);
48 kHz = F_H X 16 / 9 (1080/24p system);
48 kHz = F_H X 2002 / 1125 (1080/23.98p system).

b) The resolution of each sample is 20 bits minimum, 24 bits maximum.

c) The coding is two's complement linear PCM.

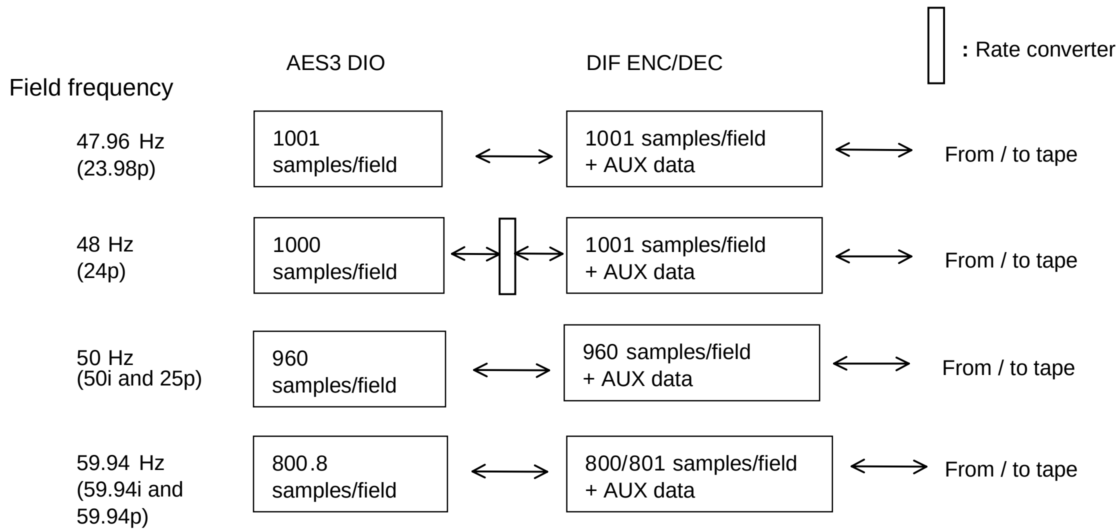


Figure 15 – AES3 audio data flow

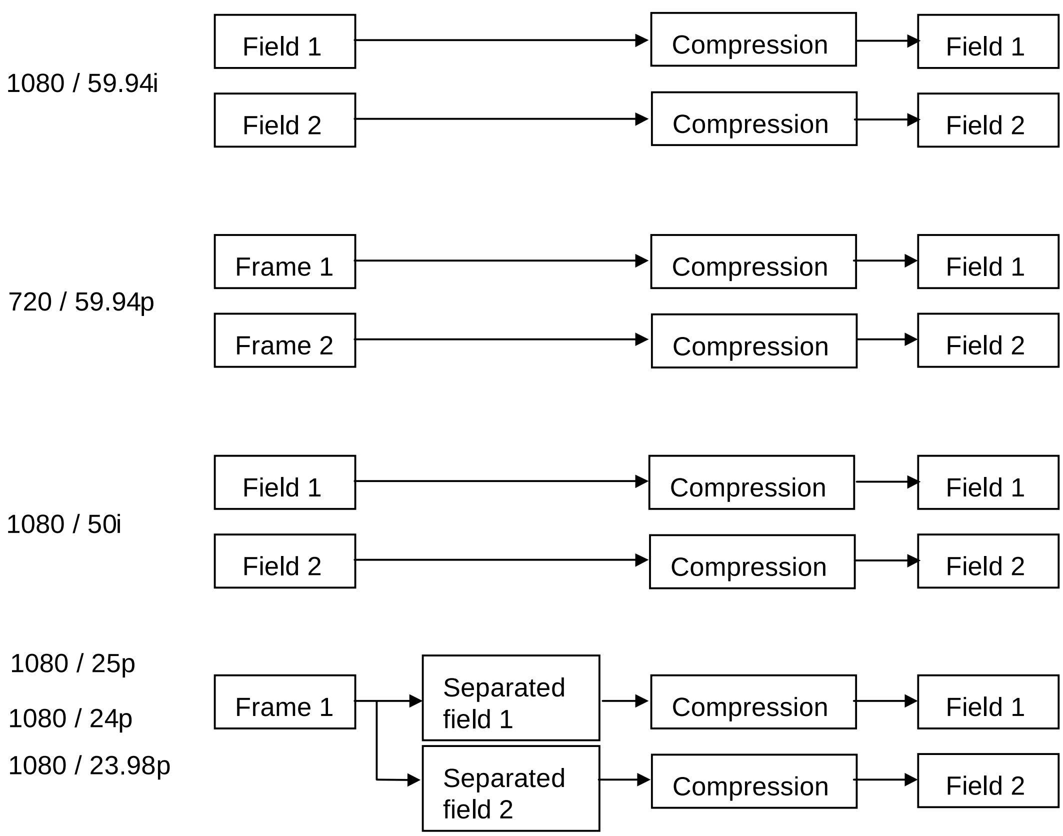


Figure 16 – Relationship between video signal and recorded data (informative)

8.1.2 Reference level

The recommended recorded audio data levels should conform to SMPTE RP 155.

8.2 Digital signal interface

The audio data signal may be input and output digitally in a bit-serial form. The bit-serial interface, if present, shall conform to AES3 without error checking.

9 Compressed video data processing

9.1 Introduction

The purpose of the compressed video processing operation is to transform the HD video compressed data into a form suitable for tape recording.

The HD video compressed data are re-configured and supplemented with the signal format information, and are distributed into 12 compressed video data blocks (4 channels, each channel with 3 compressed video data blocks).

For the data, randomization, column shuffling, outer error correction code addition, and interleaving operations are performed.

The ID is multiplexed with the interleaved data and applied to the Inner error correction coder. A sync word is added to each code block to form a sync block, the smallest data block.

Prior to recording, randomization and 8–14 conversion are performed.

9.2 Recorded data

9.2.1 Reconfiguration of DIF data

The HD compressed video data is composed of 5760 DIF blocks and each DIF block is composed of 85 bytes of data, defined in SMPTE 342M.

Each data D(DN,BN) of DIF blocks are reconfigured into a matrix as data P(S,L,H) (Where S=0, 1, 2, 3, ;L = 0, 1, ..., 254; H = 0, 1, ..., 959) as shown in figure 17.

The rule of reconfiguration is described as:

$$S = (85 \times DN + BN) \bmod 4$$
$$L = (\mathrm{int}((85 \times DN + BN) / 4)) \bmod 255$$
$$H = 8 \times ((\mathrm{int}(DN/12)) \bmod 120) + 2 \times (\mathrm{int}(DN/1\,440)) + \mathrm{int}(S/3)$$

where DN: DIF block number (DN = 0, 1, ..., 5759)

BN: Byte location number in DIF block (BN = 0, 1, ..., 84)

9.2.2 Signal format information

To identify the signal format, the signal format Information shown in table 8 replaces the following five data. P(0,0,0) and P(1,0,0) are replaced by byte 0 of signal format information. P(3,0,1) is replaced by byte 1; P(1,0,2) is replaced by byte 2; P(3,0,3) is replaced by byte 3 of the signal format information. These data exist at the first part of L = 0.

If the remaining data P(S,0,H) of L=0 is not filled by other data, the rest of P(1,0,H) and P(3,0,H) shall be set to 10_h, and the rest of P(0,0,H) and P(2,0,H) shall be set to 80_h.

Table 8 – Signal format information

	Byte 0	Byte 1	Byte 2	Byte 3
1080/59.94i	21 h	02 h	02 h	20 h
720/59.94p	23 h	01 h	02 h	20 h
1080/50i	24 h	01 h	02 h	20 h
1080/25p	27 h	01 h	02 h	20 h
1080/24p	28 h	01 h	02 h	20 h
1080/23.98p	28 h	02 h	02 h	20 h

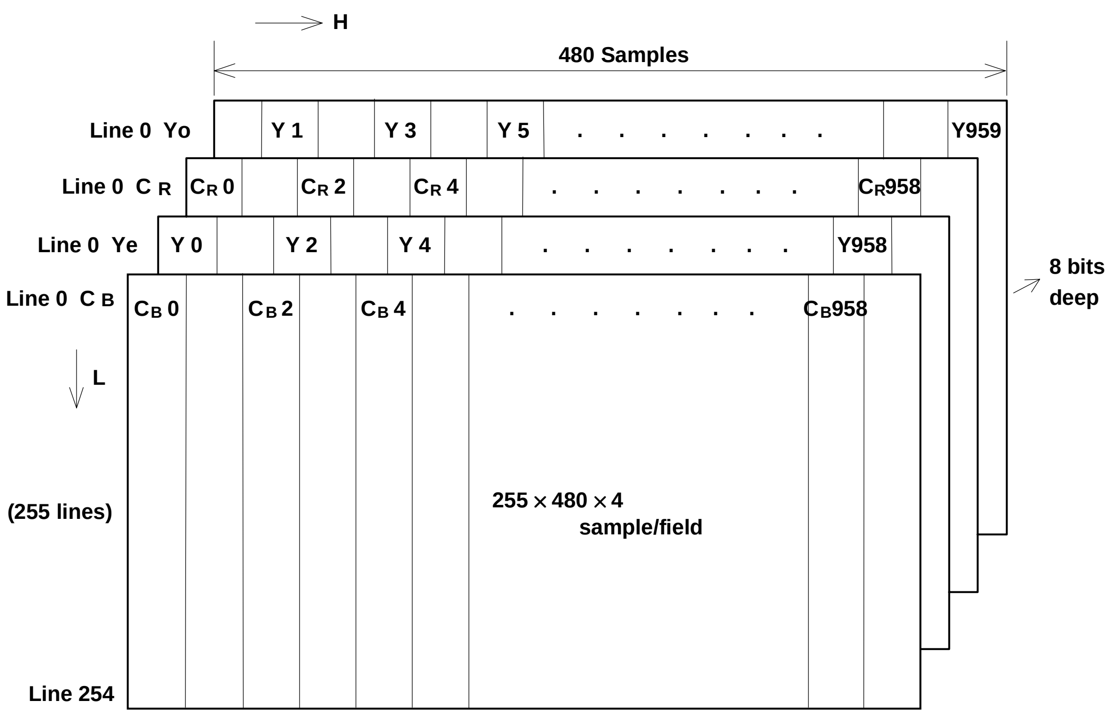


Figure 17 – Reconfigured data

9.3 Channel and compressed video block distribution

The data P(S,L,H) shall be distributed by channel and segment as follows:

The actual index for channel distribution (Ch) and compressed video data block distribution (Vblk) is indicated below:

Ch = {int (H/2)} mod 4,

Vblk = int (H/320)

Spls means the data position of the horizontal direction of figure 18.

Spls = {int (H/8)} mod 40

where

Spls = 0, 1, 2, ... 39

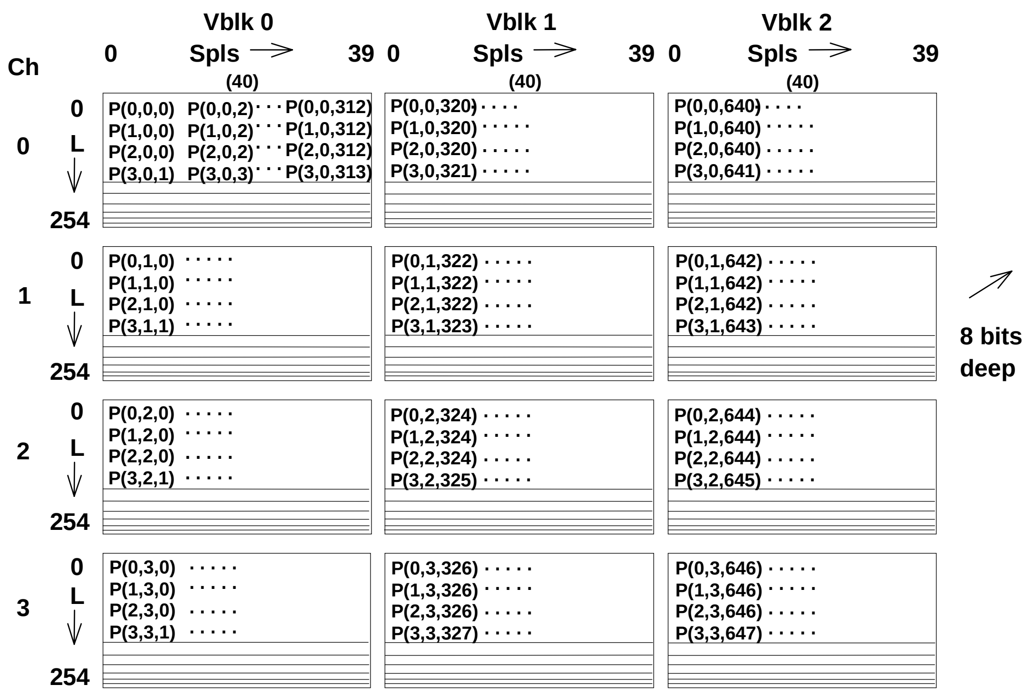


Figure 18 – Channel and compressed video data block distribution

9.4 Word data arrangement

Each data word consists of 8 bits.

Let Oc (= 0, 1, 2, 3) be the outer code number.

Oc = 0: for S=0
Oc = 1: for S=2
Oc = 2: for S=1
Oc = 3: for S=3

Let Splo be the sample number within an outer code block.

Splo = 40 x Vblk + Spls

Splo = 0, 1, ... 119

9.5 Compressed video data randomization

Compressed video data randomization is performed to further reduce the direct current content of the compressed video data stream. It is done prior to the integration of the outer code. Each compressed video data word (byte) is replaced by a new word produced by an exclusive-OR operation between the original word and a random word. The random words are serial-to-parallel converted words (LSB-first order) from the random serial bit stream generated by the following polynomial function:

$x^8 + x^4 + x^3 + x^2 + 1$, (in GF(2))

The random bit stream shall be pre-set to the following value for each outer code block:

M0 = 128 + (L mod 128)

The next word of the random bit stream shall be exclusive-OR operated to the 1st word of the outer code block.

9.6 Outer error protection

Eight rows of each compressed video data field data array contain the error correction check data associated with each column of 8-bit bytes.

Type: Reed-Solomon.
Galois field: GF(256).

Field generator polynomial: $x^8 + x^4 + x^3 + x^2 + 1$,
where x^i are place-keeping variables in GF(2), the binary field.

Order of use: The left-most term is most significant, and oldest in time computationally.

Code Generator Polynomial in GF(256):

G(x) = (x+1)(x+a)(x+a2)(x+a3)(x+a4)(x+a5)(x+a6)(x+a7),

where a is given by 02h in GF(256).

Check characters: $K_7, K_6, K_5, K_4, K_3, K_2, K_1, K_0$ in $K_7x^7 + K_6x^6 + K_5x^5 + K_4x^4 + K_3x^3 + K_2x^2 + K_1x + K_0$ are obtained as the remainder after dividing $x^8D(x)$ by G(x) , where D(x) is the polynomial given by $D(x) = B_{119}x^{119} + B_{118}x^{118} + . . . + B_2x^2 + B_1x + B_0$.

Equation of full code is given by: $B_{119}x^{127} + B_{118}x^{126} + B_{117}x^{125}. . . + B_1x^9 + B_0x^8 + K_7x^7 + K_6x^6 + K_5x^5 + K_4x^4 + K_3x^3 + K_2x^2 + K_1x + K_0$.

9.7 Field data array block

The columns and rows for each field are 1020 and 128 respectively.

The field data array block is shown in figure 19.

Column shuffling is the relocation of the column of the field data array.

The sample number of the data in the outer code block Oc, Splo, is written into the field memory at the coordinates shown below:

Row = Splo

Col = 4 x L + B (Oc)

where B (0) = 0; B (1) = 1; B (2) = 2; B (3) = 3.

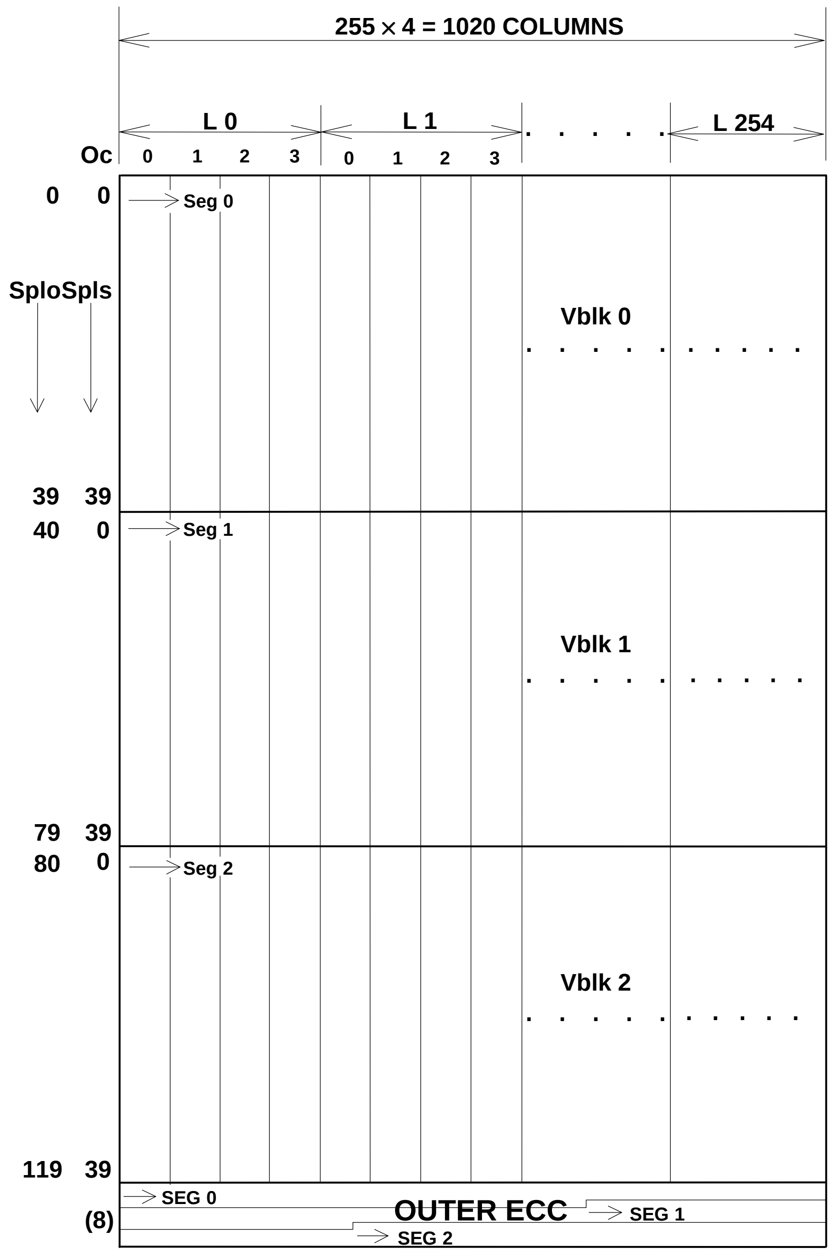


Figure 19 – Field data array block

9.8 Order of transmission to inner coding

The field memory array data is written to tape first by ascending column order, then by ascending row order. Compressed video data bytes and outer check bytes shall be divided into 3 segments. The outer check bytes are written to tape first and followed by data bytes.

Let Seg be the segment number within a compressed video data field:

Seg = 0, 1, 2

Let Fld be the field number within a colour frame:

Fld = 0, 1, 2, 3

The start point address number Xin of the field memory array is as follows:

For the outer check bytes:

Xin = 1440 + 32 x Seg

For the outer data bytes:

Xin = 480 x Seg mod 1440

The relationship between Xin and Row or Col of the field memory is:

Xin = 12 x Row + int (Col/85)

10 AES3 audio data processing

10.1 Introduction

Audio data in each of the eight channels is processed independently and identically into a product block for each channel of dimensions 85 x 4 columns by 8 rows. The audio data samples of each channel are shuffled in a field before the addition of error correction data in the vertical (row) direction. Error correction in the horizontal (column) dimension is common with compressed video data.

Auxiliary words are multiplexed with the audio data in the product block to provide housekeeping in the interface and in processing. Figures 20 (1080/59.94i and 720/59.94p system) and 21 (1080/50i, 1080/25p, 1080/24p and 1080/23.98p system) show the audio data block field array.

10.2 Source coding

Audio data records that meet the requirements of AES3 are formed independently for each of eight AES3 audio data channels, from audio data and ancillary data at the input interface. The data include AES3 audio data, channel status data (C), user data (U), and validity data (V). Parity bits are discarded. The remaining bit positions in the audio data words are reserved (R) for future use. Block sync marks for ancillary data are also processed. CCITT J.17 pre-emphasis is not recognized.

Source data is defined as follows:

a) AES3 audio data:

– Sampling frequency: 48 kHz ± 3 parts in 10^6, synchronous with video

b) Channel status data:

- Bit rate: 48 kbit/s (nominal)
- Word rate: 6 kByte/s
- Word length: 8 bits
- Block length: 192 bits, 24 words
- Coding: See AES3

NOTES

1 Bytes 0 and 1 of AES status data are selected only for special processing in the DVTR. The contents of bytes 0 and 1 are shown in tables 9 and 10, respectively.

2 Bytes 22 and 23 of AES status data contain protection and validity information for bytes 0-21 and may be used in some source decoders.

c) User data:

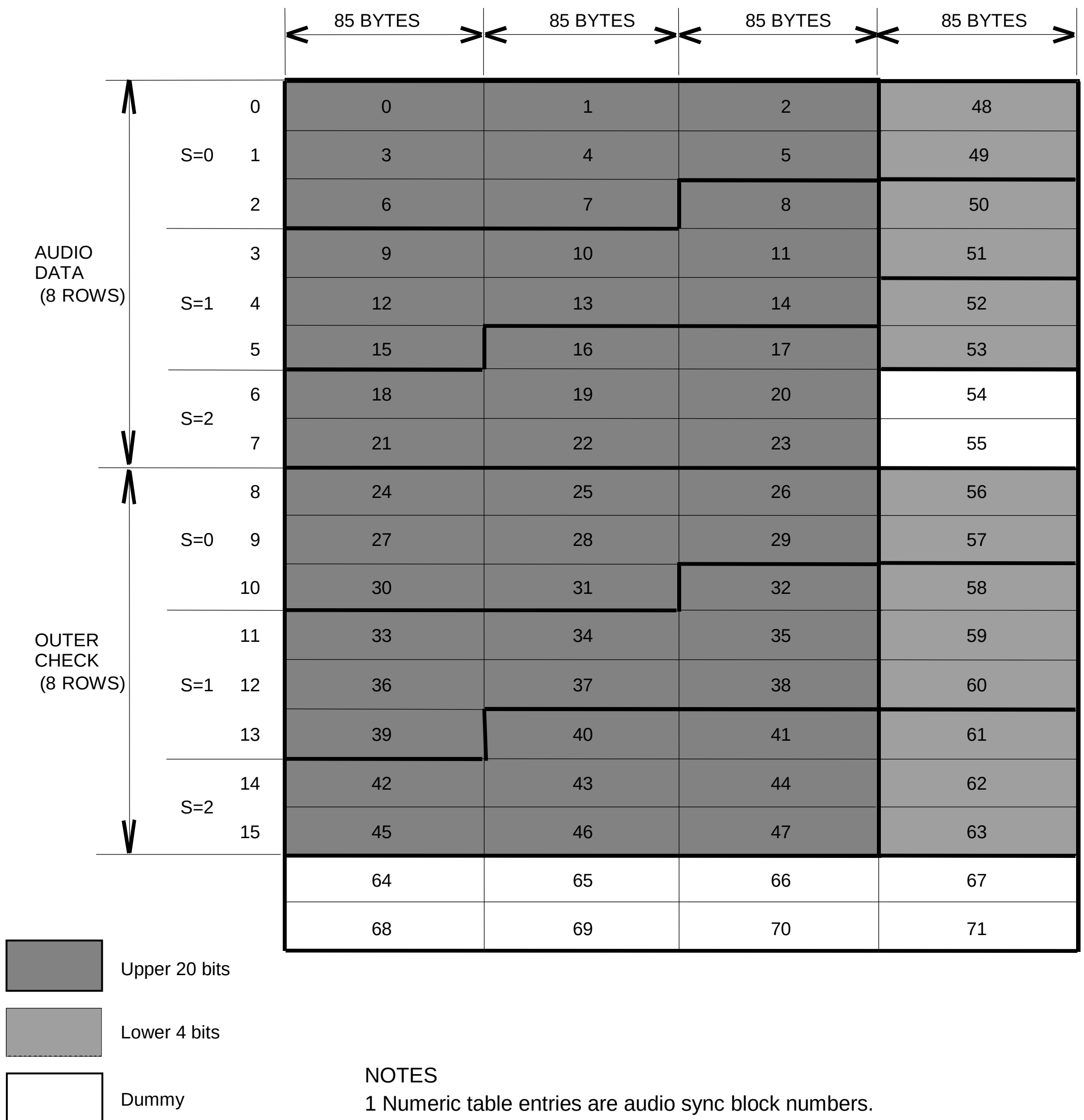
- Bit rate: One bit associated with each audio data word
- Coding: Undefined

d) Validity data:

- Bit rate: One bit associated with each audio data word
- Coding: 0 = sample valid
  1 = sample defective

e) Parity bit:

- Bit rate: One bit associated with each audio data word
- Coding: Even parity of associated word including audio data, status, user, and validity data



NOTES
1 Numeric table entries are audio sync block numbers.
2 S = Segment number (0, 1, 2).

Figure 20 – Audio data block field array (1080/59.94i and 720/59.94p system)

			85 BYTES	85 BYTES	85 BYTES	85 BYTES
AUDIO DATA (10 ROWS)	S=0	0	0	1	2	3
		1	4	5	6	7
		2	8	9	10	11
		3	12	13	14	15
	S=1	4	16	17	18	19
		5	20	21	22	23
		6	24	25	26	27
	S=2	7	28	29	30	31
		8	32	33	34	35
		9	36	37	38	39
OUTER CHECK (8 ROWS)	S=0	10	40	41	42	43
		11	44	45	46	47
		12	48	49	50	51
	S=1	13	52	53	54	55
		14	56	57	58	59
		15	60	61	62	63
	S=2	16	64	65	66	67
		17	68	69	70	71

NOTES
1 Numeric table entries are audio sync block numbers.
2 S = Segment number (0, 1, 2).

Figure 21 – Audio data block field array (1080/50i, 1080/25p, 1080/24p and 1080/23.98p system)

Table 9 – AES status data (Byte 0)

LSB							MSB
0	1	2	3	4	5	6	7

Bit 0: 0 = Consumer use
1 = Professional use
Bit 1: 0 = Audio
1 = Data
Bit 2: Preemphasis 0
Bit 3: Preemphasis 1
Bit 4: Preemphasis 2
Bit 5: 0
Bit 6: Sampling frequency 0
Bit 7: Sampling frequency 1

NOTE – Bits 2, 3, and 4 of this byte are recorded in an auxiliary word.

Table 10 – AES status data (Byte 1)

LSB							MSB
0	1	2	3	4	5	6	7

Bit 0: Channel mode bit 0
Bit 1: Channel mode bit 1
Bit 2: Channel mode bit 2
Bit 3: Channel mode bit 3
Bit 4: Reserved
Bit 5: Reserved
Bit 6: Reserved
Bit 7: Reserved

Mode	0 1 2 3	Definition
0	0 0 0 0	Undefined-2 channel
1	0 0 0 1	2 Channel
2	0 0 1 0	Single channel
3	0 0 1 1	Primary/secondary 2 channel
4	0 1 0 0	Stereophonic
5	0 1 0 1	Reserved
	through	
F	1 1 1 1	Reserved

NOTE – Bits 0, 1, and 3 of this byte are recorded in an auxiliary word.

10.3 Source processing

10.3.1 Introduction

AES3 audio data is processed in fields. Each field contains 801 or 800 AES3 audio data samples (1080/59.94i and 720/59.94p system) or 960 AES3 audio data samples (1080/50i and 25p system) or 1001 AES3 audio data samples (1080/23.98p and 24p system) for an AES3 audio data channel with associated status, user, and validity data. In addition, a number of control and user words are added to the data.

10.3.2 Relative audio video signal timing

An audio data field begins with the audio data sample acquired zero samples (± 20 sample periods) before the first preequalizing pulse of the vertical interval of the analog input video signal. For digital input video signal a corresponding point (mark) to analog input is chosen as the beginning of the sampled audio field. That point depends on a relevant system line number (different for interlaced or progressive system) and status of the F and V bits on the digital interface.

Audio signal timing relative to video signal timing at the output interface during playback shall be the same (temporal skew is equal to zero) as it was at the input interface

10.3.3 Audio data in fields

Audio data in fields is processed into an audio data block of 85 x 6 x 12 bytes, each corresponding to 12 audio data sectors on tape. The data portion of the block is 85 x 30 bytes and the outer error check bytes portion of the block is also 85 x 32 bytes (1080/59.94i and 720/59.94p system). The data portion of the block is 85 x 4 x 10 bytes and the outer error check bytes portion of the block is also 85 x 4 x 8 bytes (1080/23.98p and 24p system and 1080/50i and 25p system).

AES3 audio data words:

> 801 or 800 words (1080/59.94i and 720/59.94p system) or 960 words (1080/50i and 25p system) or 1001 words (1080/23.98p and 24p system — see note in 6.3.3.d) with associated C, U, V, R bits (20 bits total per word).

Auxiliary data words:

> 15 words (20 bits per word) + 170 words (8 bits per word) + 219 words (4 bits per word) (1080/59.94i and 720/59.94p system); 160 words (24 bits per word) + 40 words (8 bits per word) (1080/50i and 25p system); 119 words (24 bits per word) + 40 words (8 bits per word) (1080/23.98p and 24p system).

10.3.4 Intrafield shuffling

The audio data for each channel in each field is shuffled. The intrafield shuffling process operates identically for all fields.

For 1080/59.94i and 720/59.94p system

For upper 20 bits data:

Let Col be the column number within an audio data field:

> Col = 0, 1, . . . , 115.

Let Row be the row number within an audio data field:

> Row = 0, 1, . . . , 15

Rows 8 to 15 contain the error correction data.

Let Oblk be the data block number:

$$Oblk = 3 \times Row + int(Col / 34)$$

The data block array for upper 20 bits is shown in figures 22. Then sample number Smp within an audio data field is obtained according to the following formula:

$$Smp = 24 \times (Col \bmod 34) + int(Oblk / 8) + 3 \times (Oblk \bmod 8)$$

When Smp is larger than 800, Smp = 801, 802, ..., 815 are replaced by AUX 0, AUX 1, ..., AUX 14, respectively.

For lower 4 bits data.

Let Col be the column number within an audio data field:

Col = 0, 1, ..., 169.

Let Row be the row number within an audio data field:

Row = 0, 1, ..., 15

Row 8 to 15 contain the error correction data.

The data block array for lower 4 bits is shown in figures 23. Then sample number Smp within a lower 4 bits audio data field is obtained according to the following formula:

$$Smp = 6 \times (col - 2\, int(Row / 2)) + 3 \times (Row \bmod 2) + int (Row/2).$$

(Lower 4 bits)

When Smp is larger than 800, Smp = 801, 802, . . . , 815 are replaced by AUX 0, AUX 1, . . . , AUX 14. When Smp is smaller than 0, Smp is replaced by AUX 219 + Smp respectively.

For 1080/50i; 1080/23.98p, 1080/24p and 1080/25p system.

Let Col be the column number within an audio data field:

Col = 0, 1, . . . , 115.

Let Row be the row number within an audio data field:

Row = 0, 1, . . . , 15

Rows 8 to 15 contain the error correction data.

Let Oblk be the data block number:

$$Oblk = 4 \times Row + int(Col / 29) \text{ (Upper 20 bits)}$$

The data block arrays are shown in figures 24 (1080/50i and 25p system) and figure 25 (1080/23.98p and 1080/24p system).

Then sample number Smp within an audio data field is obtained according to the following formula:

$$Smp = 40 \times (Col \bmod 29) + int(Oblk / 14) + 3 \times (Oblk \bmod 14) \quad (0 \le Oblk \le 26).$$

$$Smp = 40 \times (Col \bmod 29) + 2 \times int(Oblk / 27) + 3 \times (Oblk \bmod 27) \quad (27 \le Oblk \le 39).$$

When Smp is larger than 959, Smp = 960, 961, ..., 1159 are replaced by AUX 0, AUX 1, ..., AUX 158, respectively, for the 1080/50i and 25p system; When Smp is larger than 959, Smp = 960, 961, ..., 1159 are replaced by AUX 0, AUX 1, ..., AUX 199, respectively, for 1080/23.98p and 24p system).

Figures 22 and 23 (1080/59.94i and 720/59.94p system), 24 (1080/50i and 25p system) and 25 (1080/23.98p and 1080/24p system) show the layout of the shuffled samples in a field array. Outer ECC codes are situated at Row = 8 to 15 for 1080/59.94i and 720/59.94p system and Row = 10 to 19 for 1080/50i, 1080/23.98p, 1080/24p and 25p system.

10.3.5 Block shuffling

The block shuffling process operates after the intrafield shuffling identically for all fields. Let N be the recording order of the data block in an audio data sector:

N = 0, 1, 2, 3

Let Seg be the segment number:

Seg = 0, 1, 2

Let T be the track number:

T = 0, 1, 2, 3

Then the data block Oblk within a field array is mapped according to the following formula:

Oblk = N' + T' + 8 x Seg + 2 x (12-T') x (N' mod 2) (1080/59.94i and 720/59.94p system)
Oblk = N' + T' + 8 x Seg + 2 X (16-T') x (N' mod 2) (1080/50i and 25p system)

where

N' = N + 4 x int(T/2)
T' = T mod 2

Figure 26 shows the data block arrangement of an audio data channel in three groups of sectors for the 1080/59.94i and 720/59.94p system. Figure 27 shows the data block arrangement of an audio data channel in three groups of sectors for the 1080/50i, 1080/23.98p, 24p and 25p system.

10.3.6 Audio data word processing

Input data are formed into words of 24 bits in the sequence:

a) Assignment of the 24-bit word to audio data and associated data is controlled by user input (see table 11 (1080/59.94i and 720/59.94p) and 12 (1080/50i, 1080/23.98p, 24p and 25p system)).

The most significant bit of the audio data word is bit 23 and unused bits of lower significance are removed. The auxiliary word LNGH (four bits) signals the word mode selected.

b) Each group of 24-bit words is divided into 8-bit bytes as shown in figures 28 (1080/59.94i and 720/59.94p system) and 29 (1080/50i, 1080/23.98p, and 24p and 25p system) and arranged alternately by the MSB and the LSB of the first word of the word group.

c) Each group is distributed into the product block in accordance with figures 22 and 23 (1080/59.94i and 720/59.94p system), figure 24 (1080/50i and 25p system) and figure 25 (1080/23.98p and 24p system)

d) For the 1080/59.94i and 720/59.94p system, every fifth field shall contain 800 samples. All other fields shall contain 801 samples. The 5-field sequence of the number of audio data samples begins at an arbitrarily chosen field. Continuity of the 5-field sequence shall be preserved throughout the recording, including editing. The 5-field sequence is indicated by the value of the auxiliary word FNCT, as defined in 10.4.5. Furthermore, every fifth field of 800 samples is identified by the field address AF2 for audio data sync blocks, as defined in 6.3.3.

		Upper 20 bits																						
		85bytes (34 words)							85bytes (34 words)								85bytes (34 words)							
		0	1	2	3		32	33	34	35	36	37		66	67	68	69	70	71		100	101
AUDIO DATA 8 bytes	0	0	24	48	72	.....	768	792	3	27	51	75	.....	771	795	6	30	54	78	.....	774	798
	1	9	33	57	81	.....	777	AUX 0	12	36	60	84	.....	780	AUX 3	15	39	63	87	.....	783	AUX 6
	2	18	42	66	90	.....	786	AUX 9	21	45	69	93	.....	789	AUX 12	1	25	49	73	.....	769	793
	3	4	28	52	76	.....	772	796	7	31	55	79	.....	775	799	10	34	58	82	.....	778	AUX 1
	4	13	37	61	85	.....	781	AUX 4	16	40	64	88	.....	784	AUX 7	19	43	67	91	.....	787	AUX 10
	5	22	46	70	94	.....	790	AUX 13	2	26	50	74	.....	770	794	5	29	53	77	.....	773	797
	6	8	32	56	80	.....	776	800	11	35	59	83	.....	779	AUX 2	14	38	62	86	.....	782	AUX 5
	7	17	41	65	89	.....	785	AUX 8	20	44	68	92	.....	788	AUX 11	23	47	71	95	.....	791	AUX 14
OUTER CHECK 8 bytes	8	PV0	PV0	PV0	PV0	.....	PV0	PV0	PV0	PV0	PV0	PV0	.....	PV0	PV0	PV0	PV0	PV0	PV0	.....	PV0	PV0
	9	PV1	PV1	PV1	PV1	.....	PV1	PV1	PV1	PV1	PV1	PV1	.....	PV1	PV1	PV1	PV1	PV1	PV1	.....	PV1	PV1
	10	PV2	PV2	PV2	PV2	.....	PV2	PV2	PV2	PV2	PV2	PV2	.....	PV2	PV2	PV2	PV2	PV2	PV2	.....	PV2	PV2
	11	PV3	PV3	PV3	PV3	.....	PV3	PV3	PV3	PV3	PV3	PV3	.....	PV3	PV3	PV3	PV3	PV3	PV3	.....	PV3	PV3
	12	PV4	PV4	PV4	PV4	.....	PV4	PV4	PV4	PV4	PV4	PV4	.....	PV4	PV4	PV4	PV4	PV4	PV4	.....	PV4	PV4
	13	PV5	PV5	PV5	PV5	.....	PV5	PV5	PV5	PV5	PV5	PV5	.....	PV5	PV5	PV5	PV5	PV5	PV5	.....	PV5	PV5
	14	PV6	PV6	PV6	PV6	.....	PV6	PV6	PV6	PV6	PV6	PV6	.....	PV6	PV6	PV6	PV6	PV6	PV6	.....	PV6	PV6
	15	PV7	PV7	PV7	PV7	.....	PV7	PV7	PV7	PV7	PV7	PV7	.....	PV7	PV7	PV7	PV7	PV7	PV7	.....	PV7	PV7

	Lower 4 bits				
	85bytes				
	0	1		168	169
0–7	See figure 28				
8	PV0	PV0	.....	PV0	PV0
9	PV1	PV1	.....	PV1	PV1
10	PV2	PV2	.....	PV2	PV2
11	PV3	PV3	.....	PV3	PV3
12	PV4	PV4	.....	PV4	PV4
13	PV5	PV5	.....	PV5	PV5
14	PV6		.....	PV6	
15	PV7		.....	PV7	

NOTES

1 Numeric table entries are audio sample numbers.

2 PV0 to PV7 represent outer check corresponding to audio data of each column.

Figure 22 – Audio data block layout – upper 20 bits (1080/59.94i and 720/59.94p system)

	0	1	2	3	4	5		132	133	134	135	136	137	138	139		168	169
0	0	6	12	18	24	30	.....	792	798	AUX 3	AUX 9	AUX 15	AUX 21	AUX 27	AUX 33	.....	AUX 207	AUX 213
1	3	9	15	21	27	33	.....	795	AUX 0	AUX 6	AUX 12	AUX 18	AUX 24	AUX 30	AUX 36	.....	AUX 210	AUX 216
2	AUX 208	AUX 214	1	7	13	19	.....	781	787	793	799	AUX 4	AUX 10	AUX 16	AUX 22	.....	AUX 196	AUX 202
3	AUX 211	AUX 217	4	10	16	22	.....	784	790	796	AUX 1	AUX 7	AUX 13	AUX 19	AUX 25	.....	AUX 199	AUX 205
4	AUX 197	AUX 203	AUX 209	AUX 215	2	8	.....	770	776	782	788	794	800	AUX 5	AUX 11	.....	AUX 185	AUX 191
5	AUX 200	AUX 206	AUX 212	AUX 218	5	11	.....	773	779	785	791	797	AUX 2	AUX 8	AUX 14	.....	AUX 188	AUX 194
6	AUX 219		AUX 220		AUX 221		.....	AUX 285		AUX 286		AUX 287		AUX 288		.....	AUX 303	
7	AUX 304		AUX 305		AUX 306		.....	AUX 370		AUX 371		AUX 372		AUX 373		.....	AUX 388	

Figure 23 – Audio data block layout – lower 4 bits (1080/59.94i and 720/59.94p system)

		85bytes								85bytes							
		0	1		23	24	25		28	29	30		52	53	54		57
	0	0	40	.....	920	AUX 0	AUX 40		AUX 160	3	43	.....	923	AUX 3	AUX 43		AUX 163
	1	12	52	.....	972	AUX 12	AUX 52	.....	AUX 172	15	55	.....	935	AUX 15	AUX 55	.....	AUX 175
	2	24	64	.....	944	AUX 24	AUX 64	.....	AUX 184	27	67	.....	947	AUX 27	AUX 67	.....	AUX 187
AUDIO DATA 10 bytes	3	36	76	.....	956	AUX 36	AUX 76	.....	AUX 196	39	79	.....	959	AUX 39	AUX 79	.....	AUX 199
	4	7	47	.....	927	AUX 7	AUX 47	.....	AUX 167	10	50	.....	930	AUX 10	AUX 50	.....	AUX 170
	5	19	59	.....	939	AUX 19	AUX 59	.....	AUX 179	22	62	.....	942	AUX 22	AUX 62	.....	AUX 182
	6	31	71	.....	951	AUX 31	AUX 71	.....	AUX 191	34	74	.....	954	AUX 34	AUX 74	.....	AUX 194
	7	5	45	.....	925	AUX 5	AUX 45	.....	AUX 165	8	48	.....	928	AUX 8	AUX 48	.....	AUX 168
	8	17	57	.....	937	AUX 17	AUX 57	.....	AUX 177	20	60	.....	940	AUX 20	AUX 60	.....	AUX 180
	9	29	69	.....	949	AUX 29	AUX 69	.....	AUX 189	32	72	.....	952	AUX 32	AUX 72	.....	AUX 192
	10	PV0	PV0	.....	PV0	PV0	PV0	.....	PV0	PV0	PV0	.....	PV0	PV0	PV0	.....	PV0
	11	PV1	PV1	.....	PV1	PV1	PV1	.....	PV1	PV1	PV1	.....	PV1	PV1	PV1	.....	PV1
	12	PV2	PV2	.....	PV2	PV2	PV2	.....	PV2	PV2	PV2	.....	PV2	PV2	PV2	.....	PV2
OUTER CHECK W bytes	13	PV3	PV3	.....	PV3	PV3	PV3	.....	PV3	PV3	PV3	.....	PV3	PV3	PV3	.....	PV3
	14	PV4	PV4	.....	PV4	PV4	PV4	.....	PV4	PV4	PV4	.....	PV4	PV4	PV4	.....	PV4
	15	PV5	PV5	.....	PV5	PV5	PV5	.....	PV5	PV5	PV5	.....	PV5	PV5	PV5	.....	PV5
	16	PV6	PV6	.....	PV6	PV6	PV6	.....	PV6	PV6	PV6	.....	PV6	PV6	PV6	.....	PV6
	17	PV7	PV7	.....	PV7	PV7	PV7	.....	PV7	PV7	PV7	.....	PV7	PV7	PV7	.....	PV7

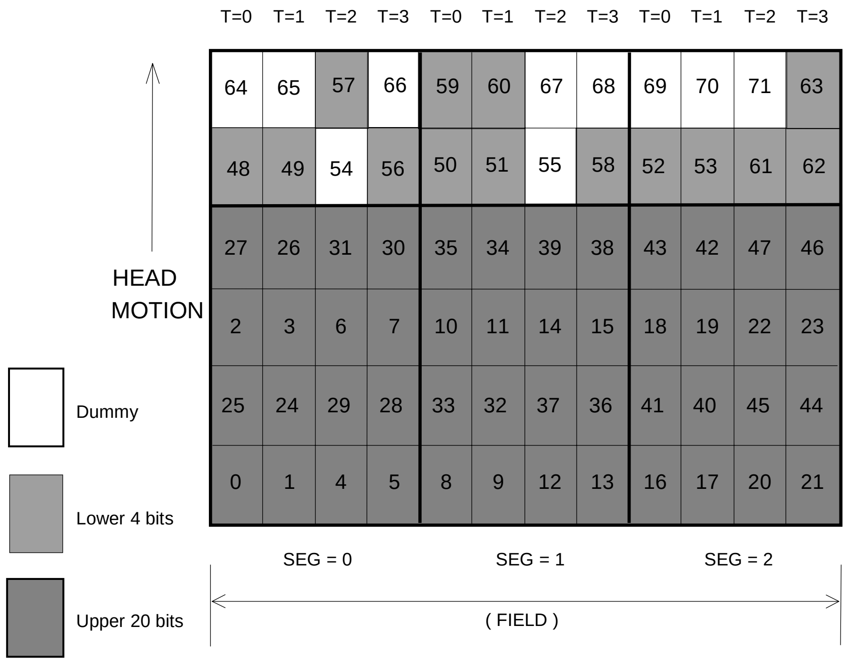
		85bytes								85bytes							
		58	59		81	82	83		86	87	88		110	111	122		125
	0	6	46	.....	926	AUX 6	AUX 46		AUX 166	9	49	.....	929	AUX 9	AUX 49		AUX 169
	1	18	58	.....	938	AUX 18	AUX 58	.....	AUX 178	21	61	.....	941	AUX 21	AUX 61	.....	AUX 181
	2	30	70	.....	950	AUX 30	AUX 70	.....	AUX 190	33	73	.....	953	AUX 33	AUX 73	.....	AUX 193
AUDIO DATA 10 bytes	3	1	41	.....	921	AUX 1	AUX 41	.....	AUX 161	4	44	.....	924	AUX 4	AUX 44	.....	AUX 164
	4	13	53	.....	933	AUX 13	AUX 53	.....	AUX 173	16	56	.....	936	AUX 16	AUX 56	.....	AUX 176
	5	25	65	.....	945	AUX 25	AUX 65	.....	AUX 185	28	68	.....	948	AUX 28	AUX 68	.....	AUX 188
	6	37	77	.....	957	AUX 37	AUX 77	.....	AUX 197	2	42	.....	922	AUX 2	AUX 42	.....	AUX 162
	7	11	51	.....	931	AUX 11	AUX 51	.....	AUX 171	14	54	.....	934	AUX 14	AUX 54	.....	AUX 174
	8	23	63	.....	943	AUX 23	AUX 63	.....	AUX 183	26	66	.....	946	AUX 26	AUX 66	.....	AUX 186
	9	35	75	.....	955	AUX 35	AUX 75	.....	AUX 195	38	78	.....	958	AUX 38	AUX 78	.....	AUX 198
	10	PV0	PV0	.....	PV0	PV0	PV0	.....	PV0	PV0	PV0	.....	PV0	PV0	PV0	.....	PV0
	11	PV1	PV1	.....	PV1	PV1	PV1	.....	PV1	PV1	PV1	.....	PV1	PV1	PV1	.....	PV1
	12	PV2	PV2	.....	PV2	PV2	PV2	.....	PV2	PV2	PV2	.....	PV2	PV2	PV2	.....	PV2
OUTER CHECK W bytes	13	PV3	PV3	.....	PV3	PV3	PV3	.....	PV3	PV3	PV3	.....	PV3	PV3	PV3	.....	PV3
	14	PV4	PV4	.....	PV4	PV4	PV4	.....	PV4	PV4	PV4	.....	PV4	PV4	PV4	.....	PV4
	15	PV5	PV5	.....	PV5	PV5	PV5	.....	PV5	PV5	PV5	.....	PV5	PV5	PV5	.....	PV5
	16	PV6	PV6	.....	PV6	PV6	PV6	.....	PV6	PV6	PV6	.....	PV6	PV6	PV6	.....	PV6
	17	PV7	PV7	.....	PV7	PV7	PV7	.....	PV7	PV7	PV7	.....	PV7	PV7	PV7	.....	PV7

Figure 24 – Audio data block layout (1080/50i and 25p system)

		85bytes									85bytes								
		0	1		24	25	26	27	28		29	30		53	54	55	56	57	
	0	0	40	.....	960	1000	AUX 39	AUX 79	AUX 119		3	43	.....	963	AUX 2	AUX 42	AUX 82	AUX 122	
	1	12	52	.....	972	AUX 11	AUX 51	AUX 91	AUX 131		15	55	.....	975	AUX 14	AUX 54	AUX 94	AUX 134	
	2	24	64	.....	984	AUX 23	AUX 63	AUX 103	AUX 143		27	67	.....	987	AUX 26	AUX 66	AUX 106	AUX 146	
AUDIO DATA 10 bytes	3	36	76	.....	996	AUX 35	AUX 75	AUX 115	AUX 155		39	79	.....	999	AUX 38	AUX 78	AUX 118	AUX 158	
	4	7	47	.....	967	AUX 6	AUX 46	AUX 86	AUX 126		10	50	.....	970	AUX 9	AUX 49	AUX 89	AUX 129	
	5	19	59	.....	979	AUX 18	AUX 58	AUX 98	AUX 138		22	62	.....	982	AUX 21	AUX 61	AUX 101	AUX 141	
	6	31	71	.....	991	AUX 30	AUX 70	AUX 110	AUX 150		34	74	.....	994	AUX 33	AUX 73	AUX 113	AUX 153	
	7	5	45	.....	965	AUX 4	AUX 44	AUX 84	AUX 124		8	48	.....	968	AUX 7	AUX 47	AUX 87	AUX 127	
	8	17	57	.....	977	AUX 16	AUX 56	AUX 96	AUX 136		20	60	.....	980	AUX 19	AUX 59	AUX 99	AUX 139	
	9	29	69	.....	989	AUX 28	AUX 68	AUX 108	AUX 148		32	72	.....	992	AUX 31	AUX 71	AUX 111	AUX 151	
	10	PV0	PV0	.....	PV0	PV0	PV0	PV0	PV0		PV0	PV0	.....	PV0	PV0	PV0	PV0	PV0	
	11	PV1	PV1	.....	PV1	PV1	PV1	PV1	PV1		PV1	PV1	.....	PV1	PV1	PV1	PV1	PV1	
	12	PV2	PV2	.....	PV2	PV2	PV2	PV2	PV2		PV2	PV2	.....	PV2	PV2	PV2	PV2	PV2	
OUTER CHECK W bytes	13	PV3	PV3	.....	PV3	PV3	PV3	PV3	PV3		PV3	PV3	.....	PV3	PV3	PV3	PV3	PV3	
	14	PV4	PV4	.....	PV4	PV4	PV4	PV4	PV4		PV4	PV4	.....	PV4	PV4	PV4	PV4	PV4	
	15	PV5	PV5	.....	PV5	PV5	PV5	PV5	PV5		PV5	PV5	.....	PV5	PV5	PV5	PV5	PV5	
	16	PV6	PV6	.....	PV6	PV6	PV6	PV6	PV6		PV6	PV6	.....	PV6	PV6	PV6	PV6	PV6	
	17	PV7	PV7	.....	PV7	PV7	PV7	PV7	PV7		PV7	PV7	.....	PV7	PV7	PV7	PV7	PV7	

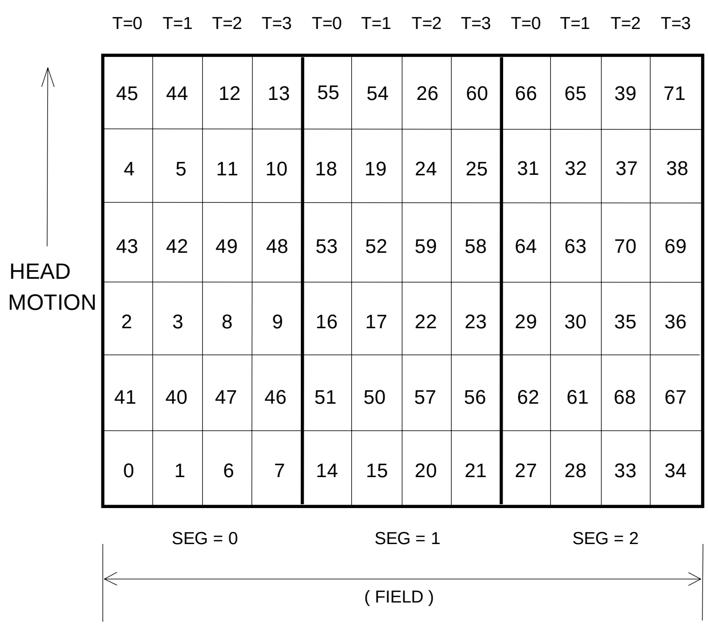
		85bytes								85bytes								
		58	59		82	83	84	85	86	87	88		121	122	123	124	125	
	0	6	46	.....	966	AUX 5	AUX 45	AUX 85	AUX 125	9	49	.....	969	AUX 8	AUX 48	AUX 88	AUX 128	
	1	18	58	.....	978	AUX 17	AUX 57	AUX 97	AUX 137	21	61	.....	981	AUX 20	AUX 60	AUX 100	AUX 140	
	2	30	70	.....	990	AUX 29	AUX 69	AUX 109	AUX 149	33	73	.....	993	AUX 32	AUX 72	AUX 112	AUX 152	
AUDIO DATA 10 bytes	3	1	41	.....	961	AUX 0	AUX 40	AUX 80	AUX 120	4	44	.....	964	AUX 3	AUX 43	AUX 83	AUX 123	
	4	13	53	.....	973	AUX 12	AUX 52	AUX 92	AUX 132	16	56	.....	976	AUX 15	AUX 55	AUX 95	AUX 135	
	5	25	65	.....	985	AUX 24	AUX 64	AUX 104	AUX 144	28	68	.....	988	AUX 27	AUX 67	AUX 107	AUX 147	
	6	37	77	.....	997	AUX 36	AUX 76	AUX 116	AUX 156	2	42	.....	962	AUX 1	AUX 41	AUX 81	AUX 121	
	7	11	51	.....	971	AUX 10	AUX 50	AUX 90	AUX 130	14	54	.....	974	AUX 13	AUX 53	AUX 93	AUX 133	
	8	23	63	.....	983	AUX 22	AUX 62	AUX 102	AUX 142	26	66	.....	986	AUX 25	AUX 65	AUX 105	AUX 145	
	9	35	75	.....	995	AUX 34	AUX 74	AUX 114	AUX 154	38	78	.....	998	AUX 37	AUX 77	AUX 117	AUX 157	
	10	PV0	PV0	.....	PV0	PV0	PV0	PV0	PV0	PV0	PV0	.....	PV0	PV0	PV0	PV0	PV0	
	11	PV1	PV1	.....	PV1	PV1	PV1	PV1	PV1	PV1	PV1	.....	PV1	PV1	PV1	PV1	PV1	
	12	PV2	PV2	.....	PV2	PV2	PV2	PV2	PV2	PV2	PV2	.....	PV2	PV2	PV2	PV2	PV2	
OUTER CHECK W bytes	13	PV3	PV3	.....	PV3	PV3	PV3	PV3	PV3	PV3	PV3	.....	PV3	PV3	PV3	PV3	PV3	
	14	PV4	PV4	.....	PV4	PV4	PV4	PV4	PV4	PV4	PV4	.....	PV4	PV4	PV4	PV4	PV4	
	15	PV5	PV5	.....	PV5	PV5	PV5	PV5	PV5	PV5	PV5	.....	PV5	PV5	PV5	PV5	PV5	
	16	PV6	PV6	.....	PV6	PV6	PV6	PV6	PV6	PV6	PV6	.....	PV6	PV6	PV6	PV6	PV6	
	17	PV7	PV7	.....	PV7	PV7	PV7	PV7	PV7	PV7	PV7	.....	PV7	PV7	PV7	PV7	PV7	

Figure 25 – Audio data block layout (1080/23.98p and 1080/24p system)



NOTES
1 Numeric entries are audio sync block numbers.
2 S = segment number (0, 1, 2).
3 T = track number (0, 1, 2, 3,).

Figure 26 – Audio data block arrangement (1080/59.94i and 720/59.94p system)



NOTES
1 Numeric entries are audio sync block numbers.
2 S = segment number (0, 1, 2).
3 T = track number (0, 1, 2, 3,).

Figure 27 – Audio data block arrangement (1080/50i, 1080/25p, 1080/23.98p and 1080/24p system)

Table 11 – Audio data word mode (1080/59.94i and 720/59.94p)

Word Mode	Bit 0-3	4	5	6	7	8-23
0 (0001)	Audio 0-3	C	U	V	R	Audio 4-20
1 (0011)	Audio 0-3	C	U	V	Audio 4	Audio 5-21
2 (0101)	Audio 0-3	C	V	Audio 4	Audio 5	Audio 6-22
3 (0111)	Audio 0-3	C	U	Audio 4	Audio 5	Audio 6-22
4 (1001)	Audio 0-3	C	Audio 4	Audio 5	Audio 6	Audio 7-23
5 (1011)	Audio 0-3	V	Audio 4	Audio 5	Audio 6	Audio 7-23
6 (1101)	Audio 0-3	U	Audio 4	Audio 5	Audio 6	Audio 7-23
7 (1111)	Audio 0-3	Audio 4	Audio 5	Audio 6	Audio 7	Audio 8-23

NOTES

1 Example, “audio 1” represents bit 1 of audio sample.

2 C = channel status bit, U = user bit, V = validity bit, R = reserved bit.

3 Audio data will be rounded from the 20-bit length of the interface word (auxiliary data truncated) to the length above with the elimination of the least significant bit(s).

4 Modes 0, 3, and 7 are the recommended modes for general use.

Table 12 – Audio data word mode (1080/50i, 1080/25p, 1080/23.98p and 1080/24p system)

Word Mode	Bit 0-3	4	5	6	7	8-23
0 (0000)	Audio 0-3	C	U	V	R	Audio 4-20
1 (0010)	Audio 0-3	C	U	V	Audio 4	Audio 5-21
2 (0100)	Audio 0-3	C	V	Audio 4	Audio 5	Audio 6-22
3 (0110)	Audio 0-3	C	U	Audio 4	Audio 5	Audio 6-22
4 (1000)	Audio 0-3	C	Audio 4	Audio 5	Audio 6	Audio 7-23
5 (1010)	Audio 0-3	V	Audio 4	Audio 5	Audio 6	Audio 7-23
6 (1100)	Audio 0-3	U	Audio 4	Audio 5	Audio 6	Audio 7-23
7 (1110)	Audio 0-3	Audio 4	Audio 5	Audio 6	Audio 7	Audio 8-23

NOTES

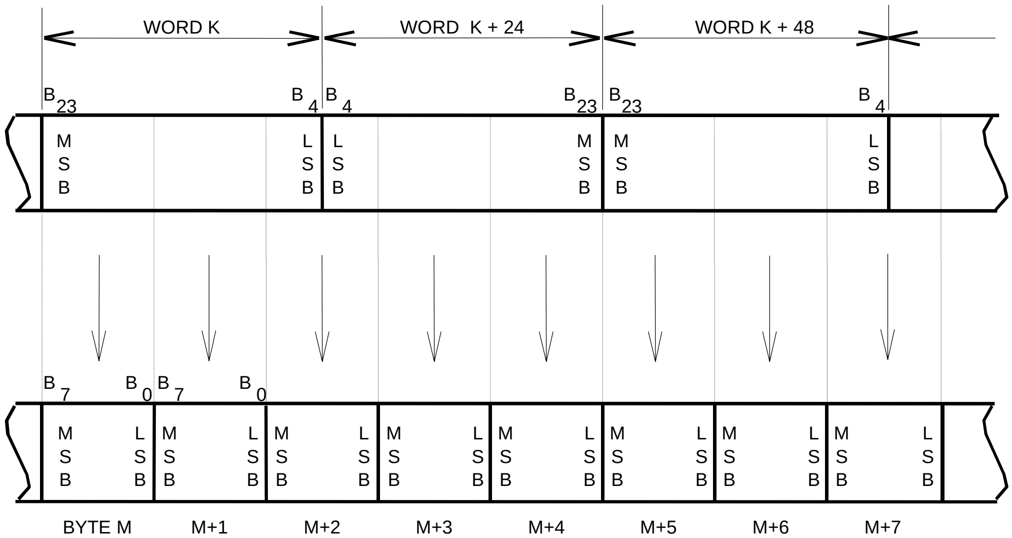
1 Example, “audio 1” represents bit 1 of audio sample.

2 C = channel status bit, U = user bit, V = validity bit, R = reserved bit.

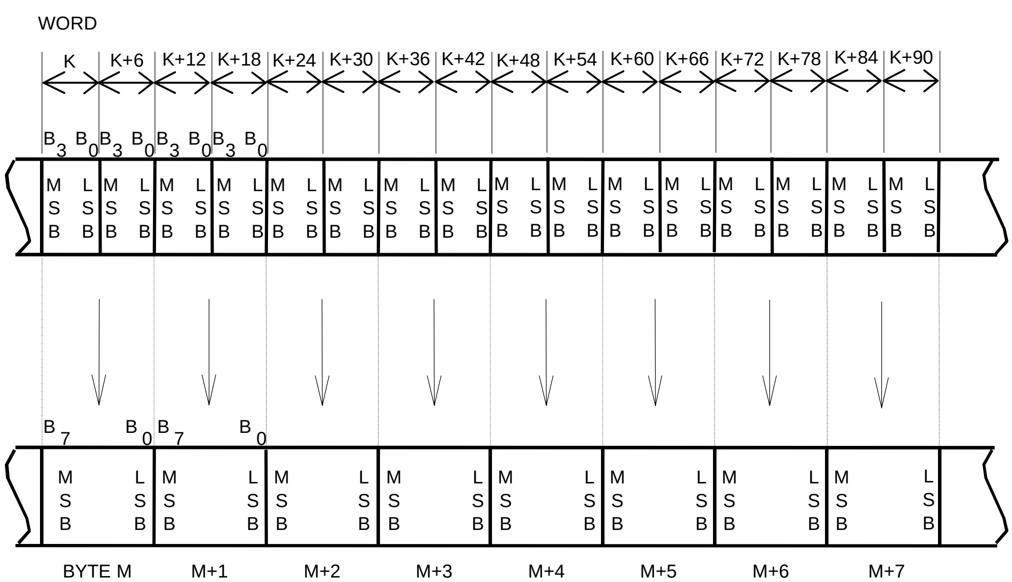
3 Audio data will be rounded from the 20-bit length of the interface word (auxiliary data truncated) to the length above with the elimination of the least significant bit(s).

4 Modes 0, 3, and 7 are the recommended modes for general use.

Upper 20 bits

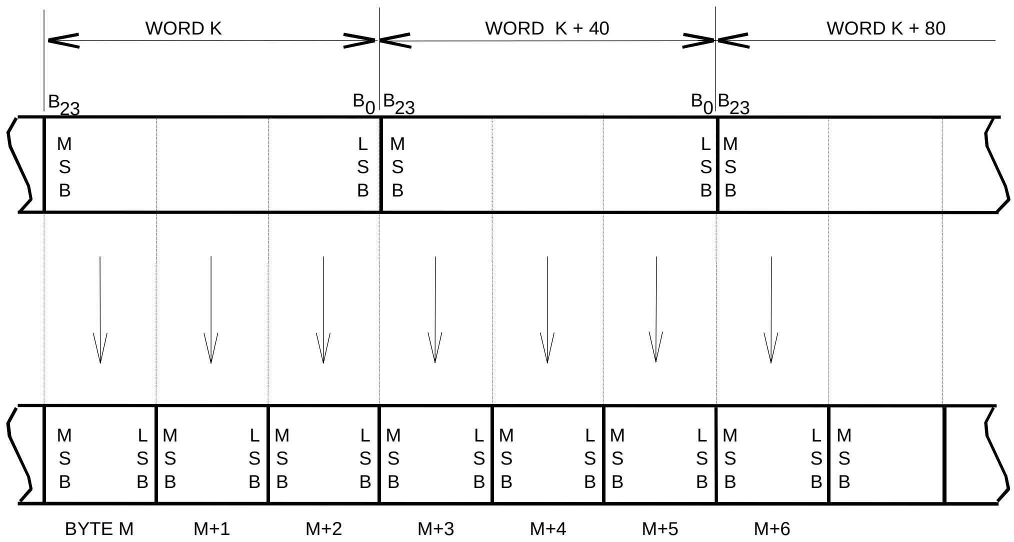


Lower 4 bits



NOTE - K = 0, 9, 18, 4, 13, 22, 8, and 17 in figure 22.

Figure 28 – Digital audio data word to byte conversion (1080/59.94i nd 720/59.94p system)



NOTE - K = 0,12, 24, 36, 7, 19, 31, 5, 17 and 29 in figures 24 and 25.

Figure 29 – Digital audio data word to byte conversion (1080/50i, 1080/25p, 1080/24p and 1080/23.98p system)

10.4 Auxiliary words

Auxiliary words are generated at the input interface from incoming data or user selection and serve to signal this information to the output interface. Auxiliary words are five words of four bits plus one word of one bit and one word of eight bits as defined in figures 30 (1080/59.94i and 720/59.94psystem) and 31 (1080/50i and 25p system) and 32 (1080/24p and 1080/23.98p system). The word EFLG is written four times in each audio data block.

Figures 30 (1080/59.94i and 720/59.94psystem) and 31 (1080/50i and 25p system) and 32 (1080/24p and 1080/23.98p system) show the format of the auxiliary words in the audio data block.

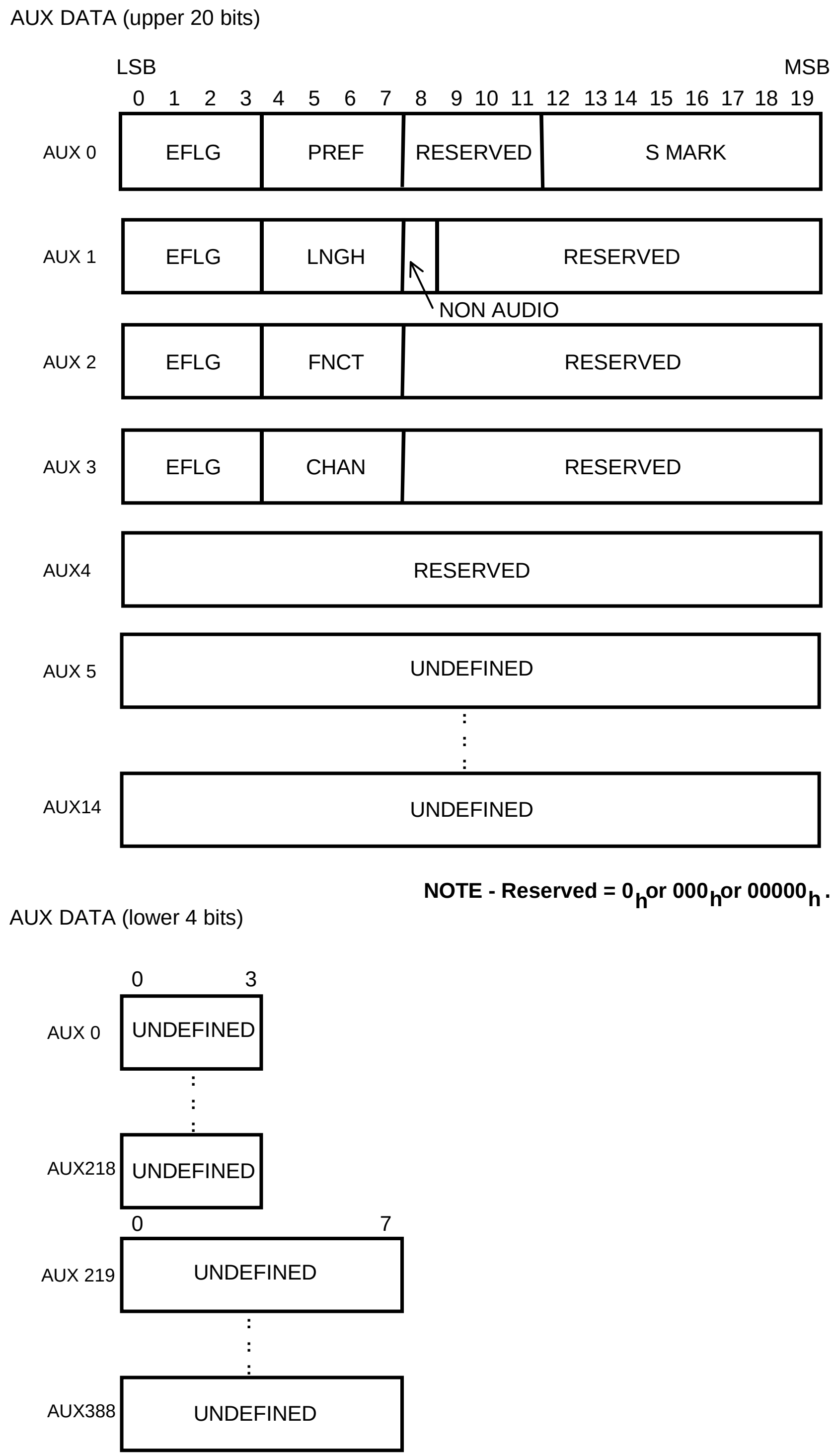
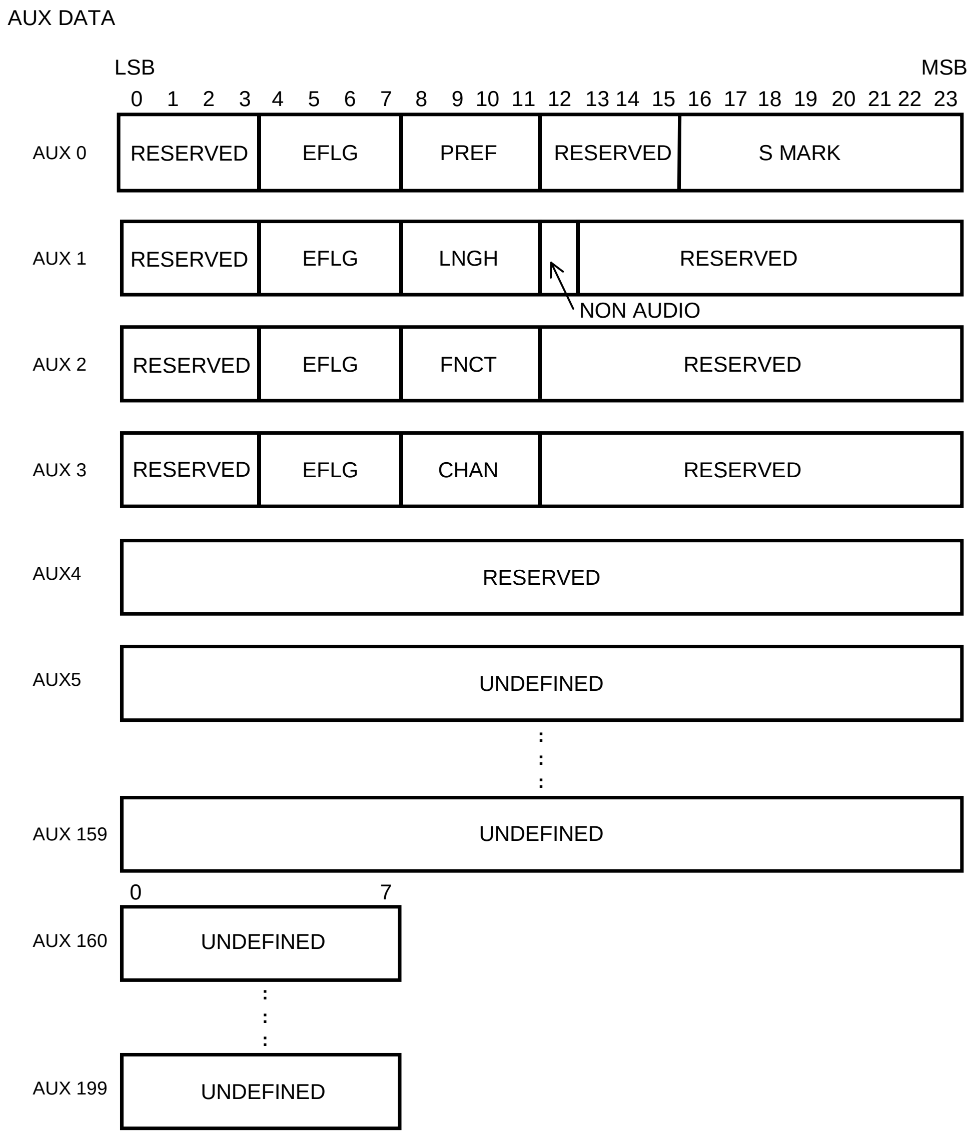
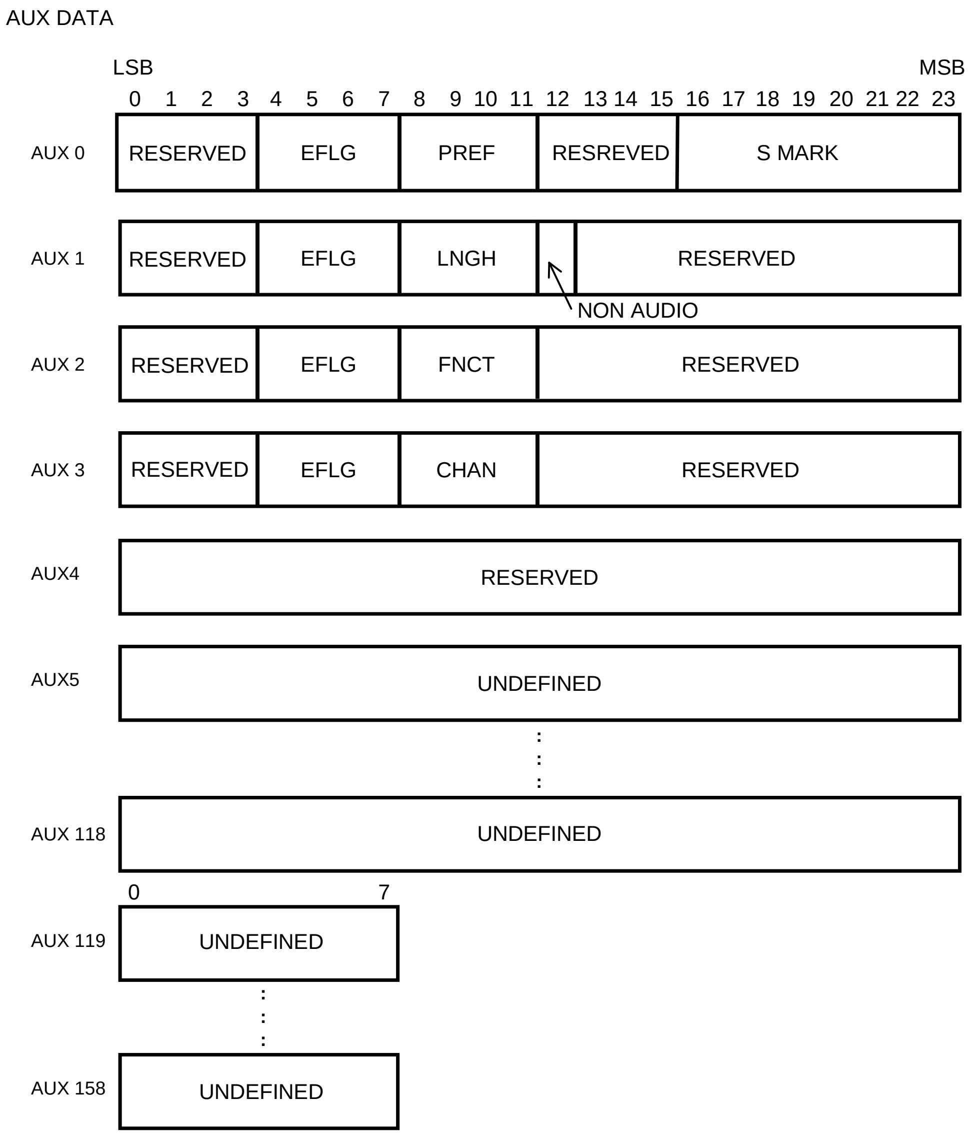


Figure 30 – Audio data block auxiliary data (1080/59.94i and 720/59.94p system)



NOTE - Reserved = 0_h or 000_h or 000000_h .

Figure 31 – Audio data block auxiliary data (1080/50i and 25p system)



NOTE - Reserved = 0_h or 000_h or 000000_h .

Figure 32 – Audio data block auxiliary data (1080/24p and 1080/23.98p system)

10.4.1 Channel use (CHAN)

This word is four bits and specifies the usage of the two input channels in an interface data stream. CHAN is derived from channel status byte 1. CHAN is inserted in bits 4-7 (1080/59.94i and 720/59.94p system) or bits 8-11 (1080/50i, 1080/23.98p, 24p, 25p system) of AUX 3. (See table 13, figures 30, 31 and 32.)

LSB — MSB

0	1	2	3	4	5	6	7	Channel Status
↓	↓	↓	↓					(AES3 Byte 1)
0	1	2	3					CHAN

Bit 0: Channel mode bit 0
Bit 1: Channel mode bit 1
Bit 2: Channel mode bit 2
Bit 3: Channel mode bit 3

Table 13 – Channel use control word

Mode	CHAN bit 0 1 2 3	Value
0	0 0 0 0	2 Channel-default
1	0 0 0 1	2 Channel
2	0 0 1 0	Single channel
3	0 0 1 1	Primary/secondary 2 channel
4	0 1 0 0	Stereophonic
5	0 1 0 1	Undefined
	through	
F	1 1 1 1	Undefined

10.4.2 Preemphasis (PREF)

This word is four bits and specifies the usage of preemphasis in the audio data coding. PREF is derived from channel status byte 0. PREF is inserted in bits 4-7 (1080/59.94i and 720/59.94p system) or bits 8-11 (1080/50i, 1080/23.98p, 24p, 25p system) of AUX 0 (see table 14, figures 30, 31 and 32).

LSB — MSB

0	1	2	3	4	5	6	7	Channel status
		↓	↓	↓	↓			(AES Byte 0)
		0	1	2	3			PREF

Bit 0: Preemphasis bit 0
Bit 1: Preemphasis bit 1
Bit 2: Preemphasis bit 2
Bit 3: 0

Table 14 - Preemphasis control word

Mode	PREF bit 0 1 2	Value
0	0 0 0	Preemphasis off - (default)
1	0 0 1	Reserved
2	0 1 0	Reserved
3	0 1 1	Reserved
4	1 0 0	Preemphasis off
5	1 0 1	Reserved
6	1 1 0	50/15 microsecond
7	1 1 1	Reserved

10.4.3 Audio data word mode (LNGH)

This word is four bits and specifies the audio data word length and the usage of the ancillary bits status, user, and validity. LNGH is derived from user control inputs and inserted in bits 4-7 (1080/59.94i and 720/59.94p system) or bits 8-11 (1080/50i, 1080/23.98p, 24p, 25p system) of AUX 1 (see table 15, figures 30, 31 and 32).

LSB			MSB	
0	1	2	3	LNGH

Bit 0: 0
Bit 1: LNGH 1 (LSB)
Bit 2: LNGH 2
Bit 3: LNGH 3 (MSB)

Table 15 – Word mode control word

Mode	LNGH bit 3 2 1	Audio data Length	Ancillary bits C U V R
0	0 0 0	20 bits	X X X X
1	0 0 1	21 bits	X X X –
2	0 1 0	22 bits	X – X –
3	0 1 1	22 bits	X X – –
4	1 0 0	23 bits	X – – –
5	1 0 1	23 bits	– – X –
6	1 1 0	23 bits	– X – –
7	1 1 1	24 bits	– – – –
NOTE – "X" means the ancillary bit is recorded.			

10.4.4 Block sync location (S MARK)

S MARK is an 8-bit word. S MARK specifies the location of the block sync associated with channel status and user data, as defined in AES3-1992. S MARK contains the word count, in the current block, of the first block sync detected; i.e., the word address in the block pointing to the first sample after the block sync mark.

LSB							MSB	
0	1	2	3	4	5	6	7	S MARK

where S MARK is from 00_h to BF_h inclusive.

S MARK = FF_h if no mark is found within the defined range.

S MARK is inserted in bits 12-19 (1080/59.94i and 720/59.94p system) or bits 16-23 (1080/50i, 1080/23.98p, 24p, 25p system) of AUX 0 (see figures 30, 31,and 32).

10.4.5 Field number count (FNCT)

In the 1080/59.94i and 720/59.94p system, this word is four bits and specifies the number of audio samples in the current field. FNCT is inserted in bits 4-7 (1080/59.94i and 720/59.94p system) or bits 8-11 (1080/50i, 1080/23.98p, 24p, 25p system) of AUX 2 (see table 16, figures 30, 31, and 32).

LSB		MSB		
0	1	2	3	FNCT

Bit 0: FNCT 0 (LSB)
Bit 1: FNCT 1
Bit 2: FNCT 2 (MSB)
Bit 3: 0

Table 16 – FNCT mode

Number of samples	FNCT bit 2 1 0
801	0 0 0
801	0 0 1
801	0 1 0
801	0 1 1
800	1 0 0

10.4.6 Edit flag (EFLG)

This word is four bits and specifies the field associated with an edit transition. EFLG is inserted in bits 0-3 (1080/59.94i and 720/59.94p system) or bits 4-7 (1080/50i, 1080/23.98p, 24p, 25p system) of AUX 0, AUX 1, AUX 2, and AUX 3 (see figures 30, 31 and 32).

LSB			MSB	
0	1	2	3	EFLG

EFLG = D_h for the first field of the edit
EFLG = 7_h for the last field of the edit
EFLG = 0_h otherwise

10.4.7 Non-audio flag (NON AUDIO)

This word is one bit and specifies whether the data is audio or non-audio (data). NON AUDIO is inserted in bit 8 (1080/59.94i and 720/59.94p system) or bit 12 (1080/50i, 1080/23.98p, 24p, 25p system) of AUX 1 (see figures 30, 31 and 32).

NON AUDIO = 0 for audio
NON AUDIO = 1 for non audio data

10.5 Outer error protection

Rows 8 through 15 of the data block, as shown in figures 22 (1080/59.94i and 720/59.94psystem) and 24 (1080/50i and 25p system) and 25 (1080/23.98p and 24p system), contain the error check bytes associated with each column.

Type: Reed-Solomon.
Galois field: GF(256).

Field generator polynomial:

$$x^8 + x^4 + x^3 + x^2 + 1,$$

where x^i are place-keeping variables in GF(2), the binary field.

Order of use: The left-most term is the most significant, "oldest" in time computationally, and written first to tape.

Code generator polynomial:

$$G(x) = (x+1)(x+a)(x+a^2)(x+a^3)(x+a^4)(x+a^5)(x+a^6)(x+a^7),$$

where a is given by 02_h in GF(256).

Check characters : K_7, K_6, K_5, K_4, K_3, K_2, K_1, K_0 (also identified respectively as PV_7, PV_6, PV_5, PV_4, PV_3, PV_2, PV_1, PV_0) in $K_7x^7 + K_6x^6 + K_5x^5 + K_4x^4 + K_3x^3 + K_2x^2 + K_1x + K_0$ are obtained as the remainder after dividing the polynomial $x^8D(x)$ by G(x) , where D(x) is the polynomial given by

$$D(x) = B_7x^7 + B_6x^6 + B_5x^5 + \ldots + B_2x^2 + B_1x + B_0 .$$

Polynomial of full code :

$$B_7x^{15} + B_6x^{14} + B_5x^{13} + \ldots + B_1x^9 + B_0x^8 + K_7x^7 + K_6x^6 + \ldots + K_2x^2 + K_1x + K_0 .$$

Outer-code check characters in each column of the 85 x 4 x 8 blocks are calculated using the data order existing prior to the rearrangement into the pattern shown in figures 22 (1080/59.94i and 720/59.94psystem) and 24 (1080/50i and 25p system) and 25 (1080/23.98p and 24p system); i.e., in ascending sample order.

The check characters K_7 through K_0 are used as the vertical protection characters identified as PV_7 through PV_0, respectively.

10.6 Inner protection

The inner protection and sync block formats are identical to those for compressed video data (see 6.3 and 6.4).

10.7 Order of transmission to inner coding

Audio data bytes (outer check bytes considered as data) are sent to the inner coder after the block shuffling.

10.8 Channel code

The channel code is identical to that for compressed video data (see 6.5).

10.9 Allocation of audio data sectors

The data blocks of an audio data channel are arranged in three groups of four sectors (12 sectors) as shown in figure 26 (1080/59.94i and 720/59.94p system) and 27 (1080/50i, 1080/25p, 1080/24p, and 1080/23.98p system). A group of six sectors from each of the eight audio data channels is recorded according to figures 33. Audio data sectors labeled Ac1 to Ac8 correspond to audio data input channels from one to eight, respectively.

The allocation of a group of sectors is a four-field sequence. The field address AF_0, AF_1 of the sector ID of four audio data sync blocks is defined in 6.3.3.

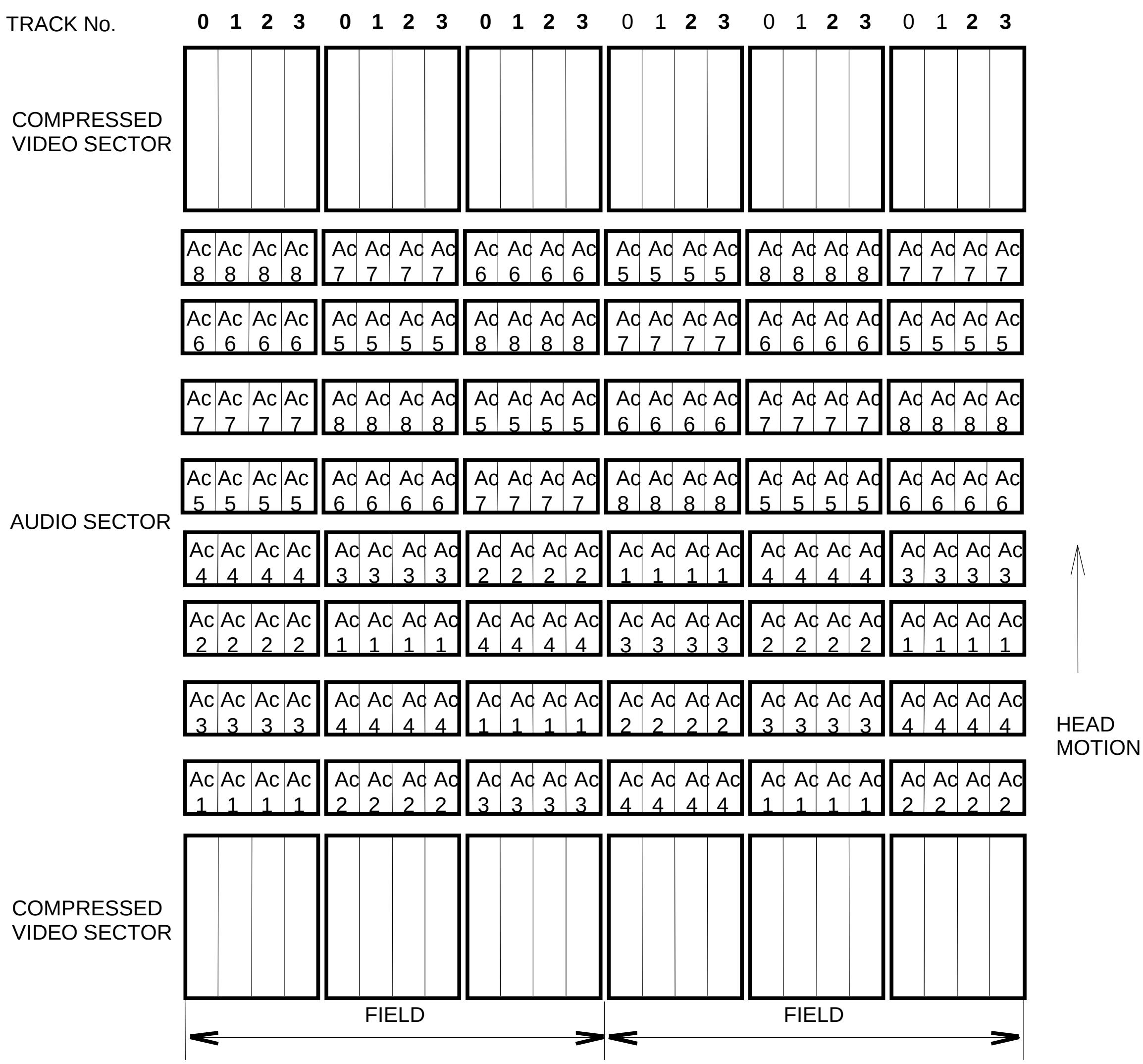


Figure 33 – Audio data channel arrangement

11 Longitudinal tracks

11.1 Relative timing

11.1.1 Time and control code input

An external time and control code input signal that meets the specifications described in SMPTE 12M, or a time and control code that is internally generated within the recorder, shall be timed for recording in a following way. The relationship between the "start of address" of the time and control code and the program reference point of a track with an even-field address (count) for the compressed video data, is as defined by figure 4 and table 1.

Time code signal timing relative to video signal timing at the output interface during playback shall be the same (temporal skew is equal to zero) as it was at the input interface during recording.

11.1.2 Time and control code information

The time and control code information shall refer to the video frame during which it is recorded (see 6.1)

11.1.3 Cue information

Cue information shall be recorded on the tape at a point referenced to the associated video information as defined by dimension P2 of figure 4, and table 1.

11.1.4 Control track servo pulse

Control track servo pulse record timing is described in 11.2.

11.2 Control track

11.2.1 Method of recording

The control track shall be recorded using the hysteresis (direct recording) method.

11.2.2 Servo reference pulse

The control track servo reference pulse, at the time of recording, shall be a series of pulses with a period of 11.122 ms ± 6 µs as shown in figure 34 (59.94i and 720/59.94p system), 13.333 ms ± 6 µs as shown in figure 35 (1080/50i and 25p system), 13.903 ms ± 6 µs as shown in figure 36 (1080/24p system) or 13.889 ms ± 6 µs as shown in figure 36 (1080/23.98p system).

11.2.3 Flux polarity

The polarities of the recorded flux shall be as shown in figure 4.

11.2.4 Flux level

The recording shall attenuate any previous recording by at least 30 dB.

11.2.5 Pulse width

The recorded pulses shall have periods of 3T, 4T, 5T, 6T or 7T where T equals to 1.1122 ms nominal (1080/59.94i and 720/59.94p system), 1.3333 ms nominal (1080/50i and 25p system), 1.3903 ms nominal (1080/24p system) or 1.3889 ms nominal (1080/23.98p system). The rise and fall times of the record current (10% to 90% points) shall be less than 150 µs.

11.2.6 Servo reference pulse timing

The servo reference pulses and the data of the program reference point, when recorded according to figure 4, shall occur at the same time.

11.2.7 Color frame pulse

A color frame sequence at the time of the start of each recording shall be indicated by a pulse rising transition point which follows a sequence of 6T-4T duration pulses. The color frame commences with color frame A field 1. It shall be located at the rising point after the 6T-4T duration pulses, coinciding with a segment count and a field count of zero in the compressed video data sector identification pattern, as defined in 6.3.3.

11.2.8 Video frame pulse

The first segment of a compressed video data frame at the time of the start of each recording shall be indicated by a pulse rising transition point, which follows a sequence of 6T-4T or 4T-6T duration pulses. It shall be located at the rising points after the 6T-4T or 4T-6T duration pulses, coinciding with a segment count and an even field count of zero in the compressed video data sector identification pattern, as defined in 6.3.3.

11.2.9 Number of audio data channels identification

Eight audio data channels recording shall be indicated by a sequence of 3T-7T pulses. These shall be located after the 6T-4T or 4T-6T duration pulses[1)] (see figures 34, 35 and 36).

NOTE – The sequence of 3T-7T pulses is unique to eight audio data tracks recording and may be used as a method for detection and differentiation of a HD-D5 recording with 4 audio data tracks.

11.3 Cue record

11.3.1 Recording method

The signals shall be recorded using the anhysteresis (ac bias) method.

11.3.2 Flux level

The recorded reference audio level shall correspond to an rms magnetic short circuit flux level of 125 nWb/m ± 3 nWb/m of track width at 1000 Hz.

11.4 Time and control code record

11.4.1 Recording method

The signals shall be recorded using the anhysteresis (ac bias) recording method.

11.4.2 Flux level

The recorded peak-to-peak flux shall correspond to a magnetic short circuit flux level of 250 nWb/m ± 20 nWb/m of track width.

11.4.3 Input signal

The signal recorded on this track shall be in accordance with SMPTE 12M.

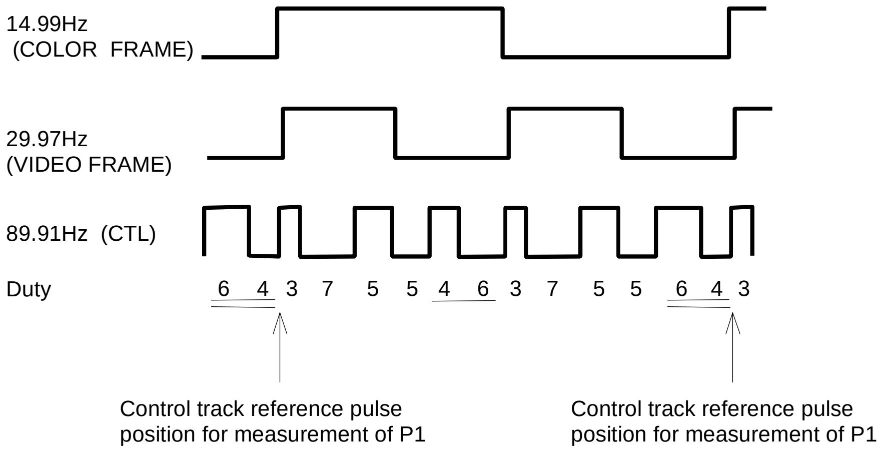


Figure 34 – Recorded control record waveform timing (1080/59.94i and 720/59.94p system)

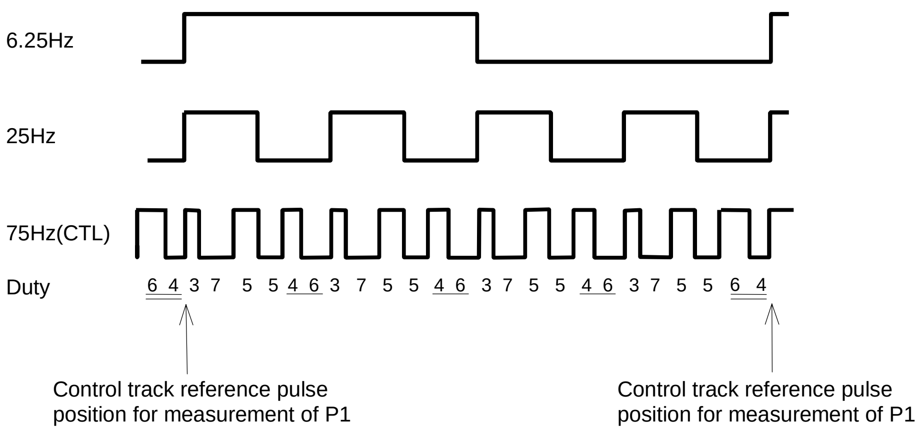


Figure 35 – Recorded control record waveform timing (1080/50i and 25p system)

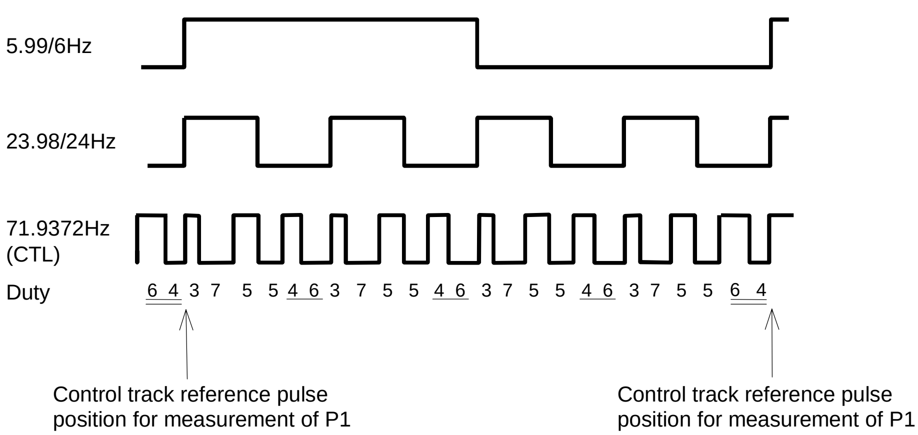


Figure 36 – Recorded control record waveform timing (1080/23.98p and 1080/24p system)

Annex A (normative)
Tape tension

The value measured with a tension monitor on the entrance side of the scanner may vary among manufacturers, but would typically be 0.31 N ± 0.05 N.

Annex B (normative)
Cross-tape track measurement technique

The cross-tape measuring technique utilizes the fact that all tracks of a helical-scan video recording, recorded by the same head at constant tape speed, have the same longitudinal track pitch, the same track angle, and the same track curvature.

From a ferrofluid development, measurements are made of the actual track positions and the distance between a minimum of 200 control track pitches. All measurements shall be made under the environmental conditions described in 3.1, except that the measurements are made without tape tension (see table B.1). The tape is then mathematically stretched to account for tape tension (see figure B.2). The theoretical track position is calculated from the corrected longitudinal track pitch and the theoretical track angle. The track location error is calculated as the difference between the theoretical track position and the actual track position (see table B.1 and figure B.3).

Track location error, which is expressed by the lower edge error of the tracks, includes track angle errors, track straightness errors, and track pitch errors. The starting point for calculations and measurements is, for example, the cross point of the lower edge of the track containing the program reference point and the line along the measurement path in figure B.2. The values for every eighth track are the errors for tolerance zone one. Shifting one track, the second tolerance zone may be measured and so on. It is not necessary to measure all tracks; a suitable number may be 20 samples per zone. A plot of the track location error against the track number must be computed (see figure B.3). The peak-to-peak value shall lie within the tolerance zones specified in 5.3.

Table B.1 – Nomenclature and calculation of track location error

		1080/59.94i, 720/59.94p, 1080/50i, 1080/25p 1080/23.98p system	1080/24p system
Y_0	Program area reference (basic)	1.639 mm	1.634 mm
θ	Track angle (basic)	4.9384°	
T	Tension	0.31 N	
E	Young's modulus	8 000 N/mm²	
A	Cross sectional area	Thickness × Width	
CTM	Distance of n control track pitches without tape tension		
CTM'	Distance of n control track pitches with tape tension	CTM' = CTM(1+ T/(A × E))	
g	Longitudinal track pitch	g= CTM'/4n	
i	Track number, i = 0 for track containing reference point		
Y_i	Measured position of track i at the recorded pattern		
ΔY	Cross section track pitch	$\Delta Y = g \times \tan\theta$	
Y_{it}	Theoretical position of track i at the recorded pattern	$Y_{it} = Y_0 + i \times \Delta Y$	
l	Track pitch	$l = g \times \sin\theta$	
TLE	Track location error	$TEL = Y_i - Y_{it}$	
Z	Tolerance zone	Z4 = 0.004 mm Z1, Z2, Z3, Z5, Z6, Z7, Z8 = 0.006 mm	
NOTE - For tolerance zone Z1: i = ... -8, 0, +8, +16, ... Z2: i = ... -9, -1, +7, +15, ... Z3: i = ... -10, -2, +6, +14, ... Z4: i = ... -11, -3, +5, +13, ... Z5: i = ... -12, -4, +4, +12, ... Z6: i = ... -13, -5, +3, +11, ... Z7: i = ... -14, -6, +2, +10, ... Z8: i = ... -15, -7, +1, +9, ...			

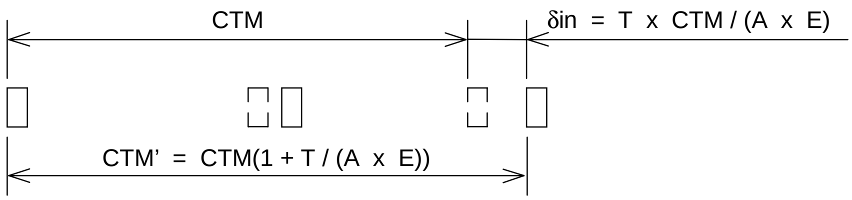
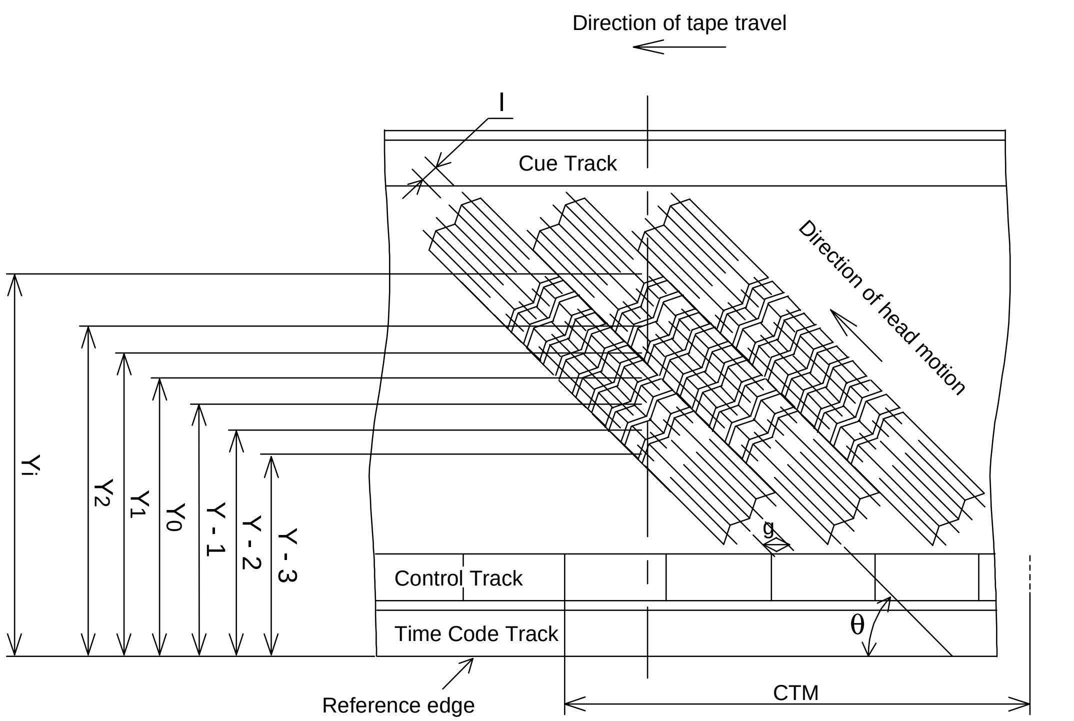


Figure B.1 – Correction factors (actual tape speed and tension)



NOTE – The same head must be used for Yi measurement (i.e., every eighth track); CTM is the distance of n control track pitches (n = 200 minimum).

Figure B.2 – Cross-tape measurement technique

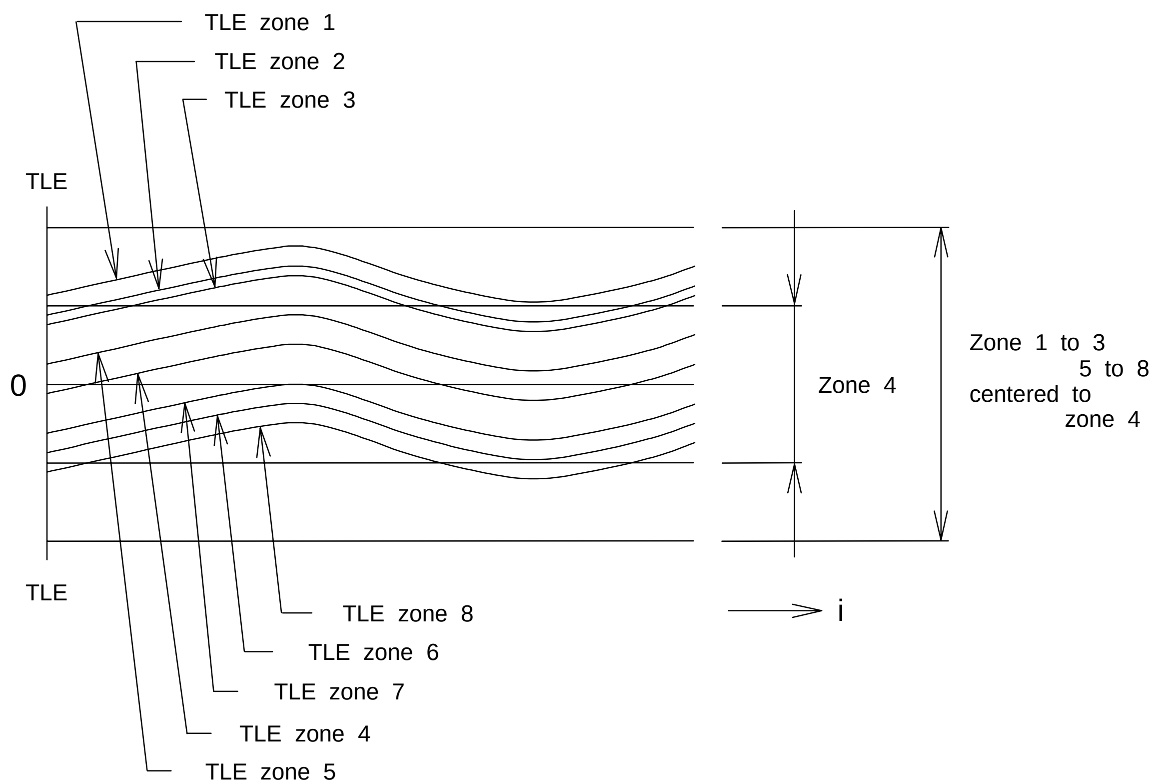
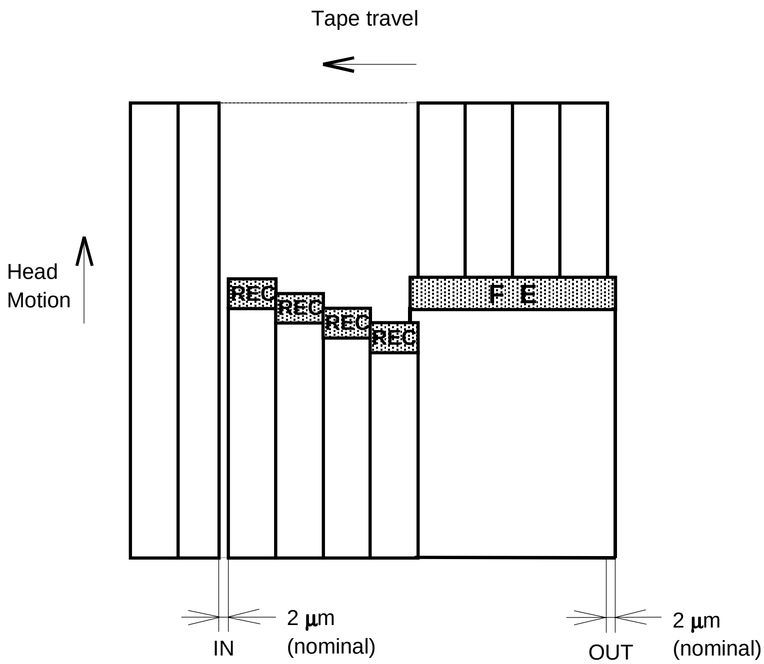


Figure B.3 – Track location error plot (example)

Annex C (normative)
Track pattern during insert editing

A guard band of 2 µm (nominal) at editing points only is shown in figure C.1.



NOTES - 1 REC is a recording head.
2 FE is a flying erase head.

Figure C.1 – A typical pattern during insert editing

Annex D (informative)
Video interface

D.1 Video parameters

The component signal source to be processed should comply with the video parameters as defined by SMPTE 274M and SMPTE 296M.

D.2 Serial digital interface

The interface of the digital video signal, if present, should conform to the component serial digital interface format interface as defined in SMPTE 292M.

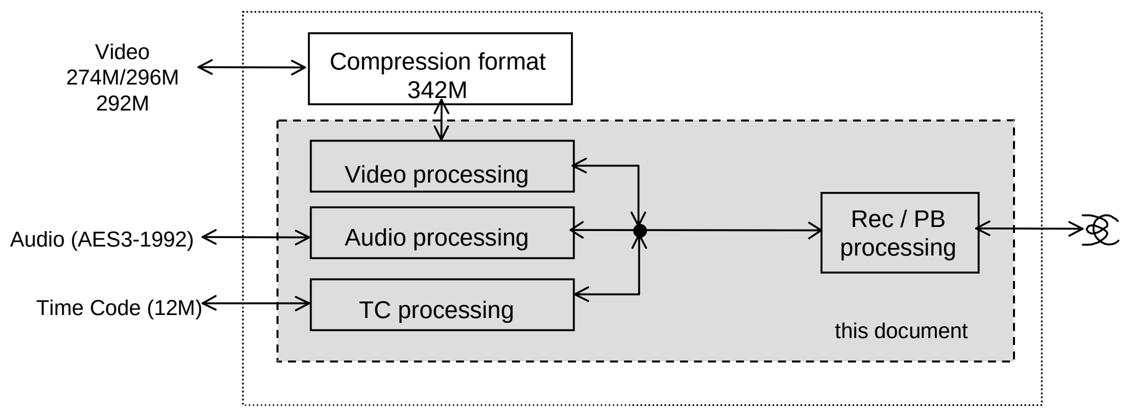


Figure D.1 – Block diagram of a recorder

Annex E (informative)
Reference and calibration tape

Blank tape for reference recordings should be available from any source meeting the tape characteristics as defined by this standard.

The calibration tapes meeting the requirements of 3.3.1 and 4 should be available from manufacturers who produce DTTRs and players in accordance with this standard. Tolerances of the record locations and dimensions shown in table 1 will be reduced by 50%.

Two sets of signals should be recorded on the calibration tape:

a) Video: 100% color bars
   Audio: 1-kHz tone at 20 dB below full scale on each of the audio data channels
   Cue: 1-kHz tone at reference level; 10-kHz tone at reference level

b) A signal of constant recorded frequency (i.e., one half the Nyquist frequency) only on tracks of field 0, segment 0 for the purpose of mechanical alignment. Recording level should conform to 6.6.3.

Annex F (informative)
Tape cassette

Tape enclosure (tape cassette) is specified in SMPTE 263M-2003

Annex G (informative)
Abbreviations

AUX	Auxiliary	
CHAN	Channel use	
EFLG	Edit flag	
FNCT	Field number count	
HD-D5	Recording format described by SMPTE 279LNGH	Audio data word mode
PREF	Preemphasis	
S MARK	Block sync location	

Annex H (informative)
Bibliography

SMPTE 263M-2003, Television Digital Recording — 1/2-in Type Magnetic Tape Cassette

SMPTE 274M-2003 Television – 1920x1080 Image Sample Structure, Digital Representation and Digital Timing Reference Sequences for Multiple Picture Rates

SMPTE 292M-1998 Television – Bit Serial Digital Interface for High-Definition Television Systems

SMPTE 296M-2001 Television – 1280x720 Progressive Image Sample Structure – Analog and Digital Representation and Analog Interface

CCITT Vol. III, Fascicle III.4, Transmission of Sound-Programme and Television Signals, Recommendation J.17, Pre-emphasis

IEC 60735 (1991-11), Measuring Methods for Video Tape Properties

ISO 2110:1989, Information Technology — Data Communication — 25-Pole DTE/DCE Interface Connector and Contact Number Assignments