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SMPTE Technology Committee N 26 on File Management and Networking Technology

SMPTE STANDARD-

3Gb/s Signal/Data Serial Interface – Source Image Format Mapping

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Foreword

SMPTE (the Society of Motion Picture and Television Engineers) is an internationally recognized standards developing organization. Headquartered and incorporated in the United States of America, SMPTE has members in over 80 countries on six continents. SMPTE's Engineering Documents, including Standards, Recommended Practices and Engineering Guidelines, are prepared by SMPTE's Technology Committees. Participation in these Committees is open to all with a bona fide interest in their work. SMPTE cooperates closely with other standards-developing organizations, including ISO, IEC and ITU.

SMPTE Engineering Documents are drafted in accordance with the rules given in Part XIII of its Administrative practices.

SMPTE Standard 425M was prepared by Technology Committee N 26.

Introduction -

The SMPTE 292M-1998, Television – Bit-Serial Digital Interface For High-Definition Television Systems, was originally developed to provide a serial digital connection between HDTV equipment operating largely with 10-bit Y'/C'$_B$/C'$_R$ 4:2:2 signals to a maximum frame rate of 30 frames per second. Over time, SMPTE 292M applications were expanded to include larger picture formats, higher refresh rates and to provide support for R'G'B' and 12-bit source signal formats and the carriage of packetized data.

The total data rate required to support these additional applications is 2.970 Gb/s or 2.970/1.001Gb/s and the digital interface used to carry these payloads is currently realised using a dual-link structure as defined in SMPTE 372M-2002 for Television – Dual Link 292M Interface for 1920 x 1080 Picture Raster.

This standard defines the mapping of various source image formats onto a single link serial digital interface operating at a nominal rate of 3Gb/s, offering an alternate method to SMPTE 372M for the transport of signals with a total payload of 2.970 Gb/s or 2.970/1.001 Gb/s.

1 Scope

This standard specifies the direct mapping of various source image formats as defined in Table 1 below; the carriage of embedded audio; the carriage of ancillary data and the stream ID, in a serial digital interface operating at a nominal rate of 3Gb/s.

This standard also specifies the mapping of 2 x SMPTE 292M HD SDI interfaces including SMPTE 372M, Dual Link 292M Interface for 1920 x 1080 Picture Raster, into a serial digital interface operating at a nominal rate of 3Gb/s.

2 Normative References

The following standards contain provisions, which, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

SMPTE 274M-2005 Television ---- 1920 x 1080 Image Sample Structure, Digital Representation and Digital Timing Reference Sequences for Multiple Picture Rates

SMPTE 296M-2001 for Television — 1280 x 720 Progressive Image Sample Structure — Analog and Digital Representation and Analog Interface

SMPTE 291M-1998 for Television ---- Ancillary Data Packet and Space Formatting

SMPTE 299M-2005 for Television - 24-Bit Digital Audio Format for SMPTE 292M Bit-Serial Interface

SMPTE 352M-2002 for Television (Dynamic) - Video Payload Identification for Digital Interfaces

SMPTE RP 188-1999 Transmission of Time Code and Control Code in the Ancillary Data Space of a Digital Television Data Stream

SMPTE 292M-1998 Television – Bit-Serial Digital Interface For High-Definition Television Systems

SMPTE 372M-2002 for Television – Dual Link 292M Interface for 1920 x 1080 Picture Raster.

3 Direct Mapping of Source Image Formats

For this interface, the source data shall be an uncompressed 10-bit or 12-bit video signal corresponding to the source image formats identified in Table 1or packetized data.

An auxiliary component signal designated A or Alpha, may optionally accompany the R'G'B' or $Y'C'_BC'_R$ video signal. Interfaces containing the auxiliary component are denoted as R'G'B'+A and $Y'C'_BC'_R$+A. The auxiliary component is referred to as either the A channel or Alpha channel in this document. The A or Alpha channel component if present shall have the same characteristics as the Y' or G' channel as defined in the source image formatting document.

Table 1 Source image formats

Mapping structure	Reference SMPTE Standard	Image Format	Signal Format sampling structure/pixel Depth	Frame/Field Rates
1	274M	1920 × 1080	4:2:2 ($Y'C'_BC'_R$)/10-bit	60, 60/1.001 and 50 Frames Progressive
2	296M	1280 x 720	4:4:4 (R'G'B'), 4:4:4:4 (R'G'B' +A)/10-bit	60, 60/1.001 and 50 Frames Progressive 30, 30/1.001, 25, 24 and 24/1.001 Frames Progressive
			4:4:4 ($Y'C'_BC'_R$), 4:4:4:4 ($Y'C'_BC'_R$+A)/10-bit	
	274M	1920 x 1080	4:4:4 (R'G'B'), 4:4:4:4 (R'G'B' +A)/10-bit	60, 60/1.001 and 50 Fields Interlaced 30, 30/1.001, 25, 24 and 24/1.001 Frames Progressive
			4:4:4 ($Y'C'_BC'_R$), 4:4:4:4 ($Y'C'_BC'_R$+A)/10-bit	
3	274M	1920 x 1080	4:4:4 (R'G'B')/12-bit	60, 60/1.001 and 50 Fields Interlaced 30, 30/1.001, 25, 24 and 24/1.001 Frames Progressive
			4:4:4 ($Y'C'_BC'_R$)/12-bit	
4	274M	1920 x 1080	4:2:2 ($Y'C'_BC'_R$)/12-bit	30, 30/1.001, 25, 24 and 24/1.001 Frames Progressive 60, 60/1.001 and 50 Fields Interlaced

3.1 20-bit Virtual interface

R', G', B', Y', C'_B, C'_R, and A components shall be mapped into a virtual interface consisting of two parallel 10-bit data streams – data stream one and data stream two, as shown in Figures 1 through 4.

Each data stream shall have an interface frequency of 148.5 MHz or 148.5/1.001 MHz.

Mapping of the data created by the signal format, sampling structure and pixel depth shall be in accordance with § 3.2.1 through § 3.2.6 of this standard.

3.1.1 Timing reference signals

EAV (End of Active Video) and SAV (Start of Active Video), timing references shall be inserted into data stream one and data stream two of the virtual interface on a line-by-line basis as shown in Figures 1 through 4.

The EAV and SAV sequence, F (field/ frame), V (vertical), H (horizontal) and parity bits P3 through P1 shall be as defined in the source image formatting document.

Mapping of the timing reference signals into the virtual interface shall be in accordance with § 3.2.1 through § 3.2.6 of this standard.

3.1.2 Line numbers

Line numbers shall be inserted into data stream one and data stream two of the virtual interface starting at the first data word (of the virtual interface) following the EAV XYZ word, as shown in Figures 1 through 4.

The virtual interface line numbers shall be in accordance with the picture source line numbers as defined in the source image formatting document.

Line number data are composed of two words, LN0 and LN1 and shall be as shown in table 2.

Table 2 -- Line number data

	9 (msb)	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
LN0	$\overline{B8}$	L6	L5	L4	L3	L2	L1	L0	Res	Res
LN1	$\overline{B8}$	Res	Res	Res	L10	L9	L8	L7	Res	Res

NOTES:
1 L10 : L0 = line number in binary code.
2 Res = reserved, set to “0” and shall be ignored by receivers.

3.1.3 Line CRC codes

CRC (Cyclic Redundancy Codes) shall be inserted into data stream one and data stream two of the virtual interface starting at the first data word (of the virtual interface) following the final word of the line number – LN1, as shown in Figures 1 through 4.

The CRC code words are used to detect errors in the active digital line, the EAV timing reference signal and line number words which follows it. The error detection code consists of two words determined by the polynomial generator equation:

$$CRC(X) = X^{18} + X^5 + X^4 + 1$$

The initial value of the CRC is set to zero. The calculation starts at the first active line word of the virtual interface and ends at the final word of the line number - LN1.

Independent CRC codes shall be produced for data stream one and data stream two of the virtual interface.

The two words of the CRC code shall be as shown in table 3.

Table 3 – CRC data

	9 (msb)	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0 (lsb)**
CR0	$\overline{B8}$	CRC8	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
CR1	$\overline{B8}$	CRC17	CRC16	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9

Informative Note – Users should be aware that data stream one and data stream two of the virtual interface may carry any type of data as defined by the application.

3.1.4 Ancillary Data

Ancillary data if present shall be mapped into the blanking area of both data stream one and data stream two of the virtual interface and shall be in conformance with SMPTE 291M.

The ancillary data shall be mapped into data stream one first, with any remaining data being mapped into data stream two.

3.1.5 Audio Data

When present, audio data shall be mapped into the ancillary data space of data stream one and data stream two of the virtual interface.

Audio control packets shall be mapped into the horizontal ancillary data space of data stream one of the virtual interface.

The formatting and location of the audio control packets shall be in conformance with SMPTE 299M.

Audio data packets shall be mapped into the horizontal ancillary data space of data stream two of the virtual interface.

The formatting and location of the audio data packets shall be in conformance with SMPTE 299M.

The audio clock phase data defined in § 5.2.1 of SMPTE 299M shall be calculated at the original interface clock frequency as defined by the source image format document.

Informative note - Designers should be aware that the virtual interface of this standard may operate at twice the clock rate of the source image format interface.

3.1.6 Time Code

When present, the time code data shall be mapped into the ancillary data space of data stream one of the virtual interface and shall be in conformance with SMPTE RP188.

3.1.7 Payload identifier

The payload identifier shall be mapped into the ancillary data space of data stream one and data stream two of the virtual interface and shall be in conformance with SMPTE 352M.

The horizontal placement of the packet shall be immediately following the last CRC code word (CR1), of the line(s) specified in SMPTE 352M for 750 line and 1125 line systems.

Informative note – the line numbers defined in SMPTE 352M for the placement of the payload identifier packet in 750-line and 1125-line interfaces avoids those lines used by SMPTE 299M for the carriage of digital audio control and data packets.

3.1.7.1 Byte 1: Video payload and digital interface identification

The first byte of the payload identifier is used to identify the combination of video payload format and digital interface transport.

For 750 line video digital transport interfaces on the 3Gb/s video payload, Byte 1 of the payload identifier shall be set to 88_h.

For 1125 line digital transport interfaces on the 3Gb/s video payload, Byte 1 of the payload identifier shall be set to 89_h.

Bytes 2 through 4 of the payload identifier shall be set in accordance with the picture rate, sampling structure, dynamic range and bit-depth etc of the image format being carried on the interface as shown in tables 4 and 5.

Table 4 Payload Identifier Definitions for SMPTE 274M on the 3Gb/s Digital Interface

Bits	Byte 1	Byte 2	Byte 3	Byte 4
Bit 7	1	Interlaced (0) or Progressive (1) transport	Reserved	Reserved
Bit 6	0	Interlaced (0) or Progressive (1) picture	Horizontal Y' sampling 1920 (0)	Reserved
Bit 5	0	Reserved	Reserved	Reserved
Bit 4	0	Reserved	Reserved	Dynamic range 100% (0h), 200% (1h), 400% (2h), Reserved (3h)
Bit 3	1	Picture Rate (see SMPTE 352M table 2)	Sampling structure (see SMPTE 352M table 3)	
Bit 2	0			Reserved
Bit 1	0			Bit depth 8-bit (0h), 10-bit (1h), 12-bit (2h), Reserved (3h)
Bit 0	1			

Table 5 Payload Identifier Definitions for SMPTE 296M on the 3Gb/s Digital Interface

Bits	Byte 1	Byte 2	Byte 3	Byte 4
Bit 7	1	Interlaced (0) or Progressive (1) transport	Reserved	Reserved
Bit 6	0	Interlaced (0) or Progressive (1) picture	Horizontal Y'/Y sampling 1280	Reserved
Bit 5	0	Reserved	Reserved	Reserved
Bit 4	0	Reserved	Reserved	Dynamic range 100% (0h), 200% (1h), 400% (2h), Reserved (3h)
Bit 3	1	Picture Rate (See SMPTE 352M table 2)	Sampling structure (See SMPTE 352M table 3)	
Bit 2	0			Reserved
Bit 1	0			Bit depth 8-bit (0h), 10-bit (1h), 12-bit (2h), Reserved (3h)
Bit 0	0			

3.2 Virtual Interface – Data Stream Mappings

3.2.1 Mapping structure 1 - SMPTE 274M - 4:2:2 ($Y'C'_BC'_R$)/10-bit Signals at 60, 60/1.001 and 50 Progressive frames / sec

Mapping of the data created by the 4:2:2 picture sampling structure into the virtual interface is shown in figure 1.

Data stream one shall contain all of the Y' sample data and data stream two shall contain a multiplex of the C'_B and C'_R sample data conveyed in the following order:

Data stream one = Y'0, Y'1, Y'2, Y'3…….
Data stream two = C'_B0, C'_R0, C'_B1, C'_R1……..

3.2.1.1 Timing Reference Signals

The EAV timing reference signal shall be inserted into the virtual interface starting at the first data word (of the virtual interface), following the last active Y' sample (data stream one) and C'_R sample (data stream two), in accordance with § 3.1.1.

The SAV timing reference signal shall be inserted into the virtual interface starting 4 data words (of the virtual interface) prior to the first active Y' sample (data stream one) and C'_B sample (data stream two), in accordance with § 3.1.1.

The location of the last sample number 'n' of the total line and the fist and last active sample numbers of the original digital interface as defined in the image formatting document are repeated here for convenience.

Table 6 Location of the first and last active samples for 4:2:2 (Y'C'$_B$C'$_R$)/10-bit Signals at 60, 60/1.001 and 50 Progressive frames / sec

Reference SMPTE Standard	Frame Rate	First active sample number	Last active sample number	Last sample number 'n' (total line)
274M system 1 & 2	60 or 60/1.001	0	1919	2199
274M system 3	50	0	1919	2639

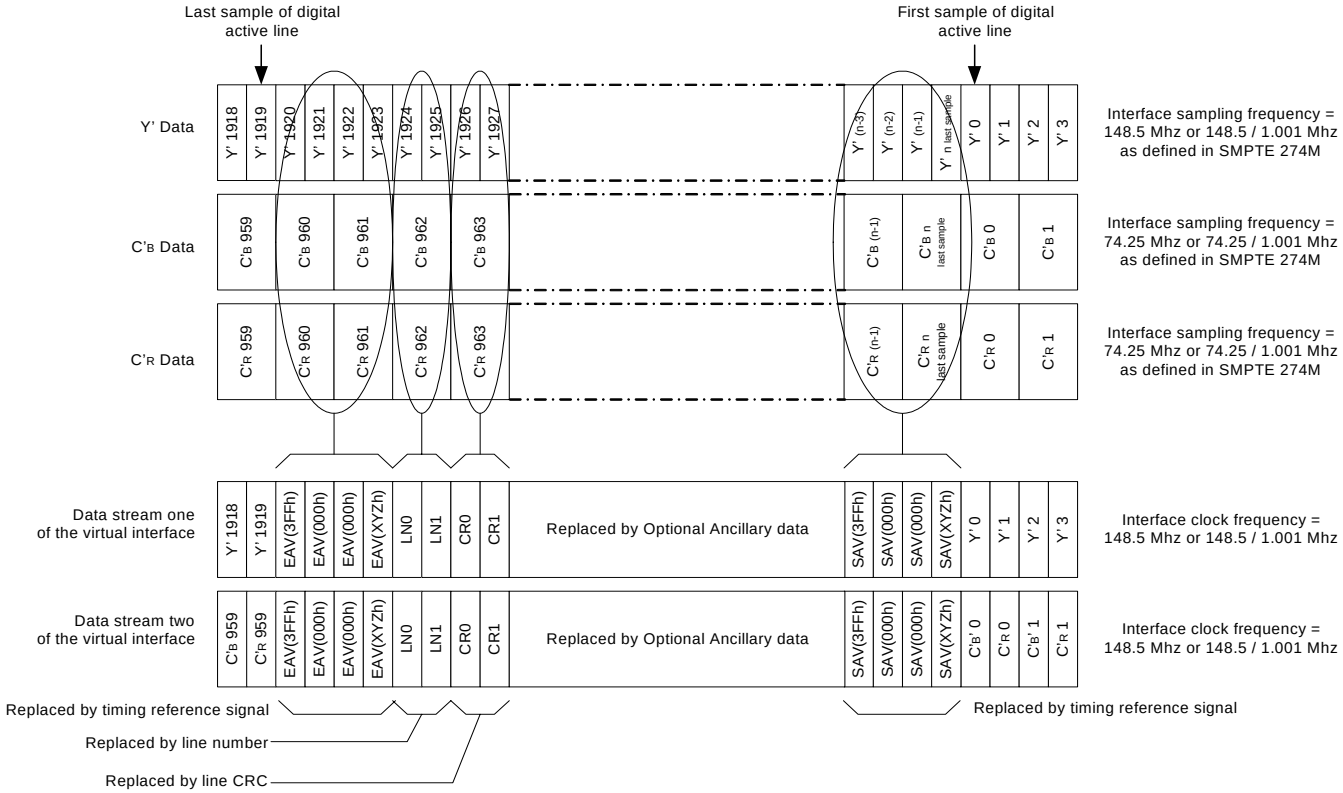

Figure 1 Mapping Structure 1 – SMPTE 274M 4:2:2 (Y'C'$_B$C'$_R$)/10-bit Signals at 60, 60/1.001 and 50 Progressive frames /sec

3.2.2 Mapping structure 2 - 4:4:4 (R'G'B')/ (Y'C'$_B$'C'$_R$) and 4:4:4:4 (R'G'B'+A)/ (Y'C'$_B$'C'$_R$+A)//10-bit Signals

Mapping of the data created by the 4:4:4 (R'G'B')/10-bit and 4:4:4:4 (R'G'B'+A)/10-bit picture sampling structure into the virtual interface is shown in Figure 2.

Data stream one shall contain all of the R' and G' sample data and data stream two shall contain all of the A (where present), and B' sample data conveyed in the following order:

Data stream one = G'0, R'0, G'1, R'1…….
Data stream two = A0, B'0, A1, B'1…….

Mapping of the data created by the 4:4:4 (Y'C'$_B$'C'$_R$) and 4:4:4:4 (Y'C'$_B$'C'$_R$+A)/10-bit image sampling structure on to the virtual interface shall be as shown in Figure 2 except that:

The R' samples shall be replaced with C'$_R$ samples;
The G' samples shall be replaced with Y' samples;
The B' samples shall be replaced with C'$_B$ samples;

3.2.2.1 Timing Reference Signals

The EAV timing reference signal shall be inserted into the virtual interface starting at the first data word (of the virtual interface), following the last active G' sample (data stream one) and R' sample (data stream two), in accordance with § 3.1.1.

The SAV timing reference signal shall be inserted into the virtual interface starting 4 data words (of the virtual interface) prior to the first active B' sample (data stream one) and A sample (data stream two), in accordance with § 3.1.1.

The location of the last sample number 'n' of the total line and the fist and last active sample numbers of the original digital interface as defined in the image formatting document are repeated here for convenience.

Table 7 Location of the first and last active samples for 4:4:4 (R'G'B')/10-bit and 4:4:4:4 (R'G'B'+A)/10-bit Signals

Reference SMPTE Standard	Frame Rate	First active sample number	Last active sample number 'a'	Last sample number 'n' (total line)
296M system 1 & 2	60 or 60/1.001	0	1279	1649
296M system 3	50	0	1279	1979
274 M system 4 & 5, 7 & 8	30 or 30/1.001	0	1919	2199
296 M system 4 & 5	30 or 30/1.001	0	1279	3299
274M system 6 & 9	25	0	1919	2639
296M system 6	25	0	1279	3959
274M system 10 & 11	24 or 24/1.001	0	1919	2749
296M system 7 & 8	24 or 24/1.001	0	1279	4124

3.2.2.2 Alpha Channel

If the alpha channel is not used, the values of the alpha channel samples shall be set to 040_h. Use of the alpha channel is application dependant.

3.2.2.2.1 If the alpha channel is used for conveying picture information, the raster format and frame rate shall be the same as the R'G'B' or $Y'C'_BC'_R$ signals carried on the virtual interface.

3.2.2.2.2 If the alpha channel is used to carry data, the data words shall be 8-bit maximum. As the virtual interface is a 10-bit interface, bit B8 shall be the even parity of bits B7 through B0 and bit B9 shall be the complement of bit B8.

3.2.2.2.3 Data values 000_h to 003_h and $3FC_h$ to $3FF_h$ shall not be permitted.

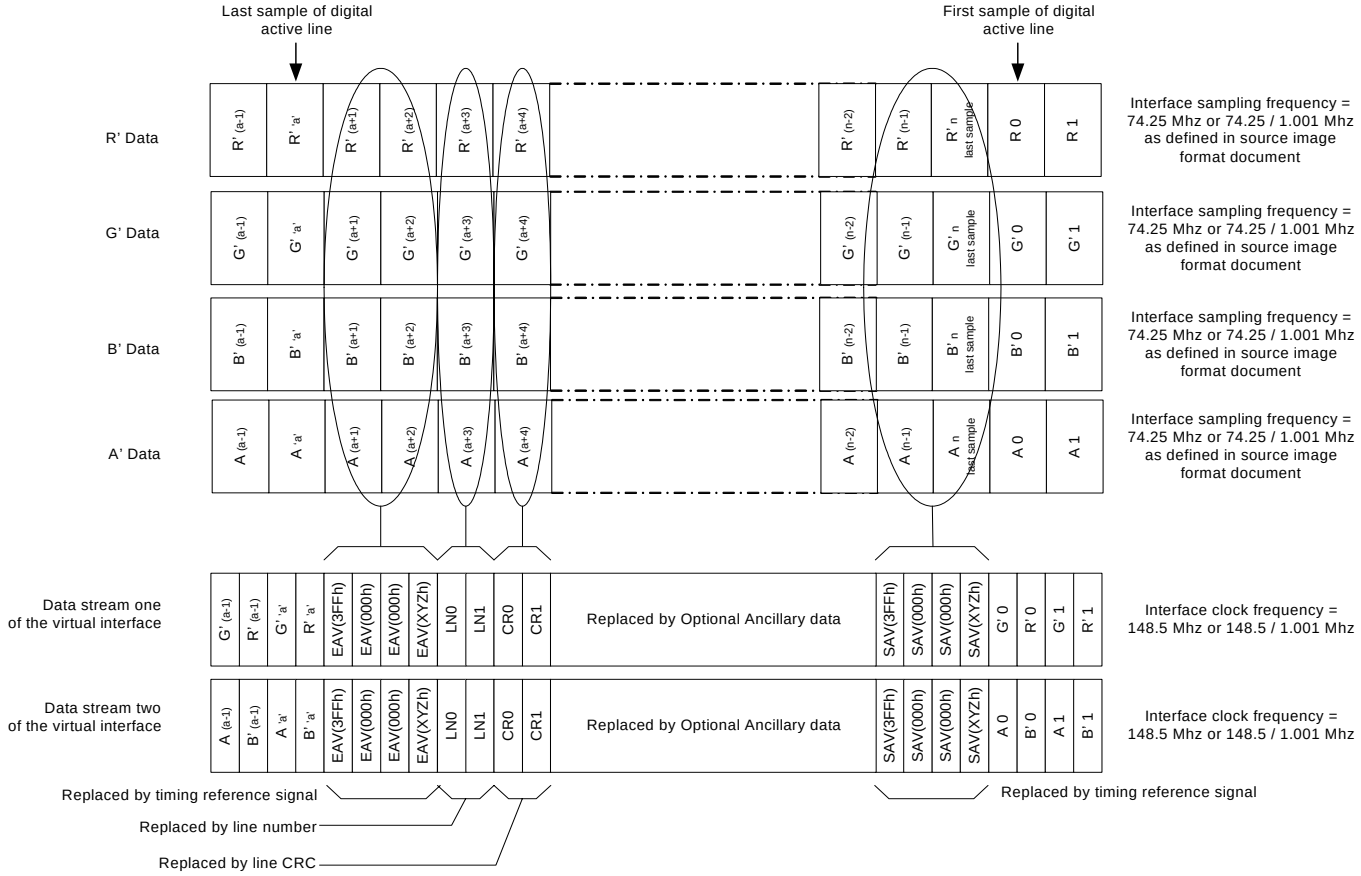

Figure 2 Mapping Structure 2 – 4:4:4 (R'G'B') and 4:4:4:4 (R'G'B'+A)/10-bit Signals

3.2.3 Mapping Structure 3 - 4:4:4 (R'G'B') / (Y'C'$_B$C'$_R$)/12-bit Signals

Mapping of the data created by the 4:4:4 (R'G'B') /12-bit picture sampling structure into the virtual interface is shown in Figure 3.

The 12-bit quantized samples - represented as R'G'B' (a)/(n)[11:0] - shall be subdivided and conveyed across two data words of data stream one and data stream two of the virtual interface in the following order:

Data stream one = R'G'B' (a)/(n) [11:9], R'G'B' (a)/(n) [5:3], R'G'B' (a+1)/(n+1) [11:9]…….
Data stream two = R'G'B' (a)/(n) [8:6], R'G'B' (a)/(n) [2:0], R'G'B' (a+1)/(n+1) [8:6]…….

The individual samples are designated suffix (a) or (n) to indicate the sample number and [x:y] to represent specific bits within the sample.

Table 8 shows the bit structure of the subdivided samples.

Table 8 – R'G'B' (a) / (n) [x:y] bit structure mapping into data words of the virtual interface

	Bit number									
Data Stream	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data stream one first word of sample (a) / (n)	$\overline{B8}$	R' (a) / (n) [11:9]			G' (a) / (n) [11:9]			B' (a) / (n) [11:9]		
Data stream one second word of sample (a) / (n)	$\overline{B8}$	R' (a) / (n) [5:3]			G' (a) / (n) [5:3]			B' (a) / (n) [5:3]		
Data stream two first word of sample (a) / (n)	$\overline{B8}$	R'' (a) / (n) [8:6]			G' (a) / (n) [8:6]			B' (a) / (n) [8:6]		
Data stream two second word of sample (a) / (n)	$\overline{B8}$	R' (a) / (n) [2:0]			G' (a) / (n) [2:0]			B' (a) / (n) [2:0]		

The Mapping and sub-divided bit structure of the data created by the 4:4:4 ($Y'C'_BC'_R$)/12-bit picture sampling structure shall be as shown in table 8 and Figure 3 respectively except that:

The R' samples shall be replaced with C'_R samples;
The G' samples shall be replaced with Y' samples;
The B' samples shall be replaced with C'_B samples;

3.2.3.1 Timing Reference Signals

The EAV timing reference signal shall be inserted into the virtual interface starting at the first data word (of the virtual interface), following the last word of the last active R'G'B' sample in data stream one and data stream two, in accordance with § 3.1.1.

The SAV timing reference signal shall be inserted into the virtual interface starting 4 data words (of the virtual interface) prior to the first word of the first active R'G'B' sample in data stream one and data stream two, in accordance with § 3.1.1.

The location of the last sample number 'n' of the total line and the fist and last active sample numbers of the original digital interface as defined in the image formatting document are repeated here for convenience.

Table 9 Location of the first and last active samples for 4:4:4 (R'G'B') /12-bit Signals

Reference SMPTE Standard	Frame Rate	First active sample number	Last active sample number 'a'	Last sample number 'n' (total line)
274 M system 4 & 5, 7 & 8	30 or 30/1.001	0	1919	2199
274M system 6 & 9	25	0	1919	2639
274M system 10 & 11	24 or 24/1.001	0	1919	2749

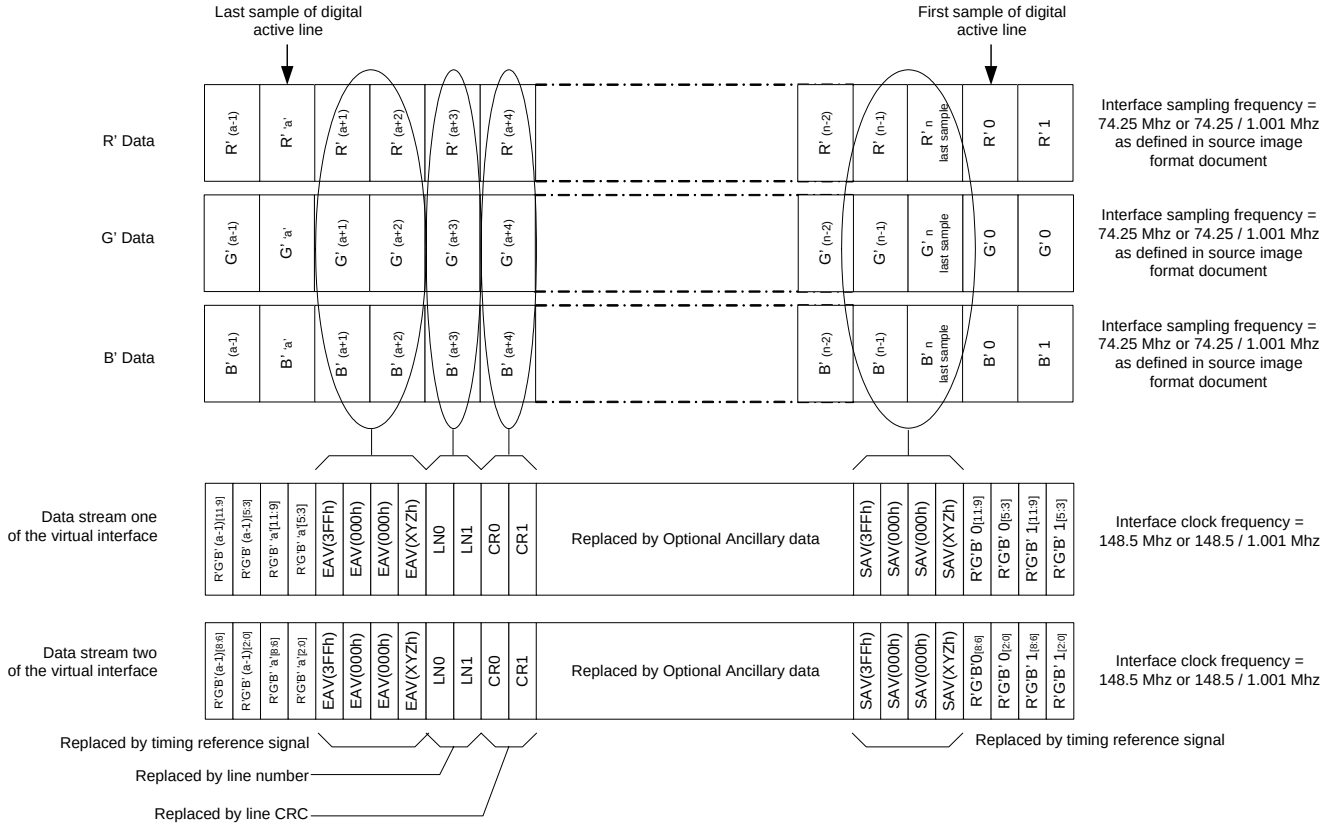

Figure 3 Mapping Structure 3 – 4:4:4 (R'G'B')/12-bit signals

3.2.4 Mapping Structure 4 - 4:2:2 (Y'C'$_B$C'$_R$)/12-bit signals at 30, 30/1.001, 25, 24 and 24/1.001 Frame Rates and 60, 60/1.001 and 50 Field Rates

Mapping of the data created by the 4:2:2 (Y'C'$_B$C'$_R$)/12-bit picture sampling structure into the virtual interface is shown in Figure 4.

The 12-bit quantized samples - represented as Y' (a)/(n)[11:0] - shall be subdivided and conveyed across two data words of data stream one of the virtual interface.

The 12-bit quantized samples - represented as C'$_B$C'$_R$ (a)/(n)[11:0] - shall be subdivided and conveyed across four data words of data stream two of the virtual interface in the following order:

Data stream one = Y' (a)/(n) [11:6], Y' (a+1)/(n+1) [5:0] Y' (a+2)/(n+2) [11:6] Y' (a+2)/(n+2) [5:0]…….
Data stream two = C'$_B$ (a)/(n) [11:6], C'$_B$ (a)/(n) [5:0], C'$_R$ (a)/(n) [11:6], C'$_R$ (a)/(n) [5:0]…..

The individual samples are designated suffix (a) or (n) to indicate the sample number and [x:y] to represent specific bits within the sample.

Table 10 and Table 11 show the bit structure of the subdivided samples.

Table 10 – Y'(a) / (n) [x:y] bit structure mapping into data words of the virtual interface

	Bit number									
Data Stream	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data stream one first word of sample (a) / (n)	1	Res			Y' (a) / (n) [11:6]					
Data stream one second word of sample (a) / (n)	1	Res			Y' (a) / (n) [5:0]					
NOTES: 1 Res = reserved, set to "0"										

Table 11 – $C'_BC'_R$(a) / (n) [x:y] bit structure mapping into data words of the virtual interface

	Bit number									
Data Stream	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data stream two first word of sample (a) / (n)	1	Res			C'_B (a) / (n) [11:6]					
Data stream two second word of sample (a) / (n)	1	Res			C'_B (a) / (n) [5:0]					
Data stream two third word of sample (a) / (n)	1	Res			C'_R (a) / (n) [11:6]					
Data stream two fourth word of sample (a) / (n)	1	Res			C'_R (a) / (n) [5:0]					
NOTES: 1 Res = reserved, set to "0".										

3.2.4.1 Timing Reference Signals

The EAV timing reference signal shall be inserted into the virtual interface starting at the first data word (of the virtual interface), following the last word of the last active Y' sample in data stream one and C'_R sample in data stream two accordance with § 3.1.1.

The SAV timing reference signal shall be inserted into the virtual interface starting 4 data words (of the virtual interface) prior to the first word of the first active Y' sample in data stream one and C'_B sample in data stream two in accordance with § 3.1.1.

The location of the last sample number 'n' of the total line and the fist and last active sample numbers of the original digital interface as defined in the image formatting document are repeated here for convenience.

Table 12 Location of the first and last active samples for 4:2:2 (Y'C'$_B$C'$_R$)/12-bit Signals

Reference SMPTE Standard	Frame Rate	First active sample number	Last active sample number 'a'	Last sample number 'n' (total line)
274 M system 4 & 5, 7 & 8	30 or 30/1.001	0	1919	2199
274M system 6 & 9	25	0	1919	2639
274M system 10 & 11	24 or 24/1.001	0	1919	2749

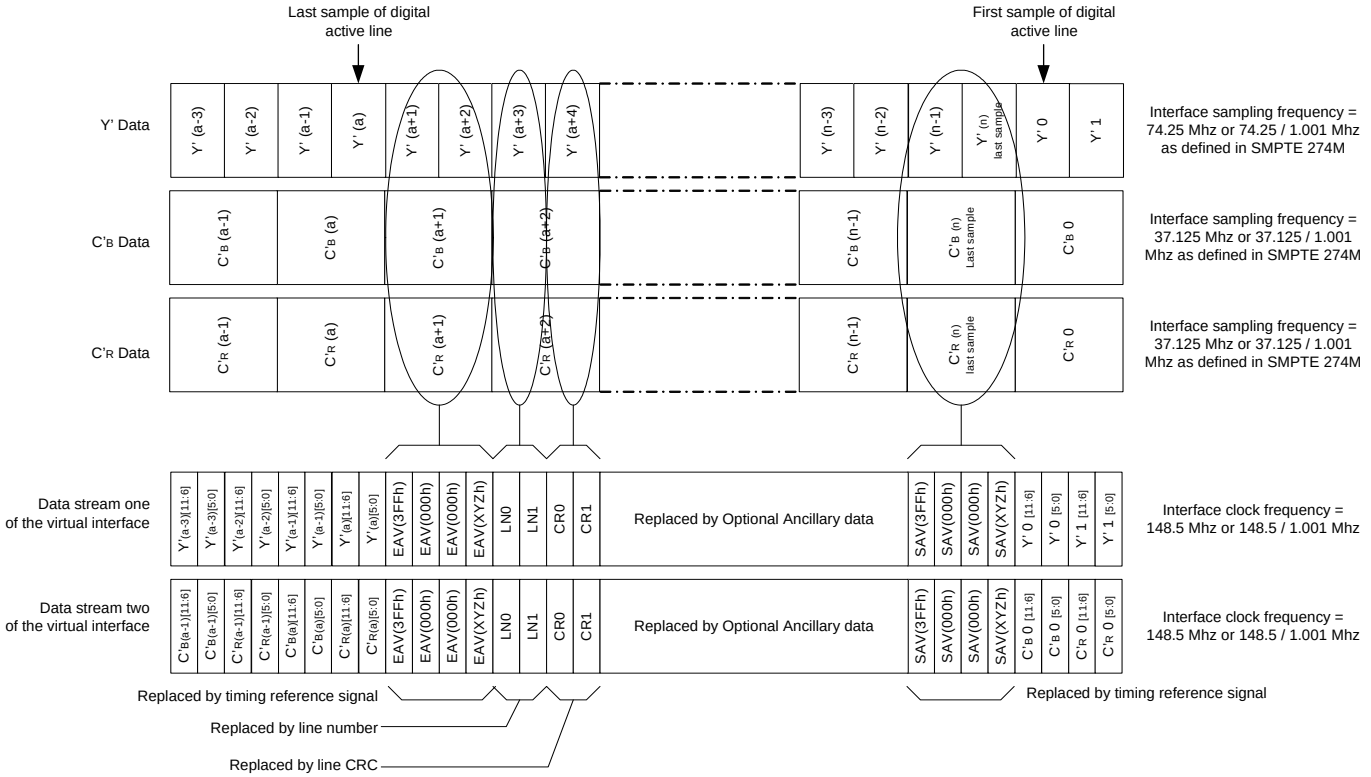

Figure 4 Mapping Structure 4 – 4:2:2 (Y'C'$_B$C'$_R$)/12-bit signals

4 Mapping of 2 x SMPTE 292M HD SDI interfaces.

4.1 20-bit Virtual interface

Two parallel 10-bit interfaces of the same line and frame structure shall be constructed in conformance with SMPTE 292M.

The source data for each 10-bit parallel interface may be packetized data, or an uncompressed video source.

Each parallel 10-bit interface shall be line and word aligned, having an interface frequency of 148.5MHz or 148.5/1.001 MHz.

An example of the 10-bit interface defined in SMPTE 292M is included in Figure 5 for convenience.

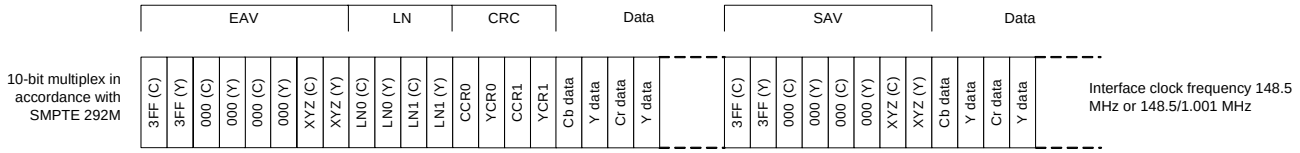

Figure 5 Example of 10-bit interface data format from SMPTE 292M

These interfaces shall be mapped into a 20-bit Virtual Interface consisting of two data streams – data stream one and data stream two.

For SMPTE 372M Dual link 1.5 Gb/s digital interface mapping, data-stream one shall contain all of the 10-bit data words of the Link A interface and data stream two shall contain all of the data words of the Link B interface, all other mappings are undefined.

4.2 Payload identifier

The payload identifier shall be mapped into the ancillary data space of data stream one and data stream two of the virtual interface and shall be in conformance with SMPTE 352M.

The horizontal placement of the packet shall be immediately following the last CRC code word (YCR1), of the line(s) specified in SMPTE 352M for 750 line and 1125 line systems.

4.2.1 Byte 1: Video payload and digital interface identification

Byte 1 of the payload identifier shall be set in accordance with Table 13 below.

Bytes 2 through 4 of the payload identifier shall be set in accordance with the picture rate, sampling structure, dynamic range and bit-depth etc of the image format being carried on the interface as defined in SMPTE 352M.

For SMPTE 372M Dual link, Link A (Ch1) and Link B (Ch2) identification shall be provided in the payload identifier mapped into data stream one and data stream two respectively.

Table 13 Video payload and digital interface identification for 2 x SMPTE 292M HD SDI mapped on the 3Gb/s serial digital Interface

Mapping Nomenclature	Byte 1: Video payload and digital interface
SMPTE 372M Dual link payloads on a 3 Gb/s serial digital interface	8Ah
2 x 720-line video payloads on a 3 Gb/s serial digital interface	8Bh
2 x 1080-line video payloads on a 3 Gb/s serial digital interface	8Ch
2 x 483/576-line video payloads on a 3 Gb/s serial digital interface	8Dh

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5 Levels of operation - informative

To define the level of support for this standard, manufacturers are encouraged to indicate in commercial publications which mapping format is supported. For example:

Level A – Direct image format mapping

Level B – 2 x SMPTE 292M HD SDI mapping (including SMPTE 372M dual link mapping)

5.1 Examples of compliance nomenclature

Equipment supporting only the direct image format mapping mode of this standard would be said to conform to SMPTE 425M-A.

Equipment supporting only the 2 x SMPTE 292M HD SDI mapping mode of this standard would be said to conform to SMPTE 425M-B

Equipment supporting both direct image format mapping and the 2 x SMPTE 292M mapping mode would be said to conform to SMPTE 425M-AB

Annex A (informative) Bibliography

SMPTE 12M-1999 Television, Audio and Film – Time and Control Code