R8800
Data Sheet
16-BIT RISC MICRO-CONTROLLER

RDC ***RISC DSP Communication***

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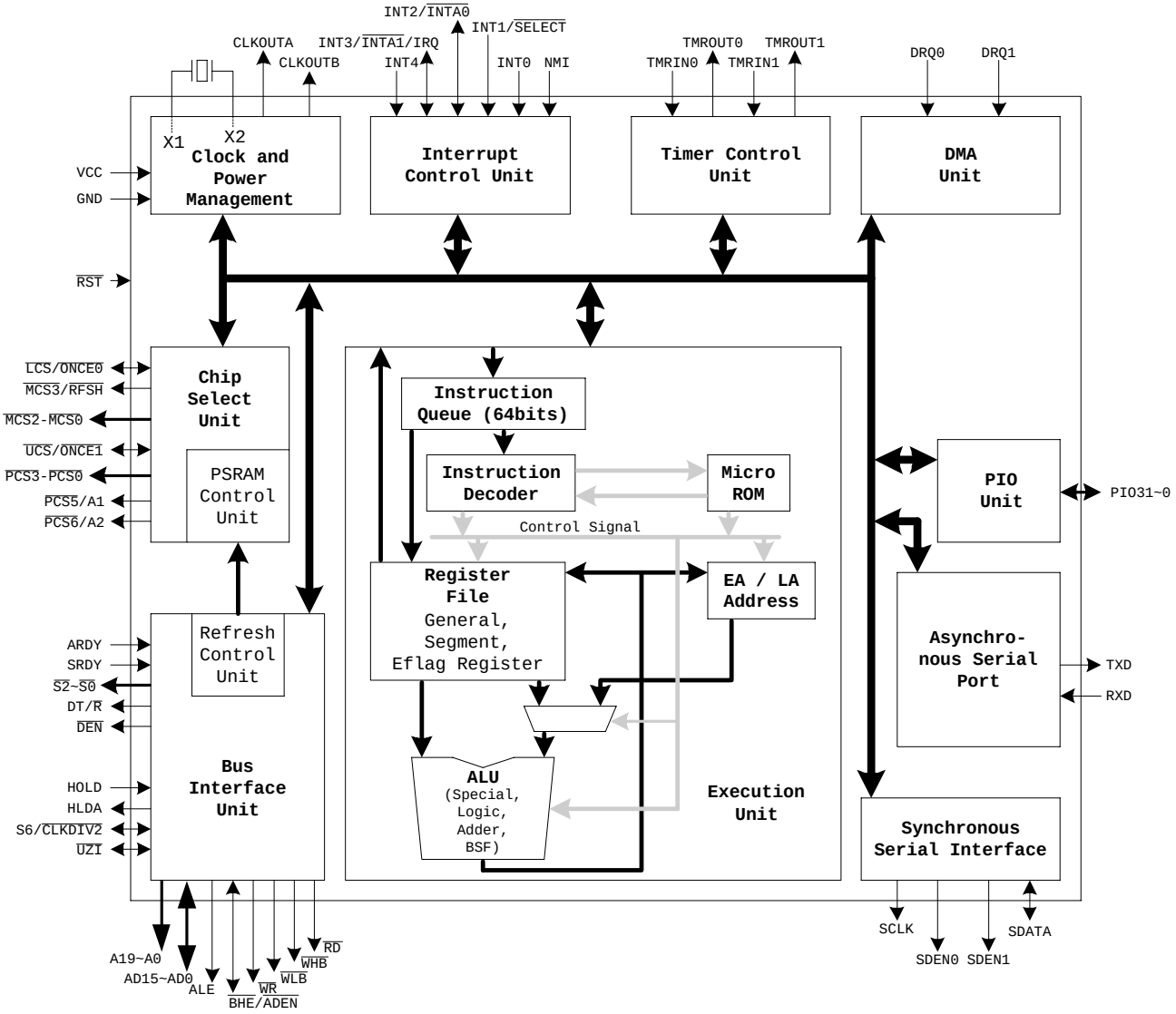
Contents

16-bit micro-controller with 16-bit external data bus

1. Features

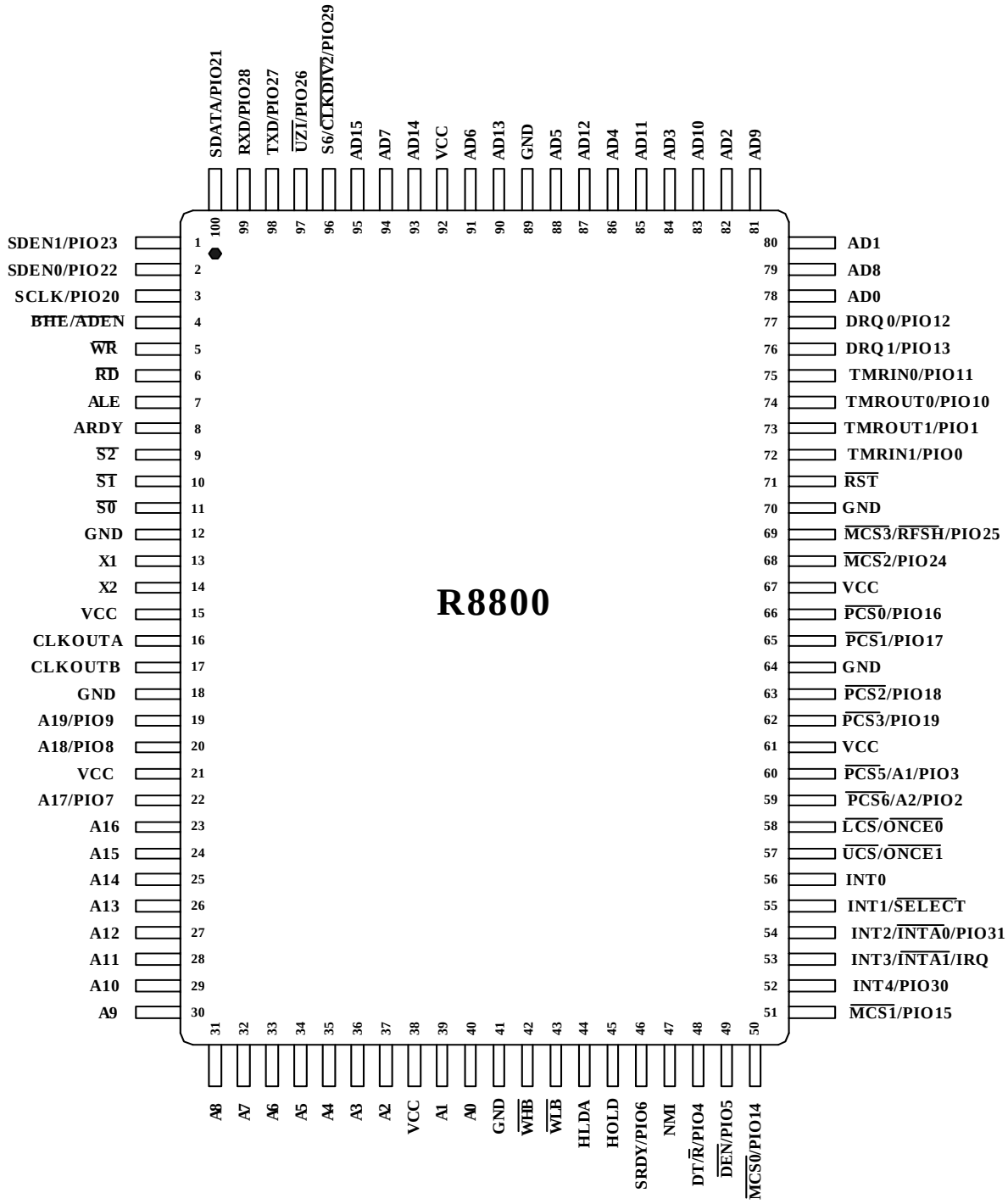
- Five-stage pipelines
- RISC architecture
- Static design & Synthesizable design
- Bus interface
  - Multiplexed address and data bus which is compatible with 80C186 microprocessor
  - Supports non-multiplexed address bus [A19:A0]
  - 1M-Byte memory address space
  - 64K-byte I/O space
- Software is compatible with the 80C186 microprocessor
- Supports one Asynchronous serial channel & one Synchronous serial channel
- Supports 32 PIO pins
- PSRAM (Pseudo static RAM) interface with auto-refresh control
- Three independent 16-bit timers and Timer 1 can be programmed as a watchdog timer
- The Interrupt controller with five maskable external interrupts and one non-maskable external interrupt
- Two independent DMA channels
- Programmable chip-select logic for Memory or I/O bus cycle decoder
- Programmable wait-state generator
- Supports CPU ID

2. Block Diagram

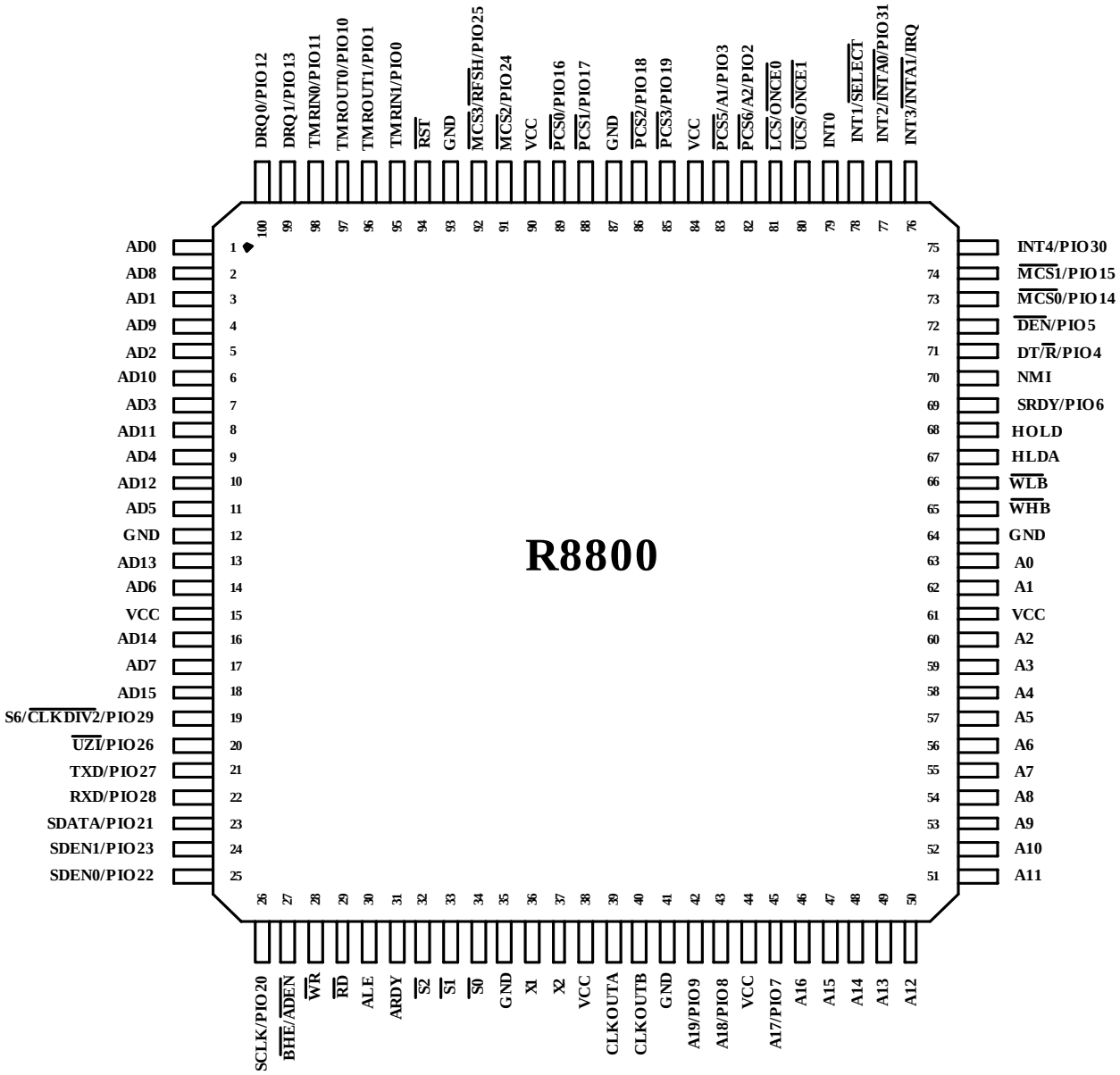


3. Pin Configuration

3.1 PQFP



3.2 LQFP


R8800
1 AD0
2 AD8
3 AD1
4 AD9
5 AD2
6 AD10
7 AD3
8 AD11
9 AD4
10 AD12
11 AD5
12 GND
13 AD13
14 AD6
15 VCC
16 AD14
17 AD7
18 AD15
19 S6/CLKDIV2/PIO29
20 UZI/PIO26
21 TXD/PIO27
22 RXD/PIO28
23 SDATA/PIO21
24 SDEN1/PIO23
25 SDEN0/PIO22
26 SCLK/PIO20
27 BHE/ADEN
28 WR
29 RD
30 ALE
31 ARDY
32 S2
33 S1
34 S0
35 GND
36 X1
37 X2
38 VCC
39 CLKOUTA
40 CLKOUTB
41 GND
42 A19/PIO9
43 A18/PIO8
44 VCC
45 A17/PIO7
46 A16
47 A15
48 A14
49 A13
50 A12
51 A11
52 A10
53 A9
54 A8
55 A7
56 A6
57 A5
58 A4
59 A3
60 A2
61 VCC
62 A1
63 A0
64 GND
65 WHB
66 WLB
67 HLDA
68 HOLD
69 SRDY/PIO6
70 NMI
71 DT/R/PIO4
72 DEN/PIO5
73 MCS0/PIO14
74 MCS1/PIO15
75 INT4/PIO30
76 INT3/INTA1/IRQ
77 INT2/INTA0/PIO31
78 INT1/SELECT
79 INT0
80 UCS/ONCE1
81 LCS/ONCE0
82 PCS6/A2/PIO2
83 PCS5/A1/PIO3
84 VCC
85 PCS3/PIO19
86 PCS2/PIO18
87 GND
88 PCS1/PIO17
89 PCS0/PIO16
90 VCC
91 MCS2/PIO24
92 MCS3/RFSH/PIO25
93 GND
94 RST
95 TMRIN1/PIO0
96 TMROUT1/PIO1
97 TMROUT0/PIO10
98 TMRIN0/PIO11
99 DRQ1/PIO13
100 DRQ0/PIO12

3.3 R8800 PQFP and LQFP Pin-Out Table

Pin name	LQFP Pin No.	PQFP Pin No.	Pin name	LQFP Pin No.	PQFP Pin No.
AD0	1	78	A11	51	28
AD8	2	79	A10	52	29
AD1	3	80	A9	53	30
AD9	4	81	A8	54	31
AD2	5	82	A7	55	32
AD10	6	83	A6	56	33
AD3	7	84	A5	57	34
AD11	8	85	A4	58	35
AD4	9	86	A3	59	36
AD12	10	87	A2	60	37
AD5	11	88	VCC	61	38
GND	12	89	A1	62	39
AD13	13	90	A0	63	40
AD6	14	91	GND	64	41
VCC	15	92	$\overline{WHB}$	65	42
AD14	16	93	$\overline{WLB}$	66	43
AD7	17	94	HLDA	67	44
AD15	18	95	HOLD	68	45
S6/ $\overline{CLKDIV2}$ /PIO29	19	96	SRDY/PIO6	69	46
$\overline{UZI}$/PIO26	20	97	NMI	70	47
TXD/PIO27	21	98	DT/ $\overline{R}$ /PIO4	70	48
RXD/PIO28	22	99	$\overline{DEN}$ /PIO5	72	49
SDATA/PIO21	23	100	$\overline{MCS0}$/PIO14	73	50
SDEN1/PIO23	24	1	$\overline{MCS1}$/PIO15	74	51
SDEN0/PIO22	25	2	INT4/PIO30	75	52
SCLK/PIO20	26	3	INT3/ $\overline{INTA1}$ /IRQ	76	53
$\overline{BHE}$/ $\overline{ADEN}$	27	4	INT2/ $\overline{INTA0}$ /PIO31	77	54
$\overline{WR}$	28	5	INT1/ $\overline{SELECT}$	78	55
$\overline{RD}$	29	6	INT0	79	56
ALE	30	7	$\overline{UCS}$/ $\overline{ONCE1}$	80	57
ARDY	31	8	$\overline{LCS}$/ $\overline{ONCE0}$	81	58
$\overline{S2}$	32	9	$\overline{PCS6}$ /A2/PIO2	82	59
$\overline{S1}$	33	10	$\overline{PCS5}$ /A1/PIO3	83	60
$\overline{S0}$	34	11	VCC	84	31
GND	35	12	$\overline{PCS3}$/PIO19	85	62
X1	36	13	$\overline{PCS2}$/PIO18	86	63
X2	37	14	GND	87	64
VCC	38	15	$\overline{PCS1}$/PIO17	88	65
CLKOUTA	39	16	$\overline{PCS0}$/PIO16	89	66
CLKOUTB	40	17	VCC	90	67
GND	41	18	$\overline{MCS2}$/PIO24	91	68
A19/PIO9	42	19	$\overline{MCS3}$/ $\overline{RFSH}$/PIO25	92	69
A18/PIO8	43	20	GND	93	70
VCC	44	21	$\overline{RST}$	94	71
A17/PIO7	45	22	TMRIN1/PIO0	95	72
A16	46	23	TMROUT1/PIO1	96	73
A15	47	24	TMROUT0/PIO10	97	74
A14	48	25	TMRIN0/PIO11	98	75
A13	49	26	DRQ1/PIO13	99	76
A12	50	27	DRQ0/PIO12	100	77

4. Pin Description

I = Input;

O = Output

Pin No.(PQFP)	Symbol	Type	Description
15, 21, 38, 61, 67, 92	VCC	I	System power: +5 volt power supply.
12, 18, 41, 64, 70, 89	GND	I	System ground.
71	$\overline{RST}$	I	Reset input. When $\overline{RST}$ is asserted, the CPU immediately terminates all operations, clears the internal registers & logic, and transfers the address to the reset address FFFF0h.
13	X1	I	Input to the oscillator amplifier.
14	X2	O	Output from the inverted oscillator amplifier.
16	CLKOUTA	O	Clock output A. The CLKOUTA operation is the same as that of crystal input frequency (X1). CLKOUTA remains active during reset and bus hold conditions.
17	CLKOUTB	O	Clock output B. The CLKOUTB operation is the same as that of crystal input frequency (X1). CLKOUTB remains active during reset and bus hold conditions.
Synchronous Serial Port Interface			
1 2	SDEN1/PIO23 SDEN0/PIO22	O/I	Serial data enables. Active-high. These pins enable data transfers of the synchronous serial interface. SDEN1 for port1, SDEN0 for port0.
3	SCLK/PIO20	O/I	Synchronous serial data clock. This pin provides the shift clock to an external device. SCLK=X1/2, 4, 8 or 16, depending on register setting. This pin is held high during the UART inactive.
100	SDATA/PIO21	I/O	Synchronous serial data. This pin delivers shift data to or receives serial data from an external device.
Asynchronous Serial Port Interface			
98	TXD/PIO27	O/I	Transmit data. This pin transmits asynchronous serial data from the UART of the micro-controller.
99	RXD/PIO28	I	Receive data. This pin receives asynchronous serial data.
Bus Interface			
4	$\overline{BHE}$ / $\overline{ADEN}$	O/I	Bus high enable/address enable. During a memory access, the $\overline{BHE}$ and (AD0 or A0) encodings indicate the types of the bus cycle. $\overline{BHE}$ is asserted during T1 and keeps the asserted to T3 and Tw. This pin is floating during bus holds and reset.

$\overline{BHE}$ and (AD0 or A0) Encodings

$\overline{BHE}$	AD0 or A0	Type of Bus Cycle
0	0	Word transfer
0	1	High byte transfer (D15-D8)
1	0	Low byte transfer (D7-D0)
1	1	Refresh

<table>
<tr><td></td><td></td><td></td><td>The address portion of the AD bus can be enabled or disabled by DA bit in the LMCS and UMCS register during LCS or UCS bus cycle access, if $\overline{BHE}$ / $\overline{ADEN}$ is held high during power-on reset. The $\overline{BHE}$ / $\overline{ADEN}$ is with an internal weakly pulled-up resistor, so no external pull-up resistor is required. The AD bus always drives both address and data during LCS or UCS bus cycle access if the $\overline{BHE}$ / $\overline{ADEN}$ pin is with external pull-low resistor during reset.</td></tr>
<tr><td>5</td><td>$\overline{WR}$</td><td>O</td><td>Write strobe. This pin indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active during T2, T3 and Tw of any write cycle, floating during a bus hold or reset.</td></tr>
<tr><td>6</td><td>$\overline{RD}$</td><td>O</td><td>Read Strobe. This active low signal indicates that the micro-controller is performing a memory or I/O read cycle. $\overline{RD}$ is floating during a bus hold or reset.</td></tr>
<tr><td>7</td><td>ALE</td><td>O</td><td>Address latch enable. Active high. This pin indicates that an address output on the AD bus. Address is guaranteed to be valid on the trailing edge of ALE. This pin is tri-stated during ONCE mode and never floats during a bus hold or reset.</td></tr>
<tr><td>8</td><td>ARDY</td><td>I</td><td>Asynchronous ready. This pin performs the microcontroller that the address memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUTA and is active high. The falling edge of ARDY must be synchronized to CLKOUTA. Tie ARDY high, so the microcontroller is always asserted in the ready condition. If the ARDY is not used, tie this pin low to yield control to SRDY.
Both SRDY and ARDY should be tied to high if the system need not assert wait states by externality.</td></tr>
<tr><td>9
10
11</td><td>$\overline{S2}$
$\overline{S1}$
$\overline{S0}$</td><td>O</td><td>Bus cycle status. These pins are encoded to indicate the bus status. $\overline{S2}$ can be used as memory or I/O indicator. $\overline{S1}$ can be used as DT/ $\overline{R}$ indicator. These pins are floating during bus holds and reset.
<table>
<tr><td colspan="4">Bus Cycle Encoding Description</td></tr>
<tr><td>$\overline{S2}$</td><td>$\overline{S1}$</td><td>$\overline{S0}$</td><td>Bus Cycle</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read data from I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write data to I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read data from memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write data to memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
<tr><td>19
20
22
23-37
39, 40</td><td>A19/PIO9
A18/PIO8
A17/PIO7
A16-A2
A1, A0</td><td>O/I</td><td>Address bus. Non-multiplexed memory or I/O addresses. The A bus is one-half of a CLKOUTA period earlier than the AD bus. These pins are high-impedance during bus holds or reset.</td></tr>
<tr><td>78,80,82,84,86,88
91,94</td><td>AD0-AD7
AD8-AD15</td><td>I/O</td><td>The multiplexed address and data bus for memory or I/O accessing. The address is present during the t1 clock</td></tr>
</table>

79,81,83,85,87,90 93,95			phase, and the data bus phase is in t2-t4 cycle. The address phase of the AD bus can be disabled when the $\overline{BHE}$ / $\overline{ADEN}$ pin is with external pull-low resistor during reset. The AD bus is in high-impedance state during bus hold or reset conditions and this bus is also used to load system configuration information (with pull-up or pull-Low resistors) into the F6h register when the reset input goes from low to high.
42	$\overline{WHB}$	O	Write high byte. This pin indicates the high byte data (AD15-AD8) on the bus is to be written to a memory or I/O device. $\overline{WHB}$ is the logic OR of $\overline{BHE}$ and $\overline{WR}$. This pin is floating during reset or bus holds.
43	$\overline{WLB}$	O	Write low byte. This pin indicates the low byte data (AD7-AD0) on the bus is to be written to a memory or I/O device. $\overline{WLB}$ is the logic OR of $\overline{WR}$ and A0. This pin is floating during reset or bus holds.
44	HLDA	O	Bus hold acknowledge. Active high. The micro-controller will issue an HLDA in response to a HOLD request by external bus master at the end of T4 or Ti. When the micro-controller is in hold status (HLDA is high), the AD15-AD0, A19-A0, $\overline{WR}$, $\overline{RD}$, $\overline{DEN}$, $\overline{S0}$ - $\overline{S1}$, S6, $\overline{BHE}$, DT/$\overline{R}$, $\overline{WHB}$ and $\overline{WLB}$ are floating, and $\overline{UCS}$, $\overline{LCS}$, $\overline{PCS6}$ - $\overline{PCS5}$, $\overline{MCS3}$ - $\overline{MCS0}$ and $\overline{PCS3}$ - $\overline{PCS0}$ will be driven high. After HOLD is detected as being low, the micro-controller will lower HLDA.
45	HOLD	I	Bus Hold request. Active high. This pin indicates that another bus master is requesting the local bus.
46	SRDY/PIO6	I/O	Synchronous ready. This pin performs the micro-controller that the address memory space or I/O device will complete a data transfer. The SRDY pin accepts a falling edge that is asynchronous to CLKOUTA and is active high. SRDY is accomplished by elimination of the one-half clock period required to internally synchronize ARDY. Tie SRDY high, so the microcontroller is always asserted in the ready condition. If the SRDY is not used, tie this pin low to yield control to ARDY. Both SRDY and ARDY should be tied to high if the system need not assert wait states by externality.
48	DT/$\overline{R}$ /PIO4	O/I	Data transmit or receive. This pin indicates the direction of data flow through an external data-bus transceiver. When DT/$\overline{R}$ is low, the micro-controller receives data. When DT/R is asserted high, the micro-controller writes data to the data bus.
49	$\overline{DEN}$ /PIO5	O/I	Data enable. This pin is provided as a data bus transceiver output enable. $\overline{DEN}$ is asserted during memory and I/O access. $\overline{DEN}$ is driven high when DT/$\overline{R}$ changes states. It is floating during bus hold or reset conditions.
96	S6/ $\overline{CLKDIV2}$ /PIO29	O/I	Bus cycle status bit6/clock divided by 2. For S6 feature, this pin is low to indicate a micro-controller-initiated bus cycle or high to indicate a DMA-initiated bus cycle during

			T2, T3, Tw and T4. For $\overline{\text{CLKDIV2}}$ feature, the internal clock of micro-controller is the external clock divided by 2 (CLKOUTA, CLKOUTB=X1/2) if this pin held low during power-on reset. The pin is sampled on the rising edge of $\overline{\text{RST}}$.
97	$\overline{\text{UZI}}$ /PIO26	O/I	Upper zero indicate. This pin is the logical OR of the inverted A19-A16. It is asserted in T1 and is held throughout the cycle.
Chip Select Unit Interface			
50 51 68 69	$\overline{\text{MCS0}}$ /PIO14 $\overline{\text{MCS1}}$ /PIO15 $\overline{\text{MCS2}}$ /PIO24 $\overline{\text{MCS3}}$ / $\overline{\text{RFSH}}$ /PIO25	O/I	Midrange memory chip selects. For $\overline{\text{MCS}}$ feature, these pins are active low when MMCS (A6h) register is enabled to access a memory. The address ranges are programmable. $\overline{\text{MCS3}}$ - $\overline{\text{MCS0}}$ are held high during bus hold. When LMCS (A6h) register is being programmed, pin69 is as a $\overline{\text{RFSH}}$ pin to auto refresh the PSRAM.
57	$\overline{\text{UCS}}$ / $\overline{\text{ONCE1}}$	O/I	Upper memory chip select/ONCE mode request 1. For $\overline{\text{UCS}}$ feature, this pin is active low when the system accesses the defined portion memory block of the upper 512K bytes (80000h-FFFFFh) memory region. $\overline{\text{UCS}}$ default active address region is from F0000h to FFFFFh after power-on reset. The address range for $\overline{\text{UCS}}$ is programmed by software. For $\overline{\text{ONCE1}}$ feature, if $\overline{\text{ONCE0}}$ and $\overline{\text{ONCE1}}$ are sampled low on the rising edge of $\overline{\text{RST}}$, the micro-controller enters ONCE mode. In ONCE mode and all pins are high-impedance. This pin incorporates a weakly pull-up resistor.
58	$\overline{\text{LCS}}$ / $\overline{\text{ONCE0}}$	O/I	Lower memory chip select/ONCE mode request 0. For $\overline{\text{LCS}}$ feature, this pin is active low when the micro-controller accesses the defined portion memory block of the lower 512K (00000h-7FFFFh) memory region. The address range for $\overline{\text{LCS}}$ is programmed by software. For $\overline{\text{ONCE0}}$ feature, see $\overline{\text{UCS}}$ / $\overline{\text{ONCE1}}$ description. This pin incorporates a weakly pull-up register.
59 60	$\overline{\text{PCS6}}$ /A2/PIO2 $\overline{\text{PCS5}}$ /A1/PIO3	O/I	Peripheral chip selects/latched address bit. For $\overline{\text{PCS}}$ feature, these pins are active low when the micro-controller accesses the fifth or sixth region of the peripheral memory (I/O or memory space). The base address of $\overline{\text{PCS}}$ is programmable. These pins are asserted with the AD address bus and are not floating during bus holds. For latched address bit feature. These pins output the latched address A2 and A1 when the EX bit is cleared in the $\overline{\text{PCS}}$ and $\overline{\text{MCS}}$ auxiliary register. The A2 and A1 retain previous latched data during bus holds.
62 63 65 66	$\overline{\text{PCS3}}$ /PIO19 $\overline{\text{PCS2}}$ /PIO18 $\overline{\text{PCS1}}$ /PIO17 $\overline{\text{PCS0}}$ /PIO16	O/I	Peripheral chip selects. These pins are active low when the micro-controller accesses the defined memory area of the peripheral memory block (I/O or memory address). For I/O access, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address access, the base address can be

			located in the 1M-byte memory address region. These pins are asserted with the multiplexed AD address bus and are not floating during bus hold.
Interrupt Control Unit Interface			
47	NMI	I	Non-maskable Interrupt. The NMI is the highest priority hardware interrupt and is non-maskable. When this pin is asserted (NMI transition from low to high), the micro-controller always transfers the address bus to the location specified by the non-maskable interrupt vector in the micro-controller interrupt vector table. The NMI pin must be asserted for at least one CLKOUTA period to guarantee that the interrupt is recognized.
52	INT4/PIO30	I/O	Maskable interrupt request 4. Active high. This pin indicates that an interrupt request has occurred. The micro-controller will jump to the INT4 address vector to execute the service routine if the INT4 is enabled. The interrupt input can be configured to be either edge- or level-triggered. The requesting device must hold the INT4 until the request is acknowledged to guarantee interrupt recognition.
53	INT3/ $\overline{\text{INTA1}}$ /IRQ	I/O	Maskable interrupt request 3/interrupt acknowledge 1/slave interrupt request. For INT3 feature, except the differences in interrupt line and interrupt address vector, the function of INT3 is the same as that of INT4. For $\overline{\text{INTA1}}$ feature, in cascade mode or special fully-nested mode, this pin corresponds to INT1. For IRQ feature, when the micro-controller is as a slave device, this pin issues an interrupt request to the master interrupt controller.
54	INT2/ $\overline{\text{INTA0}}$ /PIO31	I/O	Maskable interrupt request 2/interrupt acknowledge 0. For INT2 feature, except the differences in interrupt line and interrupt address vector, the function of INT2 is the same as that of INT4. For $\overline{\text{INTA0}}$ feature, in cascade mode or special fully-nested mode, this pin corresponds to INT0.
55	INT1/ $\overline{\text{SELECT}}$	I/O	Maskable interrupt request 1/slave select. For INT1 feature, except the differences in interrupt line and interrupt address vector, the function of INT1 is the same as that of INT4. For $\overline{\text{SELECT}}$ feature, when the micro-controller is as a slave device, this pin is driven from the master interrupt controller decoding. This pin is activated to indicate that an interrupt appears on the address and data bus. The INT0 must be activated before $\overline{\text{SELECT}}$ is activated when the interrupt type appears on the bus.
56	INT0	I	Maskable interrupt request 0. Except the interrupt line and interrupt address vector, the function of INT0 is the same as that of INT4.
Timer Control Unit Interface			
72 75	TMRIN1/PIO0 TMRIN0/PIO11	I/O	Timer input. These pins can be used as clock or control signal input, depending upon the programmed timer mode. After internally synchronizing low to high transitions on TMRIN, the timer controller increments. These pins must be pulled up if not being used.
73	TMROUT1/PIO1	O/I	Timer output. Depending on timer mode select, these

74	TMROUT0/PIO10		pins provide single pulse or continuous waveforms. The duty cycle of the waveforms is programmable. These pins float during a bus hold or reset.
DMA Unit Interface			
76 77	DRQ1/PIO13 DRQ0/PIO12	/O	DMA request. These pins are asserted high by an external device when the device is ready for DMA channel 1 or channel 0 to perform a transfer. These pins are level-triggered and internally synchronized. The DRQ signals are not latched and must remain active until finish being serviced.

Notes:

1. When PIO mode and direction registers are set, 32 MUX definition pins can be as PIO pins. For example, the DRQ1/PIO13 (pin76) can be as a PIO13.

2. The PIO status during Power-On reset: PIO1, PIO10, PIO22, and PIO23 are input with pull-down, PIO4 to PIO9 are in normal operations and the others are input with pull-up.

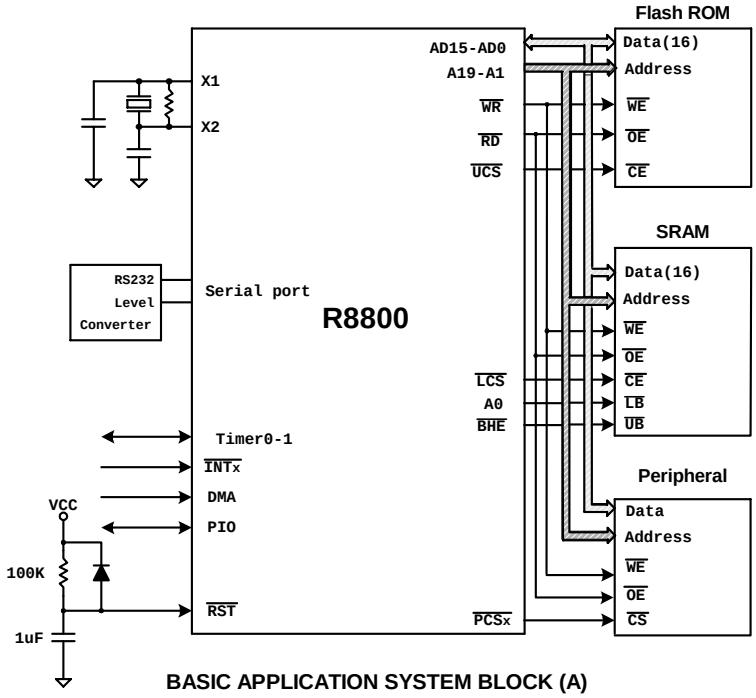
4.1 R8800 I/O Characteristics of Each Pin

PQFP Pin No.	Pin Name	Characteristics
71	$\overline{\text{RST}}$	Schmitt Trigger input, with a 50K internal pull-up resistor
8	ARDY	Schmitt Trigger input, with a 50K internal pull-down resistor
45 47	HOLD NMI	CMOS input, with a 50K internal pull-down resistor
56 55	INT0 INT1/$\overline{\text{SELECT}}$	Schmitt Trigger TTL input, with a 10K internal pull-down resistor
16 17	CLKOUTA CLKOUTB	8mA 3-State CMOS output
9	$\overline{\text{S2}}$	Bi-directional I/O, with a 50 K internal pull-up resistor 4mA TTL output
10 11	$\overline{\text{S1}}$ $\overline{\text{S0}}$	4mA 3-State CMOS output
43 6 5	$\overline{\text{WLB}}$ $\overline{\text{RD}}$ $\overline{\text{WR}}$	12mA 3-State CMOS output
19 20 22	A19/PIO9 A18/PIO8 A17/PIO7	Bi-directional I/O, with an enabled/disabled 10 K internal pull-up resistor when functioning as PIO, for normal function, the 10k pull-up resistor is disabled. 16mA TTL output

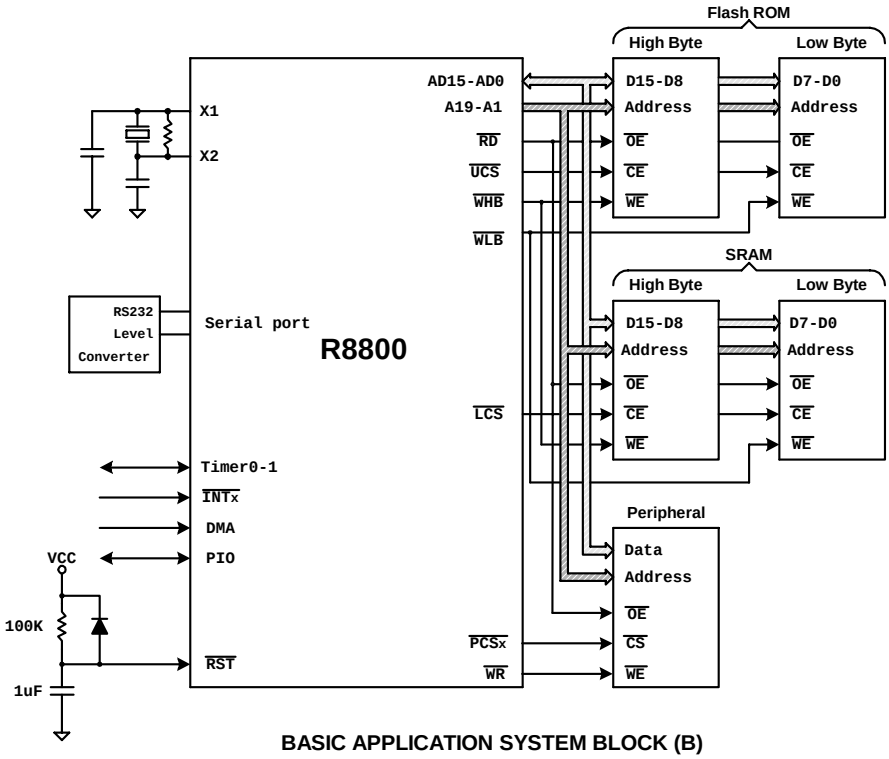
PQFP Pin No.	Pin Name	Characteristics
23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 39 40	A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	16mA 3-State CMOS output
78 80 82 84 86 88 91 94 79 81 83 85 87 90 93 95	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15	Bi-directional I/O, 16mA TTL output
7	ALE	Bi-directional I/O, with a 50 K internal pull-down resistor 4mA TTL output
46 74 73 2 1	SRDY/PIO6 TMROUT0/PIO10 TMROUT1/PIO1 SDEN0/PIO22 SDEN1/PIO23	Bi-directional I/O, with an enabled/disabled 10 K internal pull-down resistor when functioning as PIO, for normal function, the 10k pull-down resistor is disabled. 8mA TTL output
4	$\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$	Bi-directional I/O, with a 50 K internal pull-up resistor 4mA TTL output
42	$\overline{\text{WHB}}$	Bi-directional I/O, with a 50 K internal pull-up resistor 12mA TTL output
44	HLDA	4mA CMOS output
54 52	INT2/$\overline{\text{INTA0}}$/PIO31 INT4/PIO30	Bi-directional I/O, with an enabled/disabled 10 K internal pull-up resistor when functioning as PIO, for normal function, the 10k pull-up resistor is disabled. 8mA TTL output, TTL Schmitt Trigger input

PQFP Pin No.	Pin Name	Characteristics
53	INT3/$\overline{\text{INTA1}}$/IRQ	Bi-directional I/O, with a 10 K internal pull-up resistor 8mA TTL output, TTL Schmitt Trigger input
57 58	$\overline{\text{UCS}}$/$\overline{\text{ONCE1}}$ $\overline{\text{LCS}}$/$\overline{\text{ONCE0}}$	Bi-directional I/O, with a 10 K internal pull-up resistor 8mA TTL output, TTL Schmitt Trigger input
49 48 66 65 63 62 60 59 50 51 68 69 97 96 75 72 77 76 98 99 100 3	$\overline{\text{DEN}}$/PIO5 DT/$\overline{\text{R}}$/PIO4 $\overline{\text{PCS0}}$/PIO16 $\overline{\text{PCS1}}$/PIO17 $\overline{\text{PCS2}}$/PIO18 $\overline{\text{PCS3}}$/PIO19 $\overline{\text{PCS5}}$/A1/PIO3 $\overline{\text{PCS6}}$/A2/PIO2 $\overline{\text{MCS0}}$/PIO14 $\overline{\text{MCS1}}$/PIO15 $\overline{\text{MCS2}}$/PIO24 $\overline{\text{MCS3}}$/$\overline{\text{RFSH}}$/PIO25 $\overline{\text{UZI}}$/PIO26 S6/$\overline{\text{CLKDIV2}}$/PIO29 TMRIN0/PIO11 TMRIN1/PIO0 DRQ0/PIO12 DRQ1/PIO13 TXD/PIO27 RXD/PIO28 SDATA/PIO21 SCLK/PIO20	Bi-directional I/O, with an enabled/disabled 10 K internal pull-up resistor when functioning as PIO, for normal function, the 10k pull-up resistor is disabled. 8mA TTL output

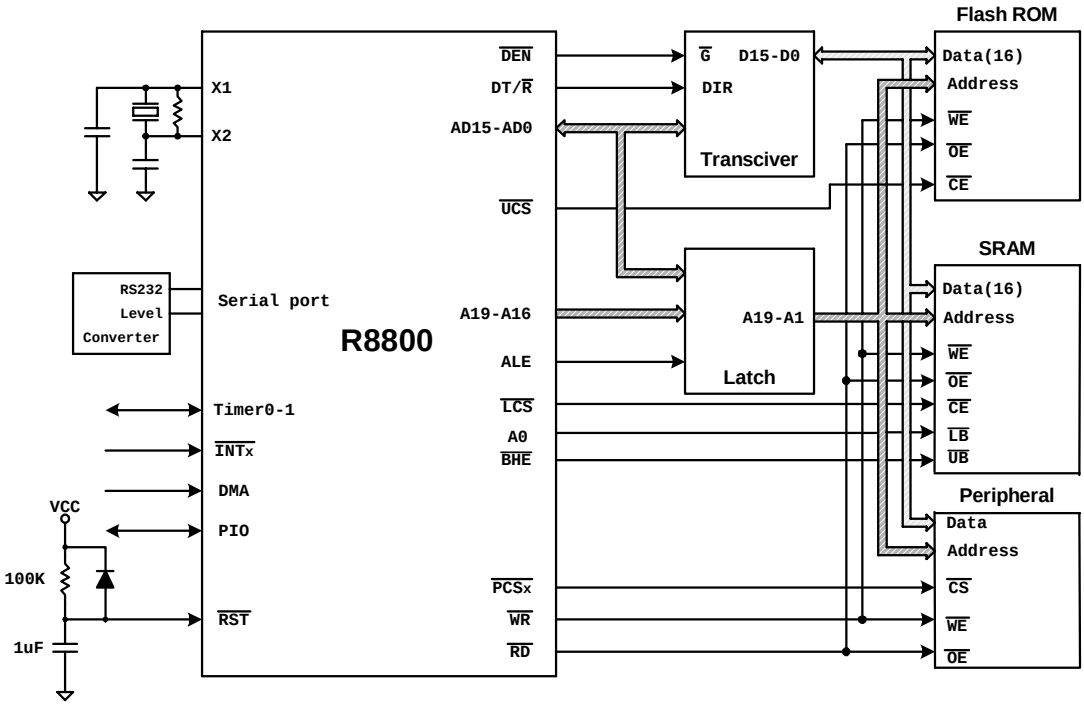
5. Basic Application System Block



BASIC APPLICATION SYSTEM BLOCK (A)

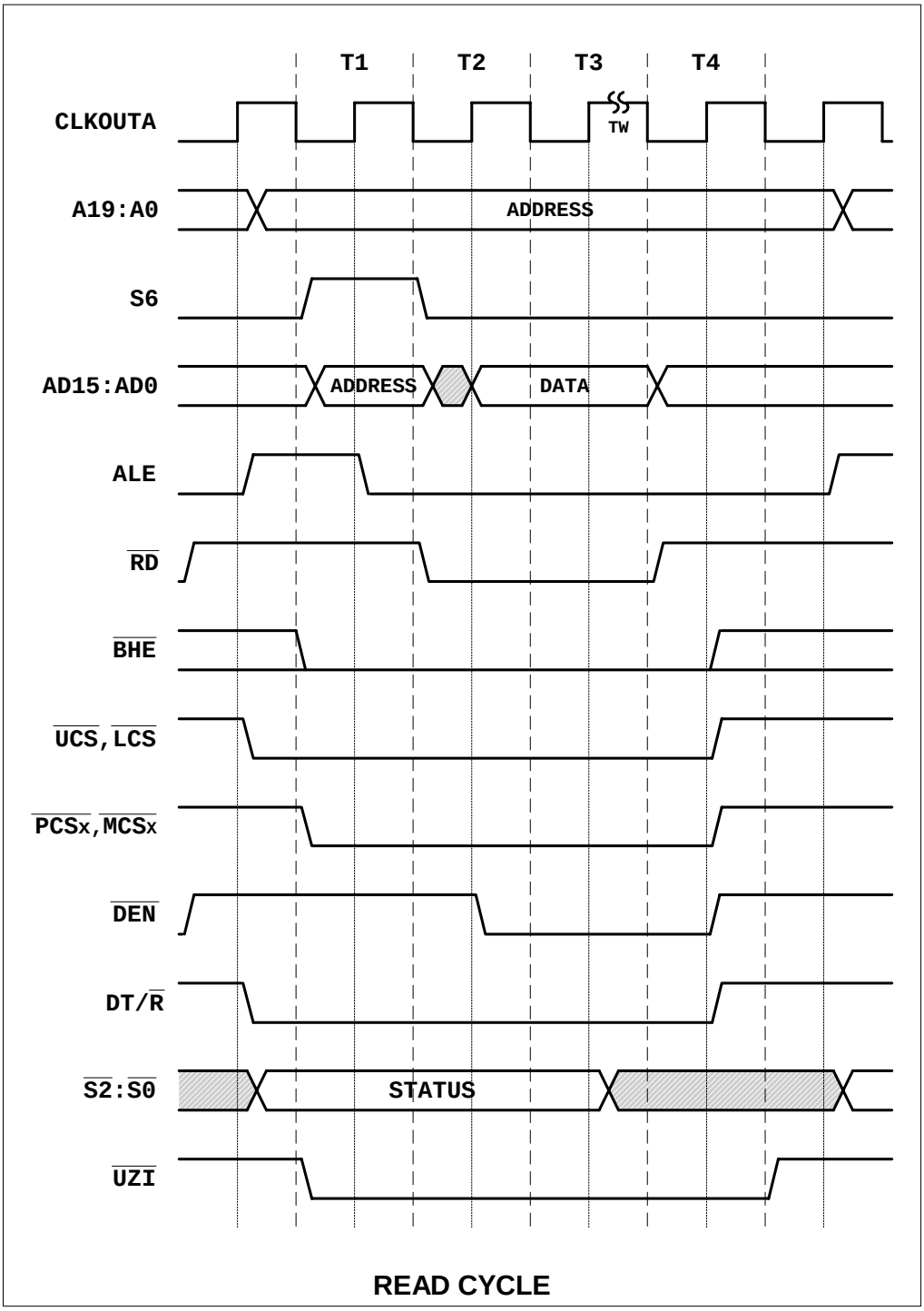


BASIC APPLICATION SYSTEM BLOCK (B)

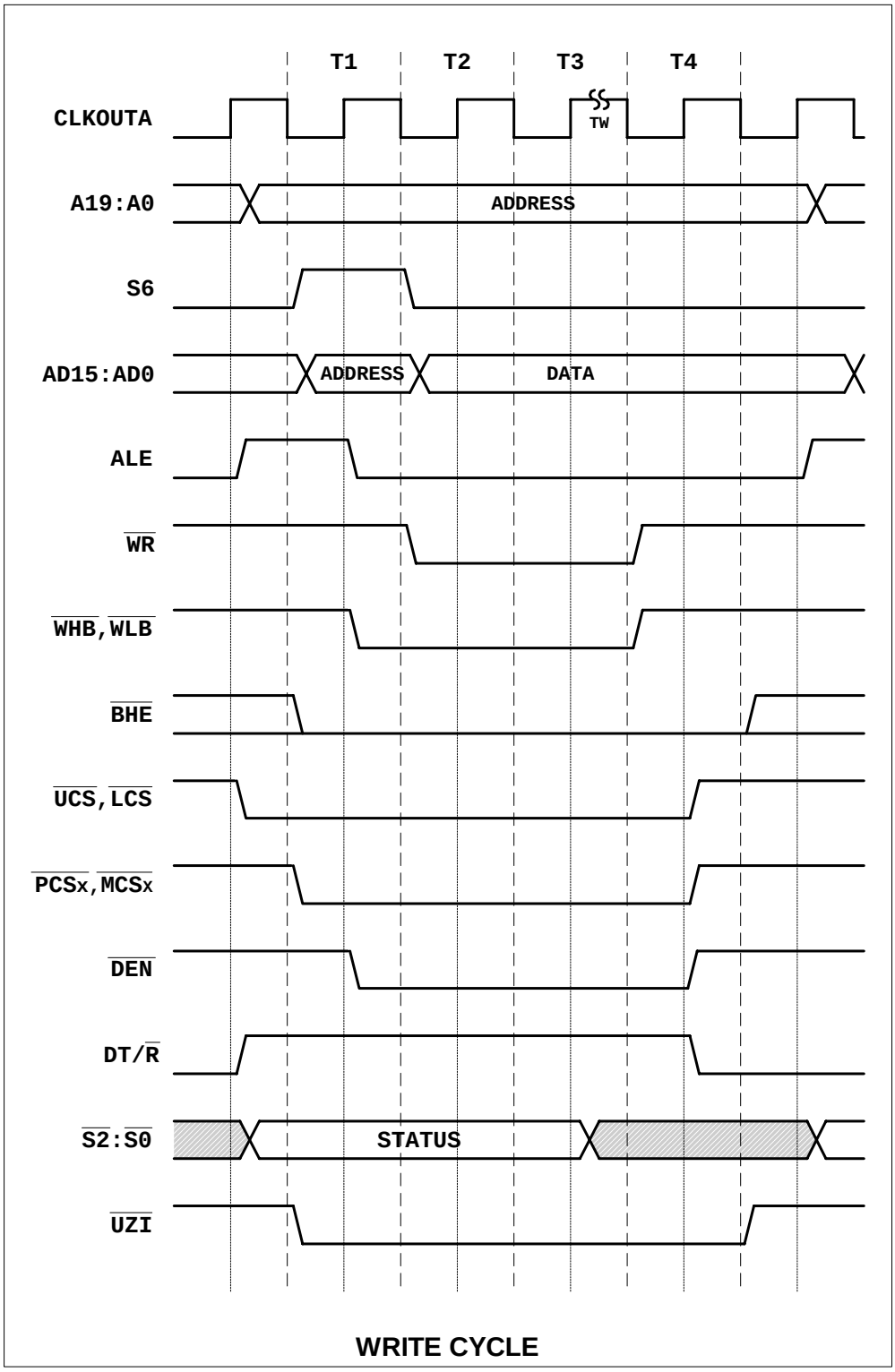


BASIC APPLICATION SYSTEM BLOCK (C)

6. Read/Write Timing Diagram

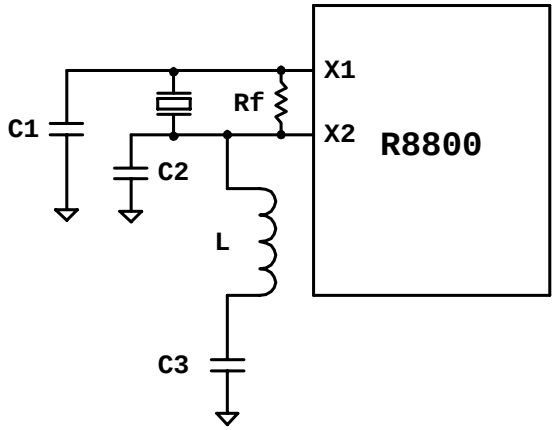


READ CYCLE


T1
T2
T3
T4
TW
CLKOUTA
A19:A0
ADDRESS
S6
AD15:AD0
ADDRESS
DATA
ALE
WR
WHB, WLB
BHE
UCS, LCS
PCSx, MCSx
DEN
DT/R
S2:S0
STATUS
UZI

WRITE CYCLE

7. Crystal Characteristics



For fundamental-mode crystal:

Reference values

Frequency	10.8288MHz	19.66MHz	30MHz	33MHz	40MHz
Rf	None	None	None	None	None
C1	10Pf	10Pf	None	None	None
C2	10Pf	10Pf	10Pf	10Pf	10Pf
C3	None	None	None	None	None
L	None	None	None	None	None

For third-overtone mode crystal:

Reference values

Frequency	22.1184MHz	28.322MHz	33.177MHz	40MHz
Rf	1M	1.5M	1.5M	1.5M
C1	15Pf	15Pf	15Pf	15Pf
C2	30Pf	30Pf	30Pf	30Pf
C3	None	220Pf	220Pf	220Pf
L	None	10uL	4.7uL	2.7uL

8. Execution Unit

8.1 General Registers

The R8800 has eight 16-bit general registers. And the AX, BX, CX and DX can be subdivided into two 8-bit registers (AH, AL, BH, BL, CH, CL, DH and DL). The functions of these registers are described as follows.

AX: Word Divide, Word Multiply, Word I/O operation.

AL: Byte Divide, Byte Multiply, Byte I/O, Decimal Arithmetic, Translate operation.

AH: Byte Divide, Byte Multiply operation.

BX: Translate operation.

CX: Loops, String operation

CL: Variable Shift and Rotate operation.

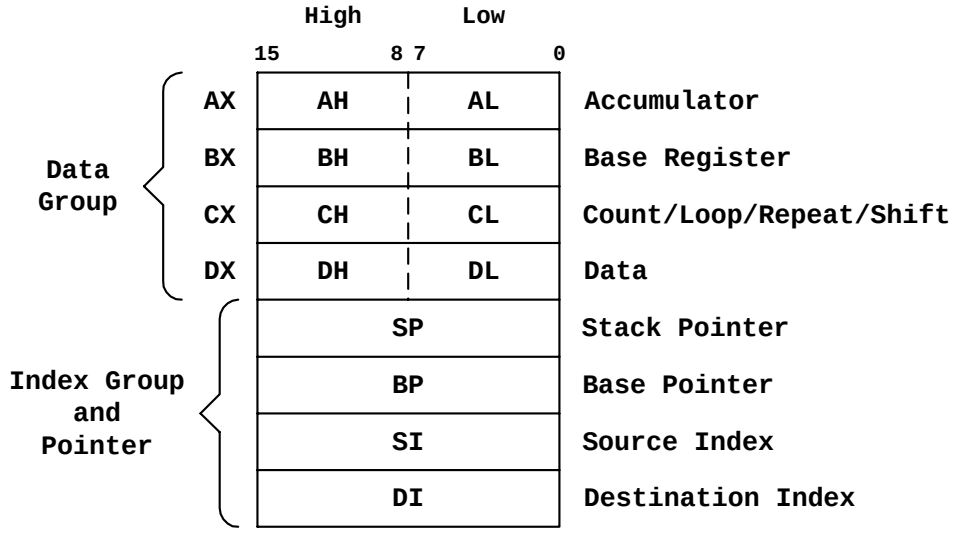
DX: Word Divide , Word Multiply, Indirect I/O operation

SP: Stack operations (POP, POPA, POPF, PUSH, PUSHA, PUSHF)

BP: General-purpose registers which can be used to determine offset address of operands in Memory.

SI: String operations

DI: String operations



GENERAL REGISTERS

8.2 Segment Registers

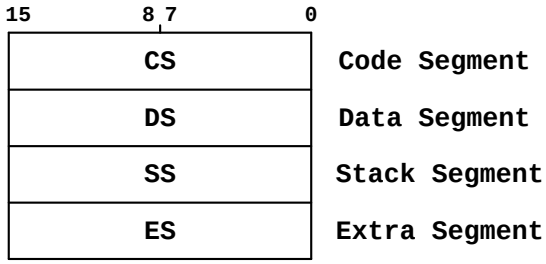
R8800 has four 16-bit segment registers, CS, DS, SS and ES. The segment registers contain the base addresses (starting location) of these memory segments, and they are immediately addressable for code (CS), data (DS & ES), and stack (SS) memory.

CS (Code Segment): The CS register points to the current code segment, which contains instruction to be fetched. The default location memory space for all instruction is 64K. The initial value of CS register is 0FFFFh.

DS (Data Segment): The DS register points to the current data segment, which generally contains program variables. The DS register is initialized to 0000h.

SS (Stack Segment): The SS register points to the current stack segment, which is for all stack operations, such as pushes and pops. The stack segment is used for temporary space. The SS register is initialized to 0000h.

ES (Extra Segment): The ES register points to the current extra segment which is typically for data storage, such as large string operations and large data structures. The ES register is initialized to 0000h.



SEGMENT REGISTERS

8.3 Instruction Pointer and Status Flags Registers

IP (Instruction Pointer): The IP is a 16-bit register and contains the offset of the next instruction to be fetched. The IP register cannot be directly accessed by software and is updated by Bus Interface Unit. This register can be changed, saved or restored as a result of program execution. It is initialized to 0000h and the CS:IP starting execution address is at 0FFFF0h.

Processor Status Flags Registers **FLAGS**

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				OF	DF	IF	TF	SF	ZF	Res	AF	Res	PF	Res	CF

These flags reflect the status after the Execution Unit is executed.

Bit 15-12: Reserved

Bit 11: OF, Overflow Flag. An arithmetic overflow occurs, this flag will be set.

Bit 10: DF, Direction Flag. If this flag is set, the string instructions are in the process of incrementing address. If DF is cleared, the string instructions are in the process of decrementing address. Refer to the STD and CLD instructions for setting and clearing the DF flag.

Bit 9: IF, Interrupt-Enable Flag. Refer to the STI and CLI instructions for setting and clearing the IF flag.

Set 1: The CPU enables the maskable interrupt request.

Set 0: The CPU disables the maskable interrupt request.

Bit 8: TF, Trace Flag. Set to enable single-step mode for debugging; Clear to disable the single-step mode. If an application program sets the TF flag with POPF or IRET instruction, a debug exception is generated after the instruction (The CPU automatically generates an interrupt after each instruction) that follows the POPF or IRET instruction.

Bit 7: SF, Sign Flag. If this flag is set, the high-order bit of the result of an operation is 1,indicating it is negative.

Bit 6: ZF, Zero Flag. If this flag is set, the result of operation is zero.

Bit 5: Reserved

Bit 4: AF, Auxiliary Flag. If this flag is set, there will be a carry from the low nibble to the high one or a borrow from the high nibble to the low nibble of the AL general-purpose register. It is used in BCD operation.

Bit 3: Reserved.

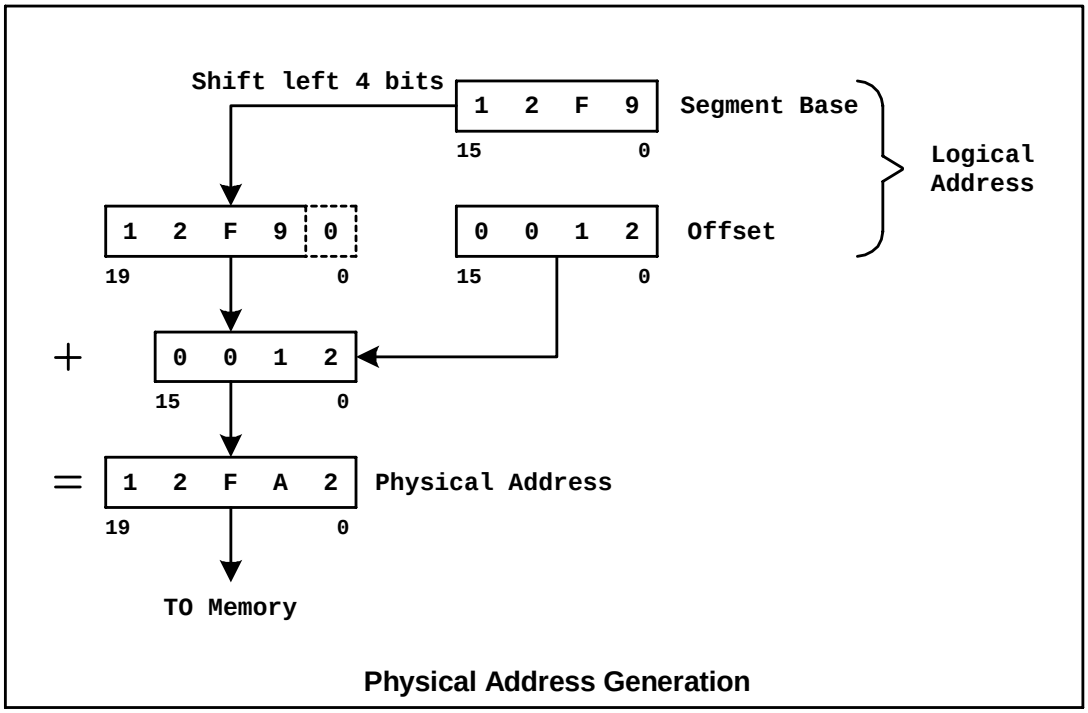
Bit 2: PF, Parity Flag. This flag will be set if the result of low-order 8-bit operation has even parity.

Bit 1: Reserved

Bit 0: CF, Carry Flag. If CF is set, there will be a carry out or a borrow into the high-order bit of the instruction result.

8.4 Address Generation

The Execution Unit generates a 20-bit physical address to Bus Interface Unit by the Address Generation. Memory is organized in sets of segments. Each segment contains a 16-bit value. Memory is addressed with a two-component address that consists of a 16-bit segment and 16-bit offset. The Physical Address Generation figure describes how the logical address is transferred to the physical address.



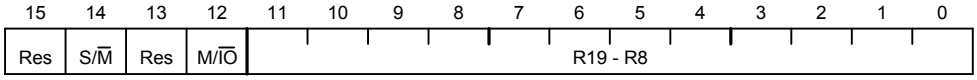
Physical Address Generation

9. Peripheral Control Block Registers

The peripheral control block can be mapped into either memory or I/O space by programming the FEh register. And it starts at FF00h in I/O space when the microprocessor is reset. The following table lists the definitions of all the Peripheral Control Block Registers, and the detailed descriptions will be arranged on the related Block Unit.

Offset (HEX)	Register Name	Page	Offset (HEX)	Register Name	Page
FE	Peripheral Control Block Relocation Register	28	66	Timer 2 Mode / Control Register	70
FA	Disable Peripheral Clock Register	31	62	Timer 2 Maxcount Compare A Register	71
F6	Reset Configuration Register	33	60	Timer 2 Count Register	71
F4	Processor Release Level Register	28	5E	Timer 1 Mode / Control Register	69
F0	Power-Save Control Register	30	5C	Timer 1 Maxcount Compare B Register	70
E4	Enable RCU Register	84	5A	Timer 1 Maxcount Compare A Register	70
E2	Clock Pre-caler Register	84	58	Timer 1 Count Register	70
E0	Memory Partition Register	84	56	Timer 0 Mode / Control Register	67
DA	DMA 1 Control Register	64	54	Timer 0 Maxcount Compare B Register	69
D8	DMA 1 Transfer Count Register	64	52	Timer 0 Maxcount Compare A Register	69
D6	DMA 1 Destination Address High Register	65	50	Timer 0 Count Register	69
D4	DMA 1 Destination Address Low Register	65	46	Power Down Configuration Register	31
D2	DMA 1 Source Address High Register	65	44	Serial Port Interrupt Control Register	47
D0	DMA 1 Source Address Low Register	65	42	Watchdog Timer Control Register	72
CA	DMA 0 Control Register	61	40	INT4 Control Register	47
C8	DMA 0 Transfer Count Register	63	3E	INT3 Control Register	48
C6	DMA 0 Destination Address High Register	63	3C	INT2 Control Register	48
C4	DMA 0 Destination Address Low Register	63	3A	INT1 Control Register	49
C2	DMA 0 Source Address High Register	64	38	INT0 Control Register	50
C0	DMA 0 Source Address Low Register	64	36	DMA 1 Interrupt Control Register	51
A8	$\overline{\text{PCS}}$ and $\overline{\text{MCS}}$ Auxiliary Register	41	34	DMA 0 Interrupt Control Register	51
A6	Midrange Memory Chip Select Register	40	32	Timer Interrupt Control Register	52
A4	Peripheral Chip Select Register	42	30	Interrupt Status Register	53
A2	Low Memory Chip Select Register	39	2E	Interrupt Request Register	53
A0	Upper Memory Chip Select Register	38	2C	Interrupt In-service Register	54
88	Serial Port Baud Rate Divisor Register	76	2A	Priority Mask Register	56
86	Serial Port Receive Register	75	28	Interrupt Mask Register	57
84	Serial Port Transmit Register	75	26	Poll Status Register	58
82	Serial Port Status Register	74	24	Poll Register	58
80	Serial Port Control Register	73	22	End-of-Interrupt Register	59
7A	PIO Data 1 Register	82	20	Interrupt Vector Register	59
78	PIO Direction 1 Register	82	18	Synchronous Serial Receive Register	79
76	PIO Mode 1 Register	83	16	Synchronous Serial Transmit 0 Register	78
74	PIO Data 0 Register	83	14	Synchronous Serial Transmit 1 Register	78
72	PIO Direction 0 Register	83	12	Synchronous Serial Enable Register	77
70	PIO Mode 0 Register	83	10	Synchronous Serial Status Register	77

Peripheral Control Block Relocation Register: **Offset : FEh**
Reset Value : 20FFh



The peripheral control block can be mapped into either memory or I/O space by programming this register. When the other chip selects ($\overline{PCSx}$ or $\overline{MCSx}$) are programmed to zero wait state and the external ready is ignored, the $\overline{PCSx}$ or $\overline{MCSx}$ can overlap the control block.

Bit 15: Reserved

Bit 14: S/$\overline{M}$, Slave/Master – Configures the interrupt controller

Set 0 : Master mode; Set 1: Slaved mode

Bit 13: Reserved

Bit 12: M/$\overline{IO}$, Memory/IO space. At reset, this bit is set to 0 and the PCB map starts at FF00h in I/O space.

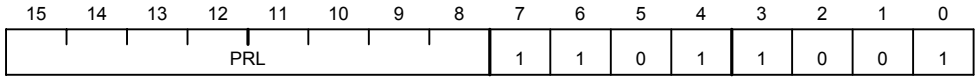
Set 1- The peripheral control block (PCB) is located in memory space.

Set 0- The PCB is located in I/O space.

Bit 11-0: R19-R8, Relocation Address Bits

The upper address bits of the PCB base address. Defaults for the lower eight bits are 00h. When the PCB is mapped to I/O space, the R19-R16 must be programmed to 0000b.

Processor Release Level Register **Offset : F4h**
Reset Value : –D9h



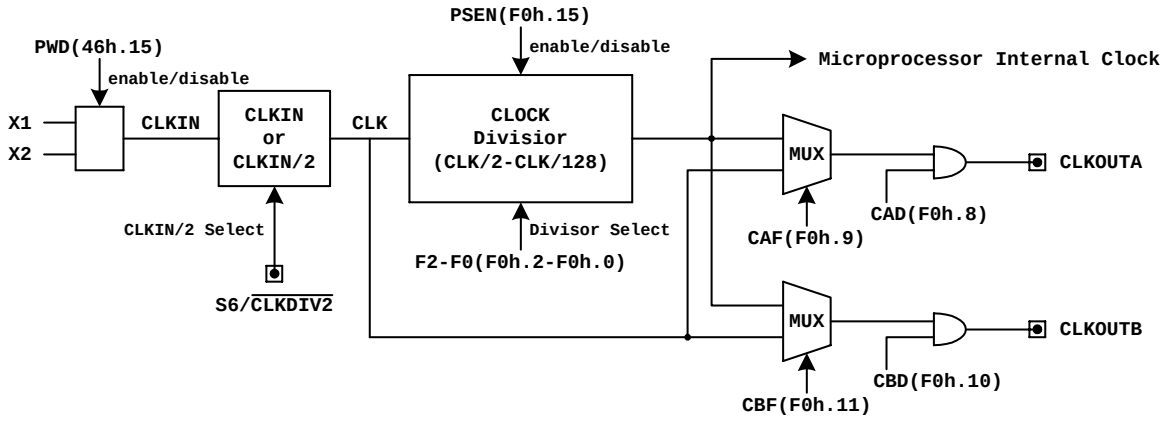
The read only register specifies the processor release version and RDC identification number

Bit 15-8: Processor version

01h: version A, 02h: version B, 03h: version C, 04h: version D

Bit 7-0: RDC identification number - D9h

10. Power Save & Power Down



System Clock

The CPU provides power-save & power-down function.

*** Power-Save:**

In power-save mode, users can program the Power-Save Control Register to divide the internal operating clock. Users can also disable each non-use peripheral clock by programming the Disable Peripheral Clock Register.

*** Power-Down:**

This CPU can enter power-down mode (stop clock) when the Power Down Configuration Register is programmed during the CPU is running in full speed mode or power-save mode. The CPU will be waked up when each one of the external INT0, INT1, INT2, INT3, and INT4 pins is active high and the CPU operating clock will get back to full speed mode if the INT is serviced (the interrupt flag is enabled). If the interrupt flag is disabled, the CPU will be waked up by INT, the operating clock will get back to the previous operating clock state, and the CPU will execute the next program counter instruction. There is 19-bit counter time waiting the crystal clock to be stable when the CPU wakes up from stop clock mode.

Power-Save Control Register

Offset : F0h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSEN	MCSBIT	0	0	CBF	CBD	CAF	CAD	0	0	0	0	0	F2	F1	F0

Bit 15: PSEN, Enable Power-save Mode. This bit is cleared by hardware when an external interrupt occurs. This bit will not be changed when software interrupts (INT instruction) and exceptions occur.

Set 1: enables power-save mode and divides the internal operating clock by the value in F2-F0.

Bit14: MCSBIT, $\overline{\text{MCS0}}$ control bit.

Set 0: $\overline{\text{MCS0}}$ operates normally. Set 1: $\overline{\text{MCS0}}$ is active over the entire $\overline{\text{MCSx}}$ range

Bit13-12: Reserved

Bit 11: CBF, CLKOUTB Output Frequency selection.

Set 1: CLKOUTB output frequency is the same as crystal input frequency.

Set 0: CLKOUTB output frequency is from the clock divisor, which is the same as that of microprocessor's internal clock.

Bit 10: CBD, CLKOUTB Drive Disable

Set 1: Disable the CLKOUTB. This pin will be three-stated. Set 0 : Enable the CLKOUTB.

Bit 9: CAF, CLKOUTA Output Frequency selection.

Set 1: CLKOUTA output frequency is the same as crystal input frequency.

Set 0: CLKOUTA output frequency is from the clock divisor, which is the same as that of microprocessor's internal clock .

Bit 8: CAD, CLKOUTA Drive Disable.

Set 1: Disable the CLKOUTA. This pin will be three-stated.

Set 0: Enable the CLKOUTA.

Bit 7-3: Reserved

Bit 2-0: F2- F0, Clock Divisor Select.

F2,	F1,	F0	-----	Divider Factor
0,	0,	0	----	Divided by 1
0,	0,	1	----	Divided by 2
0,	1,	0	----	Divided by 4
0,	1,	1	----	Divided by 8
1,	0,	0	----	Divided by 16
1,	0,	1	----	Divided by 32
1,	1,	0	----	Divided by 64
1,	1,	1	----	Divided by 128

Disable Peripheral Clock Register

Offset : FAh
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IntClk	UART Clk	DMA Clk	Timer Clk	Reserved											

Bit 15: Int Clk. Set 1 to stop the Interrupt controller clock

Bit 14: UART Clk. Set 1 to stop the asynchronous serial port controller clock

Bit 13: DMA Clk. Set 1 to stop the DMA controller clock

Bit 12: Timer Clk. Set 1 to stop the Timer controller clock

Bit 11-0: Reserved

Power Down Configuration Register

Offset : 46h
Reset Value : 00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWD	0	0	0	0	0	0	WIF	0	0	0	I4	I3	I2	I1	I0

Bit 15: PWD, Power- Down Enable. When this bit is set to 1, the CPU will enter power-down mode and the crystal clock will stop. The CPU will be waked up when an external INT (INT0 – INT4) is active high. It will wait 19-bit counter time for the crystal clock to be stable before the CPU is waked up.

Bit 14-9: Reserved

Bit 8: WIF, Wake-up Interrupt Flag. Read only bit. When the CPU is waked up by interrupt from power-down mode, this bit will be set to 1 by hardware. Otherwise this bit is 0.

Bit 7-5: Reserved

Bit 4-0: I4 -I0, Enable the external interrupt (INT4 – INT0) wake-up function.
Set these bits to 1 to make the INT pins function as power-down wake-up pins.

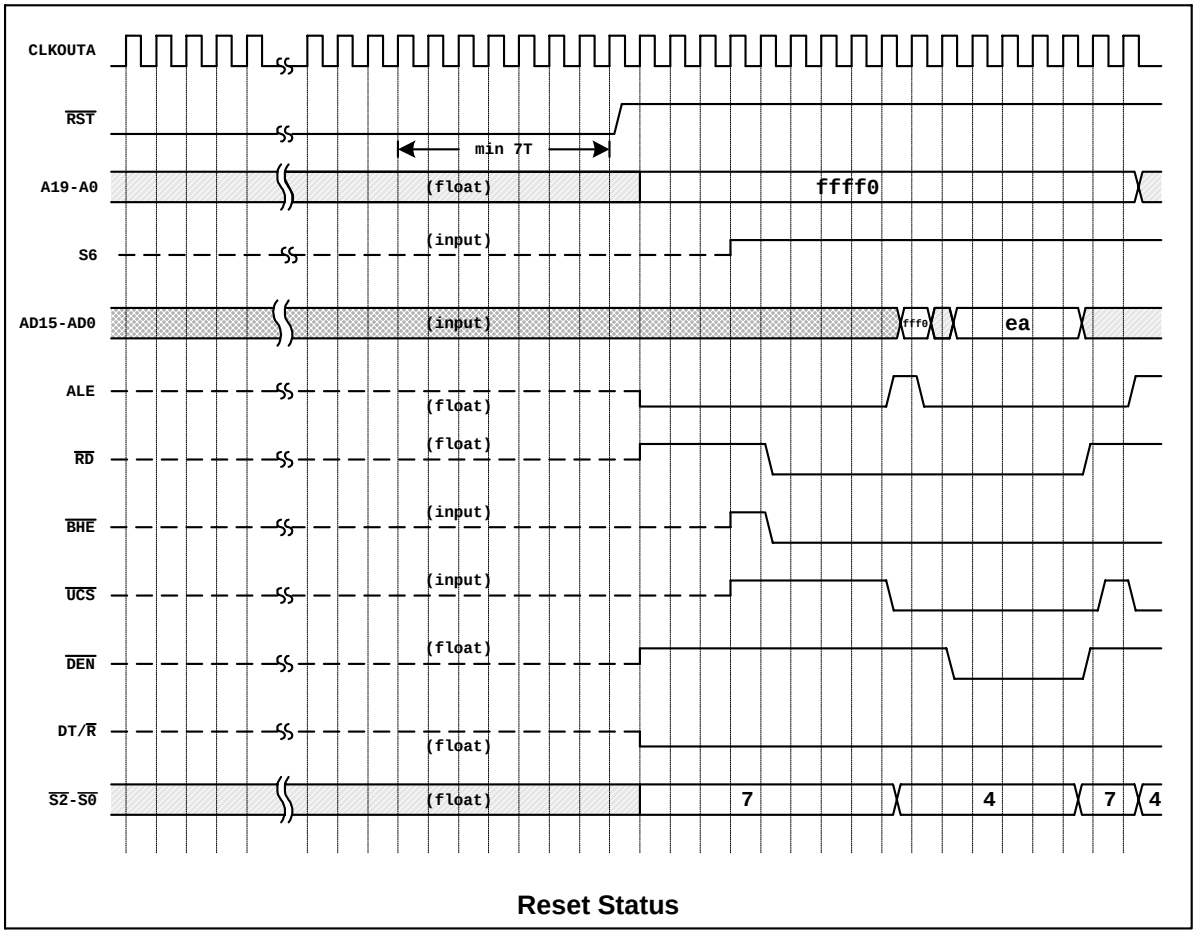
---

11. Reset

Processor initialization is accomplished with activation of the $\overline{RST}$ pin. To reset the processor, this pin should be held low for at least seven oscillator periods. The Reset Status Figure shows the status of the $\overline{RST}$ pin and other related pins.

When $\overline{RST}$ goes from low to high, the state of input pin (with a weakly pulled-up or pulled-down) will be latched, and each pin will perform the individual function. The AD15-AD0 will be latched into the register F6h.

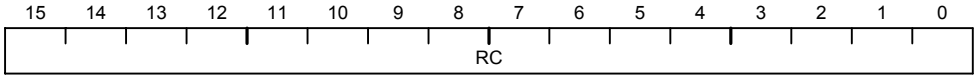
$\overline{UCS}/\overline{ONCE1}$ and $\overline{LCS}/\overline{ONCE0}$ will enter ONCE mode (All of the pins will float except X1 and X2) when they are with pull-low resistors. The input clock will be divided by 2 when S6/$\overline{CLKDIV2}$ is with a pull-low resistor. The AD15-AD0 bus will drive both of the address and data regardless of the DA bit setting during $\overline{UCS}$ and $\overline{LCS}$ cycles if $\overline{BHE}/\overline{ADEN}$ is with a pull-low resistor



Reset Status

Reset Configuration Register

Offset : F6h
Reset Value : AD15-AD0



Bit 15- 0: RC, Reset Configuration AD15 – AD0.

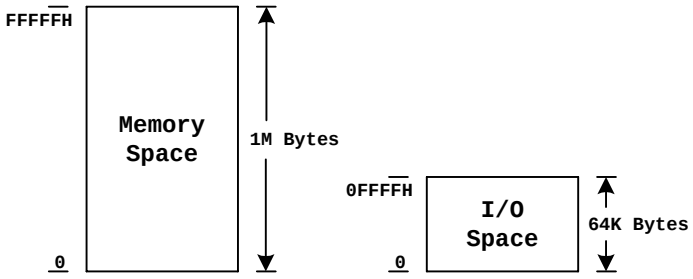
The AD15 to AD0 must be with weakly pulled-up or pulled-down resistors to correspond to the contents when they are latched into this register as the $\overline{\text{RST}}$ pin goes from low to high. And the value of the reset configuration register provides the system information when this register is read by software. This register is read only and the contents remain valid until next processor reset.

12. Bus Interface Unit

In order to define a bus cycle, the bus interface unit drives address, data, status and control information. The bus A19-A0 are non-multiplexed memory or I/O addresses. The AD15-AD0 are multiplexed addresses and data bus for memory or I/O accessing. The $\overline{S2}$-$\overline{S0}$ are encoded to indicate the bus status, which is described in the Pin Description table in page 11. The Basic Application System Block (page 18) and Read/Write Timing Diagram (page 20) describe the basic bus operations.

12.1 Memory and I/O Interface

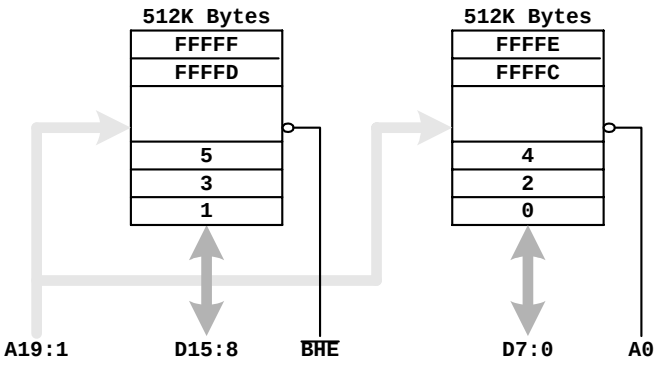
The memory space consists of 1M bytes (512k 16-bit port) and the I/O space consists of 64k bytes (32k 16-bit port). Memory devices exchange information with the CPU during memory read, memory write and instruction fetch bus cycles. I/O read and I/O write bus cycles use a separate I/O address space. Only IN/OUT instruction can access I/O address space, and information must be transferred between the peripheral devices and the AX register. The first 256 bytes of I/O space can be accessed directly by the I/O instructions. The entire 64k bytes of I/O address space can be accessed indirectly, through the DX register. I/O instructions always force address A19-A16 to low level.



Memory and I/O Space

12.2 Data Bus

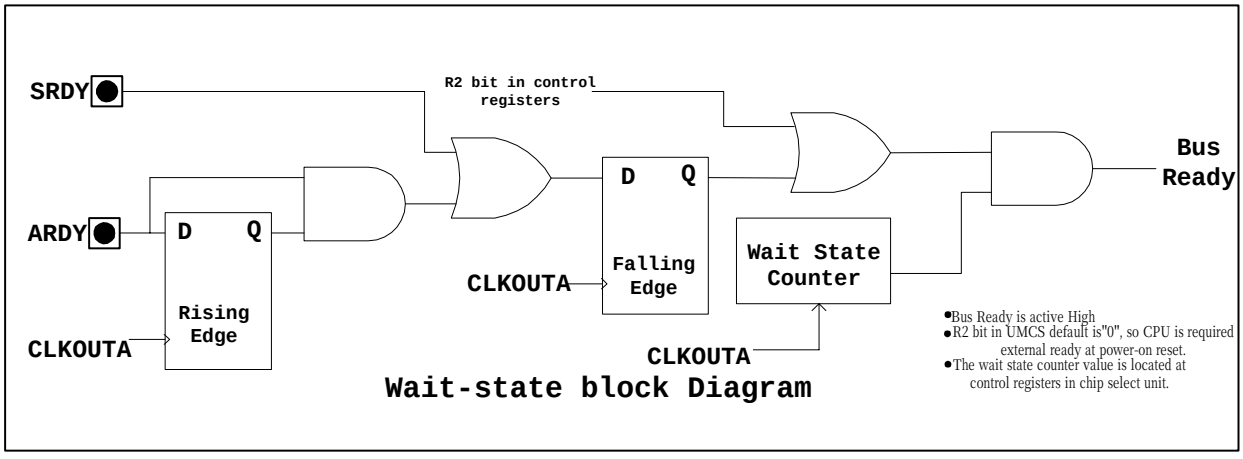
The memory address space data bus is physically implemented by dividing the address space into two banks of up to 512k bytes. One bank connects to the lower half of the data bus and contains the even-addressed bytes (A0=0), the other bank connects to the upper half of the data bus and contains odd-addressed bytes (A0=1). A0 and BHE determine whether one bank or both banks participate in the data transfer.



Physical Data Bus Models

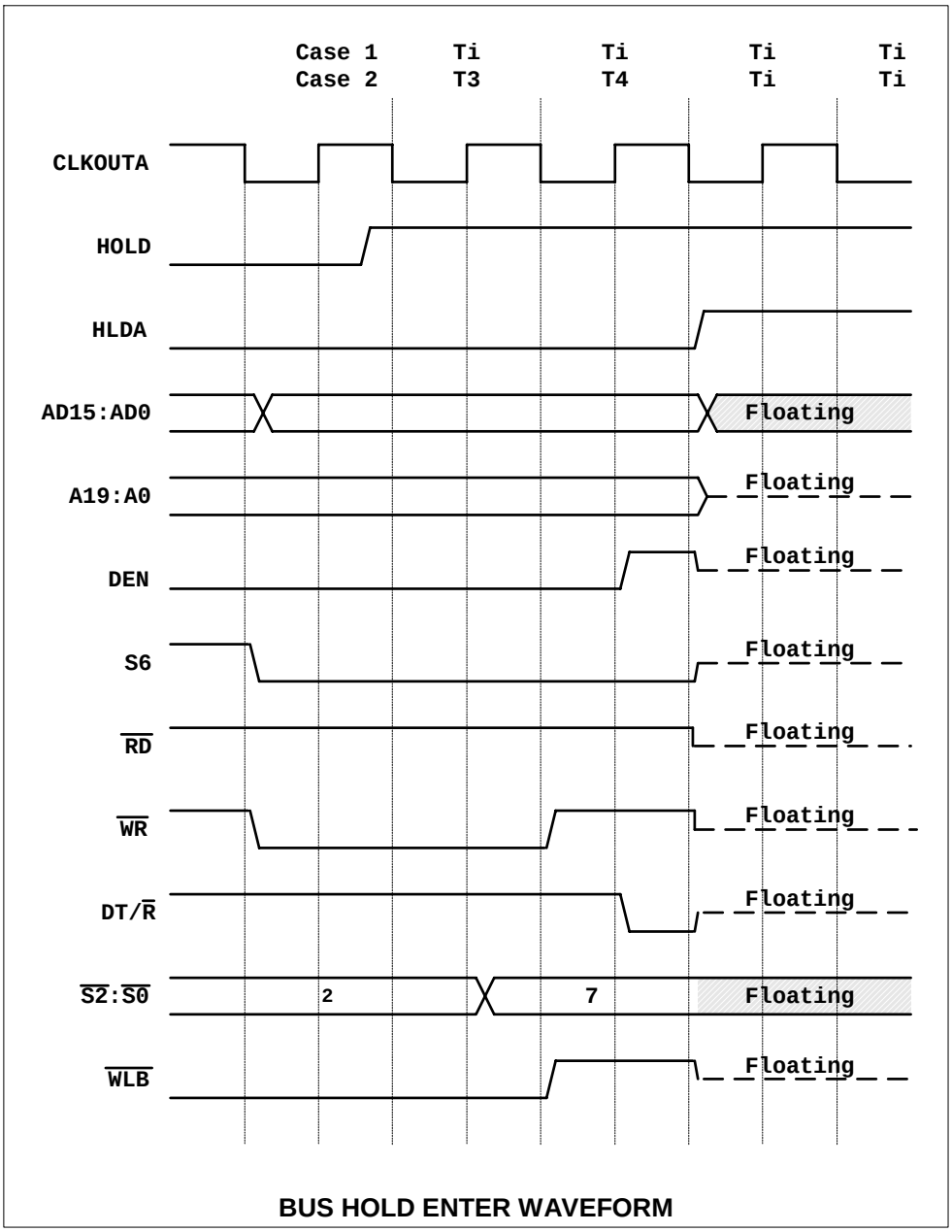
12.3 Wait States

Wait states extend the data phase of the bus cycle. The ARDY or SRDY input with low level will be inserted wait states in. If R2 bit=0, users can also insert wait states by programming the internal chip select registers. The R2 bit of UMCS (offset 0A0h) default is low, so each one of the ARDY or SRDY should be in ready state (with pull-high resistors) when at power on reset or external reset. The wait-state counter value is decided by the R3, R1 and R0 bits in each chip select register. There are five group R3, R1 and R0 bits in the registers offset A0h, A2h, A4h, A6h and A8h, and each group is independent.

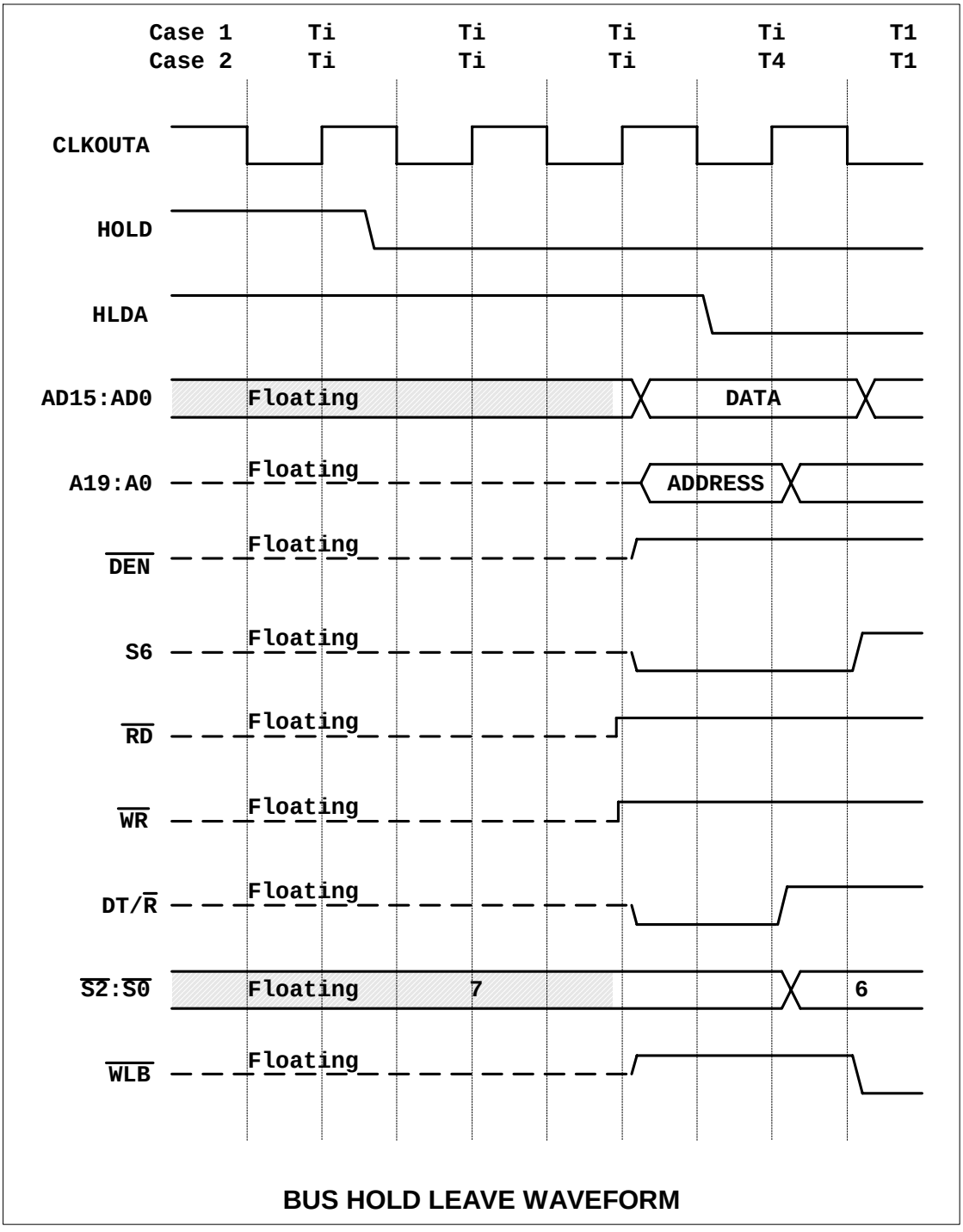


12.4 Bus Hold

When the bus hold requested (the HOLD pin is active high) by another bus master, the microprocessor will issue an HLDA in response to a HOLD request at the end of T4 or Ti. When the microprocessor is in hold status (HLDA is high), the AD15-AD0, A19-A0, $\overline{WR}$, $\overline{RD}$, $\overline{DEN}$, $\overline{S1}$-$\overline{S0}$, S6, $\overline{BHE}$, DT/$\overline{R}$, $\overline{WHB}$ and $\overline{WLB}$ are floating, and the $\overline{UCS}$, $\overline{LCS}$, $\overline{PCS6}$-$\overline{PCS5}$, $\overline{MCS3}$-$\overline{MCS0}$ and $\overline{PCS3}$-$\overline{PCS0}$ will be driven high. After HOLD is detected as being low, the microprocessor will lower the HLDA.



BUS HOLD ENTER WAVEFORM



BUS HOLD LEAVE WAVEFORM

13. Chip Select Unit

The Chip Select Unit provides 12 programmable chip select pins to access a specific memory or peripheral device. The chip selects are programmed through five peripheral control registers (A0h, A2h, A4h, A6h and A8h), and all of the chip selects can be inserted wait states in by programming the peripheral control registers.

13.1 $\overline{\text{UCS}}$

The $\overline{\text{UCS}}$ default is active on reset for code access. The memory active range is upper 512k (80000h – FFFFFh), which is programmable. And the default memory active range of $\overline{\text{UCS}}$ is 64k (F0000h – FFFFFh). The $\overline{\text{UCS}}$ will drive low four CLKOUTA oscillators if no wait state is inserted. There are three wait-states inserted to $\overline{\text{UCS}}$ active cycle on reset.

Upper Memory Chip Select Register — **Offset : A0h** — **Reset Value :F03Bh**

15	14 13 12	11	10	9	8	7	6	5	4	3	2	1	0
1	LB2 - LB0	0	0	0	0	DA	0	1	1	1	R2	R1	R0

Bit 15: Reserved

Bit 14-12: LB2-LB0, Memory block size selection for $\overline{\text{UCS}}$ chip select pin.

The active region of $\overline{\text{UCS}}$ chip select pin can be configured by the LB2-LB0.

The default memory block size is from F0000h to FFFFFh.

LB2, LB1, LB0 ---- Memory Block size , Start address, End Address

1 ,	1 ,	1	----	64k	, F0000h	, FFFFFh
1 ,	1 ,	0	----	128k	, E0000h	, FFFFFh
1 ,	0 ,	0	----	256k	, C0000h	, FFFFFh
0 ,	0 ,	0	----	512k	, 80000h	, FFFFFh

Bit 11-8: Reserved

Bit 7: DA, Disable Address. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held high on the rising edge of $\overline{\text{RST}}$, the DA bit is valid to enable/disable the address phase of the AD bus. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held low on the rising edge of $\overline{\text{RST}}$, the AD bus always drives the address and data.

Set 1: Disable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{UCS}}$ is asserted.

Set 0: Enable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{UCS}}$ is asserted.

Bit 6-3: Reserved

Bit 2: R2, Ready Mode. This bit is used to configure the ready mode for $\overline{\text{UCS}}$ chip select.

Set 1: external ready is ignored.

Set 0: external ready is required.

Bit 1-0: R1-R0, Wait-State value. When R2 is set to 0, wait-states can be inserted in for an access to the $\overline{\text{UCS}}$ memory area.

(R1,R0) = (0,0) -- 0 wait-state ; (R1,R0) = (0,1) -- 1 wait-state
(R1,R0) = (1,0) -- 2 wait-states ; (R1,R0) = (1,1) -- 3 wait-states

13.2 $\overline{\text{LCS}}$

$\overline{\text{LCS}}$ means the lower 512k bytes (00000h-9FFFFh) memory region chip selects. The memory active range is programmable, which has no default size on reset. So the A2h register must be programmed first before accessing the target memory range. The $\overline{\text{LCS}}$ pin is not active on reset, but any read or write access to the A2h register activates this pin.

Low Memory Chip Select Register

Offset : A2h
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	UB2 - UB0			1	1	1	1	DA	PSE	1	1	1	R2	R1	R0

Bit 15: Reserved

Bit 14-12: UB2-UB0, Memory block size selection for $\overline{\text{LCS}}$ chip select pin

The $\overline{\text{LCS}}$ chip select pin active region can be configured by UB2-UB0.

The $\overline{\text{LCS}}$ pin is not active on reset, but any read or write access to the A2h (LMCS) register activates this pin.

UB2, UB1, UB0		Memory Block size	Start address	End Address
0 , 0 , 0	----	64k	00000h	0FFFFh
0 , 0 , 1	----	128k	00000h	1FFFFh
0 , 1 , 1	----	256k	00000h	3FFFFh
1 , 1 , 1	----	512k	00000h	7FFFFh

Bit 11-8, 5-3: Reserved

Bit 7: DA, Disable Address. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held high on the rising edge of $\overline{\text{RST}}$, the DA bit is valid to enable/disable the address phase of the AD bus. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held low on the rising edge of $\overline{\text{RST}}$, the AD bus always drives the address and data.

Set 1: Disable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{LCS}}$ is asserted.

Set 0 : Enable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{LCS}}$ is asserted.

Bit 6: PSE, PSRAM Mode Enable. This bit is used to enable PSRAM support for the $\overline{\text{LCS}}$ chip select memory space. The refresh control unit registers E0h, E2h and E4h must be configured for auto refresh before PSRAM support is enabled.

PSE set to 1: PSRAM support is enabled.

PSE set to 0: PSRAM support is disabled.

Bit 2: R2, Ready Mode. This bit is used to configure the ready mode for $\overline{\text{LCS}}$ chip select.

Set 1: external ready is ignored.

Set 0: external ready is required.

Bit 1-0: R1-R0, Wait-State value. When R2 is set to 0, wait-states can be inserted in for an access to the $\overline{\text{LCS}}$ memory area.

(R1,R0) = (0,0) -- 0 wait-state ; (R1,R0) = (0,1) -- 1 wait-state
(R1,R0) = (1,0) -- 2 wait-states ; (R1,R0) = (1,1) -- 3 wait-states

13.3 $\overline{\text{MCSx}}$

The memory block of $\overline{\text{MCS3}}$ - $\overline{\text{MCS0}}$ can be located anywhere within the 1M-byte memory space, exclusive of the areas associated with the $\overline{\text{UCS}}$ and $\overline{\text{LCS}}$ chip selects. The maximum $\overline{\text{MCSx}}$ active memory range is 512k bytes. The 512k $\overline{\text{MCSx}}$ block size can only be used when located at address 00000h, and the $\overline{\text{LCS}}$ chip selects must not be active in this case Locating a 512k $\overline{\text{MCSx}}$ block size at 80000h always conflicts with the range of the $\overline{\text{UCS}}$ and is not allowed. The MCS chip selects are programmed through two registers A6h and A8h, and these select pins are not active on reset. Both A6h and A8h registers must be accessed with a read or write to activate $\overline{\text{MCS3}}$ - $\overline{\text{MCS0}}$. There is no default value on A6h and A8h registers, so the A6h and A8h must be programmed first before $\overline{\text{MCS3}}$ - $\overline{\text{MCS0}}$ are active.

Midranage Memory Chip Select Register

Offset : A6h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA19 - BA13							1	1	1	1	1	1	R2	R1	R0

Bit 15-9: BA19-BA13, Base Address. The BA19-BA13 correspond to bits 19-13 of the 1M bytes (20-bits) programmable base address of the $\overline{\text{MCS}}$ chip select block. The bits 12 to 0 of the base address are always 0. The base address can be set to any integer multiple of the size of the memory block size selected in these bits. For example, if the midrange block is 32Kbytes, only bits BA19 to BA15 can be programmed. So the block address could be located at 20000h or 38000h but not at 22000h. The base address of the $\overline{\text{MCS}}$ chip select can be set to 00000h only if the $\overline{\text{LCS}}$ chip select is not active. And the $\overline{\text{MCS}}$ chip select address range is not allowed to overlap the $\overline{\text{LCS}}$ chip select address range. The $\overline{\text{MCS}}$ chip select address range also is not allowed to overlap the $\overline{\text{UCS}}$ chip select address range.

Bit 8-3: Reserved

Bit 2: R2, Ready Mode. This bit is configured to enable/disable the wait states inserted for the $\overline{\text{MCS}}$ chip selects. The R1 and R0 bits of this register determine the number of wait states to be inserted.

Set 1: external ready is ignored

Set 0: external ready is required

Bit 1-0: R1-R0, Wait-State value. R1 and R0 determine the number of wait states inserted into a $\overline{\text{MCS}}$ access.

(R1,R0) : (1,1) – 3 wait states , (1,0) – 2 wait states, (0,1) – 1 wait state , (0,0) – 0 wait state

PCS and MCS Auxiliary Register

Offset : A8h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	M6 - M0							EX	MS	1	1	1	R2	R1	R0

Bit 15: Reserved

Bit 14-8: M6-M0, $\overline{MCS}$ Block Size. These bits determine the total block size for the $\overline{MCS3}$ - $\overline{MCS0}$ chip selects. Each individual chip select is active for one quarter of the total block size. For example, if the block size is 32K bytes and the base address is located at 20000h. The individual active memory address range of $\overline{MCS3}$ to $\overline{MCS0}$ is $\overline{MCS0}$ – 20000h to 21FFF, $\overline{MCS1}$-22000 to 23FFFh, MCS2- 24000h to 25FFFh, MCS3- 26000h to 27FFFh. $\overline{MCS}$ total block size is defined by M6-M0.

M6-M0	**Total block size**	**MCSx address active range**
0000001b	8k	2k
0000010b	16k	4k
0000100b	32k	8k
0001000b	64k	16k
0010000b	128k	32k
0100000b	256k	64k
1000000b	512k	128k

Bit 7: EX, Pin Selector. This bit determines whether the $\overline{PCS6}$ - $\overline{PCS5}$ pins are configured as chip selects or as alternative outputs for A2-A1.

Set 1: $\overline{PCS6}$, $\overline{PCS5}$ are configured as peripheral chip select pins.

Set 0: $\overline{PCS6}$ is configured as address bit A2 and $\overline{PCS5}$ is configured as A1.

Bit 6: MS, Memory or I/O space Selector.

Set 1: The $\overline{PCSx}$ pins are active for memory bus cycle.

Set 0: The $\overline{PCSx}$ pins are active for I/O bus cycle.

Bit 5-3: Reserved

Bit 2: R2, Ready Mode. This bit is configured to enable/disable the wait states inserted for the PCS5 and PCS6 chip selects. The R1 and R0 bits of this register determine the number of wait states to be inserted.

Set 1: external ready is ignored

Set 0: external ready is required

Bit 1-0: R1-R0, Wait-State value. R1 and R0 determine the number of wait states inserted into a $\overline{PCS5}$ - $\overline{PCS6}$ access.

(R1,R0) : (1,1) – 3 wait states , (1,0) – 2 wait states, (0,1) – 1 wait state , (0,0) – 0 wait state

13.4 $\overline{\text{PCSx}}$

In order to define these pins, the peripheral or memory chip selects which are programmed through A4h and A8h register. The base address memory block can be located anywhere within the 1M-byte memory space, exclusive of the areas associated with the $\overline{\text{UCS}}$, $\overline{\text{LCS}}$ and $\overline{\text{MCS}}$ chip selects. If the chip selects are mapped to I/O space, the access range is 64k bytes. PCS6 – PCS5 can be configured from 0 wait-state to 3 wait-states. $\overline{\text{PCS3}}$ – $\overline{\text{PCS0}}$ can be configured from 0 wait-state to 15 wait-states.

Peripheral Chip Select Register

Offset : A4h
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA19 - BA11									1	1	1	R3	R2	R1	R0

Bit 15-7: BA19-BA11, Base Address. BA19-BA11 correspond to bit 19-11 of the 1M-byte (20-bits) programmable base address of the $\overline{\text{PCS}}$ chip select block. When the $\overline{\text{PCS}}$ chip selects are mapped to I/O space, BA19-BA16 must be written to 0000b because the I/O address bus is only 64K bytes (16-bits) wide.

$\overline{\text{PCSx}}$ address range:

$\overline{\text{PCS0}}$: Base Address - Base Address + FFh
$\overline{\text{PCS1}}$: Base Address + 100h - Base Address + 1FFh
$\overline{\text{PCS2}}$: Base Address + 200h - Base Address + 2FFh
$\overline{\text{PCS3}}$: Base Address + 300h - Base Address + 3FFh
$\overline{\text{PCS5}}$: Base Address + 500h - Base Address + 5FFh
$\overline{\text{PCS6}}$: Base Address + 600h - Base Address + 6FFh

Bit 6-4: Reserved

Bit 3: R3; **Bit 1-0: R1-R0**, Wait-State Value. The R3, R1 and R0 determine the number of wait-states inserted into a $\overline{\text{PCS3}}$ - $\overline{\text{PCS0}}$ access.

R3,	R1,	R0	--	Wait States
0,	0,	0	--	0
0,	0,	1	--	1
0,	1,	0	--	2
0,	1,	1	--	3
1,	0,	0	--	5
1,	0,	1	--	7
1,	1,	0	--	9
1,	1,	1	--	15

Bit 2: R2, Ready Mode. This bit is configured to enable/disable the wait states inserted for the $\overline{\text{PCS3}}$ - $\overline{\text{PCS0}}$ chip selects.

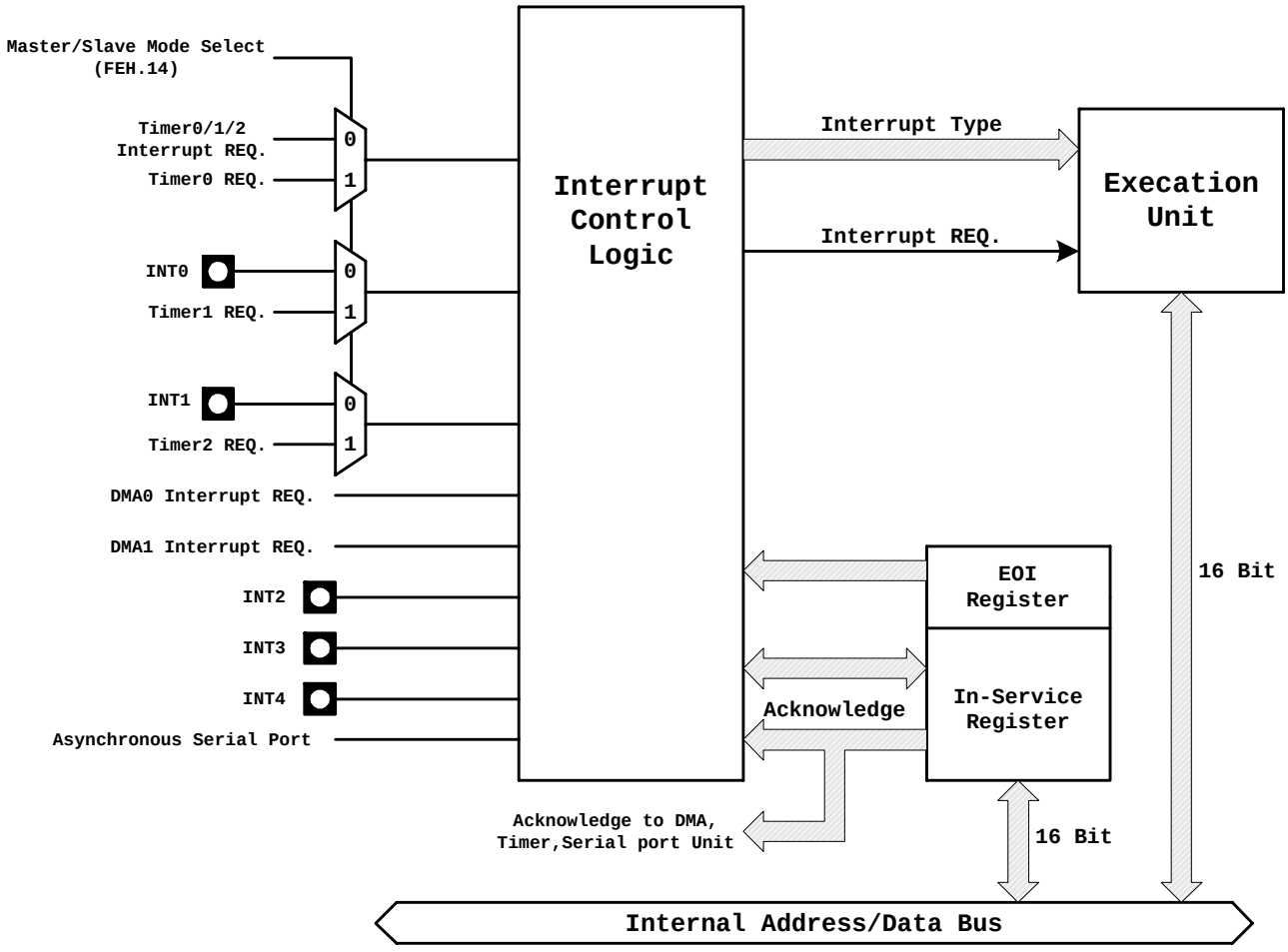
The R3, R1 and R0 bits determine the number of wait states to be inserted.

Set 1: external ready is ignored

Set 0: external ready is required

14. Interrupt Controller Unit

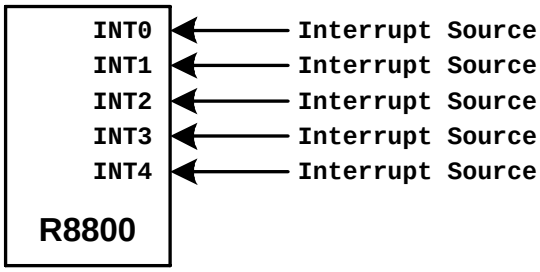
There are twelve interrupt requests source connected to the controller: five maskable interrupt pins (INT0 – INT4); one non-maskable interrupt pin (NMI); Six internal unit request source (Timer 0, 1, 2; DMA 0, 1; Asynchronous serial unit).



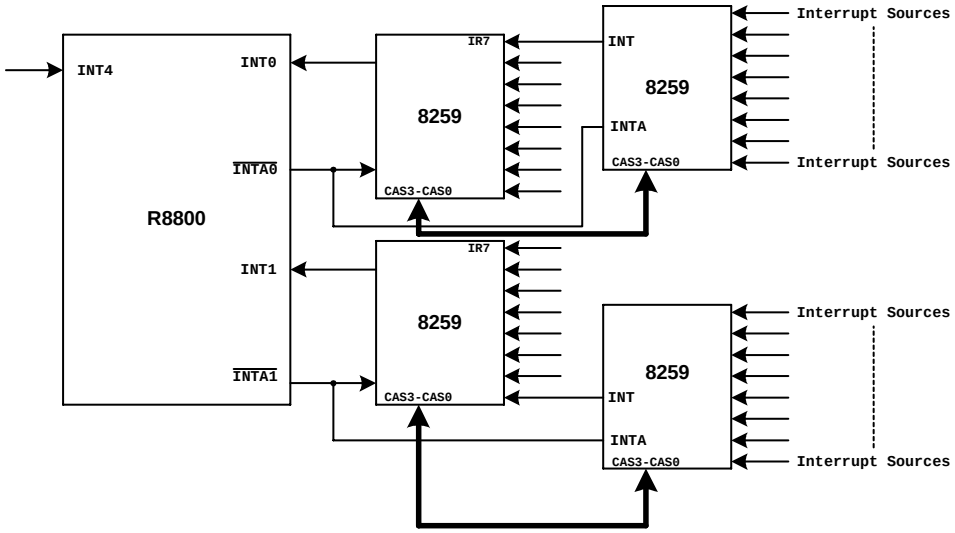
Interrupt Control Unit Block Diagram

14.1 Master Mode and Slave Mode

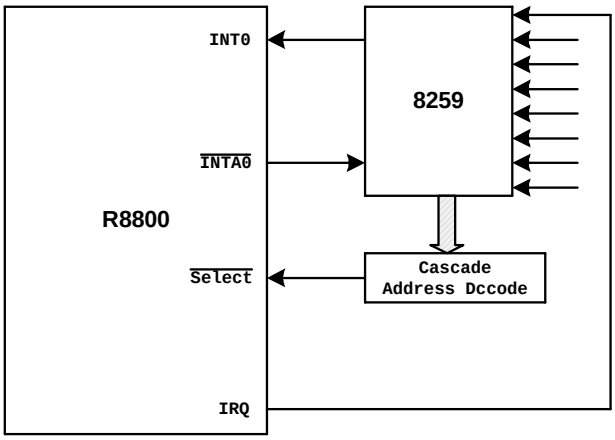
The interrupt controller can be programmed as a master or slave mode. (To program FEh, bit 14), the master mode has two connections: Fully Nested Mode connection or Cascade Mode connection.



Fully Nested Mode Connections



Cascade Mode Connection



Slave Mode Connection

14.2 Interrupt Vector, Type and Priority

The following table shows the interrupt vector addresses, type and the priority. The maskable interrupt priority can be changed by programming the priority registers. The Vector addresses for each interrupt are fixed.

Interrupt source	Interrupt Type	Vector Address	EOI Type	Priority	Note
Divide Error Exception	00h	00h		1	
Trace interrupt	01h	04h		1-1	*
NMI	02h	08h		1-2	*
Breakpoint Interrupt	03h	0Ch		1	
INTO Detected Over Flow Exception	04h	10h		1	
Array Bounds Exception	05h	14h		1	
Undefined Opcode Exception	06h	18h		1	
ESC Opcode Exception	07h	1Ch		1	
Timer 0	08h	20h	08h	2-1	*/**
Reserved	09h				
DMA 0	0Ah	28h	0Ah	3	**
DMA 1	0Bh	2Ch	0Bh	4	**
INT0	0Ch	30h	0Ch	5	
INT1	0Dh	34h	0Dh	6	
INT2	0Eh	38h	0Eh	7	
INT3	0Fh	3Ch	0Fh	8	
INT4	10h	40h	10h	9	
Watchdog Timer	11h	44h	11h	9	
Timer 1	12h	48h	08h	2-2	*/**
Timer 2	13h	4Ch	08h	2-3	*/**
Asynchronous Serial port	14h	50h	14h	9	
Reserved	15h-1Fh				

Note*: *When the interrupt occurs in the same time, the priority is (1-1 > 1-2) ; (2-1> 2-2 > 2-3)*

Note**: *The interrupt types of these sources are programmable in slave mode.*

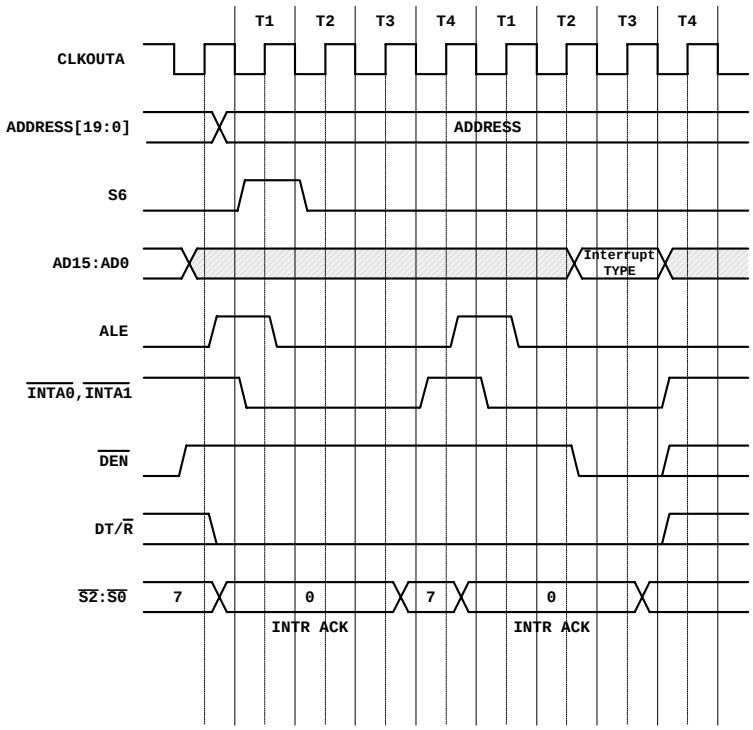
14.3 Interrupt Requests

When an interrupt is requested, the internal interrupt controller verifies that the interrupt is enabled (the IF flag is enabled and no MSK bit is set) and there are no higher priority interrupt requests being serviced or pending. If the interrupt is granted, the interrupt controller uses the interrupt type to access a vector from the interrupt vector table.

If the external INT is active (level-triggered) to request the interrupt controller service, the INT pins must be held till the micro-controller enters the interrupt service routine. There is no interrupt-acknowledged output when running in fully nested mode, so the PIO pins should be used to simulate the interrupt-acknowledged pin if necessary.

14.4 Interrupt Acknowledge

The processor requires the interrupt type as an index into the interrupt table. The internal interrupt can provide the interrupt type or an external controller can provide the interrupt type. The internal interrupt controller provides the interrupt type to the processor without external bus cycles generation. When an external interrupt controller is providing the interrupt type, the processor generates two acknowledged bus cycles, and the interrupt type is written to the AD15-AD0 lines by the external interrupt controller.



INTERRUPT ACKNOWLEDGE CYCLE
(CASECADE OR SLAVE MODE)

14.5 Programming the Registers

Software is used to program the registers (**Master mode:** 44h, 42h, 40h, 3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 26h, 24h and 22h; **Slave Mode:** 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 22h and 20h) to define the interrupt controller operation.

Serial Port Interrupt Control Register

Offset : 44h
Reset Value : 001Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of the asynchronous serial port.

Set 0: Enable the serial port interrupt.

Bit 2-0: PR2-PR0, Priority. These bits determine the priority of the serial port relative to the other interrupt signals.

The priority selection:

PR2, **PR1**, **PR0** -- **Priority**

0	0	0	--	0	(High)
0	0	1	--	1	
0	1	0	--	2	
0	1	1	--	3	
1	0	0	--	4	
1	0	1	--	5	
1	1	0	--	6	
1	1	1	--	7	(Low)

INT4 Control Register

Offset : 40h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15- 8, bit 6-5: Reserved

Bit 7: ETM, Edge trigger enable. When this bit is set to 1 and Bit 4 set to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.

Bit 4: LTM, Level-Triggered Mode.

Set 1: An interrupt is triggered by high active level

Set 0: An interrupt is triggered by the low to high edge.

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of INT4

Set 0: Enable the INT4 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT3 Control Register **Offset : 3Eh**
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-8, bit 6-5: Reserved

Bit 7: ETM, Edge trigger enable. When this bit is set to 1 and Bit 4 set to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.

Bit 4: LTM, Level-Triggered Mode.

Set 1: An interrupt is triggered by high active level.

Set 0: An interrupt is triggered by the low to high edge.

Bit 3 : MSK, Mask.

Set 1: Mask the interrupt source of INT3

Set 0: Enable the INT3 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT2 Control Register **Offset : 3Ch**
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15- 8, bit 6-5: Reserved

Bit 7: ETM, Edge trigger enable. When this bit is set to 1 and Bit 4 set to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.

Bit 4: LTM, Level-Triggered Mode.

Set 1: An interrupt is triggered by high active level.

Set 0: An interrupt is triggered by the low to high edge.

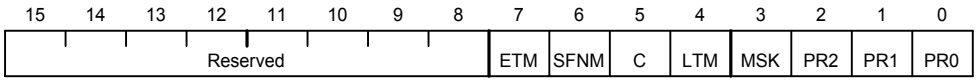
Bit 3 : MSK, Mask. Set 1: Mask the interrupt source of the INT2

Set 0: Enable the INT2 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT1 Control Register **Offset : 3Ah**
Reset Value : 000Fh



(Master Mode)

Bit 15-8: Reserved

Bit 7: ETM, Edge trigger enable. When this bit is set to 1 and Bit 4 set to 0, an interrupt is triggered by a low to high edge. The low go high edge will be latched (one level) till this interrupt is serviced.

Bit 6: SFNM, Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT1

Bit 5: C, Cascade mode. Set 1 to enable cascade mode.

Bit 4: LTM, Level-Triggered Mode.

Set 1: An interrupt is triggered by high active level.

Set 0: An interrupt is triggered by the low to high edge.

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of INT1

Set 0: Enable the INT1 interrupt.

Bit 2-0: PR, Interrupt Priority.

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h

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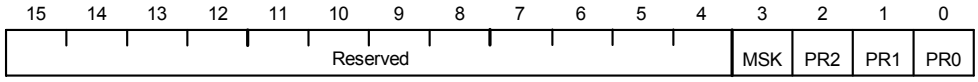
INT1 Control Register **Offset : 3Ah**
Reset Value : 0000h



(Slave Mode), Timer 2 Interrupt Control Register, reset value is 0000h

Bit 15- 4: Reserved

Bit 3: MSK, Mask.

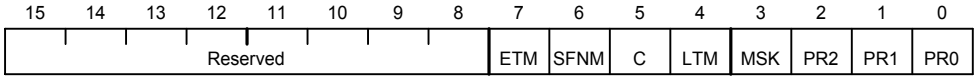
Set 1: Mask the interrupt source of the Timer 2

Set 0: Enable the Timer 2 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT0 Control Register **Offset : 38h**
Reset Value : 000Fh



(Master Mode)

Bit 15-8: Reserved

Bit 7: ETM, Edge trigger enable. When this bit set to 1 and Bit 4 set to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.

Bit 6: SFNM, Special Fully Nested Mode.

Set 1: Enable the special fully nested mode of INT0.

Bit 5: C, cascade Mode

Set 1 to enable cascade mode

Bit 4: LTM, Level-Triggered Mode.

Set 1: An interrupt is triggered by high active level.

Set 0: An interrupt is triggered by the low to high edge.

Bit 3: MSK, Mask.

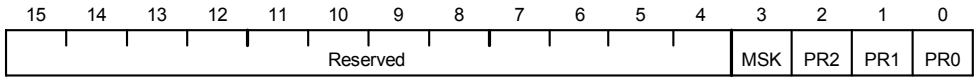
Set 1: Mask the interrupt source of the INT0

Set 0: Enable the INT0 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT0 Control Register **Offset : 38h**
Reset Value : 0000h



(Slave Mode), Timer 1 Interrupt Control Register, reset value is 0000h

Bit 15-4: Reserved

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of the timer 1

Set 0: Enable the timer 1 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

DMA 1 Interrupt Control Register

Offset : 36h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the DMA 1 controller

Set 0: Enable the DMA 1 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

DMA 1 Interrupt Control Register

Offset : 36h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Slave Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the DMA 1 controller

Set 0: Enable the DMA 1 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h

---

DMA 0 Interrupt Control Register

Offset : 34h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the DMA 0 controller

Set 0: Enable the DMA 0 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

DMA 0 Interrupt Control Register

Offset : 34h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Slave Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the DMA 0 controller

Set 0: Enable the DMA 0 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

Timer Interrupt Control Register

Offset : 32h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the Timer controller

Set 0: Enable the Timer controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

Timer Interrupt Control Register

Offset : 32h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Slave Mode), Timer 0 Interrupt Control Register, reset value is 0000h

Bit 15-4: Reserved

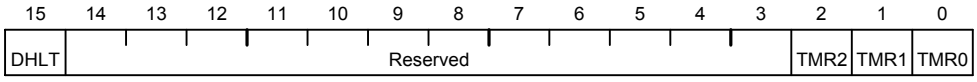
Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the Timer 0 controller

Set 0: Enable the Timer 0 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

Interrupt Status Register **Offset : 30h**
Reset Value : —



(Master Mode)

Bit 15: DHLT, DMA Halt.

Set 1: Halts any DMA activity when non-maskable interrupt occurs.

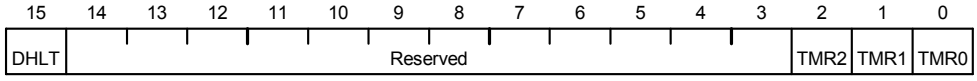
Set 0: When an IRET instruction is executed.

Bit 14-3: Reserved.

Bit 2-0: TMR2-TMR0,

Set 1: indicates the corresponding timer has an interrupt request pending.

Interrupt Status Register **Offset : 30h**
Reset Value : 0000h



(Slave Mode)

Bit 15: DHLT, DMA Halt.

Set 1: Halts any DMA activity when non-maskable interrupt occurs.

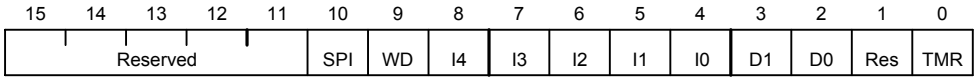
Set 0: When an IRET instruction is executed.

Bit 14-3: Reserved.

Bit 2-0: TMR2-TMR0,

Set 1: indicates the corresponding timer has an interrupt request pending.

Interrupt Request Register **Offset : 2Eh**
Reset Value : —



(Master Mode)

The Interrupt Request register is a read-only register. For internal interrupts (SPI, WD, D1, D0 and TMR), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge. For INT4-INT0 external interrupts, the corresponding bit (I4-I0) reflects the current value of the external signal.

Bit 15-11: Reserved.

Bit 10: SPI, Serial Port Interrupt Request. Indicates the interrupt state of the serial port.

Bit 9: WD, Watchdog Timer Interrupt Request.

Set 1: The Watchdog Timer has an interrupt pending.

Bit 8-4: I4-I0, Interrupt Requests.

Set 1: The corresponding INT pin has an interrupt pending.

Bit 3-2: D1-D0, DMA Channel Interrupt Request.

Set 1: The corresponding DMA channel has an interrupt pending.

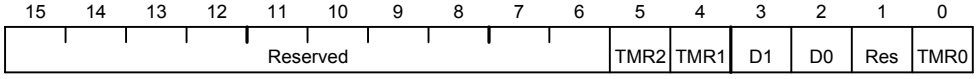
Bit 1: Reserved.

Bit 0: TMR, Timer Interrupt Request.

Set 1: The timer control unit has an interrupt pending.

Interrupt Request Register

Offset : 2Eh
Reset Value : 0000h



(Slave Mode)

The Interrupt Request register is a read-only register. For internal interrupts (D1, D0, TMR2, TMR1 and TMR0), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge.

Bit 15-6: Reserved.

Bit 5-4: TMR2/TMR1, Timer2/Timer1 Interrupt Request.

Set 1: Indicates the state of any interrupt requests form the associated timer.

Bit 3-2: D1-D0, DMA Channel Interrupt Request.

Set 1: Indicates the corresponding DMA channel has an interrupt pending.

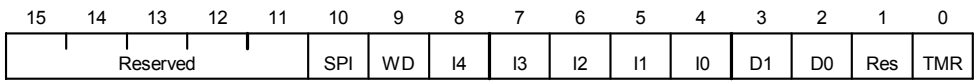
Bit 1: Reserved.

Bit 0: TMR0, Timer 0 Interrupt Request.

Set 1: Indicates the state of an interrupt request from Timer 0.

Interrupt In-Service Register

Offset : 2Ch
Reset Value : 0000h



(Master Mode)

The bits in the INSERV register are set by the interrupt controller when the interrupt is taken. Each bit in the

register is cleared by writing the corresponding interrupt type to the EOI register.

Bit 15-11: Reserved.

Bit 10: SPI, Serial Port Interrupt In-Service.

Set 1: the serial port interrupt is currently being serviced.

Bit 9: WD, Watchdog Timer Interrupt In-Service.

Set 1: the watchdog timer interrupt is currently being serviced.

Bit 8-4: I4-I0, Interrupt In-Service.

Set 1: the corresponding INT interrupt is currently being serviced.

Bit 3-2: D1-D0, DMA Channel Interrupt In-Service.

Set 1: the corresponding DMA channel interrupt is currently being serviced.

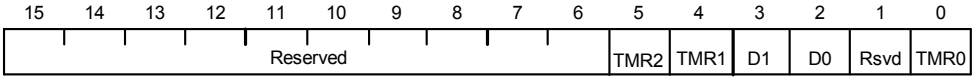
Bit 1: Reserved.

Bit 0: TMR, Timer Interrupt In-Service.

Set 1: the timer interrupt is currently being serviced.

Interrupt In-Service Register

Offset : 2Ch
Reset Value : 0000h



(Slave Mode)

The bits in the In-Service register are set by the interrupt controller when the interrupt is taken. The in-service bits are cleared by writing to the EOI register.

Bit 15-6: Reserved.

Bit 5-4: TMR2-TMR1, Timer2/Timer1 Interrupt In-Service.

Set 1: the corresponding timer interrupt is currently being serviced.

Bit 3-2: D1-D0, DMA Channel Interrupt In-Service.

Set 1: the corresponding DMA Channel is currently being serviced.

Bit 1: Reserved.

Bit 0: TMR0, Timer 0 Interrupt In-Service.

Set 1: The Timer 0 interrupt is currently being serviced.

Priority Mask Register **Offset : 2Ah**
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

(Master Mode)

Determines the minimum priority level at which maskable interrupts can generate an interrupt.

Bit 15-3: Reserved.

Bit 2-0: PRM2-PRM0, Priority Field Mask. Determines the minimum priority that is required in order for a maskable interrupt source to generate an interrupt.

Priority	PR2-PR0
(High) 0	000
1	001
2	010
3	011
4	100
5	101
6	110
(Low) 7	111

Priority Mask Register **Offset : 2Ah**
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

(Slave Mode)

Determines the minimum priority level at which maskable interrupts can generate an interrupt.

Bit 15-3: Reserved.

Bit 2-0: PRM2-PRM0, Priority Field Mask. Determines the minimum priority that is required in order for a maskable interrupt source to generate an interrupt.

Priority	PR2-PR0
(High) 0	000
1	001
2	010
3	011
4	100
5	101
6	110
(Low) 7	111

Interrupt Mask Register **Offset : 28h**
Reset Value : 07FDh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SPI	WD	I4	I3	I2	I1	I0	D1	D0	Res	TMR

(Master Mode)

Bit 15-11: Reserved.

Bit 10: SPI, Serial Port Interrupt Mask. The state of the mask bit of the asynchronous serial port interrupt.

Bit 9: WD, Virtual Watchdog Timer Interrupt Mask. The state of the mask bit of the Watchdog Timer interrupt.

Bit 8-4: I4-I0, Interrupt Masks. Indicates the state of the mask bit of the corresponding interrupt.

Bit 3-2: D1-D0, DMA Channel Interrupt Masks. Indicates the state of the mask bit of the corresponding DMA Channel interrupt.

Bit 1: Reserved.

Bit 0: TMR, Timer Interrupt Mask. The state of the mask bit of the timer control unit.

Interrupt Mask Register **Offset : 28h**
Reset Value : 003Dh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TMR1	D1	D0	Rsvd	TMR0

(Slave Mode)

Bit 15-6: Reserved.

Bit 5-4: TMR2-TMR1, Timer 2/Timer1 Interrupt Mask. The state of the mask bit of the Timer Interrupt Control register.

Set 1: Timer2 or Time1 has its interrupt requests masked

Bit 3-2: D1-D0, DMA Channel Interrupt Mask. The state of the mask bits of the corresponding DMA control register.

Bit 1: Reserved.

Bit 0: TMR0, Timer 0 Interrupt Mask. The state of the mask bit of the Timer Interrupt Control Register

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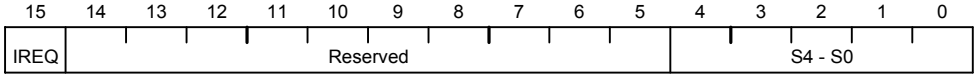
Poll Status Register **Offset : 26h**
Reset Value : —



(Master Mode)

The Poll Status (POLLST) register mirrors the current state of the Poll register. The POLLST register can be read without affecting the current interrupt request.

Bit 15: IREQ, Interrupt Request.

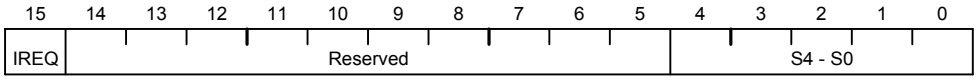
Set 1: if an interrupt is pending. The S4-S0 field contains valid data.

Bit 14-5: Reserved.

Bit 4-0: S4-S0,

Poll Status. Indicates the interrupt type of the highest priority-pending interrupt.

Poll Register **Offset : 24h**
Reset Value : —



(Master Mode)

When the Poll register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Poll register.

Bit 15: IREQ, Interrupt Request.

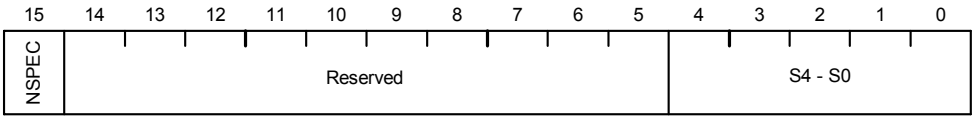
Set 1: if an interrupt is pending. The S4-S0 field contains valid data.

Bit 14-5: Reserved.

Bit 4-0: S4-S0,

Poll Status. Indicates the interrupt type of the highest priority-pending interrupt.

End-of-Interrupt Register **Offset : 22h**
Reset Value : —



(Master Mode)

Bit 15: NSPEC, Non-Specific EOI.

Set 1: indicates non-specific EOI.

Set 0: indicates the specific EOI interrupt type in S4-S0.

Bit 14-5: Reserved.

Bit 4-0: S4-S0, Source EOI Type. Specify the EOI type of the interrupt that is currently being processed.

Note: *We suggest the specific EOI is the most secure method to use for resetting In-Service bit.*

Specific End-of-Interrupt Register **Offset : 22h**
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	L2	L1	L0

(Slave Mode)

Bit 15-3: Reserved.

Bit 2-0: L2-L0, Interrupt Type. Encoded value indicates the priority of the IS (interrupt service) bit to reset. Writes to these bits cause an EOI to be issued for the interrupt type in slave mode.

Interrupt Vector Register **Offset : 20h**
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	T4 - T0					0	0	0

(Slave Mode)

Bit 15-8, 2-0: Reserved

Bit 7-3: T4-T0, Interrupt Type.

The following interrupt type of slave mode can be programmed.

Timer 2 interrupt controller: (T4,T3,T2,T1,T0, 1, 0, 1)b
Timer 1 interrupt controller: (T4,T3,T2,T1,T0, 1, 0, 0)b
DMA 1 interrupt controller: (T4,T3,T2,T1,T0, 0, 1, 1)b
DMA 0 interrupt controller: (T4,T3,T2,T1,T0, 0, 1, 0)b
Timer 0 interrupt controller: (T4,T3,T2,T1,T0, 0, 0, 0)b

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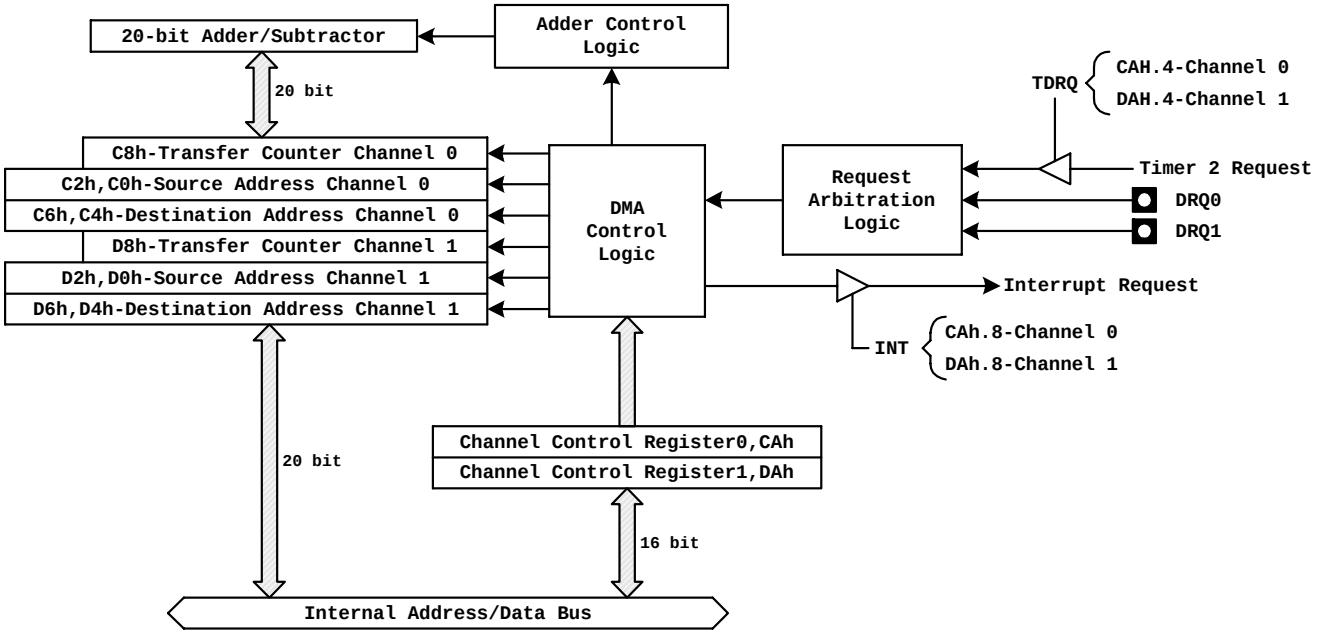
15. DMA Unit

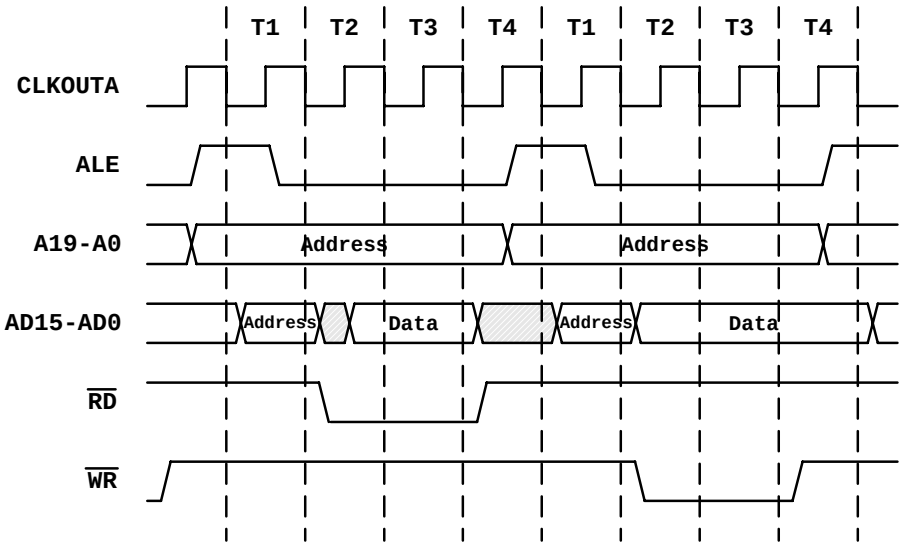
The DMA controller provides the data transfer between the memory and peripherals without the intervention of the CPU. There are two DMA channels in the DMA unit. Each channel can accept DMA request from one of two sources: an external pin (DRQ0 for channel 0 or DRQ1 for channel 1) or Timer 2 overflow. The data transfer from source to destination can be memory to memory, memory to I/O, I/O to I/O, or I/O to memory. Either bytes or words can be transferred to or from even or odd addresses and two bus cycles are necessary (reads from source and writes to destination) for each data transfer.



DMA Unit Block

15.1 DMA Operation

Every DMA transfer consists of two bus cycles (see figure of Typical DMA Transfer) and the two bus cycles cannot be separated by a bus hold request, a refresh request or another DMA request. The registers (CAh, C8h, C6h, C4h, C2h, C0h, DAh, D8h, D6h, D4h, D2h and D0h) are used to configure and operate the two DMA channels.



Typical DMA Trarsfer

DMA0 Control Register

Offset : CAh (DMA0)
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO	DDEC	DINC	SM/IO	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	Res	CHG	ST	B/W

Bit 15: DM / IO, Destination Address Space Select.

Set 1: The destination address is in memory space.

Set 0: The destination address is in I/O space.

Bit 14: DDEC, Destination Decrement.

Set 1: The destination address is automatically decremented after each transfer.

The B/W (bit 0) bit determines the decremented value which is by 1 or 2. When both the DDEC and DINC bits are set to 1, the address remains constant.

Set 0: Disable the decrement function.

Bit 13: DINC, Destination Increment.

Set 1: The destination address is automatically incremented after each transfer.

The B/W (bit 0) bit determines the incremented value which is by 1 or 2.

Set 0: Disable the increment function.

Bit 12: SM/ IO, Source Address Space Select.

Set 1: The Source address is in memory space.

Set 0: The Source address is in I/O space

Bit 11: SDEC, Source Decrement.

Set 1: The Source address is automatically decremented after each transfer.

The $\overline{B}$/W (bit 0) bit determines the decremented value which is by 1 or 2. When both the SDEC and SINC bits are set to 1, the address remains constant.

Set 0: Disable the decrement function.

Bit 10: SINC, Source Increment.

Set 1: The Source address is automatically incremented after each transfer.

The $\overline{B}$/W (bit 0) bit determines the incremented value which is by 1 or 2.

Set 0: Disable the increment function

Bit 9: TC, Terminal Count.

Set 1: The synchronized DMA transfer is terminated when the DMA transfer count register reaches 0.

Set 0: The synchronized DMA transfer is terminated when the DMA transfer count register reaches 0.

Unsynchronized DMA transfer is always terminated when the DMA transfer count register reaches 0, regardless of the setting of this bit.

Bit 8: INT, Interrupt.

Set 1: DMA unit generates an interrupt request when the transfer count is completed.

The TC bit must be set to 1 to generate an interrupt.

Bit 7-6: SYN1-SYN0, Synchronization Type Selection.

SYN1 , SYN0			**--**	**Synchronization Type**
0	,	0	--	Unsynchronized
0	,	1	--	Source synchronized
1	,	0	--	Destination synchronized
1	,	1	--	Reserved

Bit 5: P, Priority.

Set 1: It selects high priority for this channel when both DMA 0 and DMA 1 are transferred in the same time.

Bit 4: TDRQ, Timer Enable/Disable Request

Set 1: Enable the DMA requests from timer 2.

Set 0: Disable the DMA requests from timer 2.

Bit 3: Reserved.

Bit 2: CHG, Changed Start Bit. This bit must be set to 1 when the ST bit is modified.

Bit 1: ST, Start/Stop DMA channel.

Set 1: Start the DMA channel

Set 0: Stop the DMA channel

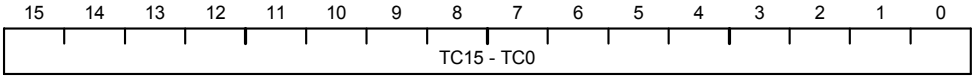
Bit 0: $\overline{B}$ /W, Byte/Word Select.

Set 1: The address is incremented or decremented by 2 after each transfer.

Set 0: The address is incremented or decremented by 1 after each transfer.

DMA0 Transfer Count Register

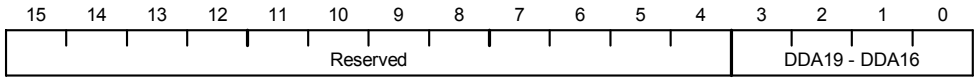
Offset : C8h (DMA0)
Reset Value : ——



Bit 15-0: TC15-TC0, DMA 0 transfer Count. The value of this register is decremented by 1 after each transfer.

DMA0 Destination Address High Register

Offset : C6h (DMA0)
Reset Value : ——

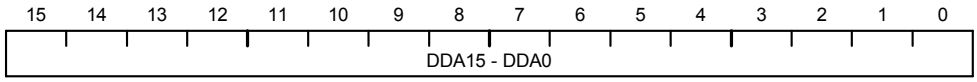


Bit 15-4: Reserved

Bit 3-0: DDA19-DDA16, High DMA 0 Destination Address. These bits are mapped to A19- A16 during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA0 Destination Address Low Register

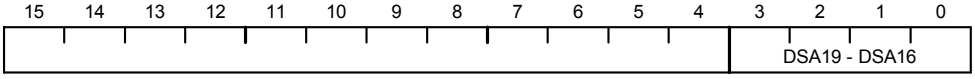
Offset : C4h (DMA0)
Reset Value : ——



Bit 15-0: DDA15-DDA0, Low DMA 0 Destination Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DDA19-DDA0) will be incremented or decremented by 1 or 2 after each DMA transfer.

DMA0 Source Address High Register

Offset : C2h (DMA0)
Reset Value : ——

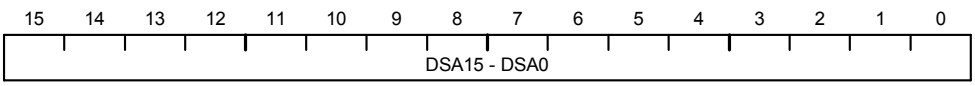


Bit 15-4: Reserved

Bit 3-0: DSA19-DSA16, High DMA 0 Source Address. These bits are mapped to A19- A16 during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA0 Source Address Low Register

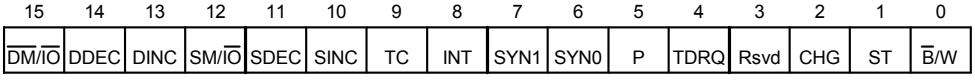
Offset : C0h (DMA0)
Reset Value : ——



Bit 15-0: DSA15-DSA0, Low DMA 0 Source Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DSA19-DSA0) will be incremented or decremented by 1 or 2 after each DMA transfer.

DMA1 Control Register

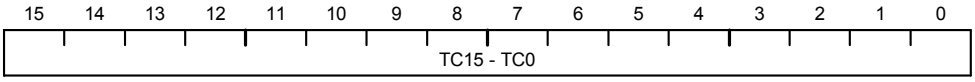
Offset : DAh (DMA1)
Reset Value : -----



The bit definitions of bit 15~0 for DMA1 are the same as those of bit 15~0 of Register CAh for DMA0.

DMA1 Transfer Count Register

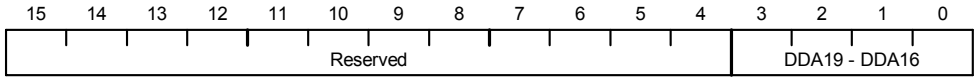
Offset : D8h (DMA1)
Reset Value : ——



Bit 15-0: TC15-TC0, DMA 1 transfer Count. The value of this register is decremented by 1 after each transfer.

DMA1 Destination Address High Register

Offset : D6h (DMA1)
Reset Value : —

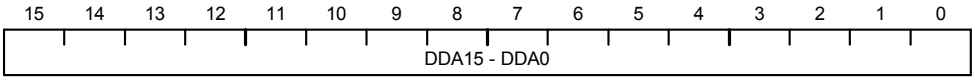


Bit 15-4: Reserved

Bit 3-0: DDA19-DDA16, High DMA 1 Destination Address. These bits are mapped to A19- A16 during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA1 Destination Address Low Register

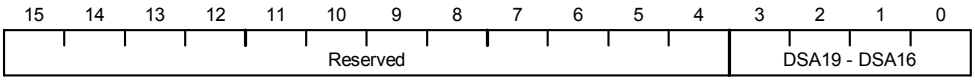
Offset : D4h (DMA1)
Reset Value : —



Bit 15-0: DDA15-DDA0, Low DMA 1 Destination Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DDA19-DDA0) will be incremented or decremented by 1 or 2 after each DMA transfer.

DMA1 Source Address High Register

Offset : D2h (DMA1)
Reset Value : —

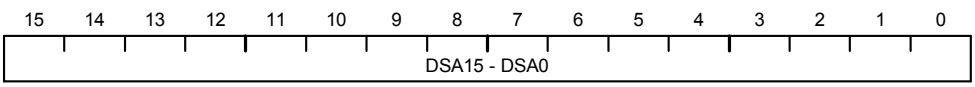


Bit 15-4: Reserved

Bit 3-0: DSA19-DSA16, High DMA 1 Source Address. These bits are mapped to A19- A16 during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA1 Source Address Low Register

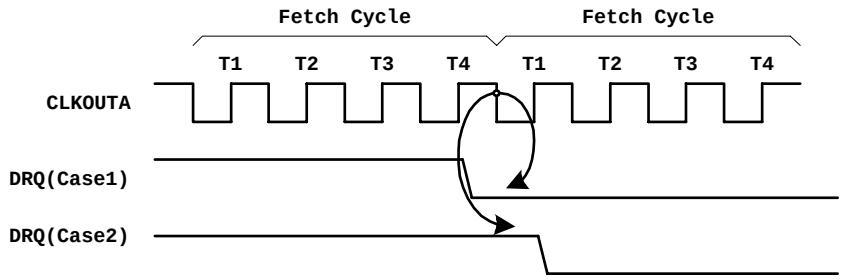
Offset : D0h (DMA1)
Reset Value : —



Bit 15-0: DSA15-DSA0, Low DMA 1 Source Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DSA19-DSA0) will be incremented or decremented by 1 or 2 after each DMA transfer.

15.2 External Requests

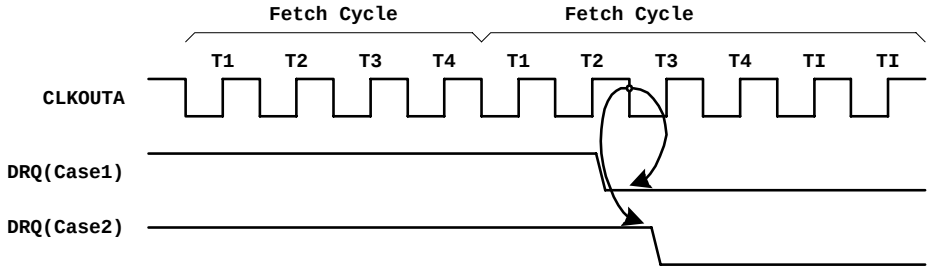
External DMA requests are asserted on the DRQ pins. The DRQ pins are sampled on the falling edge of CLKOUTA. It takes a minimum of four clocks before the DMA cycle is initiated by the Bus Interface. The DMA request is cleared four clocks before the end of the DMA cycle. And no DMA acknowledge is provided, since the chip-selects (MCSx and PCSx) can be programmed to be active for a given block of memory or I/O space, and the DMA source and destination address registers can be programmed to point to the same given block.
DMA transfer can be either source- or destination-synchronized, and it can also be unsynchronized. The Source-Synchronized Transfer figure shows the typical source-synchronized transfer which provides the source device at least three clock cycles from the time it is acknowledged to de-assert its DRQ line.



NOTES:
Case1 : Current source synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current source synchronized transfer will be immediately followed by antoher DMA transfer.

Source-Synchronized Transfers

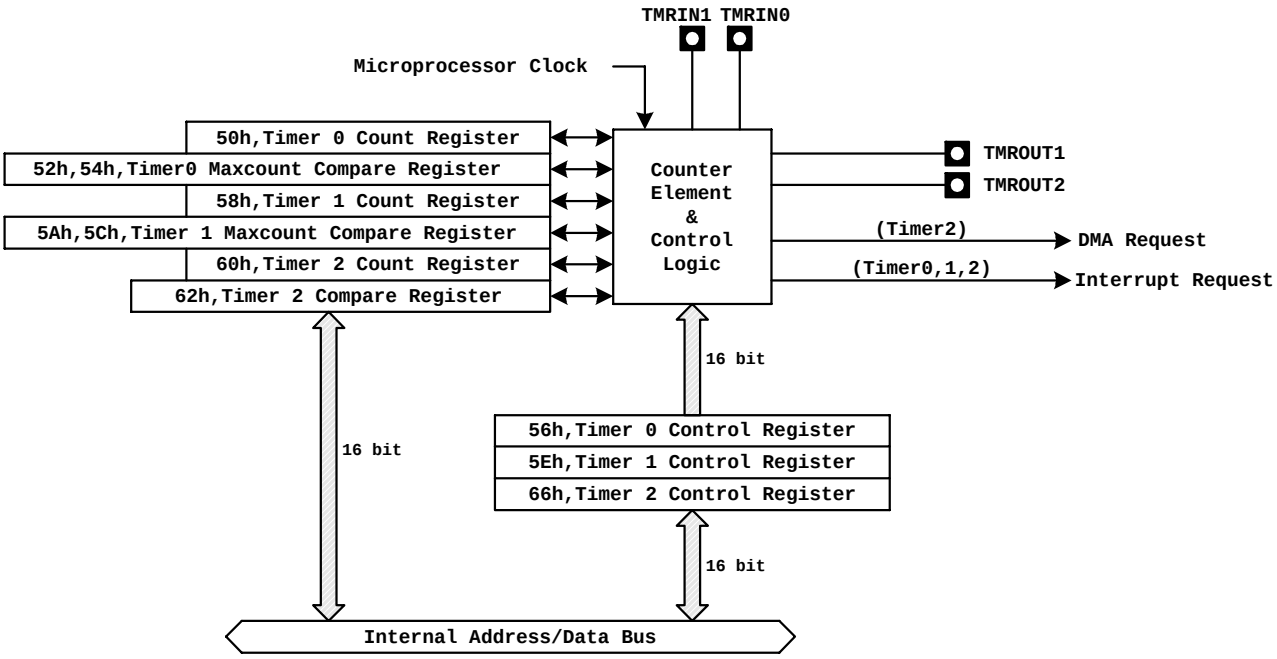
The Destination-Synchronized Transfer figure shows the typical destination-synchronized transfer which differs from a source-synchronized transfer in which two idle states are added to the end of the deposit cycle. The two idle states extend the DMA cycle to allow the destination device to de-assert its DRQ pin four clocks before the end of the cycle. If the two idle states were not inserted, the destination device would not have time to de-assert its DRQ signal.



NETES:
Case1 : Current destination synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current destination synchronized transfer will be immediately followed by another DMA transfer.

Destination-Synchronized Transfers

16. Timer Control Unit



Timer / Counter Unit Block

There are three 16-bit programmable timers in the R8800. The timer operation is independent of the CPU. The three timers can be programmed as a timer element or as a counter element. Timers 0 and 1 are each connected to two external pins (TMRIN0, TMROUT0, TMRIN1 and TMROUT1) which can be used to count or time external events, or used to generate variable-duty-cycle waveforms. Timer 2 is not connected to any external pins. It can be used as a pre-scaler to timer 0 and timer 1 or as a DMA request source.

Timer 0 Mode / Control Register

Offset : 56h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{INH}$	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

Bit 15: EN, Enable Bit.

Set 1: The timer 0 is enabled.

Set 0: The timer 0 is inhibited from counting.

The $\overline{INH}$ bit must be set to 1 when the EN bit is written, and the $\overline{INH}$ and EN bits must be in the same write.

Bit 14: $\overline{INH}$, Inhibit Bit. This bit allows selective updating the EN bit. The $\overline{INH}$ bit must be set to 1 when the EN bit is written, and both the $\overline{INH}$ and EN bits must be in the same write. This bit is not stored and always read as 0.

Bit 13: INT, Interrupt Bit.

Set 1: An interrupt request is generated when the count register equals a maximum count. If the timer is configured in dual max-count mode, an interrupt is generated each time the count reaches max-count A or max-count B

Set 0: Timer 0 will not issue interrupt requests.

Bit 12: RIU, Register in Use Bit.

Set 1: The Maxcount Compare B register of timer 0 is being used

Set 0: The Maxcount Compare A register of timer 0 is being used

Bit 11-6: Reserved.

Bit 5: MC, Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. In dual maxcount mode, this bit is set each time when either Maxcount Compare A or Maxcount Compare B register is reached. This bit is set regardless of the INT bit (56h.13).

Bit 4: RTG, Re-trigger Bit. This bit defines the control function by the input signal of the TMRIN0 pin. When EXT=1 (56h.2), this bit is ignored.

Set 1: Timer0 Count Register (50h) counts internal events; Reset the counting on every TMRIN0 input signal from low to high (rising edge trigger).

Set 0: Low input holds the timer 0 Count Register (50h) value; High input enables the counting which counts the internal events.

The definition of setting the (EXT, RTG)

(0, 0) – Timer0 counts the internal events if the TMRIN0 pin remains high.

(0, 1) – Timer0 counts the internal events; count register reset on every rising transition on the TMRIN0 pin.

(1, x) – The TMRIN0 pin input acts as clock source and timer0 count register is incremented by one every external clock.

Bit 3: P, Prescaler Bit. This bit and EXT (56h.2) define the timer0 clock source.

The definition of setting the (EXT, P)

(0, 0) – Timer0 Count Register is incremented by one every four internal processor clock.

(0, 1) – Timer0 count register is incremented by one which is prescaled by timer 2.

(1, x) – The TMRIN0 pin input acts as clock source and Timer0 Count Register is incremented by one every external clock.

Bit 2: EXT, External Clock Bit.

Set 1: Timer0 clock source from external

Set 0: Timer0 clock source from internal

Bit 1: ALT, Alternate Compare Bit. This bit controls whether the timer runs in single or dual maximum count mode.

Set 1: Specifies dual maximum count mode. In this mode, the timer counts to Maxcount Compare A and resets the count register to 0. Then the timer counts to Maxcount Compare B, resets the count

register to 0 again, and starts over with Maxcount Compare A.

Set 0: Specifies single maximum count mode. In this mode, the timer counts to the value contained in Maxcount Compare A and reset to 0. Then the timer counts to Maxcount Compare A again. Maxcount Compare B is not used in this mode.

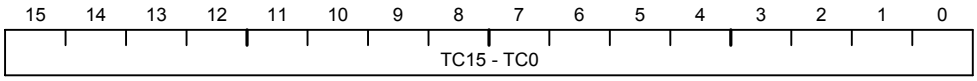
Bit 0: CONT, Continuous Mode Bit.

Set 1: The timer runs continuously.

Set 0: The timer will halt after each counting to the maximum count and the EN bit will be cleared.

Timer 0 Count Register

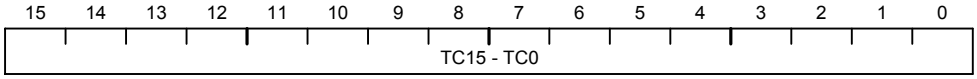
Offset : 50h
Reset Value : —



Bit 15 – 0: TC15-TC0, Timer 0 Count Value. This register contains the current count of timer 0. The count is incremented by one every four internal processor clocks, pre-scaled by timer 2, or incremented by one every external clock which is through configuring the external clock select bit based on the TMRIN0 signal.

Timer 0 Maxcount Compare A Register

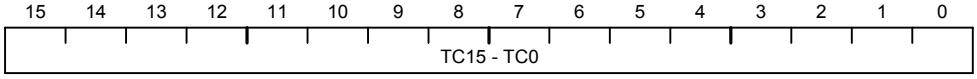
Offset : 52h
Reset Value : —



Bit 15-0: TC15 – TC0, Timer 0 Compare A Value.

Timer 0 Maxcount Compare B Register

Offset : 54h
Reset Value : —



Bit 15-0: TC15 – TC0, Timer 0 Compare B Value.

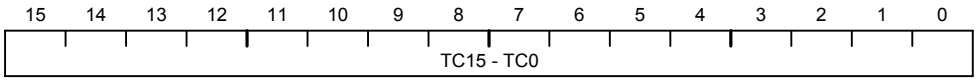
Timer 1 Mode / Control Register

Offset : 5Eh
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{INH}$	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

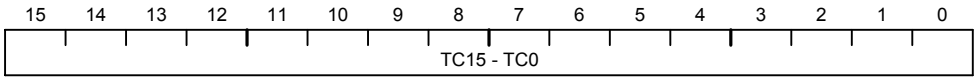
These bit definitions for timer 1 are the same as those of register 56h for timer0.

Timer 1 Count Register **Offset : 58h**
Reset Value : —



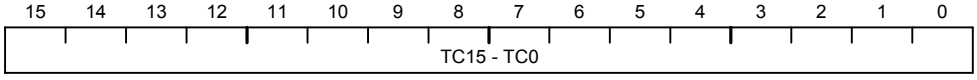
Bit 15 – 0: TC15-TC0, Timer 1 Count Value. This register contains the current count of timer 1. The count is incremented by one every four internal processor clocks, pre-scaled by timer 2, or incremented by one every external clock which is through configuring the external clock select bit based on the TMRIN1 signal.

Timer 1 Maxcount Compare A Register **Offset : 5Ah**
Reset Value : —



Bit 15-0: TC15 – TC0, Timer 1 Compare A Value.

Timer 1 Maxcount Compare B Register **Offset : 5Ch**
Reset Value : —



Bit 15-0: TC15 – TC0, Timer 1 Compare B Value.

Timer 2 Mode / Control Register **Offset : 66h**
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{INH}$	INT	0	0	0	0	0	0	0	MC	0	0	0	0	CONT

Bit 15: EN, Enable Bit.

Set 1: Timer 2 is enabled.

Set 0: Timer 2 is inhibited from counting.

The $\overline{INH}$ bit must be set to 1 when the EN bit is written, and the $\overline{INH}$ and EN bits must be in the same write.

Bit 14: $\overline{INH}$, Inhibit Bit. This bit allows selective updating the EN bit. The $\overline{INH}$ bit must be set to 1 when the EN bit is written, and both the $\overline{INH}$ and EN bits must be in the same write. This bit is not stored and

always read as 0.

Bit 13: INT, Interrupt Bit.

Set 1: An interrupt request is generated when the count register equals a maximum count.

Set 0: Timer 2 will not issue interrupt requests.

Bit 12-6: Reserved.

Bit 5: MC, Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. This bit is set regardless of the INT bit (66h.13).

Bit 4-1: Reserved.

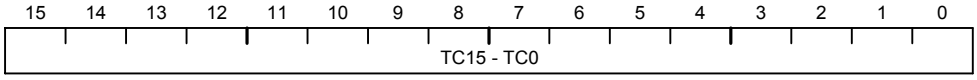
Bit 0: COUNT, Continuous Mode Bit.

Set 1: The timer is continuously running when it reaches the maximum count.

Set 0: The EN bit (66h.15) is cleared and the timer is held after each timer count reaches the maximum count.

Timer 2 Count Register **Offset : 60h**

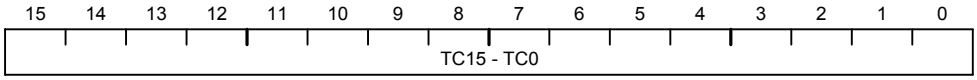
Reset Value : —



Bit 15 – 0: TC15-TC0, Timer 2 Count Value. This register contains the current count of timer 2. The count is incremented by one every four internal processor clocks.

Timer 2 Maxcount Compare A Register **Offset : 62h**

Reset Value : —



Bit 15-0: TC15 – TC0, Timer 2 Compare A Value.

16.1 Watchdog Timer

Timer 1 can also be configured as a watchdog timer. Software must first be used to program the Timer 1 Mode/Control (5Eh), Count (58h), and Max Count (5Ah and 5Ch) registers and then program the Watchdog Timer Interrupt Control Register (42h) to enable the watchdog timer interrupt. Timer 1 Count Register must be reloaded at intervals less than the Timer 1 Maxcount value to assure the watchdog interrupt will not occurred.

Watchdog Timer Interrupt Control Register

Offset : 42h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of the watchdog timer

Set 0: Enable the watchdog timer interrupt.

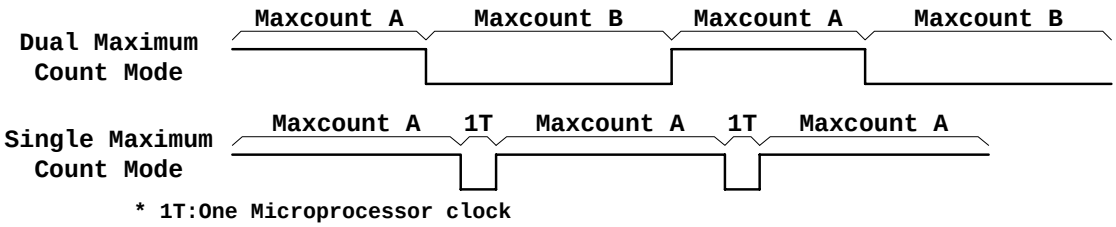
Bit 2- 0: PR, Priority.

The priority selection:

PR2, **PR1**, **PR0** -- **Priority**	
0 , 0 , 0 -- 0	(High)
0 , 0 , 1 -- 1	
0 , 1 , 0 -- 2	
0 , 1 , 1 -- 3	
1 , 0 , 0 -- 4	
1 , 0 , 1 -- 5	
1 , 1 , 0 -- 6	
1 , 1 , 1 -- 7	(Low)

16.2 Timer/Counter Unit Output Mode

Timers 0 and 1 can use one maximum count value or two maximum count values. Timer 2 can use only one maximum count value. Timer 0 and timer1 can be configured to be a single or dual Maximum Compare count mode. The TMROUT0 or TMROUT1 signals can be used to generate waveforms of various duty cycles.

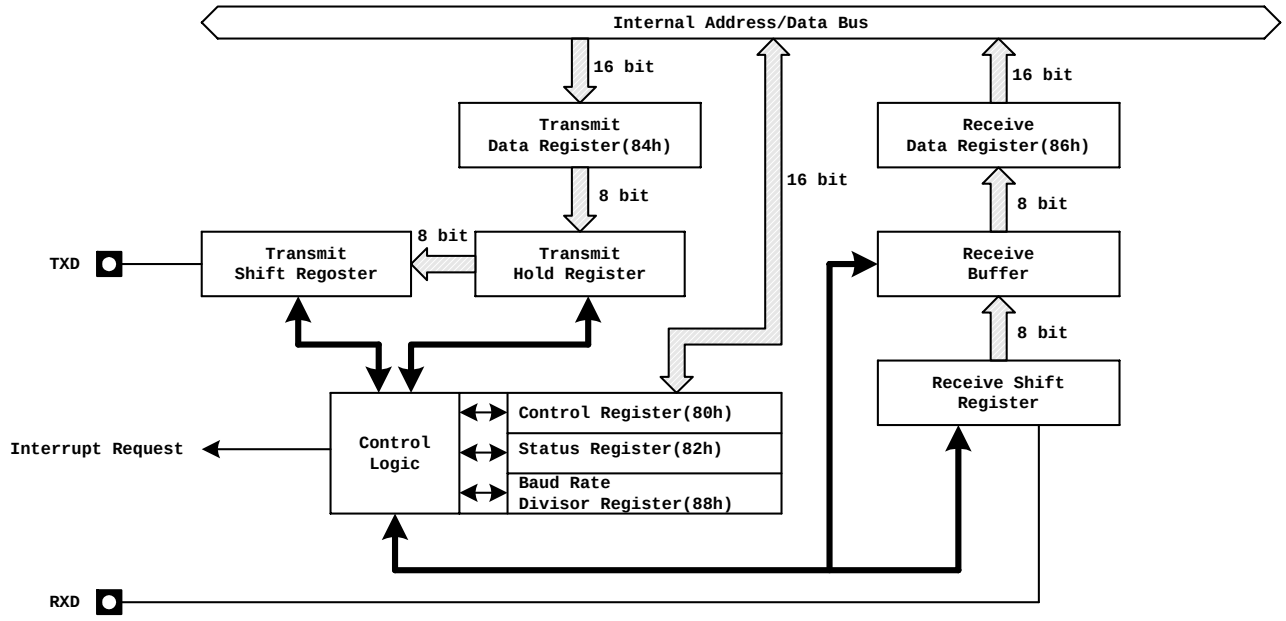


Timer/Counter Unit Output Modes

17. Asynchronous Serial Port

The R8800 asynchronous serial port provides the TXD and RXD pins for the full duplex bi-directional data transfer without handshaking signals. The UART port supports: 8-bit or 7-bit data transfers; odd parities, even parities, or no parity; 1 or 2 stop bits. DMA transfers through the serial port are not supported.

The receive/transmit clock is based on the microprocessor clock. The serial port can be used in power-saved mode, but the transfer rate must be adjusted to correctly reflect the new internal operating frequency. Software is programmed through the 80h, 82h, 84h, 86h and 88h registers to configure the asynchronous serial port.



Serial Port Block Diagram

Serial Port Control Register

Offset : 80h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				TXIE	RXIE	LOOP	BRK	BRKVAL	PMODE		WLGN	STP	TMOD	RSIE	RMODE

Bit 15-12: Reserved.

Bit 11: TXIE, Transmit Holding Register Empty Interrupt Enable.

This bit is set 1 to enable the serial port to generate an interrupt request when the transmit holding register is empty.

Bit 9: LOOP, Loopback.

Set 1: The serial port in the loopback mode. In this mode, the transmit shift register is connected to the

transmit shift register internally and the TXD pin output high. It provides the serial port testing in this mode.

Bit 8: BRK, Send Break. You should check if the TEMT bit (82h.6) is a 1 before setting the BRK bit.

Set 1: The serial port send a frame of continuous level output on the TXD pin and the output level depends on the BRAVAL bit status, when any data is written to the transmit data register.

Bit 7: BRKVAL, Break Value.

Set 1: The TXD pin continuously drives high-level signal during send break operations.

Set 0: The TXD pin continuously drives low-level signal during send break operations.

Bit 6-5: PMODE, Parity Mode. Parity generation and checking during transmission and reception.

Parity mode selection by (Bit 6, Bit 5) : (0, x) – No parity bit in frame , (1, 0) – Odd number of 1s in frame. (1, 1) – Even number of 1s in frame.

Bit 4: WLGN, Word Length. Set 1: The serial port sends and receives 8 bits of data per frame.
Set 0: The serial port sends and receives 7 bits of data per frame.

Bit 3: STP, Stop Bits. Set 1: Two stop bits are used to signify the end of a frame.
Set 0: One stop bit are used to signify the end of a frame.

Bit 2: TMODE, Transmit Mode. Set 1: Enable the transmit section of the serial port.
Set 0: Disable the transmit section of the serial port.

Bit 1: RSIE, Receive Status interrupt Enable.

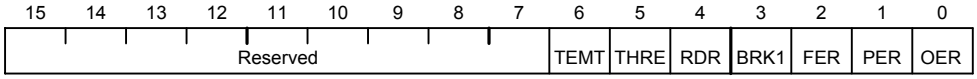
Set 1: Enable the receive section of serial port to generate an interrupt

Set 0: Disable the receive section of serial port to generate an interrupt

Bit 0: RMODE, Receive Mode. Set 1: Enable the receive section of the serial port.
Set 0: Disable the receive section of the serial port.

Serial Port Status Register

Offset : 82h
Reset Value : ——



Bit 15-7: Reserved

Bit 6: TEMT, Transmitter Empty. Read-only bit. This bit is set by H/W when the transmit shift register is empty. The transmit function cannot be disabled when the bit is 0.

Bit 5: THRE, Transmit Holding Register Empty. Read only bit. When this bit is 1, the transmit holding buffer contains invalid data and the transmit data register (84h) can be written by new data. When this bit is 0, it indicates that transmit holding buffer contains valid data that haven't been copied to transmit shift register and the transmit data register (84h) can not be written by new data.

When the transmit interrupt is enabled, a serial port interrupt is generated when this bit is 1. The THRE bit

is automatically cleared by H/W when data are copied to transmit holding buffer.

Bit 4: RDR, Receive Data Ready. Read only bit. When the receive data register is ready to read, this bit is 1. When this bit is 0, the receive data register will not contain valid data. This bit will be cleared by H/W when the receive data register is read.

Bit 3: BRKI, Break Interrupt. It indicates that a break has been received when this bit is set to 1 and it will generate a serial port interrupt request if the RISE bit (80h.1) is enabled. This bit is set by H/W and should be cleared by software.

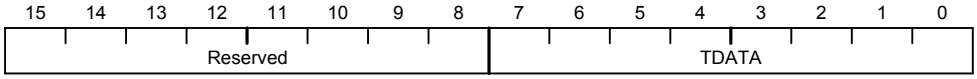
Bit 2: FER, Framing Error. This bit is set to indicate that a framing error occurred during reception of data and it will generate a serial port interrupt request if the RISE bit (80h.1) is enabled. This bit is set by H/W and should be cleared by software.

Bit 1: PER, Parity Error. This bit is set to indicate that a party error occurred during reception of data and it will generate a serial port interrupt request if the RISE bit (80h.1) is enabled. This bit is set by H/W and should be cleared by software.

Bit 0: OER, Overrun Error. This bit is set to indicate that an overrun error occurred during reception of data and it will generate a serial port interrupt request if the RISE bit (80h.1) is enabled. This bit is set by H/W and should be cleared by software.

Serial Port Transmit Data Register

Offset : 84h
Reset Value : —

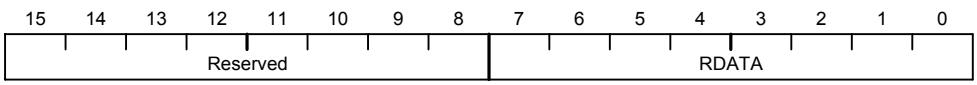


Bit 15-8: Reserved

Bit 7-0: TDATA, Transmit Data. This register is written by software with data to be transmitted on the serial port. The THRE bit (82h.5) should be read as a 1 before this register is written to avoid overwriting data to this register. When data are written to this register, the THRE bit will be cleared by H/W in the same time.

Serial Port Receive Data Register

Offset : 86h
Reset Value : —

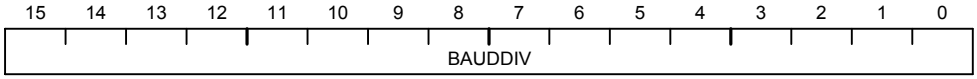


Bit 15-8: Reserved

Bit 7-0: RDATA, Received DATA. The PDR bit (82h.4) should be read as 1 before the RDATA register is read to avoid reading invalid data.

Serial Port Baud Rate Divisor Register

Offset : 88h
Reset Value : —



Bit 15-0: BAUDDIV, Baud Rate Divisor.

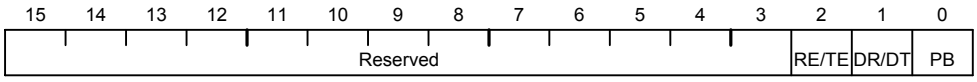
The general formula for baud rate divisor is **Baud Rate = Microprocessor Clock / [32 * (BAUDDIV+1)]**
For example, when the Microprocessor clock is 22.1184MHz and the BAUDDIV=5 (Decimal), the baud rate of serial port is 115.2k.

18. Synchronous Serial Port

There are four pins for synchronous serial port interface, which is half duplexed, bi-directional data transfer. The synchronous serial interface operates in a master/slave configuration, and the synchronous serial port of R8800 as a master mode. The SCLK frequency is affected by the reduced microprocessor clock frequency when in power-save mode. Software is used to program the 10h, 12h, 14h, 16h and 18h to configure the synchronous serial port interface.

Synchronous Serial Status Register

Offset : 10h
Reset Value : 0000h



A Read-only register that indicates the state of the SSI port.

Bit 15-3: Reserved.

Bit 2: RE/TE, Receive/Transmit Error Detect.

Set 1: Either a read of Synchronous Serial Receive register or a write to one transmit registers while the SSI is busy (PB=1).

Set 0: SDEN output is inactive.

Bit 1: DR/TR, Data Receive/Transmit Complete.

Set 1: End of the transfer of data bit 7 (SCLK rising edge) during a transmit or receive operation.

Set 0: When the SSR register is read, when one of the SSD0 or SSD1 registers is written, when the SSS register is read, or when both SDEN0 and SDEN1 become inactive.

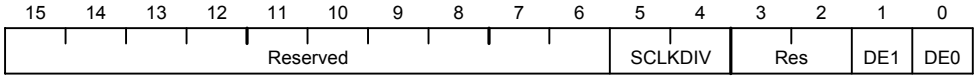
Bit 0: PB, SSI port Busy.

Set 1: A transmit or receive operation is in progress.

Set 0: The port is ready to transmit or receive data.

Synchronous Serial Control Register

Offset : 12h
Reset Value : 0000h



This read/write register which controls the operation of the SDEN0-SDEN1 outputs the transfer rate of the SSI port.

Bit 15-6, 3-2: Reserved.

Bit 5-4: SCLKDIV, SCLK Divide.

SCLKDIV	SCLK Frequency Divider
00b	Processor clock/2
01b	Processor clock/4
10b	Processor clock/8
11b	Processor clock/16

Bit 1: DE1, SDEN1 Enable.

Set 1: SDEN1 pin is held High.

Set 0: SDEN1 pint is Low.

Bit 0: DE0, SDEN0 Enable.

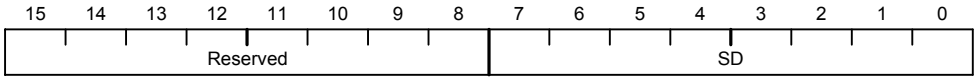
Set 1: SDEN0 pin is held High.

Set 0: SDEN0 pint is Low.

Synchronous Serial Transmit 1 Register

Offset : 14h

Reset Value : —



Synchronous Serial Transmit 1 Register. The register contains data to be transferred from the processor to the peripheral on a write operation.

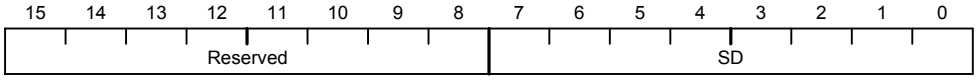
Bit 15-8: Reserved.

Bit 7-0: SD, Send Data. Data transmitted over the SDATA pin.

Synchronous Serial Transmit 0 Register

Offset : 16h

Reset Value : —



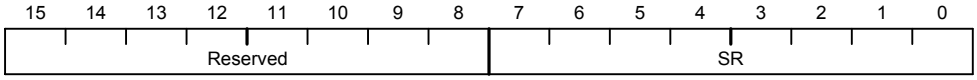
Synchronous Serial Transmit 0 Register. The register contains data to be transferred from the processor to the peripheral on a write operation.

Bit 15-8: Reserved.

Bit 7-0: SD, Send Data. Data transmitted over the SDATA pin.

Synchronous Serial receive Register

Offset : 18h
Reset Value : —



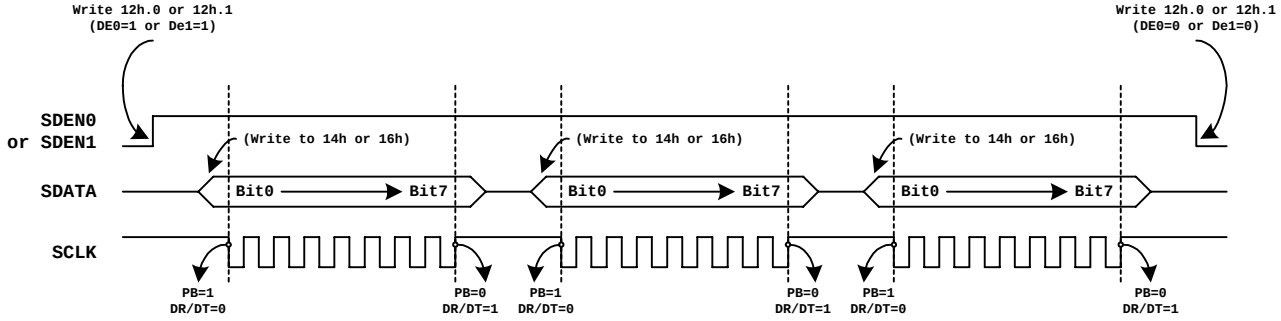
The Synchronous Serial Receive Register contains the data transferred from the peripheral to the processor on a read operation.

Bit 15-8: Reserved.

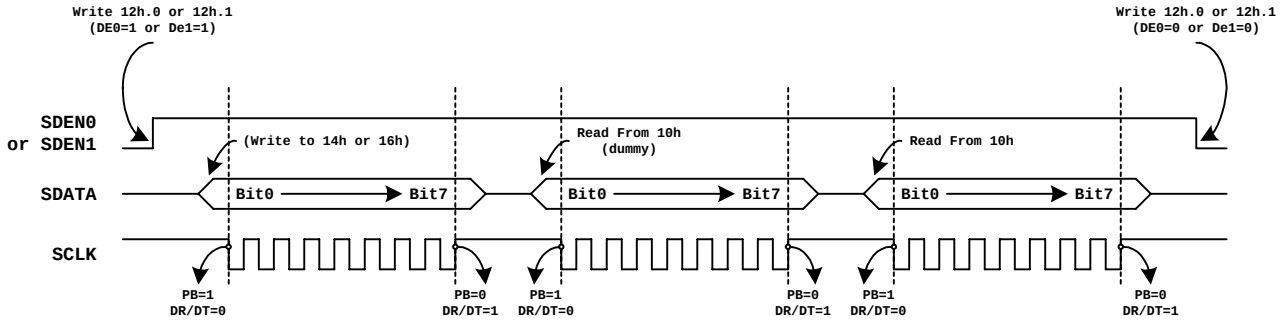
Bit 7-0: SR, Receive Data. Data received over the SDATA pin.

18.1 Synchronous Serial Port Operations

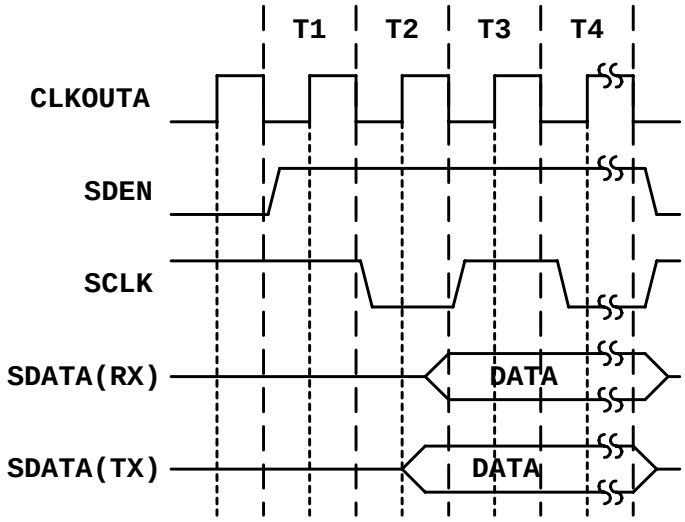
The following figures show the data transmit and receive operations.



Synchronous Serial Port Multiple Write



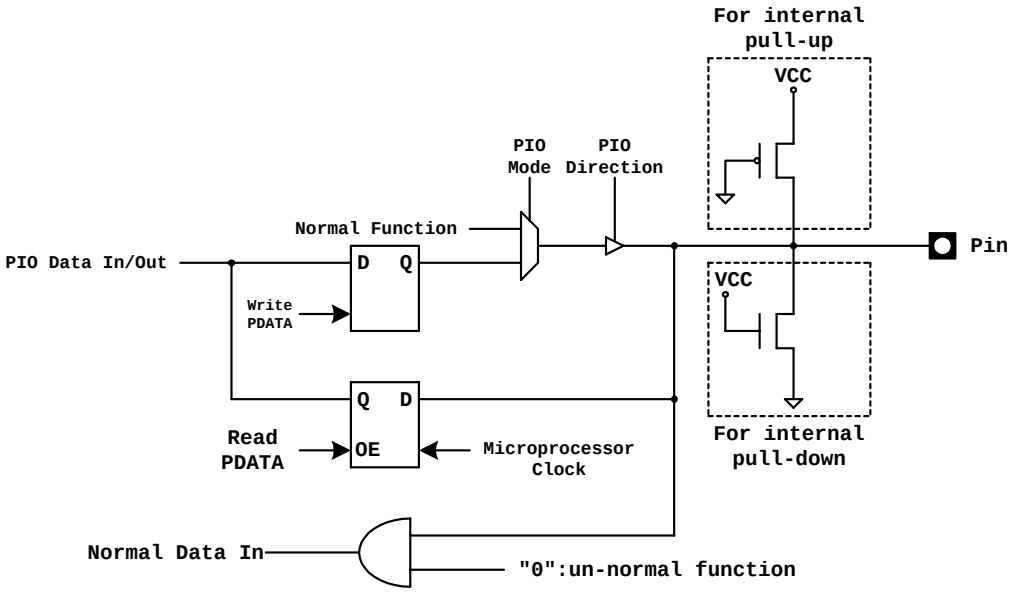
Synchronous Serial Port Multiple Read



Synchronous Serial Interface Waveforms

19. PIO Unit

The R8800 provides 32 programmable I/O signals, which are multi-functional pins, with other signals of normal functions. Software is used to program the registers (7Ah, 78h, 76h, 74h, 72h and 70h) to configure the multi-functional pins for PIO or normal functions.



PIO pin Operation Diagram

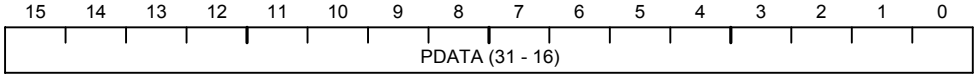
19.1 PIO Multi-Functional Pin List Table

PIO No.	Pin No.(PQFP)	Multi Function	Reset status/PIO internal resistor
0	72	TMRIN1	Input with 10k pull-up
1	73	TMROUT1	Input with 10k pull-down
2	59	$\overline{PCS6}$ /A2	Input with 10k pull-up
3	60	$\overline{PCS5}$ /A1	Input with 10k pull-up
4	48	DT/$\overline{R}$	Normal operation/ Input with 10k pull-up
5	49	DEN	Normal operation/ Input with 10k pull-up
6	46	SRDY	Normal operation/ Input with 10k pull-down
7	22	A17	Normal operation/ Input with 10k pull-up
8	20	A18	Normal operation/ Input with 10k pull-up
9	19	A19	Normal operation/ Input with 10k pull-up
10	74	TMROUT0	Input with 10k pull-down
11	75	TMRIN0	Input with 10k pull-up
12	77	DRQ0	Input with 10k pull-up
13	76	DRQ1	Input with 10k pull-up
14	50	$\overline{MCS0}$	Input with 10k pull-up
15	51	$\overline{MCS1}$	Input with 10k pull-up
16	66	$\overline{PCS0}$	Input with 10k pull-up

17	65	$\overline{PCS1}$	Input with 10k pull-up
18	63	$\overline{PCS2}$	Input with 10k pull-up
19	62	$\overline{PCS3}$	Input with 10k pull-up
20	3	SCLK	Input with 10k pull-up
21	100	SDATA	Input with 10k pull-up
22	2	SDEN0	Input with 10k pull-down
23	1	SDEN1	Input with 10k pull-down
24	68	$\overline{MCS2}$	Input with 10k pull-up
25	69	$\overline{MCS3}$ / $\overline{RFSH}$	Input with 10k pull-up
26	97	$\overline{UZI}$	Input with 10k pull-up
27	98	TXD	Input with 10k pull-up
28	99	RXD	Input with 10k pull-up
29	96	S6/ $\overline{CLKDIV2}$	Input with 10k pull-up
30	52	INT4	Input with 10k pull-up
31	54	INT2	Input with 10k pull-up

PIO Data 1 Register

Offset : 7Ah
Reset Value : ——

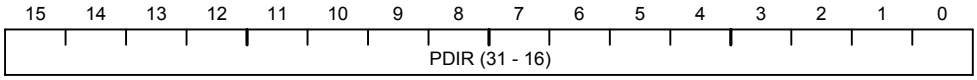


Bit 15- 0: PDATA31-PDATA16, PIO Data Bits.

These bits PDATA31- PDATA16 are mapped to PIO31 –PIO16 which indicate the driven level when the PIO pin functions as an output or reflect the external level when the PIO pin functions as an input.

PIO Direction 1 Register

Offset : 78h
Reset Value : FFFFh



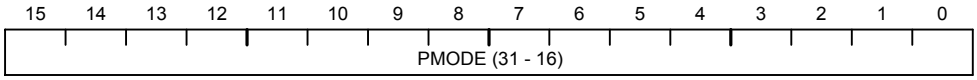
Bit 15-0: PDIR 31- PDIR16, PIO Direction Register.

Set 1: Configures the PIO pin as an input.

Set 0: Configures the PIO pin as an output or as normal pin function.

PIO Mode 1 Register

Offset : 76h
Reset Value : 0000h



Bit 15-0: PMODE31-PMODE16, PIO Mode Bit.

The definitions of PIO pins are configured by the combination of PIO Mode and PIO Direction. The PIO pins are programmed individually.

The definitions (PIO Mode, PIO Direction) for PIO pin functions:

(0 , 0) – Normal operation , (0 , 1) – PIO input with pullup/pulldown

(1 , 0) – PIO output , (1 , 1) -- PIO input without pullup/pulldown

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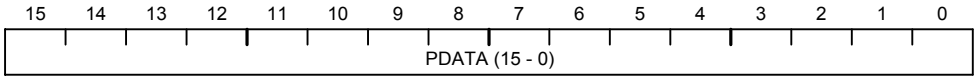
PIO Data 0 Register

Offset : 74h
Reset Value : —

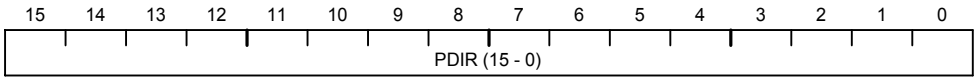


Bit 15-0: PDATA15- PDATA0: PIO Data Bus.

These bits PDATA15- PDATA0 are mapped to PIO15 –PIO0 which indicate the driven level when the PIO pin functions as an output or reflect the external level when the PIO pin functions as an input.

PIO Direction 0 Register

Offset : 72h
Reset Value : FC0Fh



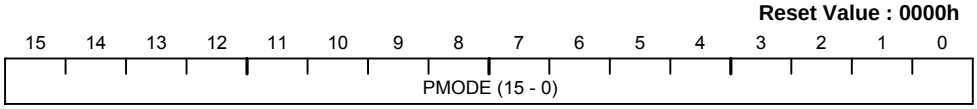
Bit 15-0: PDIR 15- PDIR0, PIO Direction Register.

Set 1: Configures the PIO pin as an input.

Set 0: Configures the PIO pin as an output or as normal pin function.

PIO Mode 0 Register

Offset : 70h
Reset Value : 0000h



Bit 15-0: PMODE15-PMODE0, PIO Mode Bit.

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20. PSRAM Control Unit

The PSRAM interface is provided by the R8800 and the refresh control unit automatically generates refresh bus cycles. The refresh control unit uses the internal microprocessor clock as an operating source clock. If the power-saved mode is enabled, the refresh control unit must be programmed to reflect the new clock rate. Software is used to program the registers (E0, E2 and E4) to control the refresh control unit operation.

Memory Partition Register **Offset : E0h**
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M6 - M0							0	0	0	0	0	0	0	0	0

Bit 15-9: M6-M0, Refresh Base. M6-M0 are mapped to A19-A13 of the 20-bit memory refresh address.
Bit 8-0: Reserved.

Clock Prescaler Register **Offset : E2h**
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RC8 - RC0								

Bit 15-9: Reserved
Bit 8-0: RC8-RC0, Refresh Counter Reload Value.

Enable RCU Register **Offset : E4h**
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E	0	0	0	0	0	0	T8 - T0								

Bit 15: E, Enable RCU.
Set 1: Enable the refresh counter unit
Set 0: Disable the refresh counter unit.
Bit 14-9: Reserved
Bit 8-0: T8-T0, Refresh Count. Read-only bits and these bits present value of the down counter which triggers refresh requests.

---

21. Instruction Set OPCodes and Clock Cycles

Function	Format				Clocks	Notes
DATA TRANSFER INSTRUCTIONS						
MOV = Move						
register to register/memory	1000100w	mod reg r/m			1/1	
register/memory to register	1000101w	mod reg r/m			1/6	
immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	1/1	
immediate to register	1011w reg	data	data if w=1		1	
memory to accumulator	1010000w	addr-low	addr-high		6	
accumulator to memory	1010001w	addr-low	addr-high		1	
register/memory to segment register	10001110	mod 0 reg r/m			3/8	
segment register to register/memory	10001100	mod 0 reg r/m			2/2	
PUSH = Push						
memory	11111111	mod 110 r/m			8	
register	01010 reg				3	
segment register	000reg110				2	
immediate	011010s0	data	data if s=0		1	
POP = Pop						
memory	10001111	mod 000 r/m			8	
register	01011 reg				6	
segment register	000 reg 111	(reg≠01)			8	
PUSHA = Push all	01100000				36	
POPA = Pop all	01100001				44	
XCHG = Exchange						
register/memory	1000011w	mod reg r/m			3/8	
register with accumulator	10010 reg				3	
XTAL = Translate byte to AL	11010111				10	
IN = Input from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
OUT = Output from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
LEA = Load EA to register	10001101	mod reg r/m			1	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		14	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		14	
ENTER = Build stack frame	11001000	data-low	data-high	L		
L = 0					7	
L = 1					11	
L > 1					11+10(L-1)	
LEAVE = Tear down stack frame	11001001				7	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				2	
PUSHF = Push flags	10011100				2	
POPF = Pop flags	10011101				11	
ARITHMETIC INSTRUCTIONS						
ADD = Add						
reg/memory with register to either	000000dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 000 r/m	data	data if sw=01	1/8	
immediate to accumulator	0000010w	data	data if w=1		1	
Function	**Format**				**Clocks**	**Notes**
ADC = Add with carry						

reg/memory with register to either	000100dw	mod reg r/m			1/7
immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	1/8
immediate to accumulator	0001010w	data	data if w=1		1
INC = Increment					
register/memory	1111111w	mod 000 r/m			1/8
register	01000 reg				1
SUB = Subtract					
reg/memory with register to either	001010dw	mod reg r/m			1/7
immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	1/8
immediate from accumulator	0001110w	data	data if w=1		1
SBB = Subtract with borrow					
reg/memory with register to either	000110dw	mod reg r/m			1/7
immediate from register/memory	100000sw	mod 011 r/m			1/8
immediate from accumulator	0001110w	data	data if w=1		1
DEC = Decrement					
register/memory	1111111w	mod 001 r/m			1/8
register	01001 reg				1
NEG = Change sign					
register/memory	1111011w	mod reg r/m			1/8
CMP = Compare					
register/memory with register	0011101w	mod reg r/m			1/7
register with register/memory	0011100w	mod reg r/m			1/7
immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	1/7
immediate with accumulator	0011110w	data	data if w=1		1
MUL = multiply (unsigned)	1111011w	mod 100 r/m			
register-byte					13
register-word					21
memory-byte					18
memory-word					26
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m			
register-byte					16
register-word					24
memory-byte					21
memory-word					29
register/memory multiply immediate (signed)	011010s1	mod reg r/m	data	data if s=0	23/28
DIV = Divide (unsigned)	1111011W	mod 110 r/m			
register-byte					18
register-word					26
memory-byte					23
memory-word					31
IDIV = Integer divide (signed)	1111011w	mod 111 r/m			
register-byte					18
register-word					26
memory-byte					23
memory-word					31
AAS = ASCII adjust for subtraction	00111111				3
DAS = Decimal adjust for subtraction	00101111				2
AAA = ASCII adjust for addition	00110111				3
DAA = Decimal adjust for addition	00100111				2
AAD = ASCII adjust for divide	11010101	00001010			14
AAM = ASCII adjust for multiply	11010100	00001010			15
CBW = Corrvert byte to word	10011000				2
CWD = Convert word to double-word	10011001				2

Function	Format				Clocks	Notes
BIT MANIPULATION INSTRUCTUIONS						
NOT = Invert register/memory	1111011w	mod 010 r/m			1/7	
AND = And						
reg/memory and register to either	001000dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1	1/8	
immediate to accumulator	0010010w	data	data if w=1		1	
OR = Or						
reg/memory and register to either	000010dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	1/8	
immediate to accumulator	0000110w	data	data if w=1		1	
XOR = Exclusive or						
reg/memory and register to either	001100dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	1/8	
immediate to accumulator	0011010w	data	data if w=1		1	
TEST = And function to flags , no result						
register/memory and register	1000010w	mod reg r/m			1/7	
immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	1/8	
immediate data and accumulator	1010100w	data	data if w=1		1	
Sifts/Rotates						
register/memory by 1	1101000w	mod TTT r/m			2/8	
register/memory by CL	1101001w	mod TTT r/m			1+n / 7+n	
register/memory by Count	1100000w	mod TTT r/m	count		1+n / 7+n	
STRING MANIPULATION INSTRUCTIONS						
MOVS = Move byte/word	1010010w				13	
INS = Input byte/word from DX port	0110110w				13	
OUTS = Output byte/word to DX port	0110111w				13	
CMPS = Compare byte/word	1010011w				18	
SCAS = Scan byte/word	101011w				13	
LODS = Load byte/word to AL/AX	1010110w				13	
STOS = Store byte/word from AL/AX	1010101w				7	
Repeated by count in CX:						
MOVS = Move byte/word	11110010	1010010w			4+9n	
INS = Input byte/word from DX port	11110010	0110110w			5+9n	
OUTS = Output byte/word to DX port	11110010	0110111w			5+9n	
CMPS = Compare byte/word	1111011z	1010011w			4+18n	
SCAS = Scan byte/word	1111001z	1010111w			4+13n	
LODS = Load byte/word to AL/AX	11110010	0101001w			3+9n	
STOS = Store byte/word from AL/AX	11110100	0101001w			4+3n	
PROGRAM TRANSFER INSTRUCTIONS						
Conditional Transfers — jump if:						
JE/JZ = equal/zero	01110100	disp			1/9	
JL/JNGE = less/not greater or equal	01111100	disp			1/9	
JLE/JNG = less or equal/not greater	01111110	disp			1/9	
JC/JB/JNAE = carry/below/not above or equal	01110010	disp			1/9	
JBE/JNA = below or equal/not above	01110110	disp			1/9	
JP/JPE = parity/parity even	01111010	disp			1/9	
JO = overflow	01110000	disp			1/9	
JS = sign	01111000	disp			1/9	
JNE/JNZ = not equal/not zero	01110101	disp			1/9	
JNL/JGE = not less/greater or equal	01111101	disp			1/9	
JNLE/JG = not less or equal/greater	01111111	disp			1/9	
JNC/JNB/JAE = not carry/not below /above or equal	01110011	disp			1/9	
JNBE/JA = not below or equal/above	01110111	disp			1/9	
JNP/JPO = not parity/parity odd	01111011	disp			1/9	

Function	Format			Clocks	Notes
JNO = not overflow	01110001	disp		1/9	
JNS = not sign	01111001	disp		1/9	
Unconditional Transfers					
CALL = Call procedure					
direct within segment	11101000	disp-low	disp-high	11	
reg/memory indirect within segment	11111111	mod 010 r/m		12/17	
indirect intersegment	11111111	mod 011 r/m	(mod≠11)	25	
direct intersegment	10011010	segment offset		18	
		selector			
RET = **Retum from procedure**					
within segment	11000011			16	
within segment adding immed to SP	11000010	data-low	data-high	16	
intersegment	11001011			23	
instersegment adding immed to SP	1001010	data-low	data-high	23	
JMP = **Unconditional jump**					
short/long	11101011	disp-low		9/9	
direct within segment	11101001	disp-low	disp-high	9	
reg/memory indirect within segment	11111111	mod 100 r/m		11/16	
indirect intersegment	11111111	mod 101 r/m	(mod ?11)	18	
direct intersegment	11101010	segment offset		11	
		selector			
Iteration Control					
LOOP = Loop CX times	11100010	disp		7/16	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp		7/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp		7/16	
JCXZ = Jump if CX = zero	11100011	disp		7/15	
Interrupt					
INT = Interrupt					
Type specified	11001101	type		41	
Type 3	11001100			41	
INTO = Interrupt on overflow	11001110			43/4	
BOUND = Detect value out of range	01100010	mod reg r/m		21-60	
IRET = Interrupt return	11001111			31	
PROCESSOR CONTROL INSTRUCTIONS					
CLC = clear carry	11111000			2	
CMC = Complement carry	11110101			2	
STC = Set carry	11111001			2	
CLD = Clear direction	11111100			2	
STD = Set direction	11111101			2	
CLI = Clear interrupt	11111010			5	
STI = Set interrupt	11111011			5	
HLT = Halt	11110100			1	
WAIT = Wait	10011011			1	
LOCK = Bus lock prefix	11110000			1	
ESC = Math coprocessor escape	11011MMM	mod PPP r/m		1	
NOP = No operation	10010000			1	
SEGMENT OVERRIDE PREFIX					
CS	00101110			2	
SS	00110110			2	
DS	00111110			2	
ES	00100110			2	

22. R8800 Execution Timings

The above instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

1. The opcode, along with data or displacement required for execution, has been prefetched and resided in the instruction queue at the time needed.

2. No wait states or bus HOLDs occur.

3. All word -data is located on even-address boundaries.

4. One RISC micro operation (*u*OP) maps one cycle (according to the pipeline stages described below), except the following case:

Pipeline Stages for single micro operations (one cycle):

Fetch → Decode → op_r → ALU → WB (For ALU function *u*OP)

Fetch → Decode → EA → Access → WB (For Memory function *u*OP)

4.1 *Memory read u*OP needs 6 cycles for bus.

Pipeline stages for *Memory read u*OP(6 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB

Bus Cycle

4.2 *Memory push u*OP needs 1 cycle if it has no previous *Memory push u*OP, and 5 cycles if it has previous *Memory push* or *Memory Write u*OP.

Pipeline stages for *Memory push u*OP after *Memory push u*OP (another 5 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB (1st *Memory push u*OP)

(2nd *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

pipeline stall

4.3 *MUL u*OP and *DIV* of ALU function *u*OP for 8-bit operation need both 8 cycles, for 16-bit operation need both 16 cycles.

4.4 All jumps, calls, ret and loopXX instructions required to fetch the next instruction for the destination address (*Unconditional Fetch u*OP) will need 9 cycles.

Pipeline stages for unconditional fetch:

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → Fetch (*Fetch u*OP)

(next *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

will be flushed

These 9 cycles caused branch penalty

→ Fetch → Decode → following stages...(New *u*OP)

***Note**: op_r: operand read stage, EA: Calculate Effective Address stage, Idle: Bus Idle stage, T0..T3: Bus T0..T3 stage, Access: Access data from cache memory stage.*

23. DC Characteristics

23.1 Absolute Maximum Rating

Symbol	Rating	Commercial	Unit	Note
V_{Term}	Terminal Voltage with Respect to GND	-0.5~V_{CC}+0.5	V	
T_A	Ambient Temperature	0~+70	°C	

23.2 Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5	5.25	V
GND	Ground	0	0	0	V
Vih	Input High Voltage (**Note 1**)	2.0	---	Vcc+0.5	V
Vih1	Input High Voltage ($\overline{RST}$)	3	---	Vcc+0.5	V
Vih2	Input High Voltage (X1)	3	---	Vcc+0.5	V
Vil	Input Low voltage	-0.5	0	0.8	V

Note 1: *The* $\overline{RST}$ *and X1 pins are not included.*

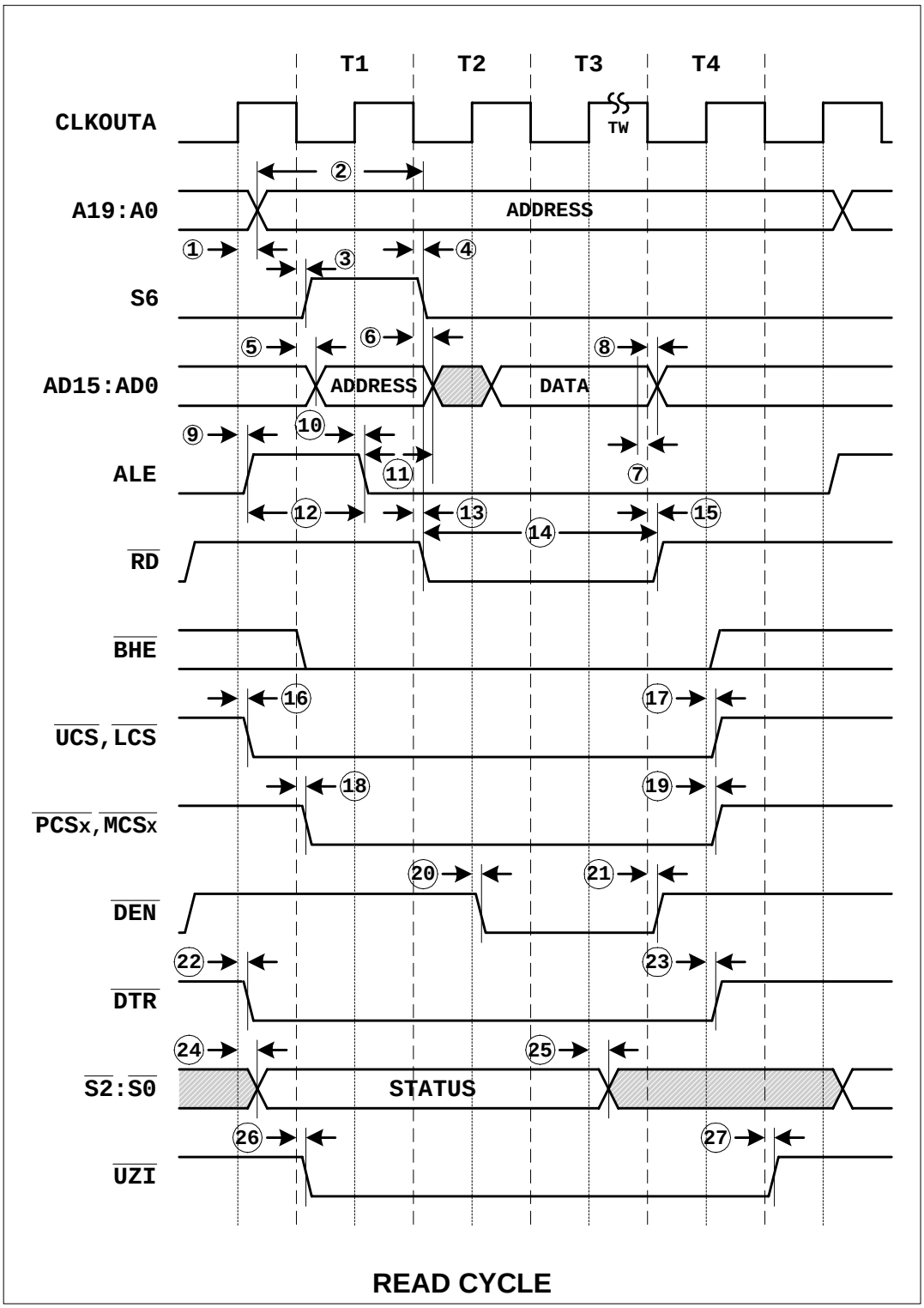
23.3 DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Unit
Ili	Input Leakage Current	Vcc=Vmax Vin=GND to Vmax	-10	10	uA
Ili (with 10K pull R)	Input Leakage Current With Pull_R 10K enable	Vcc=Vmax Vin=GND to Vmax	-400	400	uA
Ili (with 50K pull R)	Input Leakage Current With Pull_R 50K	Vcc=Vmax Vin=GND to Vmax	-120	120	uA
Ilo	Output Leakage Current	Vcc=Vmax Vin=GND to Vmax	-10	10	uA
VOL	Output Low Voltage	Iol=6mA, Vcc=Vmin.	---	0.4	V
VOH	Output High Voltage	Ioh=-6mA, Vcc=Vmin.	2.4	---	V
Icc	Max Operating Current	Vcc=5.25V 40MHz	---	180	mA

Note 2:*Vmax=5.25V Vmin=4.75V*

Symbol	Parameter	Min.	Max.	Unit	Note
F_{Max}	Max operation clock frequency of commercial	---	40	Mhz	$V_{CC} \pm 5\%$

24. AC Characteristics



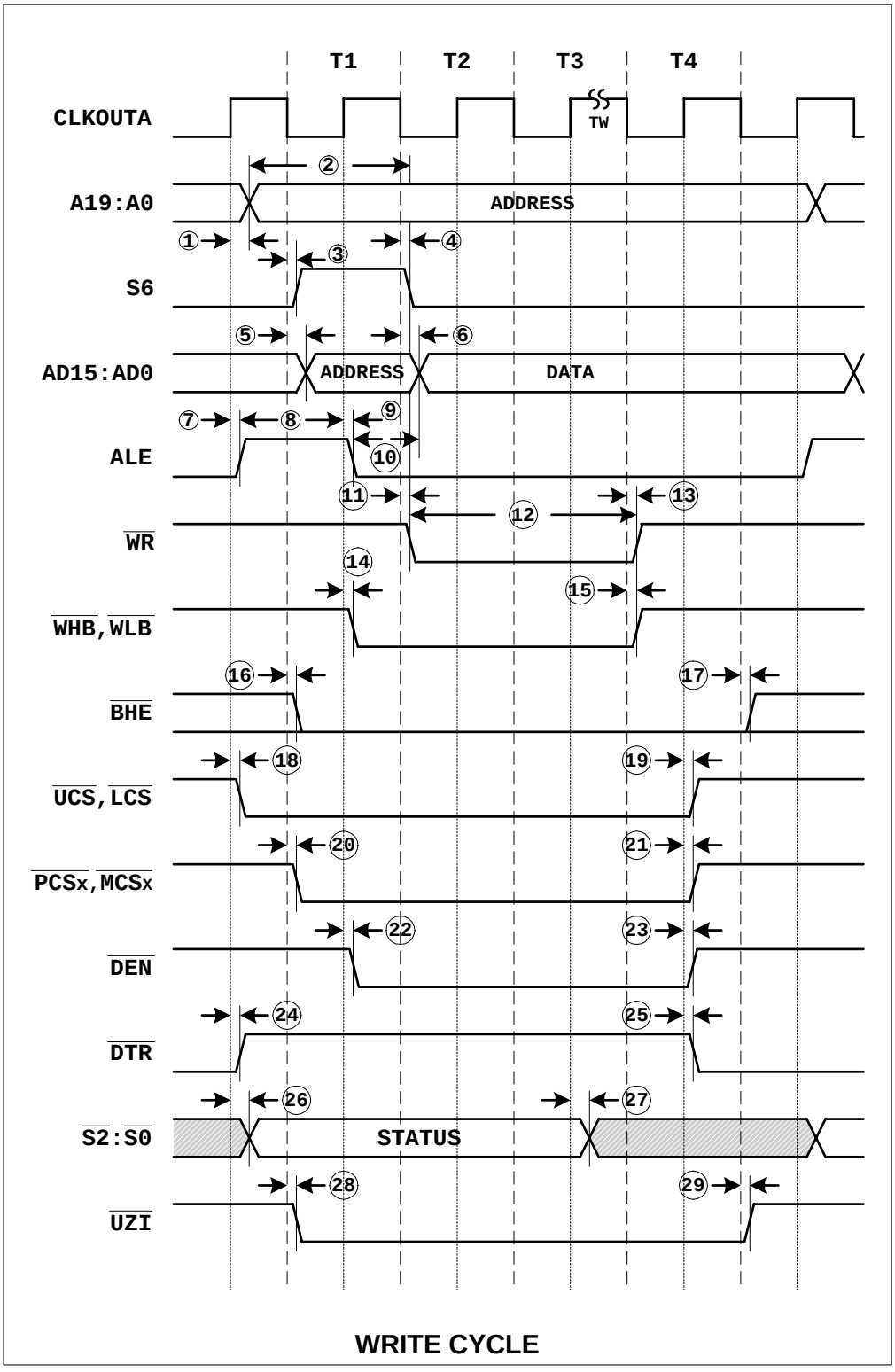
READ CYCLE

No.	Description	MIN	MAX	Unit
1	CLKOUTA high to A Address Valid	0	12	ns
2	A address valid to $\overline{RD}$ low	1.5T-9		ns
3	S6 active delay	0	15	ns
4	S6 inactive delay	0	15	ns
5	AD address Valid Delay	0	12	ns
6	Address Hold	0	12	ns
7	Data in setup	5		ns
8	Data in Hold	2		ns
9	ALE active delay	0	12	ns
10	ALE inactive delay	0	12	ns
11	Address Valid after ALE inactive	T/2-5		ns
12	ALE width	T-5		ns
13	$\overline{RD}$ active delay	0	12	ns
14	$\overline{RD}$ Pulse Width	2T-10		ns
15	$\overline{RD}$ inactive delay	0	12	ns
16	CLKOUTA HIGH to $\overline{LCS}$ / $\overline{UCS}$ valid	0	15	ns
17	UCS/LCS inactive delay	0	15	ns
18	$\overline{PCS}$ / $\overline{MCS}$ active delay	0	15	ns
19	$\overline{PCS}$ / $\overline{MCS}$ inactive delay	0	15	ns
20	$\overline{DEN}$ active delay	0	15	ns
21	$\overline{DEN}$ inactive delay	0	15	ns
22	DTR active delay	0	15	ns
23	DTR inactive delay	0	15	ns
24	Status active delay	0	15	ns
25	Status inactive delay	0	15	ns
26	$\overline{UZI}$ active delay	0	15	ns
27	$\overline{UZI}$ inactive delay	0	15	ns

1. T means a clock period time

2. All timing parameters are measured at 1.5V with 50 PF loading on CLKOUTA

. All output test conditions are with CL=50 pF


T1
T2
T3
T4
TW
CLKOUTA
A19:A0
ADDRESS
S6
AD15:AD0
ADDRESS
DATA
ALE
WR
WHB, WLB
BHE
UCS, LCS
PCSx, MCSx
DEN
DTR
S2:S0
STATUS
UZI
1
2
3
4
5
6
7
8
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11
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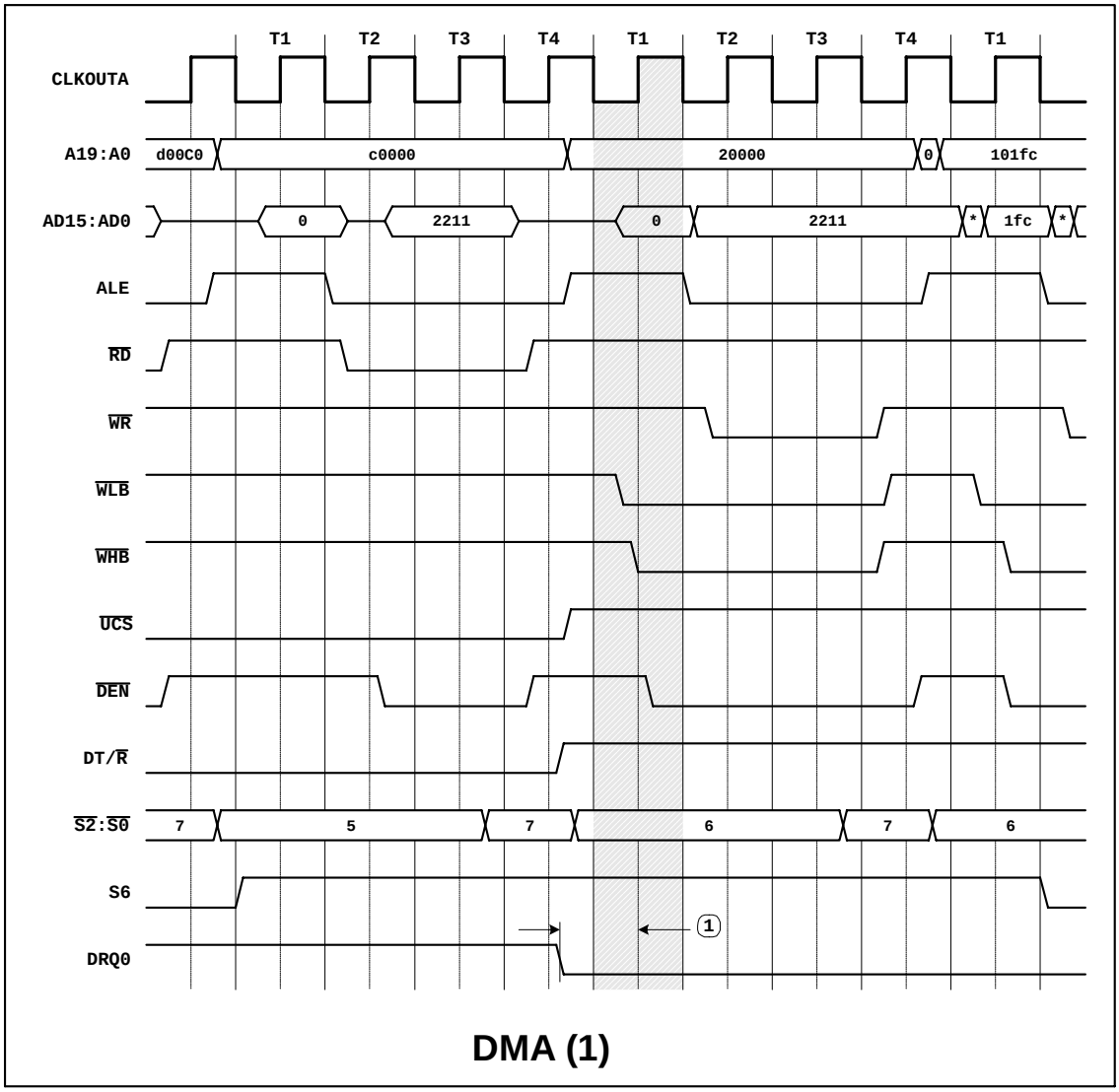
29

WRITE CYCLE

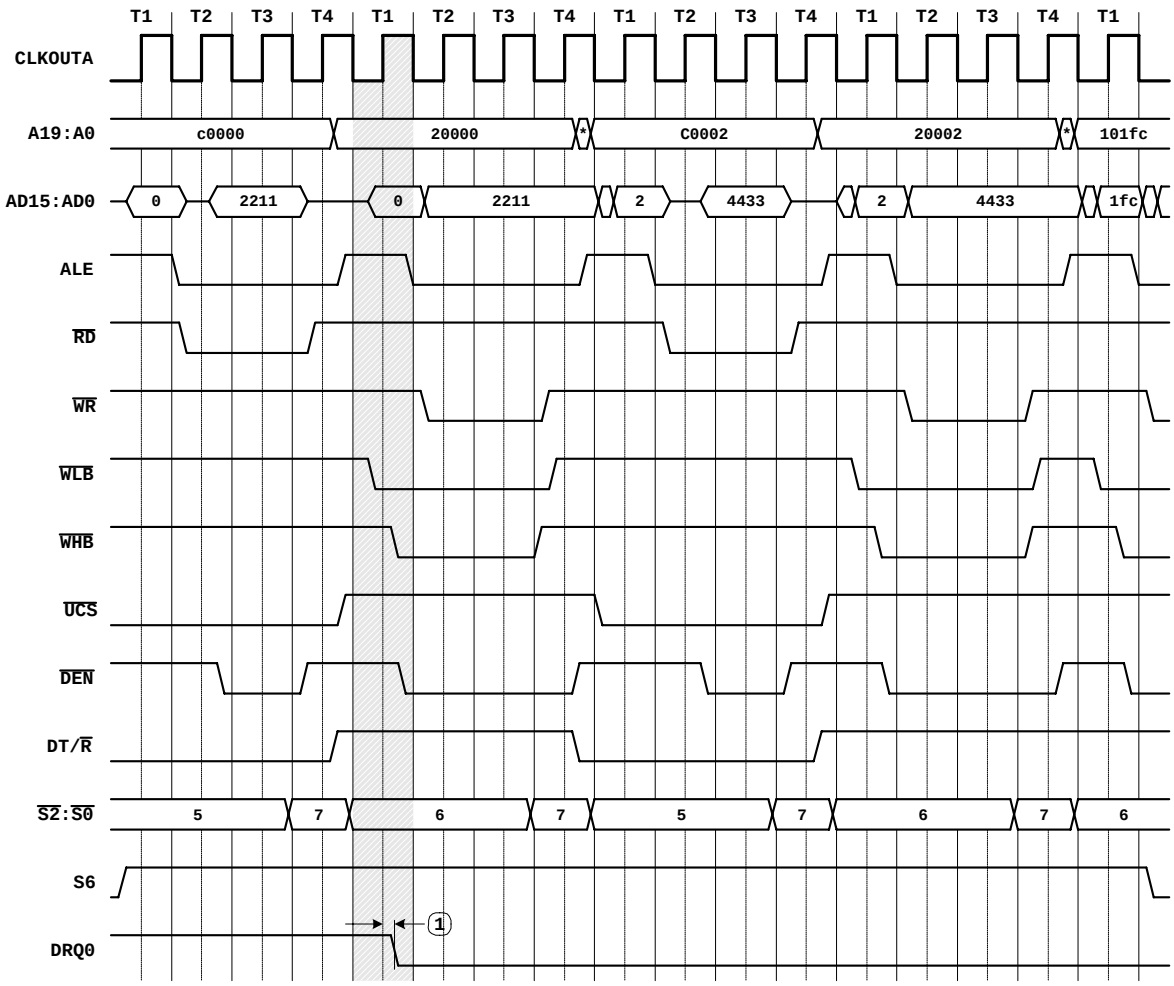
No.	Description	MIN	MAX	Unit
1	CLKOUTA high to A Address Valid	0	12	ns
2	A address valid to $\overline{WR}$ low	1.5T-9		ns
3	S6 active delay	0	15	ns
4	S6 inactive delay	0	15	ns
5	AD address Valid Delay	0	12	ns
6	Address Hold			ns
7	ALE active delay	0	12	ns
8	ALE width	T-10		ns
9	ALE inactive delay	0	12	ns
10	Address valid after ALE inactive	1/2T-5		ns
11	$\overline{WR}$ active delay	0	12	ns
12	$\overline{WR}$ pulse width	2T-10		ns
13	$\overline{WR}$ inactive delay	0	12	ns
14	$\overline{WHB}$ / $\overline{WLB}$ active delay	0	15	ns
15	$\overline{WHB}$ / $\overline{WLB}$ inactive delay	0	15	ns
16	BHE active delay	0	15	ns
17	BHE inactive delay	0	15	ns
18	CLKOUTA high to $\overline{UCS}$ / $\overline{LCS}$ valid	0	15	ns
19	$\overline{UCS}$ / $\overline{LCS}$ inactive delay	0	15	ns
20	$\overline{PCS}$ / $\overline{MCS}$ active delay	0	15	ns
21	$\overline{PCS}$ / $\overline{MCS}$ inactive delay	0	15	ns
22	$\overline{DEN}$ active delay	0	15	ns
23	$\overline{DEN}$ inactive delay	0	15	ns
24	$\overline{DTR}$ active delay	0	15	ns
25	$\overline{DTR}$ inactive delay	0	15	ns
26	Status active delay	0	15	ns
27	Status inactive delay	0	15	ns
28	$\overline{UZI}$ active delay	0	15	ns
29	$\overline{UZI}$ inactive delay	0	15	ns



DMA (1)

*** The source-synchronized transfer is not followed immediately by another DMA transfer**

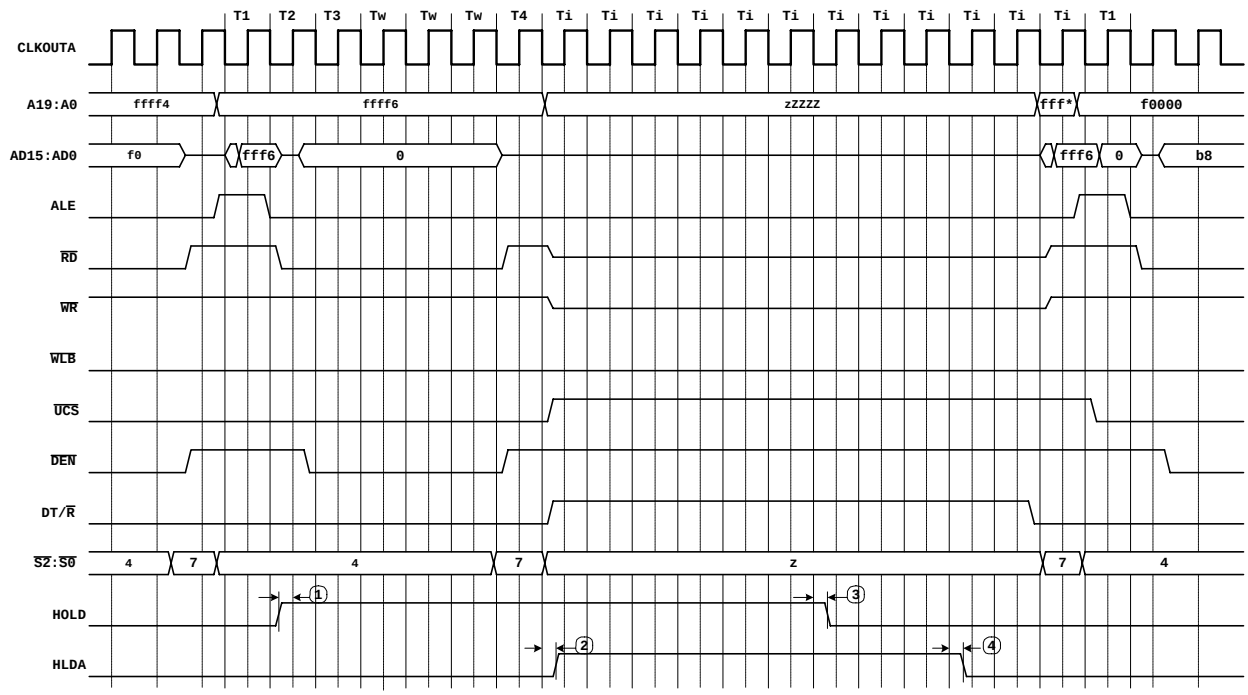
No.	Description	MIN	MAX	Unit
1	DRQ is confirmed time	5		ns



DMA (2)

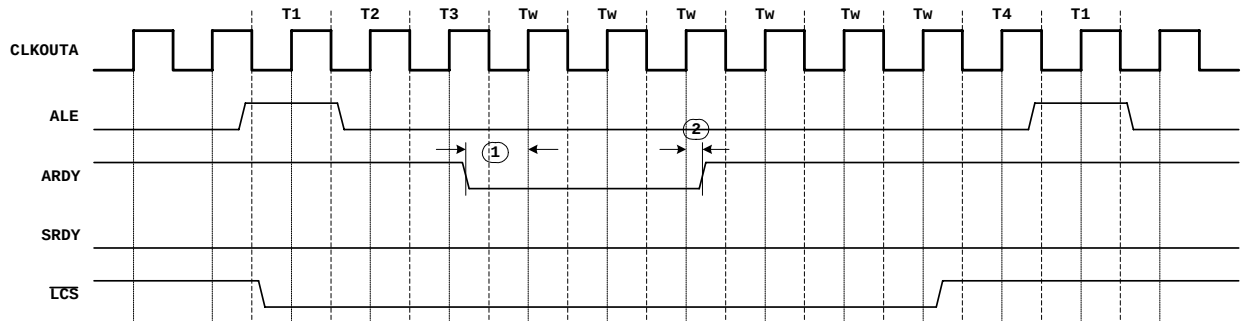
*** The source-synchronized transfer is followed immediately by another DMA transfer**

No.	Description	MIN	MAX	Unit
1	DRQ is confirmed time	2	0	ns



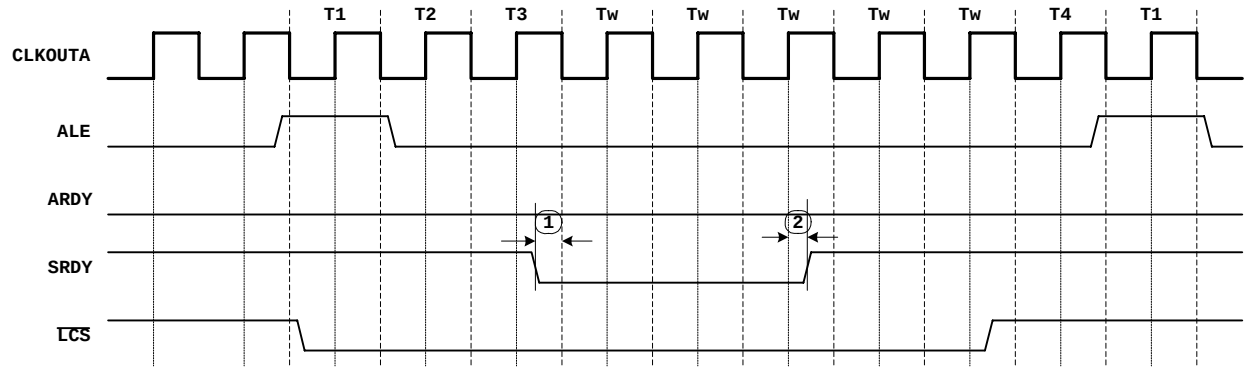
HOLD/HLDA Timing

No.	Description	MIN	MAX	Unit
1	HOLD setup time	5	0	ns
2	HLDA Valid Delay	0	15	ns
3	HOLD hold time	2	0	ns
4	HLDA Valid Delay	0	15	ns



ARDY Timing

No.	Description	MIN	MAX	Unit
1	ARDY Resolution Transition setup time	5	0	ns
2	ARDY active hold time	5	0	ns



SRDY Timing

No.	Description	MIN	MAX	Unit
1	SRDY transition setup time	5	0	ns
2	SRDY transition hold time	5	0	ns

25. Thermal Characteristics

θ_{JA}: thermal resistance from device junction to ambient temperature

P: operation power

T_A: maximum ambient temperature in operation mode

$T_A=T_J-(P\times\theta_{JA})$

Package/Board	Air Flow (m/s)	θ_{JA}
PQFP/2-Layer	0	48.8
	1	44.9
	2	42.7
	3	41.9
LQFP/2-Layer	0	53.6
	1	48.9
	2	45.5
	3	44.5
PQFP/4-Layer	0	38.9
	1	35.7
	2	33.8
	3	33.3
LQFP/4-Layer	0	42.6
	1	38.0
	2	36.1
	3	35.3

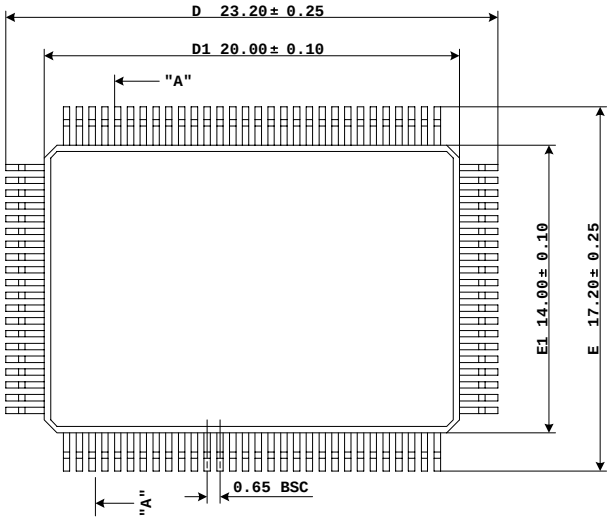
Unit: °C/Watt

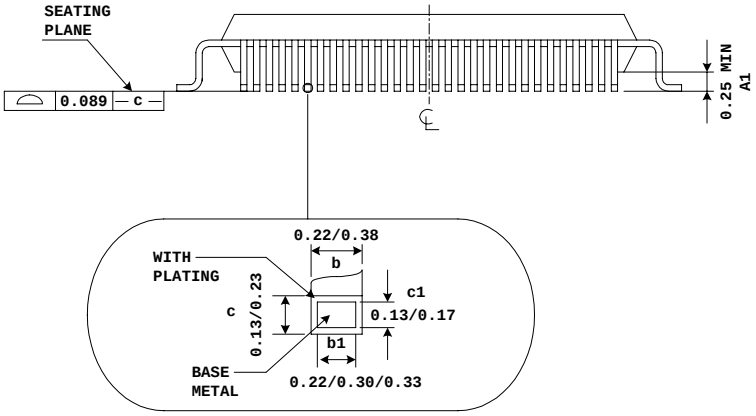
Recommended Storage Temperature: –65°C to +125°C

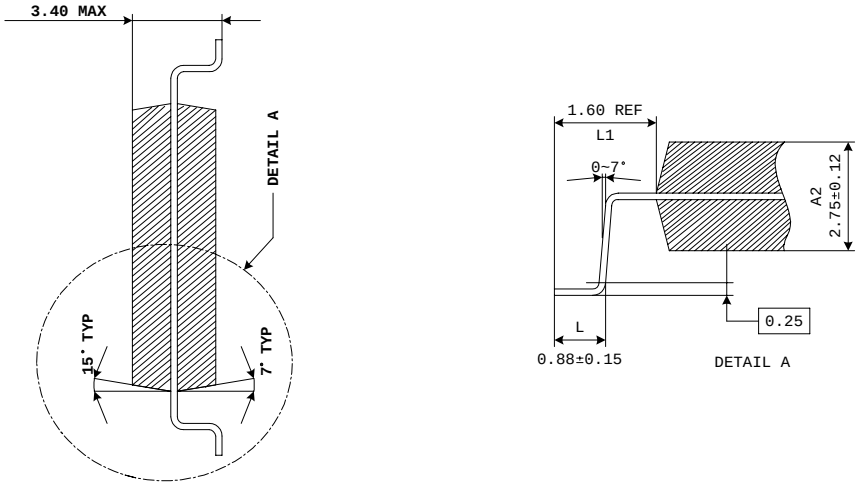
Note: *The IC should be mounted on PCB within 7 days after the dry pack is opened. If the IC is out of dry pack more than 7 days, it should be burned in oven (+125°C, > 12 hours) before mounted on PCB.*

26. Package Information

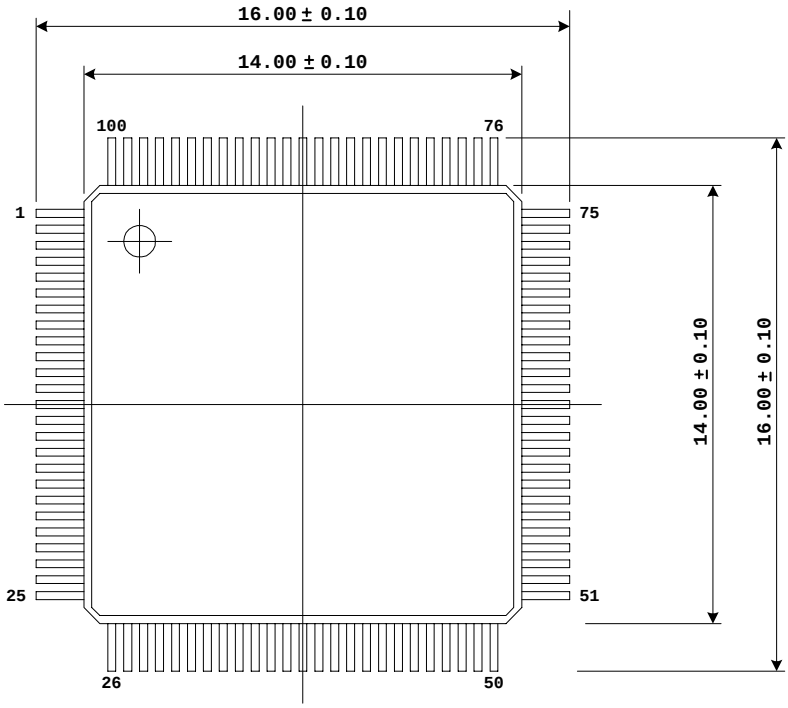
26.1 PQFP

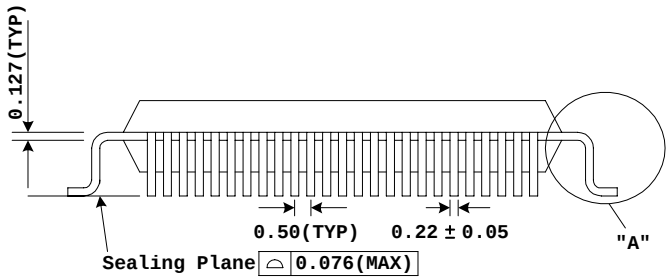


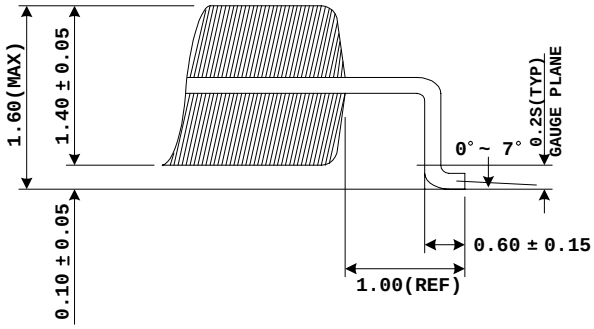




26.2 LQFP







UNIT:mm

27. Revision History

Rev.	Date	History
P01	2000/3/8	Preliminary release Version 0.1
F10	2000/7/31	Formal release Version 1.0
F11	2000/9/1	Adding the pin configuration & package information for LQFP package.
F12	2001/2/20	Add AC/DC.
F13	2001/3/13	Add PQFP and LQFP Pin-Out Table
F14	2001/8/7	Modify Wait state description(p26).
F15	2001/12/12	DC Characteristics
F16	2001/12/24	Modify Oscillator Characteristics
F17	2002/05/06	Modify Wait State Description
F18	2004/01/05	1. Modify DC Characteristics. 2. Add Chapters of Power Save & Power Down and Thermal Characteristics.
F19		