OPERATIONS MANUAL
SAT-V41

REVISION HISTORY

P/N 403-242-000

ECO Number	Date Code	Rev Level
Originated	960426	C
98-120	981209	C1

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1 GENERAL INFORMATION

1.1 FEATURES

- 8-Mhz V40 Processor, 8088 compatible with integral peripherals
  - DMA controller
  - 8259 Compatible Interrupt controller
  - Serial Communications Unit (SCU)
  - 8254 Compatible Counter/Timer
  - Refresh/Wait State Controller
- 2 Meg on board memory addressable through 4 JEDEC 32-pin sockets
- Two 8250 Compatible Serial channels, fully PC COM1, COM2 compatible.
- 1 PC Style Parallel Printer Port as LPT1
- Optional 12-Bit A/D converter
- 24 Lines of Parallel I/O using on-board 71055
- On-Board Dallas Semiconductor DS1202 Clock/Calendar/RAM
- Watchdog Timer with Software Enable/Disable capability
- Software Controlled Activity/Status LED
- Precision Power-Fail/Brown-out supervisory circuit
- Operating Temperature Range of -40°C to +85°C
- PC/104 Expansion Bus
- +5 Volt only operation

1.2 General Description

The SAT-V41 is a compact medium-performance industrial control and monitoring engine with a highly diverse set of integrated I/O peripherals. The 8088 code compatible V40 processor offers an enhanced instruction set, coupled with an improved instruction pipeline resulting in a performance increase over the 8088. The DMA controller, Timer/Counter Unit, Serial Communications Unit, Refresh Controller, 8259 Compatible interrupt controller, and wait state controller are all integrated into the V40 CPU. A memory paging scheme allows for up to 2 megabytes of SRAM, PSRAM, EPROM, and PEROM to be accessed by the processor through the 4 on-board 32-pin JEDEC standard memory sockets. An optional on-board battery allows for protection of SRAM as well as power-down time keeping for the Dallas Semiconductor DS1202 Clock/Calendar Chip. This chip also provides 24 bytes of battery backed configuration RAM. The addition of the Startech 16C452 provides two 8250 Compatible serial ports and a parallel printer port. These 2 serial ports are mapped at PC standard COM1 and COM2 addresses and can use generic PC communications I/O routines. These serial ports may be optionally configured for RS-422 or RS-485. The Parallel printer port is also fully PC compatible. To provide control capability an 71055 PPI (Intel 8255 equivalent) chip allows for 24

lines of multi-mode digital I/O, including OPTO-22 interface compatibility. An additional on-board option is for 8 channels of Analog input with 12-bit resolution. The SAT-V41 packs all of the most requested functions onto a single 4.5" x 7.0", 5 Volt only board which is function expandable through low-cost PC/104 modules from WinSystems and a variety of international suppliers.

1.3 SAT-V41 SPECIFICATIONS

1.3.1 Electrical

Bus Interface : PC/104 8-Bit compatible

System Clock : 8 MHz.

Interrupts : TTL Level

VCC : +5 Volts +/-5% at 200mA with no memory devices installed.

VCC1 : +12V +/-5% for PC/104 module use only

VCC2 : -12V +/-5% for PC/104 module use only

1.3.2 Memory

Addressing : 1 Megabyte directly addressable. 4 Megabyte capability provided through an 8-bit page register.

Memory Sockets : Four 32-pin JEDEC compatible sockets. 1 ROM only. 1 RAM only, 2 for RAM, ROM, EPROM, or PEROM.

1.3.3 Mechanical

Dimensions : 4.5 X 7.0 X 0.6 inches

PC Board : FR-4 epoxy glass with 2 signal layers and 2 power planes with screened component legend and plated through holes.

Jumpers : 0.025" square posts on 0.10" centers

Connectors :

Serial Port Connectors (3) : 10 Pin RN type IDH-10-LP
Printer Port : 26 Pin RN type IDH-26-LP
Parallel I/O : 50 Pin RN type IDH-50-LP
Analog Input : 26 Pin RN type IDH-26-LP
PC/104 BUS : SAMTECH type ESQ-132-12-G-D
Power Input : Molex 22-11-2082

1.3.4 Environmental

Operating Temperature :	-40° C to +85° C
Non-condensing Humidity :	5 to 95%

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2 SAT-V41 TECHNICAL REFERENCE

2.1 Introduction

This section of the manual is intended to provide sufficient information for the configuration and usage of the SAT-V41 board. WinSystems maintains a technical support group to help answer questions regarding configuration, usage, or programming of the board. For answers to questions not adequately addressed in this manual contact Technical Support at (817) 274-7553 between 8AM and 5PM Central Time, Monday through Friday. The SAT-V41 board utilizes a number of complex VLSI devices in its design. The manufacturer's data sheets for these devices are reprinted in the Appendices. Refer to these documents for programming information.

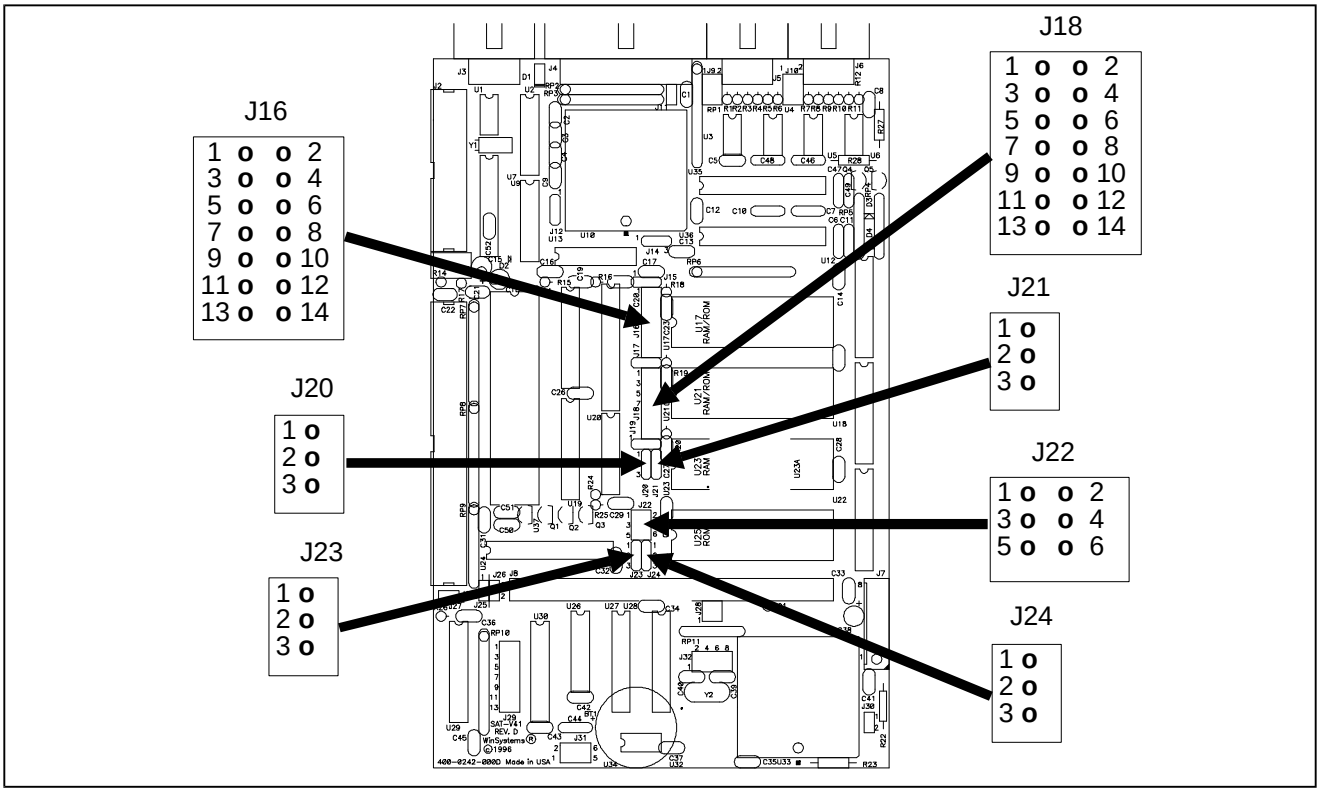
2.2 V40 CPU

The V40 processor is a high-performance, low-power processor which incorporates a number of commonly used peripheral devices directly into the processor. The peripherals include

- 4 Channel 8-bit DMA controller
- Serial Communications Unit
- 8259 Compatible Interrupt Controller
- 8254 Compatible Timer/Counter
- DRAM Refresh control circuitry
- Programmable wait-state generator

The V40 CPU is fully object code compatible with the INTEL 8088 and provides hardware and instruction set enhancements for improved performance over the 8088. The SAT-V41 is easily programmed using MS-DOS based assemblers, compilers and development tools. Contact your WinSystems Application Engineer for details on available debugging and operating system options. Refer to the V40 Data Sheet reprint in the Appendix for complete information regarding the usage and programming of the V40's peripherals and features.

2.3 Memory Addressing



The V40 processor on the SAT-V41, like its INTEL counterparts, directly addresses 1 megabyte of memory using 20 address lines. The SAT-V40 adds an 8-bit paging register to allow accessing of up to 4 megabytes through 16K byte pages. The address bus to the memory array actually consists of 22 bits. The mapping of the individual JEDEC sockets is controlled by a PLD device at U24 and by three jumper positions on J22. The standard memory maps are shown in the following table. Note that accessing of any device at or above address 100000H must be done through the 16K page window.

2.4 Memory Map Selection

Memory Map No.	J22 Jumpering	U25	U23	U21	U17
0	1-2 3-4 5-6	128K ROM at 0E0000H	32K RAM at 000000H	32K ROM/RAM at 008000H	32K ROM/RAM at 010000H
1	3-4 5-6	256K ROM at 0C0000H	128K RAM at 000000H	128K ROM/RAM at 020000H	128K ROM/RAM at 040000H
2	1-2 5-6	512K ROM at 080000H	512K RAM at 000000H	512K ROM/RAM at 100000H	512K ROM/RAM at 180000H
3	5-6	64K ROM at 0F0000H	128K RAM at 000000H	512K ROM/RAM at 100000H	512K ROM/RAM at 180000H
4	1-2 3-4	64K ROM at 0F0000H	512K RAM at 000000H	512K ROM/RAM at 100000H	512K ROM/RAM at 180000H
5	3-4	64K ROM at 0F0000H 512K ROM at 100000H	512K RAM at 000000H	512K ROM/RAM at 200000H	512K ROM/RAM at 280000H
6	1-2	64K ROM at 0F0000H 512K ROM at 180000H	512K RAM at 000000H	128K RAM at 080000H 512K RAM at 280000H	512K ROM/RAM at 100000H
7	None	64K ROM at 0F0000H 512K ROM at 180000H	512K RAM at 000000H	512K ROM/RAM at 100000H	512K ROM/RAM at 200000H

2.5 Memory Device Configuration

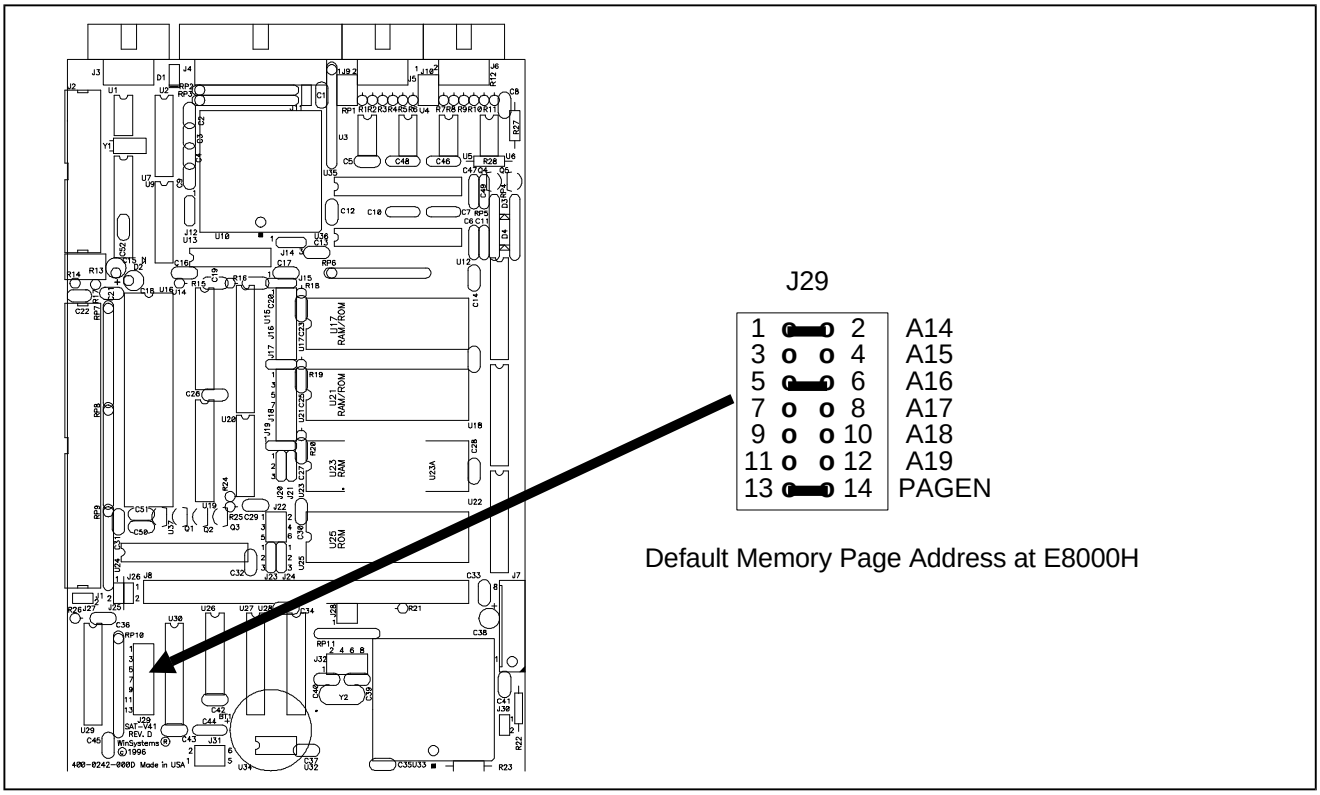
The 4 memory sockets U25, U23, U21 and U17 can be populated with standard PSRAM, SRAM, EPROM, and PEROM devices. Each socket must be configured for the actual type of device installed regardless of the memory map space allocated. A table of device types and jumpering for each socket is provided on the following page.

Device Type	U25 ROM ONLY J23	U25 ROM ONLY J24	U23 RAM ONLY J20	U23 RAM ONLY J21	U21 RAM/ROM J18	U17 RAM/ROM J16
32K ROM	OPEN	1-2			1-2 11-12	1-2 11-12
64K ROM	2-3	1-2			1-2 4-6 11-12	1-2 4-6 11-12
128K ROM	2-3	OPEN			1-2 4-6 9-11	1-2 4-6 9-11
256K ROM	2-3	2-3			1-2 4-6 9-11 12-14	1-2 4-6 9-11 12-14
512K ROM	2-3	2-3			1-2 4-6 5-7 9-11 12-14	1-2 4-6 5-7 9-11 12-14
32K PEROM					1-3 2-4 11-12	1-3 2-4 11-12
128K PEROM					1-2 4-6 3-5	1-2 4-6 3-5
256K PEROM					1-2 4-6 3-5 8-9 12-14	1-2 4-6 3-5 8-9 12-14
512K PEROM					1-2 4-6 3-5 7-9 12-14	1-2 4-6 3-5 7-9 12-14
32K SRAM			1-2	OPEN	1-3 2-4 11-12	1-3 2-4 11-12
128K SRAM			1-2	OPEN	1-3 2-4 5-6 11-12	1-3 2-4 5-6 11-12
256K SRAM			2-3	OPEN	1-3 2-4 5-6 12-14	1-3 2-4 5-6 12-14
512K SRAM			2-3	2-3	1-3 2-4 5-6 7-9 12-14	1-3 2-4 5-6 7-9 12-14
128K PSRAM			1-2	1-2	1-3 2-4 5-6 9-10 11-12	1-3 2-4 5-6 9-10 11-12
512K PSRAM			2-3	2-3	1-3 2-4 5-6 7-9 12-14	1-3 2-4 5-6 7-9 12-14

NOTE : A jumper must be installed at J30 anytime a PSRAM is used in any of the sockets in order to enable REFRESH from the V40.

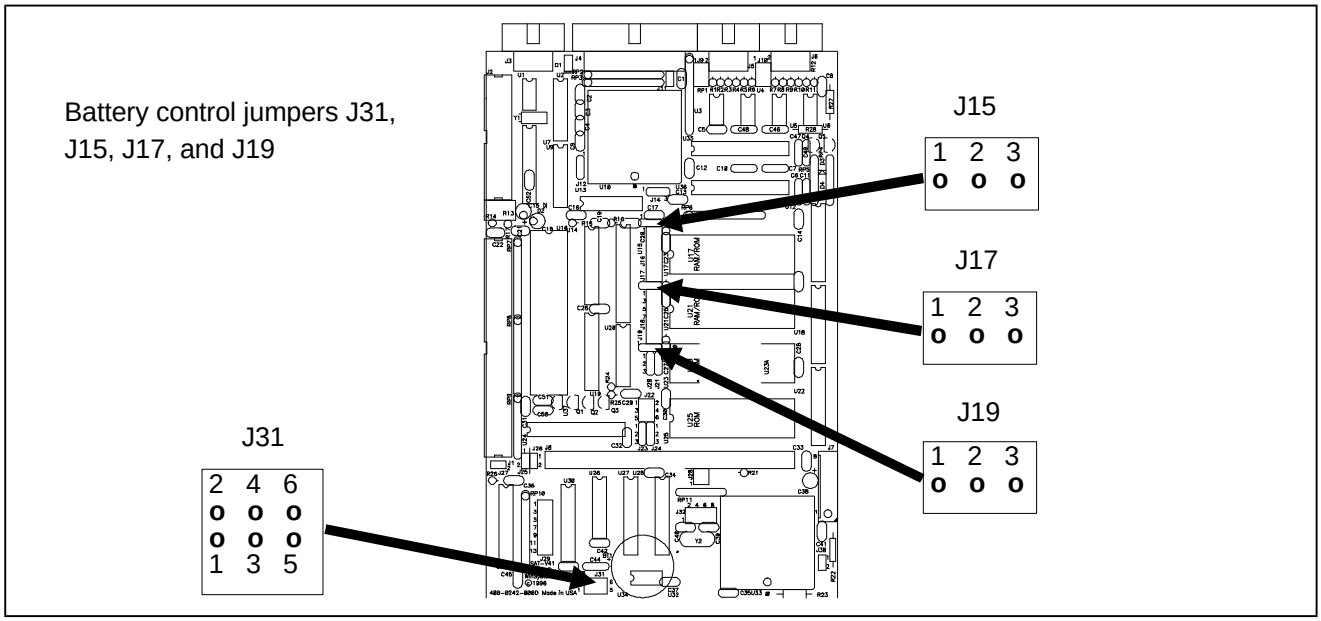
2.6 Memory Paging Configuration

The 16K window through which the 4 megabyte address space can be accessed is jumper addressable via jumper block J29. This jumper block sets the base address for the window. The normal setting for use with ROM-DOS and WinSystems RAM/ROM Disk drivers is at address E8000H as shown here.



The memory page register is mapped at I/O port 1D0H and is write only. When a CPU memory access occurs that matches Address lines A19 through A14 as jumpered via J29, a translated address is generated by using the 8 bits from the page register to form Addresses A21 through A14 combining with the addresses A13 through A0 from the CPU. Access outside the 16K window are made using the CPU addresses A19 through A0 with addresses A20 through A21 always 0. The memory paging option is enabled by placing a jumper on J29 pins 13-14.

2.7 Battery Select Options



An optional on-board battery at BT1 provides for power-off backup of the selected RAM socket(s), and backup power for the DS-1202 Clock/Calendar/RAM. A master battery enable is provided via J31 pins 3-4. When jumpered, the battery power is provided to the supervisory circuit and is available to each of the SRAM battery select jumpers. The DS-1202 clock has a separate enable jumper on pins 1-2 of J31. RAM sockets U17, U21, and U23 each have a battery backup select jumper as J15, J17, and J19 respectively. If the jumper block pins 1-2 are connected, the installed device will receive battery power when the main power is removed. When pins 2-3 are jumpered, +5 volts from the power supply is provided to the sockets.

2.8 Serial Communications

The SAT-V41 provides three serial channels, the V40 SCU and two 8250 compatible ports at PC compatible addresses of 3F8h and 2F8h terminated at J5 and J6 respectively.

The V40 Serial Communication Unit (SCU) is terminated at J3. The pinout of J3 is shown below. This serial port supports RS232 only and provides only CTS/RTS handshake support through auxiliary registers. Refer to APPENDIX D for programming details on the V40 SCU.

J3

N/C	1 o o 6	N/C
RX DATA	2 o o 7	RTS
TXDATA	3 o o 8	CTS
N/C	4 o o 9	N/C
GND	5 o o 10	N/C

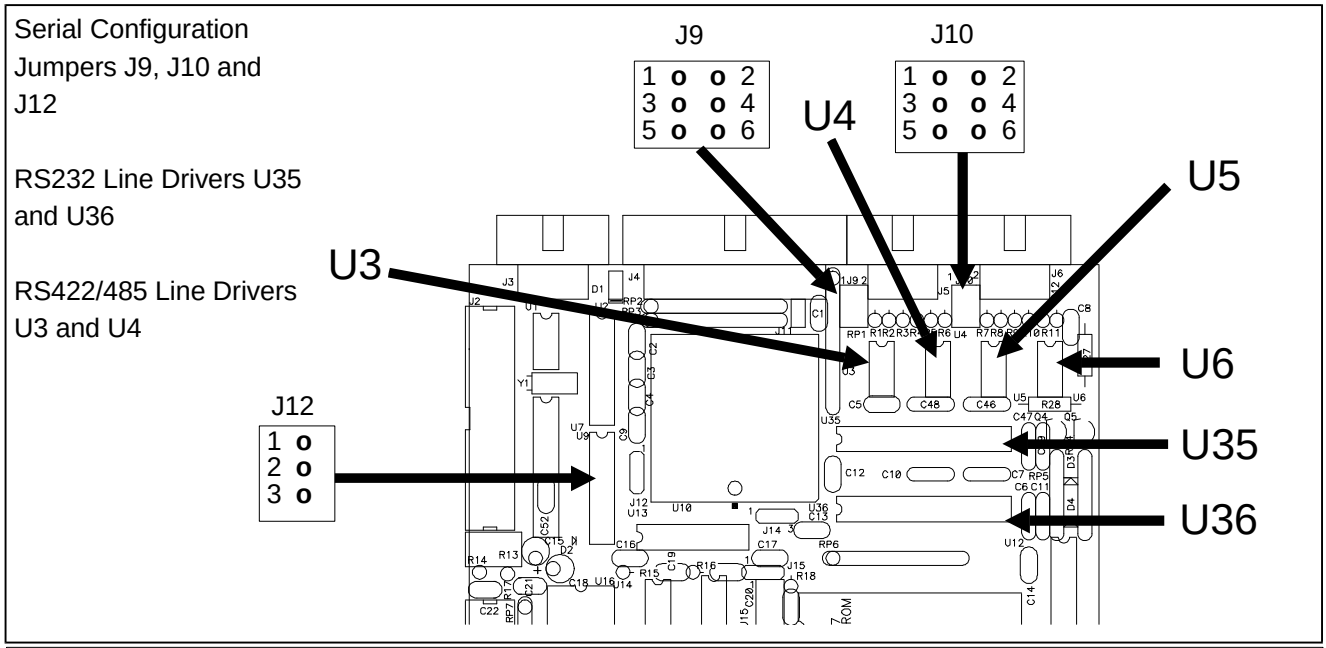
RTS SOURCE SELECT

RTS from V40 INTAK PIN

RTS from MISC I/O Bit 6

The 8250 compatible serial ports are mapped to PC compatible addresses of 3F8H for COM1 and 2F8H for COM2. Each of these ports may be individually configured for RS232, RS422, or RS485.

Optional chip kits part number CK-75176-2 are required in order to allow configuration of RS422 or RS485. One chip kit will allow one channel of RS422 or two channels of RS485. When configuring a channel for RS422 or RS485 it will be necessary to remove the RS232 line driver(s) at U35 and/or U36 as appropriate. Each of the configurations is documented below.



Configuration COM1	COM2	J9 Jumpers	J10 Jumpers	U35 Installed	U36 Installed	U3 Installed	U4 Installed	U5 Installed	U6 Installed
RS232	RS232	OPEN	OPEN	YES	YES	NO	NO	NO	NO
RS232	RS422	OPEN	1-2 5-6	YES	NO	NO	NO	YES	YES
RS232	RS485	OPEN	3-4 5-6	YES	NO	NO	NO	YES	NO
RS422	RS232	1-2 5-6	OPEN	NO	YES	YES	YES	NO	NO
RS422	RS422	1-2 5-6	1-2 5-6	NO	NO	YES	YES	YES	YES
RS422	RS485	1-2 5-6	3-4 5-6	NO	NO	YES	YES	YES	NO
RS485	RS232	3-4 5-6	OPEN	NO	YES	YES	NO	NO	NO
RS485	RS422	3-4 5-6	1-2 5-6	NO	NO	YES	NO	YES	YES
RS485	RS485	3-4 5-6	3-4 5-6	NO	NO	YES	NO	YES	NO

J5/J6

CD	1 o o 6	DSR
RXDATA	2 o o 7	RTS
TXDATA	3 o o 8	CTS
DTR	4 o o 9	RI
GND	5 o o 10	N/C

RS232 PIN DEFINITIONS

J5/J6

N/C	1 o o 6	RX+
TX+	2 o o 7	RX-
TX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	N/C

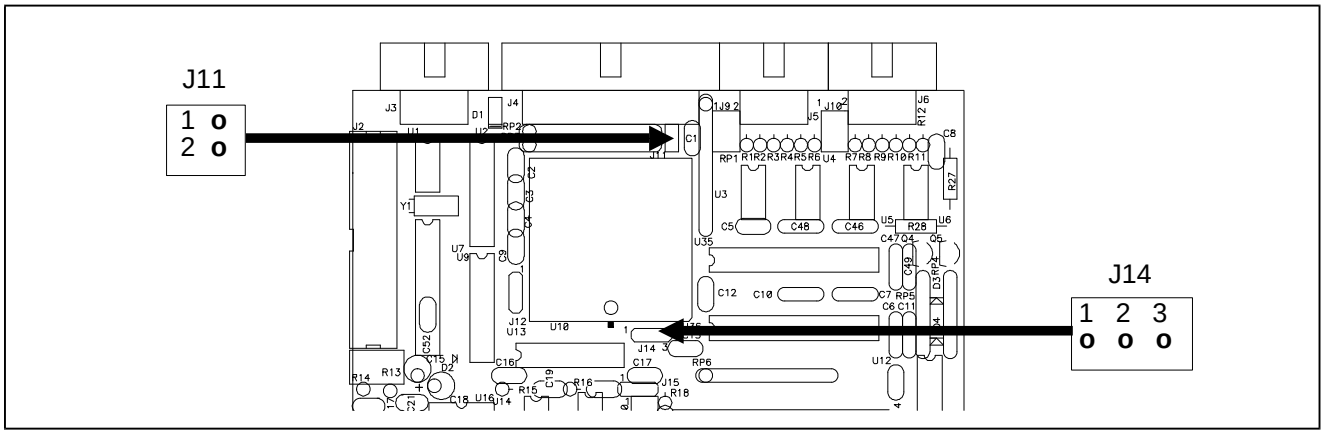
RS422 PIN DEFINITIONS

J5/J6

N/C	1 o o 6	N/C
TX/RX+	2 o o 7	N/C
TX/RX-	3 o o 8	N/C
N/C	4 o o 9	N/C
GND	5 o o 10	N/C

RS485 PIN DEFINITIONS

2.9 Parallel Printer port



The SAT-V41 contains a PC compatible Centronics Parallel printer port terminated at J4. When used with cable CBL-122-1, standard PC printer cables can be connected to the SAT-V41. The pin definitions for J4 are shown below.

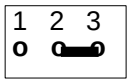
J4

/STB	1 o o 14	/AFD
PD0	2 o o 15	/ERROR
PD1	3 o o 16	/INIT
PD2	4 o o 17	/SLIN
PD3	5 o o 18	GND
PD4	6 o o 19	GND
PD5	7 o o 20	GND
PD6	8 o o 21	GND
PD7	9 o o 22	GND
/ACK	10 o o 23	GND
BUSY	11 o o 24	GND
PE	12 o o 25	GND
SLCT	13 o o 26	+5V / NC

2.9.1 Bi-directional Data control

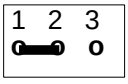
The 16C452 Serial/Parallel controller allows for a bi-directional printer port data bus. J14 allows selection of the method of control for the data port direction.

J14



Output Only

J14

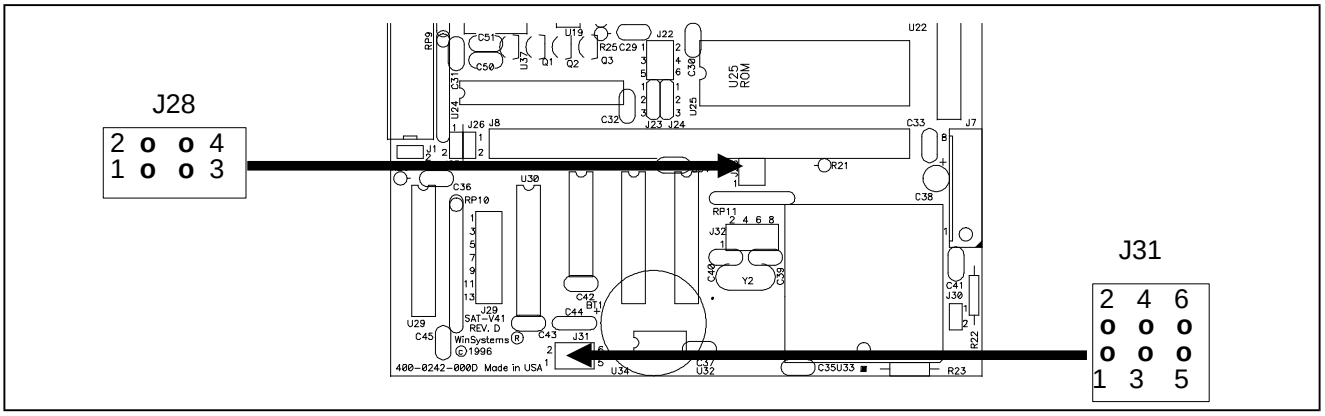


Software Direction Control

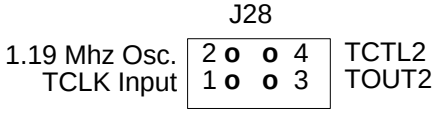
When selected for software direction control, bit 3 of the miscellaneous control register at I/O address 1D4H allows for dynamic direction control. When the bit is 0, the data port is configured for output, when set to 1, it is configured for input.

When the printer port is used as a general purpose I/O port, it may be desirable to provide power via the parallel printer I/O connector. Pin 26 of J4 can be used for this power feed by jumpering J11. Current consumption through this feed is not fused or otherwise limited on the board and it is the user's responsibility to assure adequate current limiting so as to avoid damage to the SAT-V41 board.

2.10 Counter/Timer I/O



The V40 processor contains internally the equivalent of an 8254 type counter/ timer module with three separate channels. Each channel's source can be individually programmed as internal or external. External sources can be fed into J28 pin 1. A 1.19Mhz oscillator is provided on SAT-V41 boards running DOS to allow for software timing compatibility with PC hardware. Channel 0 of the counter is typically used as a periodic interrupt which is available at IRQ0 of the internal interrupt controller. Channel 1 is used as the baud rate generator for the V40 Serial Control Unit. Channel 2 is used for sound in standard PC architectures but is left available to the user on the SAT-V41. The available Output and control (gate) pins are terminated on J28. The pinout of J28 is shown below.



2.11 Watchdog Timer

The SAT-V41 utilizes the MAXIM 690 supervisory circuit which provides power on reset timing, power brown-out protection, battery back-up switching, and watchdog timer functions. The watchdog timer once enabled must be strobed at least once every 1.5 seconds or a reset will be asserted to the processor. This strobing or petting occurs by issuing an I/O write instruction to I/O port 1C8H. The data value written is irrelevant. In order to activate the watchdog timer, two steps are necessary. First the jumper at J31

5-6 must be installed, and second, a write of 1 to I/O port 1C0H will start the timer. To disable the watchdog, write a 0 to I/O port 1C0H.

2.12 DS-1202 Clock/Calendar/RAM

The SAT-V41 utilizes the Dallas Semiconductor DS-1202 Clock/Calendar/RAM IC for time and date keeping. Up to 24 bytes of configuration information may be stored in RAM within the clock chip. The DS-1202 is accessed in a serial fashion using bits in the miscellaneous I/O register at 1D4H. The complete bit definitions for this port I/O port are shown below.

Bit	Write	Read
D7	N/C	CTS
D6	RTS	RTS
D5	LED	LED
D4	CKDIR	CKDIR
D3	LPTOE	LPTOE
D2	SELCT	SELCT
D1	SHCLK	SHCLK
D0	I/O	I/O

D7 - Write no operation, Read for V40 SCU serial RTS input

D6 - Write/read for RTS on V40 SCU serial channel

D5 - Write/read 1= LED ON, 0 = LED OFF

D4 - Write/Read ,Clock Write = 0, Clock Read or Analog I/O = 1

D3 - Write/Read ,LPT Data output = 0, LPT Data input = 1

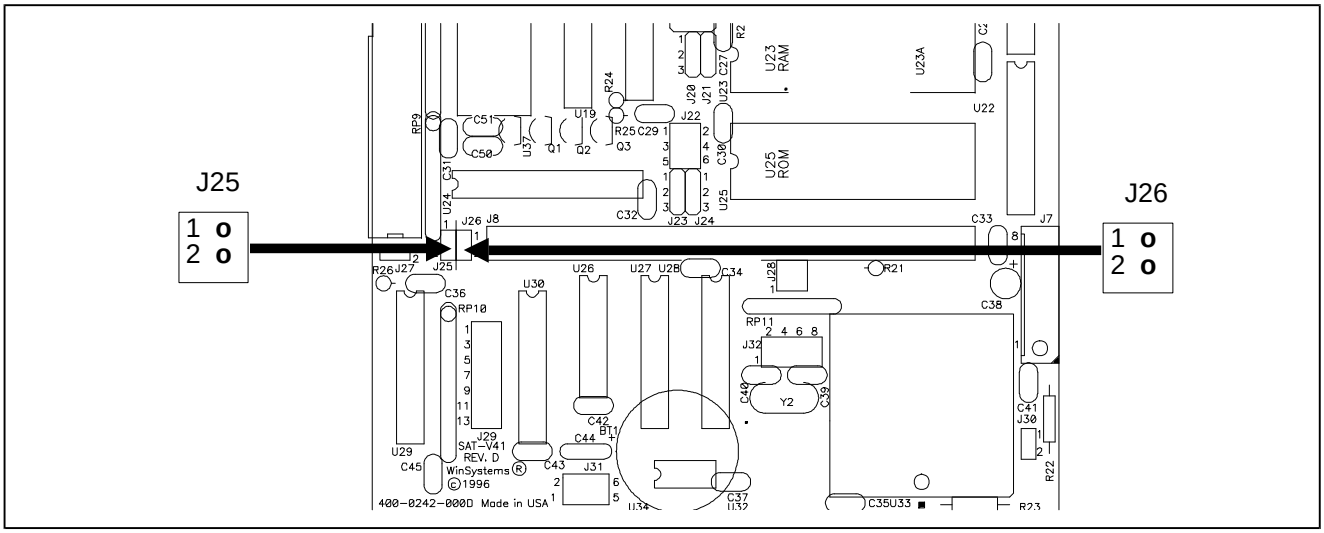
D2 - Write/Read, Device Select Clock = 1, Analog = 0

D1 - Write/Read ,Serial peripheral Shift Clock

D0 - Write/Read, Serial Peripheral Data

Refer to the Reprint of the DS-1202 Datasheet in Appendix G for complete details regarding programming and register/RAM implementation. The supplied “sample programs” diskette has sample clock/calendar, RAM, and A/D converter access routines written in 'C' that can be incorporated into the user's application program.

2.13 Interrupt routing



External interrupts to the V40 are provided via the PC/104 Expansion bus. (See PC/104 pinout in later section) All interrupts are rising edge active and unterminated on the bus. Two jumper blocks are provided to allow enabling and disabling of enhanced interrupt options. Jumpering J26 allows the PC/104 0WS (pin B8) line to be used as an input for IRQ1. This allows PC configured systems to use the standard interrupt for keyboard input which is normally not available on the PC/104 bus. This option would typically be jumpered only when used with the PCM-DSKIO, disk, keyboard, accessory module. The PC/104 bus defines pin A1 as a non-maskable interrupt (NMI). This input may be defeated by removing the jumper from J25.

2.14 Status LED

The SAT-V41 provides a status/diagnostic LED port which can be used by application software to signal activity, error or other user-defined functions. To illuminate the LED it is only necessary to set bit 5 of I/O port 1D4. Extinguishing of the LED is accomplished by clearing bit 5. The miscellaneous I/O port is read/write so the proper procedure to avoid changing outputs on other bits, is to read in the current value, set or clear bit 5 as desired and rewrite the value.

2.15 Analog Input

The SAT-V41 utilizes the MAX186 8-Channel Analog to Digital converter providing 12-bit resolution for a 0 to 4.096V input signal. An internal 1.7 Mhz conversion clock allows for a minimum 5.5 uS conversion time. The actual conversion throughput is highly dependent upon coding and has been demonstrated at between 2Khz and 500hz using assembly and C respectively. Each channel can be software configured for Unipolar and

Single-Ended/Differential operation. Refer to Appendix H for the MAXIM186 datasheet reprint for additional usage and programming details. The A/D converter is accessed serially through the Miscellaneous I/O register. The diagram below shows the analog input connector J2.

J2

CH0	1	14		CH1
CH1	2	15		CH3
GND	3	16		GND
CH2	4	17		CH5
GND	5	18		GND
CH3	6	19		CH7
GND	7	20		GND
CH4	8	21		N/C
GND	9	22		GND
CH5	10	23		N/C
GND	11	24		GND
CH6	12	25		N/C
CH7	13	26		N/C

2.16 Parallel I/O

The SAT-V41 uses the NEC 71055 PIO chip (Intel 8255 compatible) to provide for 24 lines of digital I/O. Several modes are supported as documented in the 71055 datasheet reprint in Appendix F. The Base address of the chip is at 50H. The digital I/O is terminated at J1. The pinout of J1 is shown below :

J1

Port C bit 7	1	2		GND
Port C bit 6	3	4		GND
Port C bit 5	5	6		GND
Port C bit 4	7	8		GND
Port C bit 3	9	10		GND
Port C bit 2	11	12		GND
Port C bit 1	13	14		GND
Port C bit 0	15	16		GND
Port B bit 7	17	18		GND
Port B bit 6	19	20		GND
Port B bit 5	21	22		GND
Port B bit 4	23	24		GND
Port B bit 3	25	26		GND
Port B bit 2	27	28		GND
Port B bit 1	29	30		GND
Port B bit 0	31	32		GND
Port A bit 7	33	34		GND
Port A bit 6	35	36		GND
Port A bit 5	37	38		GND
Port A bit 4	39	40		GND
Port A bit 3	41	42		GND
Port A bit 2	43	44		GND
Port A bit 1	45	46		GND
Port A bit 0	47	48		GND
+5V/NC	49	50		GND

Note that Pin 49 may be configured to supply +5 volts to the I/O connector. This is accomplished by placing a jumper on J27. The current drawn from this pin should be 300 mA or less.

2.17 PC/104 Expansion Bus

The SAT-V41 provides for expansion through a single PC/104 8-Bit expansion connector at J8. PC/104 expansion modules are available from a number of vendors and include disk, network, digital, and analog I/O cards. The pin definitions for the PC/104 connector are shown here :

J8

GND	B1	o o	A1	IOCHK
RESET	B2	o o	A2	BD7
+5V	B3	o o	A3	BD6
IRQ2	B4	o o	A4	BD5
-5V	B5	o o	A5	BD4
DRQ2	B6	o o	A6	BD3
-12V	B7	o o	A7	BD2
0WS	B8	o o	A8	BD1
+12V	B9	o o	A9	BD0
GND	B10	o o	A10	IOCHRDY
MEMW	B11	o o	A11	AEN
MEMR	B12	o o	A12	SA19
IOW	B13	o o	A13	SA18
IOR	B14	o o	A14	SA17
DACK3	B15	o o	A15	SA16
DRQ3	B16	o o	A16	SA15
DACK1	B17	o o	A17	SA14
DRQ1	B18	o o	A18	SA13
DACK0	B19	o o	A19	SA12
SYSCLK	B20	o o	A20	SA11
IRQ7	B21	o o	A21	SA10
IRQ6	B22	o o	A22	SA9
IRQ5	B23	o o	A23	SA8
IRQ4	B24	o o	A24	SA7
IRQ3	B25	o o	A25	SA6
DACK2	B26	o o	A26	SA5
TC	B27	o o	A27	SA4
BALE	B28	o o	A28	SA3
+5V	B29	o o	A29	SA2
OSC	B30	o o	A30	SA1
GND	B31	o o	A31	SA0
GND	B32	o o	A32	GND

2.18 Power Input

Power is supplied to the SAT-V41 through connector J7. A pre-wired harness cable CBL-174-1 is available to facilitate connection to the SAT-V41. The pin definitions for J7 are shown below.

J7

8	o	-12V
7	o	+12V
6	o	+5V
5	o	+5V
4	o	GND
3	o	GND
2	o	GND
1	o	/RESET

2.19 Connector/Jumper Summary

Connector/Jumper	Description	Page Reference
J1	Parallel I/O connector	2-12
J2	Analog Input Connector	2-12
J3	V40-SCU Connector	2-6
J4	LPT1 Connector	2-8
J5	COMM1 I/O	2-7
J6	COMM2 I/O	2-7
J7	Power Connector	2-13
J8	PC/104 Bus Connector	2-13
J9	COMM1 Serial Configuration	2-7
J10	COMM2 Serial Configuration	2-7
J11	LPT Port VCC Enable	2-8, 2-9
J12	RTS Source Select V40 SCU	2-6, 2-7
J13	COMM1/COMM2 RS232 Enable	2-7
J14	LPT1 Direction Control	2-8
J15	U17 VBAT/VCC Select	2-6
J16	U17 Device Configuration Jumper	2-2, 2-4
J17	U21 VBAT/VCC Select	2-6
J18	U21 Device Configuration Jumper	2-2, 2-4
J19	U23 VBAT/VCC Select	2-6
J20	U23 Device size Select	2-4
J21	U23 Device size Select	2-4
J22	Memory Map Select	2-2, 2-3
J23	U25 Device size Select	2-2, 2-4
J24	U25 Device size Select	2-2, 2-4
J25	NMI Enable	2-11
J26	IRQ1 to PC/104 Interrupt Routing	2-11
J27	Parallel I/O VCC enable	2-12
J28	Counter/Timer config jumper	2-9
J29	Memory page address select	2-5
J30	Refresh enable jumper	2-4
J31	VBAT/Watchdog timer control	2-6, 2-9

3 APPENDIX A

SAT-V41 I/O Port Map

I/O Address	Description
050-053H	71055 PIO Chip
1C0-1C3H	Watchdog Timer Enable
1D0-1D3H	Memory Page Register
1D4-1D7H	Misc. I/O Register
1C8-1CBH	Watchdog Pet
2F8-2FFh	COMM2
378-37FH	LPT1
3F8-3FF	COMM1
FFF0H	V40 TCKS Register
FFF1H	V40 Reserved
FFF2H	V40 RFC Register
FFF3h	V40 Reserved
FFF4H	V40 WMB Register
FFF5H	V40 WCY1 Register
FFF6H	V40 WCY2 Register
FFF7H	V40 Reserved
FFF8H	V40 SULA Register
FFF9H	V40 TULA Register
FFFAH	V40 IULA Register
FFFBH	V40 DULA Register
FFFCH	V40 OPHA Register
FFFDH	V40 OPSEL Register
FFFEH	V40 OPCN Register
FFFFH	V40 Reserved

NOTE : All internal V40 peripherals are software located within the I/O space based on the content of the OPHA register and the indivdual placement registers i.e. DULA, TULA, SULA, IULA. Refer to the V40 datasheet for additional details.

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4 APPENDIX B

SAT-V41 Parts List

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BEGINNING RANGE: SAT-V41PA-8-0 ENDING RANGE: SAT-V41PA-8-0

LEVEL	ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED
1	SAT-V41PA-8-0	V40 SBC, 8 MHZ WITH PC BIOS & 12	BIT A/D				1
2	999-9999-001	SPECIAL NOTES	03-28-96 MEB (NEW)	ARLIN		Inv	1
2	0242-101-0000	ASSY SAT-V41PA-8 MHZ REV.D W/ANA		ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	12-04-96 MEB ECO 96-95	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	03-28-96 MEB (NEW)	ARLIN		Inv	1
3	>110-0011-003	CAP .1uF 50v 20% CER RAD .1	C1-C5,C8,C9,C12-C14,C16,C17,C19,C20,	ARLIN		Inv	33
3	>999-9999-001	SPECIAL NOTES	C23-C37,C41-C43,C45	ARLIN		Inv	1
3	>110-0012-003	CAP 1uF 50v 20% CER RAD .2	C6,C7,C10,C11,C46-C49	ARLIN		Inv	8
3	>110-0014-005	CAP 10uF 25v 10% TAN RAD .1	C15	ARLIN		Inv	1
3	>110-0036-003	CAP .01uF 50v 20% CER .2 (4500)	C44	ARLIN		Inv	1
3	>110-0044-005	CAP 22uF 10v 10% TAN RAD .1	C38	ARLIN		Inv	1
3	>114-0102-450	RESISTOR 1K 1/4 5%	R18-R21,R23	ARLIN		Inv	5
3	>114-0103-450	RESISTOR 10K 1/4 5%, CR25 10k 5%	R16,R24-26	ARLIN		Inv	4
3	>114-0331-450	RESISTOR 330 OHM 1/4 5%	R22	ARLIN		Inv	1
3	>114-0471-450	RESISTOR 470 OHM 1/4 5%	R15	ARLIN		Inv	1
3	>114-0472-450	RESISTOR CF 4.7K 1/4W 5%	R27,R28	ARLIN		Inv	2
3	>115-0103-050	RN SIP 6P-5 RES 10K (BKMN)L061S1	RP4,RP5,RP11	ARLIN		Inv	3
3	>117-0103-050	RN SIP 10P-9 RES 10K L101S103 (B	RP1-RP3,RP6-RP8,RP10	ARLIN		Inv	7
3	>116-0103-050	RN SIP 8P-7 RES 10K (BI)L8-1S-10	RP9	ARLIN		Inv	1
3	>124-0016-000	LED RED RECTANGLE L-153HDT (KNGB	D1	ARLIN		Inv	1
3	>124-0004-000	DIODE 1N4148	D3,D4	ARLIN		Inv	2
3	>125-0003-000	TRANSISTOR VN2222LL (TO92)/ VN10	Q1-Q3	ARLIN		Inv	3
3	>125-0001-000	TRANSISTOR PN2222 (TO92)	Q4,Q5	ARLIN		Inv	2
3	>200-0064-000	SOCKET 64 POS QPHF2-64-020-1W (P	J8	ARLIN		Inv	1
3	>200-0083-100	SOCKET 8 PIN ICO-083-S8A-T (4488	U3-U6	ARLIN		Inv	4
3	>200-0163-100	SOCKET 16 PIN ICO-163-S8A-T (220	U2	ARLIN		Inv	1
3	>200-0243-100	SOCKET 24 P .3 ICO-243-S8A-T (14	U15,U24,U35,U36	ARLIN		Inv	4
3	>200-0326-100	SOCKET 32 P .6 ICO-326-S8A-T (72	U17,U21,U23,U25	ARLIN		Inv	4
3	>200-0406-100	SOCKET 40 P .6 ICO-406-S8A-T (60	U16	ARLIN		Inv	1
3	>201-0008-601	HDR 8 POS MOLEX 22-11-2082	J7	ARLIN		Inv	1
3	>201-0010-121	HDR 2X5 RA PRO IDH-10LP-SR3-TR/T	J3,J5,J6	ARLIN		Inv	3
3	>201-0026-121	HDR 26 P RA IDH-26LP-SR3-TG/TR (	J4	ARLIN		Inv	1
3	>201-0036-010	HDR 1X36 UN TSW-136-07-G-S (SAM)	J11,J25-J27,J30=1X2 J12,J14,J15,J17,	ARLIN		Inv	1.02
3	>999-9999-001	SPECIAL NOTES	J19-J21,J23,J24=1X3	ARLIN		Inv	1
3	>201-0050-021	HDR 2X25 ST PRO IDH50LP-S3-TG/TR	J1	ARLIN		Inv	1
3	>201-0072-120	HDR 2X36 UN TSW-136-07-G-D	J13,J28=2X2 J9,J10,J22,J31=2X3	ARLIN		Inv	1.027
3	>999-9999-001	SPECIAL NOTES	J16,J18,J29=2X7	ARLIN		Inv	1
3	>220-0056-000	XTAL R26-32.768KHz-6pF (RALTRON)	X1 USE FOAM TAPE UNDER XTAL	ARLIN		Inv	1
3	>220-0032-001	XTAL-14.31818 (ABRACON) ABL-14.3	Y2	ARLIN		Inv	1
3	>220-0000-000	HC49 INSULATOR XTAL	PLACE UNDER Y2	ARLIN		Inv	1
3	>230-0068-150	SOCKET PLCCE-068-S1-TT (16) (RN)	U10,U33	ARLIN		Inv	2
3	>730-0072-000	IC, DS1202	U1	ARLIN		Inv	1
3	>741-0004-200	IC, 74HC04	U13	ARLIN		Inv	1
3	>741-0032-200	IC, 74HC32	U20	ARLIN		Inv	1
3	>741-0075-200	IC, 74HC75	U26	ARLIN		Inv	1
3	>741-0125-200	IC, 74HC125	U9	ARLIN		Inv	1
3	>741-0244-200	IC, 74HC244	U12,U19,U27,U28	ARLIN		Inv	4
3	>741-0273-200	IC, 74HC273	U14	ARLIN		Inv	1
3	>741-0374-200	IC, 74HC374	U18	ARLIN		Inv	1
3	>741-0373-200	IC, 74HC373	U22	ARLIN		Inv	1
3	>741-0688-200	IC, 74HC688	U29	ARLIN		Inv	1
3	>745-0245-200	IC, 74HCT245	U30	ARLIN		Inv	1

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BEGINNING RANGE: SAT-V41PA-8-0 ENDING RANGE: SAT-V41PA-8-0

LEVEL	ITEM KEY	ITEM DESCRIPTION	BOM DESCRIPTION	LOC	OVHD KEY	ITEM TYPE	QTY REQUIRED
3	>999-9999-001	SPECIAL NOTES	MASK HOLES FOR R1-R12	ARLIN		Inv	1
3	>730-0029-000	IC, MAX 690CPA (MAX690CPA ONLY)	U34	ARLIN		Inv	1
3	>622-0001-002	IC, ICS2694 M-004 (31)	U32	ARLIN		Inv	1
3	>400-0242-000D	PCB, SAT-V41 REV.D		ARLIN		Inv	1
3	>200-0203-100	SOCKET 20 PIN ICO-203-S8A-T (176	U7	ARLIN		Inv	1
3	>201-0026-021	HDR 26 PIN ST IDH-26LP-S3-TG/TR	J2	ARLIN		Inv	1
3	>124-0004-000	DIODE 1N4148	D2	ARLIN		Inv	1
3	>114-0514-450	RESISTOR 510K 1/4 W 5%	R17	ARLIN		Inv	1
3	>114-0243-450	RESISTOR 24K 1/4 W 5%	R14	ARLIN		Inv	1
3	>113-0104-102	POT 100K (BI) 64WR100K RJ26FW104	R13	ARLIN		Inv	1
3	>110-0014-005	CAP 10uF 25v 10% TAN RAD .1	C18	ARLIN		Inv	1
3	>110-0011-003	CAP .1uF 50v 20% CER RAD .1	C21,C22	ARLIN		Inv	2
2	0242-401-0000	SUB ASSY SAT-V41A-8 MHZ REV.D		ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	10-29-98 MEB (-5S)	ARLIN		Inv	1
3	>111-0001-000	BAT 3V LI COIN CR2032-H04 (SONY)	BT1	ARLIN		Inv	1
3	>901-0012-000	IC, 27C512-15 CER EPROM	U25 CS=ABD9 BIOS	ARLIN		Inv	1
3	>743-0005-100	IC, MAX232CPE, SP232ACP, DS232A-	U2	ARLIN		Inv	1
3	>801-0045-200	IC, D70208L-8 V40 CPU CMOS (NEC)	U33	ARLIN		Inv	1
3	>730-0031-000	IC, SP238ACS, ADM238LJN, MAX238C	U35,U36	ARLIN		Inv	2
3	>801-0060-200	IC, ST16C452CJ68 (AT) (STARTECH)	U10	ARLIN		Inv	1
3	>901-0011-000	IC, PALC22V10-35PC (15,TI) (17,C	U15 CS=B4F0	ARLIN		Inv	2
3	>999-9999-001	SPECIAL NOTES	U24 CS=F78F	ARLIN		Inv	1
3	>801-0031-200	IC, uPD71055C PROG PAR INTERFACE	U16	ARLIN		Inv	1
3	>500-0027-002	INSULATOR SAT BATTERY PROTECT	* PUT IN OPEN BAG LOOSE UNTIL SHIPPING *	ARLIN		Inv	1
3	>201-0002-000	PLUG JUMPER 999-19-310-00	JUMPERS TO TEST 'PC' VERSION SAT-V40	ARLIN		Inv	29
3	>999-9999-001	SPECIAL NOTES	J14=1-2	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J15=1-2	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J16=1-3 2-4 5-6 11-12	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J17=2-3	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J18=1-2 4-6 5-7 9-11 12-14	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J19=2-3	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J20=2-3	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J21=2-3	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J22=1-2 3-4	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J23=2-3	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J24=1-2	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J28=1-2 ***VERTICAL (LIKE J31)***	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J29=1-2 5-6 13-14	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J30=1-2	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J31=1-2 3-4 5-6	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J9=OPEN	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J10=OPEN	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J11=OPEN	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J12=OPEN	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J25=1-2	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J26=1-2	ARLIN		Inv	1
3	>999-9999-001	SPECIAL NOTES	J27=OPEN	ARLIN		Inv	1
3	>730-0073-000	IC, MAX186DCPP {18}	U7	ARLIN		Inv	1
2	910-0024-000	LABEL, STATIC SENSITIVE 130-02	LABEL, STATIC SENSITIVE 130-02	ARLIN		Inv	1
2	950-0002-000	BAG PINK POLY 6X10 6 MIL 09-0610	BAG PINK POLY 6X10 6 MIL 09-0610	ARLIN		Inv	1

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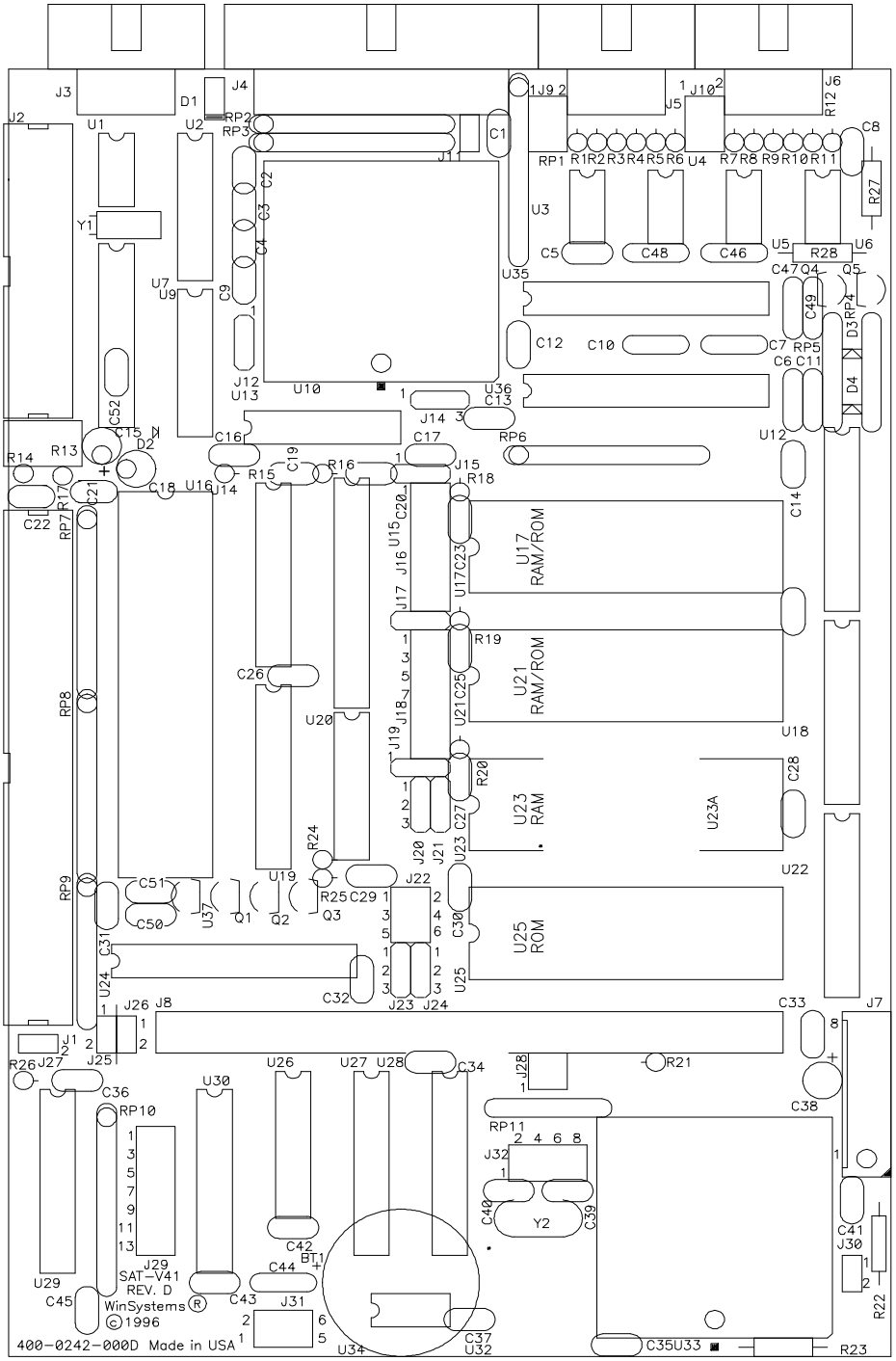
5 APPENDIX C

SAT-V41 Parts Placement Guide



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6 APPENDIX D

NEC V40 Datasheet Reprint

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NEC

NEC Electronics Inc.

μPD70208 (V40™) 8/16-BIT, HIGH-INTEGRATION CMOS MICROPROCESSOR

PRELIMINARY INFORMATION

Description

The μPD70208 (V40™) is a high-performance, low-power 16-bit microprocessor integrating a number of commonly used peripherals to dramatically reduce the size of microprocessor systems. The CMOS construction makes the μPD70208 ideal for the design of portable computers, instrumentation, and process control equipment.

The μPD70208 contains a powerful instruction set that is compatible with the μPD70108/μPD70116 (V20™/V30™) and μPD8086/μPD8088 instruction sets. Instruction set support includes a wide range of arithmetic, logical, and control operations as well as bit manipulation, BCD arithmetic, and high-speed block transfer instructions. The μPD70208 can also execute the entire μPD8080AF instruction set using the 8080 emulation mode. Also available is the μPD70216 (V50™), identical to the μPD70208 but with a 16-bit external data bus.

Features

- ☐ V20/V30 instruction set compatible
- ☐ Minimum instruction execution time: 250 ns (at 8 MHz)
- ☐ Direct addressing of 1M bytes of memory
- ☐ Powerful set of addressing modes
- ☐ 14 16-bit registers
- ☐ On-chip peripherals including
  - — Clock generator
  - — Bus interface
  - — Bus arbitration
  - — Programmable wait state generator
  - — DRAM refresh control
  - — Three 16-bit timer/counters
  - — Asynchronous serial I/O control
  - — Eight-input interrupt control
  - — Four-channel DMA control
- ☐ Hardware effective address calculation logic
- ☐ Maskable and nonmaskable interrupts
- ☐ μPD72191 Floating Point Processor interface
- ☐ IEEE 796 compatible bus interface
- ☐ Low-power standby mode
- ☐ Low-power CMOS technology

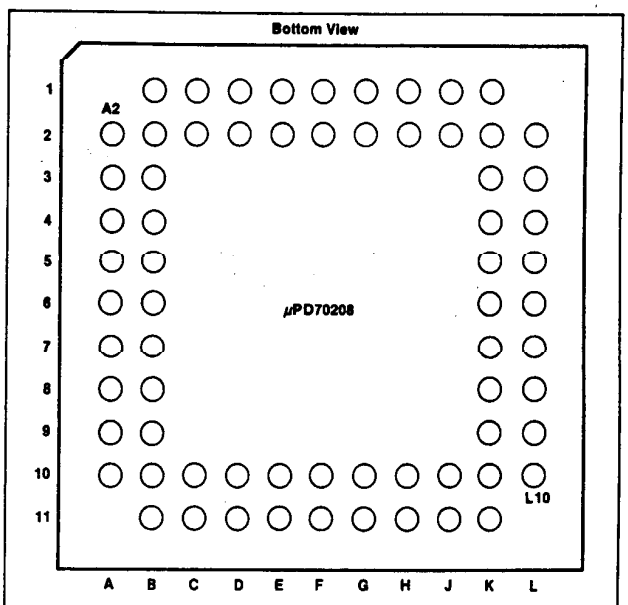
V20, V30, V40, and V50 are trademarks of NEC Corporation.

Ordering Information

Part Number	Package	Maximum Frequency
μPD70208R-8	68-pin PGA	8 MHz
μPD70208L-8	68-pin PLCC	8 MHz
μPD70208G-8	80-pin plastic miniflat	8 MHz

Pin Configurations

68-Pin PGA

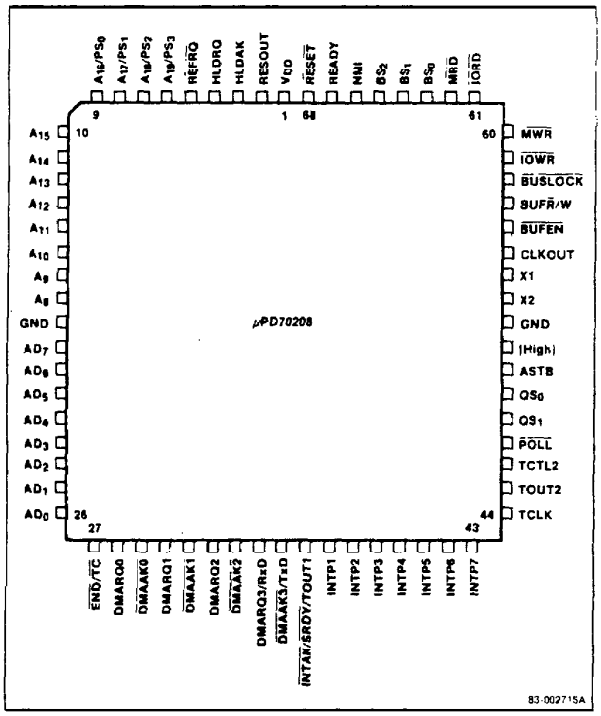


Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
A2	INTP7	B9	DMARQ1	F10	AD_7	K4	NMI
A3	INTP5	B10	DMARQ0	F11	GND	K5	$\overline{RESET}$
A4	INTP3	B11	AD_0	G1	X1	K6	RESOUT
A5	INTP1	C1	TCTL2	G2	CLKOUT	K7	HLDRQ
A6	$\overline{DMAAK3}$/TxD	C2	$\overline{FOLL}$	G10	A_8	K8	A_{19}/PS_3
A7	$\overline{DMAAK2}$	C10	AD_1	G11	A_9	K9	A_{17}/PS_1
A8	$\overline{DMAAK1}$	C11	AD_2	H1	$\overline{BUFEN}$	K10	A_{14}
A9	$\overline{DMAAK0}$	D1	QS_1	H2	BUFR/W	K11	A_{15}
A10	$\overline{END}/\overline{TC}$	D2	QS_0	H10	A_{10}	L2	$\overline{IORD}$
B1	TCLK	D10	AD_3	H11	A_{11}	L3	BS_0
B2	TOUT2	D11	AD_4	J1	$\overline{BUSLOCK}$	L4	BS_2
B3	INTP6	E1	ASTB	J2	$\overline{IOWR}$	L5	READY
B4	INTP4	E2	[High]	J10	A_{12}	L6	V_{DD}
B5	INTP2	E10	AD_5	J11	A_{13}	L7	HLDAK
B6	$\overline{INTAK}/\overline{SRDY}$/TOUT1	E11	AD_6	K1	$\overline{MWR}$	L8	$\overline{REFRQ}$
B7	DMARQ3/RxD	F1	GND	K2	$\overline{MRD}$	L9	A_{18}/PS_2
B8	DMARQ2	F2	X2	K3	BS_1	L10	A_{16}/PS_0

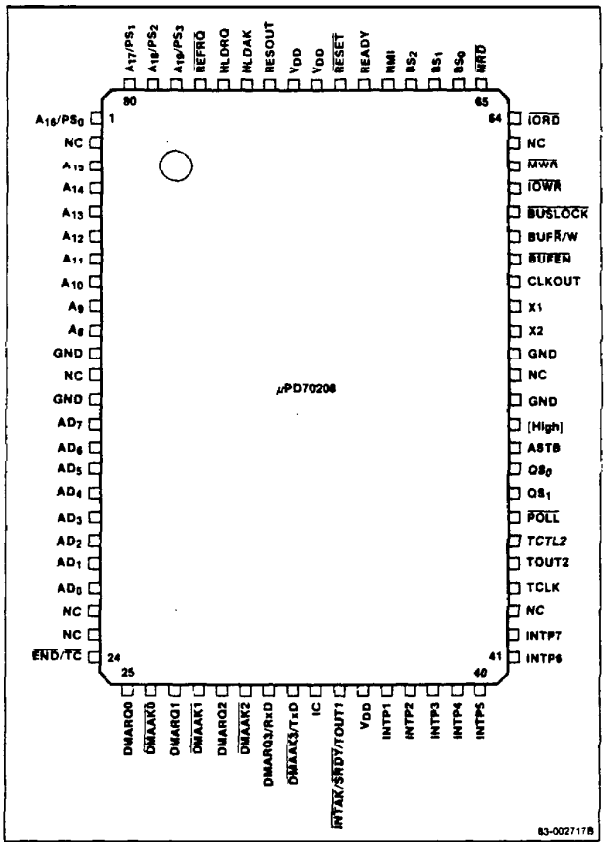
83-0027168

Pin Configurations (cont)

68-Pin PLCC



80-Pin Plastic Miniflat



Pin Identification

Symbol	Function
A_{19}-A_{16}/PS_3-PS_0	Multiplexed address/processor status outputs
A_{15}-A_8	Address bus outputs
AD_7-AD_0	Multiplexed address/data bus
ASTB	Address strobe output
$\overline{BUFEN}$	Data bus transceiver enable output
BUFR/W	Data bus transceiver direction output
$\overline{BUSLOCK}$	Buslock output
BS_2-BS_0	Bus status outputs
CLKOUT	System clock output
$\overline{DMAAK0}$	DMA channel 0 acknowledge output
$\overline{DMAAK1}$	DMA channel 1 acknowledge output
$\overline{DMAAK2}$	DMA channel 2 acknowledge output
$\overline{DMAAK3}$/TxD	DMA channel 3 acknowledge output/Serial transmit data output
DMARQ0	DMA channel 0 request input
DMARQ1	DMA channel 1 request input
DMARQ2	DMA channel 2 request input
DMARQ3/RxD	DMA channel 3 request input/Serial receive data input
$\overline{END}$/$\overline{TC}$	End input/Terminal count output
GND	Ground
High	High-level output except during hold acknowledge when it is placed in the high-impedance state
HLDAK	Hold acknowledge output
HLDRQ	Hold request input
IC	Internal connection; leave unconnected
$\overline{INTAK}$/TOUT1/$\overline{SRDY}$	Interrupt acknowledge output/Timer/counter 1 output/Serial ready output
INTP1-INTP7	Interrupt request inputs
$\overline{IORD}$	I/O read strobe output
$\overline{IOWR}$	I/O write strobe output
$\overline{MRD}$	Memory read strobe output
$\overline{MWR}$	Memory write strobe output
NC	No connection
NMI	Nonmaskable interrupt input
$\overline{POLL}$	Poll input
QS_1-QS_0	CPU queue status outputs
READY	Ready input
$\overline{REFRQ}$	Refresh request output
$\overline{RESET}$	Reset input
RESOUT	Synchronized reset output
TCLK	Timer/counter external clock input
TCTL2	Timer/counter 2 control input
TOUT2	Timer/counter 2 output
V_{DD}	+5 V power supply input
X1, X2	Crystal/external clock inputs

Pin Functions

A_{19}-A_{16}/PS_3-PS_0 [Address/Status Bus]

These three-state output pins contain the upper 4 bits of the 20-bit address during T1 and processor status information during T2, T3, Tw, and T4. During T1 of a memory read or write cycle, these pins contain the upper 4 bits of the 20-bit address. These pins are forced low during T1 of an I/O bus cycle.

Processor status is output during T2, T3, Tw, and T4 of both memory and I/O bus cycles. PS_3 is zero during any CPU native mode bus cycle. During any DMA, refresh, or 8080 emulation mode bus cycle, PS_3 outputs a high level. PS_2 outputs the contents of the interrupt enable (IE) flag in the CPU PSW register. PS_1 and PS_0 indicate the segment register used to form the physical address of a CPU bus cycle as follows:

PS_1	PS_0	Segment
0	0	Data segment 1 (DS1)
0	1	Stack segment (SS)
1	0	Program segment (PS)
1	1	Data segment 0 (DS0)

These pins are in the high-impedance state during hold acknowledge.

A_{15}-A_8 [Address Bus]

These three-state pins form the active-high address bus. During any CPU, DMA, or refresh bus cycle, A_{15}-A_8 output the middle 8 bits of the 20-bit memory or I/O address. The A_{15}-A_8 pins enter the high-impedance state during hold acknowledge or an internal interrupt acknowledge bus cycle. During a slave interrupt acknowledge bus cycle, A_{10}-A_8 contain the address of the slave interrupt controller.

AD_7-AD_0 [Address/Data Bus]

These three-state pins form the active-high, time-multiplexed address/data bus. During T1 of a bus cycle, AD_7-AD_0 output the lower 8 bits of the 20-bit memory or I/O address. During the T2, T3, Tw, and T4 states, AD_7-AD_0 form the 8-bit bidirectional data bus.

The AD_7-AD_0 pins enter the high-impedance state during hold acknowledge or internal interrupt acknowledge bus cycles or while $\overline{RESET}$ is asserted.

ASTB [Address Strobe]

This active-high output is used to latch the address from the multiplexed address bus in an external address latch during T1 of a bus cycle. ASTB is held at a low level during hold acknowledge.

$\overline{\text{BUFEN}}$ [Buffer Enable]

$\overline{\text{BUFEN}}$ is an active-low output for enabling an external data bus transceiver during a bus cycle. $\overline{\text{BUFEN}}$ is asserted during T2 through T4 of a read cycle, T2 through T3 of a slave interrupt acknowledge cycle, and T1 through T4 of a write cycle. $\overline{\text{BUFEN}}$ is not asserted when the bus cycle corresponds to an internal peripheral, DMA, refresh, or internal interrupt acknowledge cycle. $\overline{\text{BUFEN}}$ enters the high-impedance state during hold acknowledge.

BUF$\overline{\text{R}}$/W [Buffer Read/Write]

BUF$\overline{\text{R}}$/W is a three-state, active-low output used to control the direction of an external data bus transceiver. A high level indicates the μPD70208 will perform a write cycle and a low level indicates a read cycle. BUF$\overline{\text{R}}$/W enters the high-impedance state during hold acknowledge.

$\overline{\text{BUSLOCK}}$

This active-low output provides a means for the CPU to indicate to an external bus arbiter that the bus cycles of the next instruction are to be kept contiguous. $\overline{\text{BUSLOCK}}$ is asserted for the duration of the instruction following the BUSLOCK prefix. $\overline{\text{BUSLOCK}}$ is also asserted during interrupt acknowledge cycles and enters the high-impedance state during hold acknowledge. While $\overline{\text{BUSLOCK}}$ is asserted, DMAU, RCU, and external bus requests are disabled.

BS_2-BS_0 [Bus Status]

Outputs BS_2-BS_0 indicate the type of bus cycle being performed as follows.

BS_2	BS_1	BS_0	Bus Cycle
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Memory read (1)
1	1	0	Memory write (2)
1	1	1	Passive state

Note:

(1) Memory read bus cycles include CPU, DMA read, DMA verify, and refresh bus cycles.

(2) Memory write bus cycles include CPU and DMA write bus cycles.

BS_2-BS_0 are three-state outputs and are high impedance during hold acknowledge.

CLKOUT

The CLKOUT output is used to generate all internal timing for the μPD70208. CLKOUT has a 50-percent duty cycle at half the frequency of the input clock source.

$\overline{\text{DMAAK0}}$-$\overline{\text{DMAAK2}}$ [DMA Acknowledge]

This set of outputs contains the DMA acknowledge signals for channels 0-2 from the internal DMA controller and indicate that the peripheral can perform the requested transfer.

$\overline{\text{DMAAK3}}$/TxD [DMA Acknowledge 3]/[Serial Transmit Data]

Two output signals multiplexed on this pin are selected by the PF field of the on-chip peripheral connection register.

- $\overline{\text{DMAAK3}}$ is an active-low output and enables an external DMA peripheral to perform the requested DMA transfer for channel 3.
- TxD is the serial output from the serial control unit.

DMARQ0-DMARQ2 [DMA Request]

These synchronized inputs are used by external peripherals to request DMA service for channels 0-2 from the internal DMA controller.

DMARQ3/RxD [DMA Request 3]/[Serial Receive Data]

Two input signals multiplexed on this pin are selected by the PF field of the on-chip peripheral connection register.

- DMARQ3 is used by an external peripheral to request a DMA transfer cycle for channel 3.
- RxD is the serial input to the serial control unit.

$\overline{END}/\overline{TC}$ [End/Terminal Count]

This active-low bidirectional pin controls the termination of a DMA service. Assertion of $\overline{END}$ by external hardware during DMA service causes the service to terminate. When a DMA channel reaches its terminal count, the DMAU asserts $\overline{TC}$, indicating the programmed operation has completed.

$\overline{END}/\overline{TC}$ is an open-drain I/O pin, and requires an external 2.2-kΩ pull-up resistor.

HLDAK [Hold Acknowledge]

When an external bus requester has become the highest priority requester, the internal bus arbiter will assert the HLDAK output indicating the address, data, and control buses have entered a high-impedance state and are available for use by the external bus master.

Should the internal DMAU or RCU (demand mode) request the bus, the bus arbiter will drive HLDAK low. When this occurs, the external bus master should complete the current bus cycle and negate the HLDRQ signal. This allows the bus arbiter to reassign the bus to the higher priority requester.

HLDRQ [Hold Request]

This active-high signal is asserted by an external bus master requesting to use the local address, data, and control buses. The HLDRQ input is used by the internal bus arbiter, which gives control of the buses to the highest priority bus requester in the following order.

Bus Master	Priority
RCU	Highest (demand mode)
DMAU	•
HLDRQ	•
CPU	•
RCU	Lowest (normal operation)

$\overline{INTAK}/TOUT1/\overline{SRDY}$ [Interrupt Acknowledge]/[Timer 1 Output]/[Serial Ready]

Three output signals multiplexed on this pin are selected by the PF field of the on-chip peripheral connection register.

- $\overline{INTAK}$ is an interrupt acknowledge signal used to cascade external slave μPD71059 Interrupt Controllers. $\overline{INTAK}$ is asserted during T2, T3, and Tw states of an interrupt acknowledge cycle.
- TOUT1 is the output of timer/counter 1.
- $\overline{SRDY}$ is an active-low output and indicates that the serial control unit is ready to receive the next character.

INTP1-INTP7 [Peripheral Interrupts]

INTP1-INTP7 accept either rising-edge or high-level triggered asynchronous interrupt requests from external peripherals. These INTP1-INTP7 inputs are internally synchronized and prioritized by the interrupt control unit, which requests the CPU to perform an interrupt acknowledge bus cycle. External interrupt controllers such as the μPD71059 can be cascaded to increase the number of vectored interrupts.

These interrupt inputs cause the CPU to exit both the standby and 8080 emulation modes.

INTP1-INTP7 contain internal pull-up resistors and may be left unconnected.

$\overline{IORD}$ [I/O Read]

This three-state pin outputs an active-low I/O read strobe during T2, T3, and Tw of an I/O read bus cycle. Both CPU I/O read and DMA write bus cycles assert $\overline{IORD}$. $\overline{IORD}$ is not asserted when the bus cycle corresponds to an internal peripheral. It enters the high-impedance state during hold acknowledge.

$\overline{IOWR}$ [I/O Write]

This three-state pin outputs an active-low I/O write strobe during T2, T3, and Tw of a CPU I/O write or an extended DMA read cycle and during T3 and Tw of a DMA read bus cycle. $\overline{IOWR}$ is not asserted when the bus cycle corresponds to an internal peripheral. It enters the high-impedance state during hold acknowledge.

$\overline{MRD}$ [Memory Read Strobe]

This three-state pin outputs an active-low memory read strobe during T2, T3, and Tw of a memory read bus cycle. CPU memory read, DMA read, and refresh bus cycles all assert $\overline{MRD}$. $\overline{MRD}$ enters the high-impedance state during hold acknowledge.

$\overline{MWR}$ [Memory Write Strobe]

This three-state pin outputs an active-low memory write strobe during T2, T3, and Tw of a CPU memory write or DMA extended write bus cycle and during T3 and Tw of a DMA normal write bus cycle. $\overline{MWR}$ enters the high-impedance state during hold acknowledge.

NMI [Nonmaskable Interrupt]

The NMI pin is a rising-edge-triggered interrupt input that cannot be masked by software. NMI is sampled by CPU logic each clock cycle and when found valid for five or more CLKOUT cycles, the NMI interrupt is accepted. The CPU will process the NMI interrupt immediately after the current instruction finishes execution by fetching the segment and offset of the NMI handler from interrupt vector 2. The NMI interrupt causes the CPU to exit both the standby and 8080 emulation modes. The NMI input takes precedence over the maskable interrupt inputs.

$\overline{POLL}$ [Poll]

The active-low $\overline{POLL}$ input is used to synchronize the operation of external devices with the CPU. During execution of the POLL instruction, the CPU checks the $\overline{POLL}$ input state every five clocks until $\overline{POLL}$ is once again asserted.

QS_1-QS_0 [Queue Status]

The QS_1 and QS_0 outputs maintain instruction synchronization between the μPD70208 CPU and external devices such as the μPD72191 Floating Point Processor. These outputs are interpreted as follows.

QS_1	QS_0	Instruction Queue Status
0	0	No operation
0	1	First byte of instruction fetched
1	0	Flush queue contents
1	1	Subsequent byte of instruction fetched

Queue status is valid for one clock cycle after the CPU has accessed the instruction queue.

READY [Ready]

This active-high input synchronizes external memory and peripheral devices with the μPD70208. Slow memory and I/O devices can lengthen a bus cycle by negating the READY input and forcing the BIU to insert Tw states. READY must be negated prior to the rising edge of CLKOUT during the T2 state to guarantee recognition. When READY is once again asserted and recognized by the BIU, the BIU will proceed to the T4 state.

The READY input operates in parallel with the internal μPD70208 wait control unit and can be used to insert more than three wait states into a bus cycle.

$\overline{REFRQ}$ [Refresh Request]

$\overline{REFRQ}$ is an active-low output indicating the current bus cycle is a memory refresh operation. $\overline{REFRQ}$ is used to disable memory address decode logic and refresh dynamic memories. The 9-bit refresh row address is placed on A_8-A_0 during a refresh bus cycle.

$\overline{RESET}$ [Reset]

The $\overline{RESET}$ input is used to force the μPD70208 to a known state by resetting the CPU and on-chip peripherals. $\overline{RESET}$ must be asserted for a minimum of four clocks to guarantee recognition. After $\overline{RESET}$ has been released, the CPU will start program execution from address FFFF0H.

$\overline{RESET}$ will release the CPU from the low-power standby mode and force it to the native mode.

RESOUT [Reset Output]

This active-high output is available to perform a system-wide reset function. Reset is internally synchronized with CLKOUT and output on the RESOUT pin.

TCLK

TCLK is an external clock source for the timer control unit. The three timer/counters can be programmed to operate with either the TCLK input or a prescaled CLKOUT input.

TCTL2

TCTL2 is the control input for timer/counter 2.

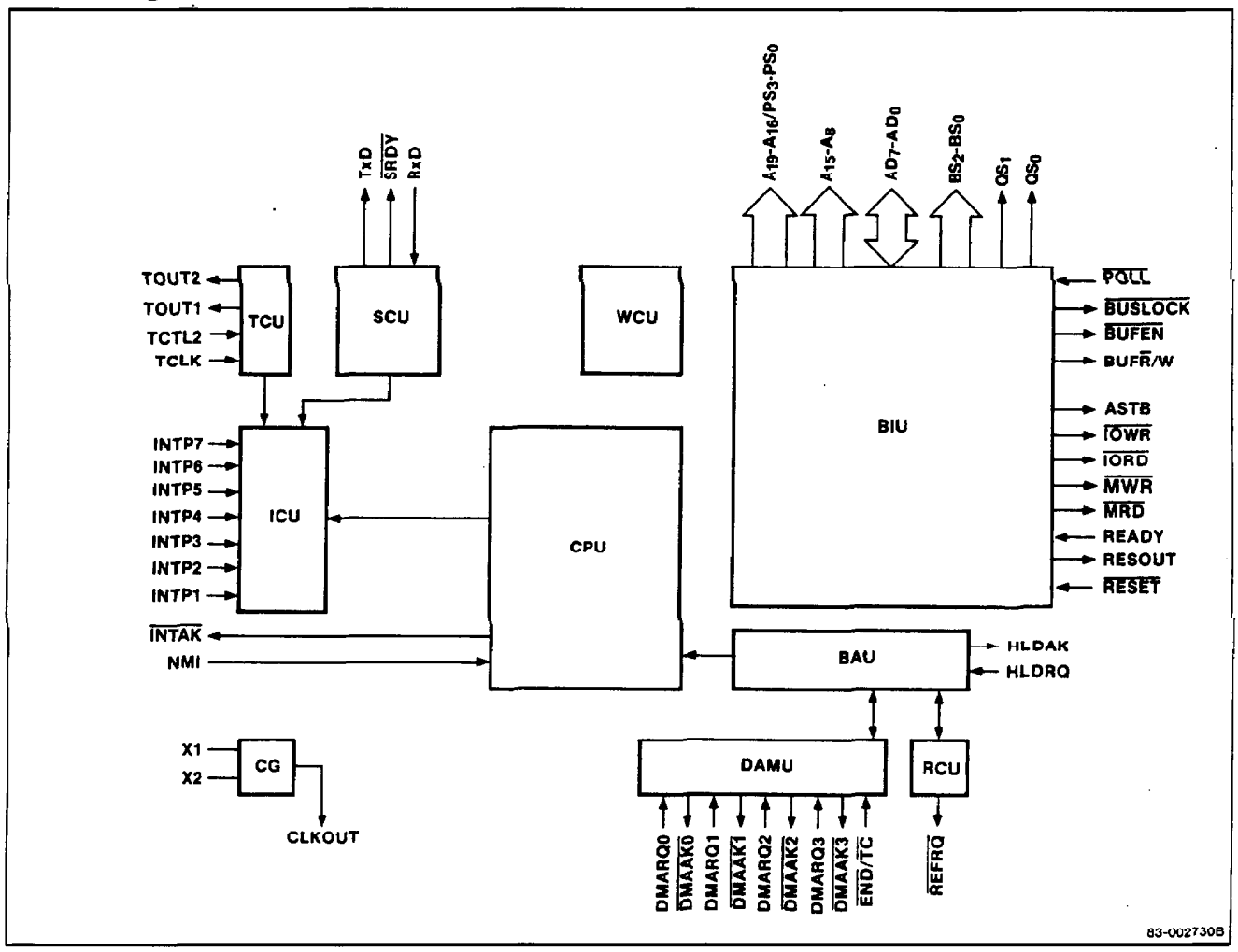
TOUT2

TOUT2 is the output of timer/counter 2.

X1, X2 [Clock Inputs]

These pins accept either a parallel resonant, fundamental mode crystal or an external oscillator input with a frequency twice the desired operating frequency.

Block Diagram



3

Absolute Maximum Ratings

T_A = +25°C

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.3 V
CLK input voltage, V_K	−0.5 to V_{DD} + 1.0 V
Output voltage, V_O	−0.5 to V_{DD} + 0.3 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposing the device to stresses above those listed in the Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.2	V_{DD} + 0.3	V	
Input voltage, low	V_{IL}	−0.5	0.8	V	
X1, X2 input voltage, high	V_{KH}	3.9	V_{DD} + 1.0	V	
X1, X2 input voltage, low	V_{KL}	−0.5	0.6	V	
Output voltage, high	V_{OH}	0.7 V_{DD}		V	I_{OH} = −400 μA
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 2.5 mA
Input leakage current, high	I_{LIH}		10	μA	$V_I = V_{DD}$
Input leakage current, low	I_{LIPL}		−300	μA	V_I = 0 V, INTP input pins
	I_{LIL}		−10	μA	V_I = 0 V, other input pins
Output leakage current, high	I_{LOH}		10	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}		−10	μA	V_O = 0 V
Supply current	I_{DD}		90 20	mA mA	Normal mode Standby mode

Capacitance

T_A = +25°C, V_{DD} = 0 V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input capacitance	C_I		15	pF	f_C = 1 MHz; unmeasured pins are returned to 0 V.
Output capacitance	C_O		15	pF	

AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%; C_L = 100 pF

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
External clock input cycle time	t_{CYX}	62	250	ns	
External clock pulse width, high	t_{XXH}	20		ns	V_{KH} = 3.0 V
External clock pulse width, low	t_{XXL}	20		ns	V_{KL} = 1.5 V
External clock rise time	t_{XR}		10	ns	1.5 → 3.0 V
External clock fall time	t_{XF}		10	ns	3.0 → 1.5 V
CLKOUT cycle time	t_{CYK}	124	500	ns	
CLKOUT pulse width, high	t_{KKH}	0.5 t_{CYK} − 7		ns	V_{KH} = 3.0 V
CLKOUT pulse width, low	t_{KKL}	0.5 t_{CYK} − 7		ns	V_{KL} = 1.5 V
CLKOUT rise time	t_{KR}		7	ns	1.5 → 3.0 V
CLKOUT fall time	t_{KF}		7	ns	3.0 → 1.5 V
CLKOUT delay time from external clock	t_{DXK}		55	ns	
Input rise time (except external clock)	t_{IR}		20	ns	0.8 → 2.2 V
Input fall time (except external clock)	t_{IF}		12	ns	2.2 → 0.8 V
Output rise time (except CLKOUT)	t_{OR}		20	ns	0.8 → 2.2 V
Output fall time (except CLKOUT)	t_{OF}		12	ns	2.2 → 0.8 V
$\overline{\text{RESET}}$ setup time to CLKOUT↓	t_{SRESK}	25		ns	
$\overline{\text{RESET}}$ hold time after CLKOUT↓	t_{HKRES}	35		ns	
RESOUT delay time from CLKOUT↓	t_{DKRES}	5	60	ns	
READY inactive setup time to CLKOUT↑	t_{SRYLK}	15		ns	
READY inactive hold time after CLKOUT↑	t_{HKRYL}	25		ns	
READY active setup time to CLKOUT↑	t_{SRYHK}	15		ns	
READY active hold time after CLKOUT↑	t_{HKRYH}	25		ns	
NMI, $\overline{\text{POLL}}$ setup time to CLKOUT↑	t_{SIK}	15		ns	

AC Characteristics (cont)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Data setup time to CLKOUT↓	t_{SDK}	20		ns	
Data hold time after CLKOUT↓	t_{HKD}	15		ns	
Address delay time from CLKOUT↓	t_{DKA}	10	60	ns	
Address hold time after CLKOUT↓	t_{HKA}	10		ns	
PS delay time from CLKOUT↓	t_{DKP}	10	60	ns	
PS float delay time from CLKOUT↑	t_{FKP}	10	60	ns	
Address setup time to ASTB↓	t_{SAST}	t_{KKL} − 30		ns	
Address float delay time from CLKOUT↓	t_{FKA}	t_{HKA}	60	ns	
ASTB↑ delay time from CLKOUT↓	t_{DKSTH}		50	ns	
ASTB↓ delay time from CLKOUT↑	t_{DKSTL}		55	ns	
ASTB pulse width, high	t_{STST}	t_{KKL} − 10		ns	
Address hold time after ASTB↓	t_{HSTA}	t_{KKH} − 10		ns	
Control delay time from CLKOUT	t_{DKCT}	15	60	ns	
$\overline{RD}$↓ delay time from address float	t_{DAFRL}	0		ns	
$\overline{RD}$↓ delay time from CLKOUT↓	t_{DKRL}	10	70	ns	
$\overline{RD}$↑ delay time from CLKOUT↓	t_{DKRH}	15	60	ns	
Address delay time from CLKOUT	t_{DRHA}	t_{CYK} − 40		ns	
$\overline{RD}$ pulse width, low	t_{RR}	$2t_{CYK}$ − 50		ns	
BUF$\overline{R}$/W delay from BUFEN↑	t_{DBECT}	t_{KKL} − 20		ns	Read cycle
	t_{DWCT}	t_{KKL} − 20		ns	Write cycle
Data output delay time from CLKOUT↓	t_{DKD}	10	60	ns	
Data float delay time from CLKOUT↓	t_{FKD}	10	60	ns	
$\overline{WR}$ pulse width, low	t_{WW}	$2t_{CYK}$ − 40		ns	
BS↓ delay time from CLKOUT↑	t_{DKBL}	10	60	ns	
BS↑ delay time from CLKOUT↓	t_{DKBH}	10	65	ns	

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
HLDRQ setup time to CLKOUT↑	t_{SHQK}	20		ns	
HLDAK delay time from CLKOUT↓	t_{DKHA}	10	100	ns	
Address drive delay time from CLKOUT↓	t_{DKA2}	t_{CYK}		ns	
$\overline{DMAAK}$ delay time from CLKOUT↑	t_{DKDAL}	10	70	ns	
$\overline{DMAAK}$ delay time from CLKOUT↓	t_{DKDAH}	10	115	ns	Cascade mode
$\overline{WR}$ pulse width, low (DMA cycle)	t_{WW1}	$2t_{CYK}$ − 40		ns	DMA extended write cycle
$\overline{WR}$ pulse width, low (DMA cycle)	t_{WW2}	t_{CYK} − 40		ns	DMA normal write cycle
$\overline{TC}$ output delay time from CLKOUT↑	t_{DKTCL}		60	ns	
$\overline{TC}$ off delay time from CLKOUT↑	t_{DKTCF}		60	ns	
$\overline{TC}$ pulse width, low	t_{TCTCL}	t_{CYK} − 15		ns	
$\overline{TC}$ pullup delay time from CLKOUT↑	t_{DKTCH}		t_{KKH} + t_{CYK} − 10	ns	
$\overline{END}$ setup time to CLKOUT↑	t_{SEDK}	35		ns	
$\overline{END}$ pulse width, low	t_{EDEDL}	100		ns	
DMARQ setup time to CLKOUT↑	t_{SDQK}	35		ns	
INTPn pulse width, low	t_{IPIPL}	100		ns	
RxD setup time to SCU internal clock↓	t_{SRX}	1		μs	
RxD hold time after SCU internal clock↓	t_{HRX}	1		μs	
$\overline{SRDY}$ delay time from CLKOUT↓	t_{DKSR}		150	ns	
TxD delay time from TOUT1↓	t_{DTX}		500	ns	
TCTL2 setup time from CLKOUT↓	t_{SGX}	50		ns	
TCTL setup time to TCLK↑	t_{SGTK}	50		ns	
TCTL2 hold time after CLKOUT↓	t_{HKG}	100		ns	
TCTL2 hold time after TCLK↑	t_{HTKG}	50		ns	
TCTL2 pulse width, high	t_{GGH}	50		ns	

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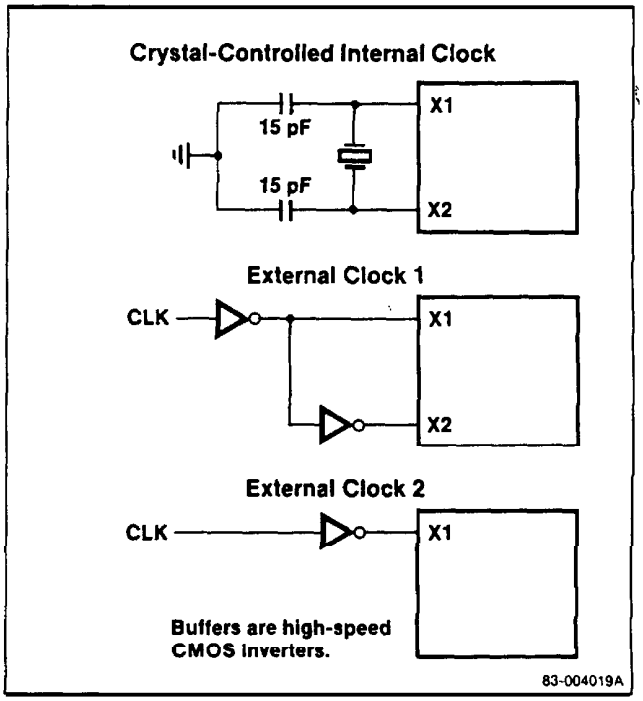
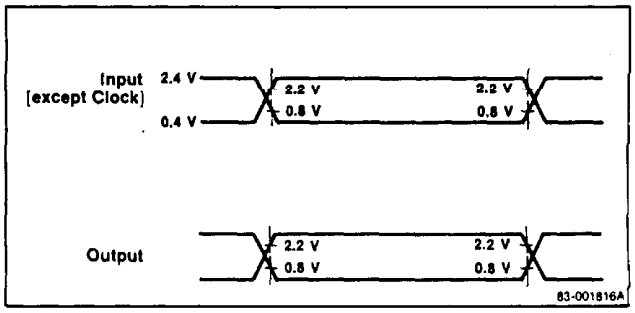
AC Characteristics (cont)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
TCTL2 pulse width, low	t_{GGL}	50		ns	
TOUT output delay time from CLKOUT↓	t_{DKTO}		200	ns	
TOUT output delay time from TOUT↓	t_{DTKTO}		150	ns	
TOUT output delay time from TCTL2↓	t_{DGTO}		120	ns	
TCLK rise time	t_{TKR}		25	ns	
TCLK fall time	t_{TKF}		25	ns	
TCLK pulse width, high	t_{TKTKH}	50		ns	
TCLK pulse width, low	t_{TKTKL}	50		ns	
TCLK cycle time	t_{CYTK}	124	Dc	ns	
RD↓, WR↓ delay from DMAAK↓	t_{DDARW}	t_{KKH} − 30		ns	
DMAAK↑ delay from RD↑	t_{DRHDAH}	t_{KKL} − 30		ns	
RD↑ delay from WR↑	t_{DWHRH}	5		ns	

Clock Input Configurations

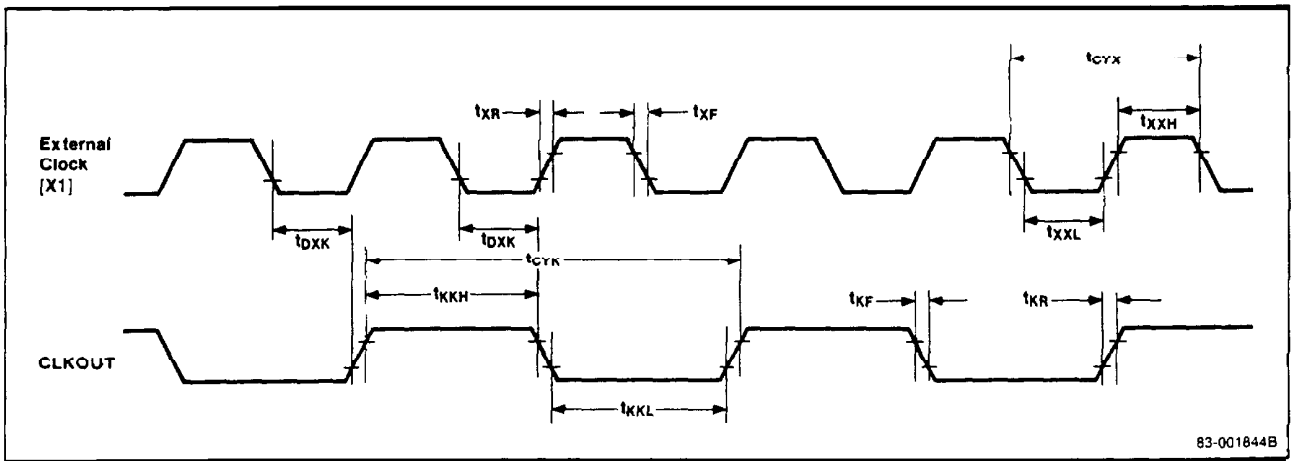


Timing Measurement Points



Timing Waveforms

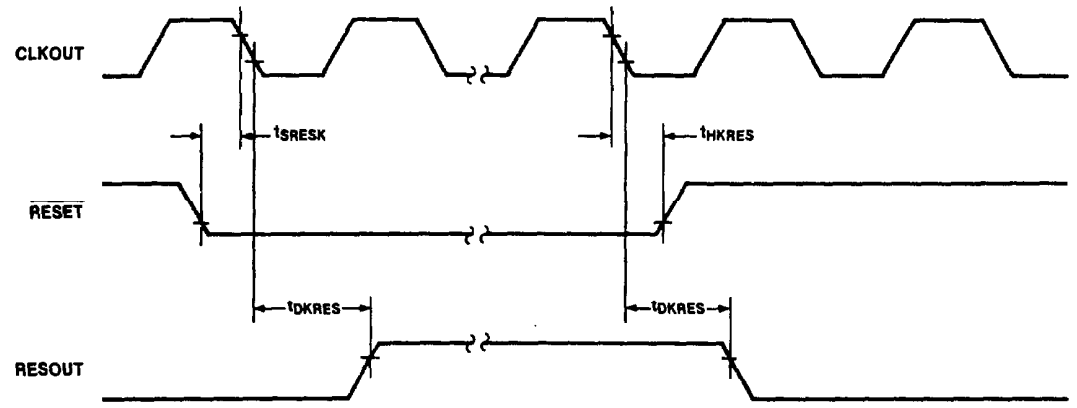
Clock Timing



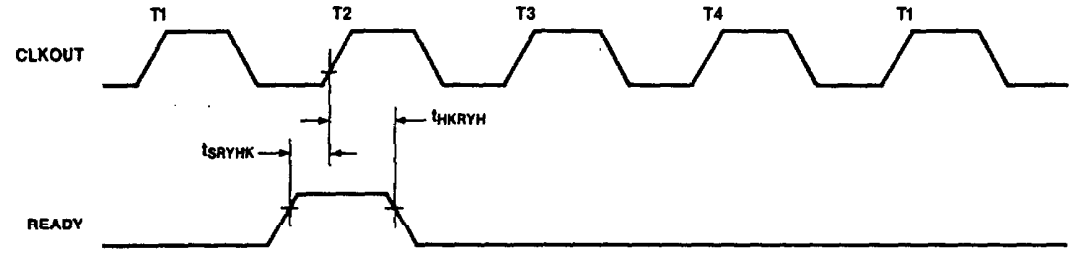
Timing Waveforms (cont)

Reset and Ready Timing

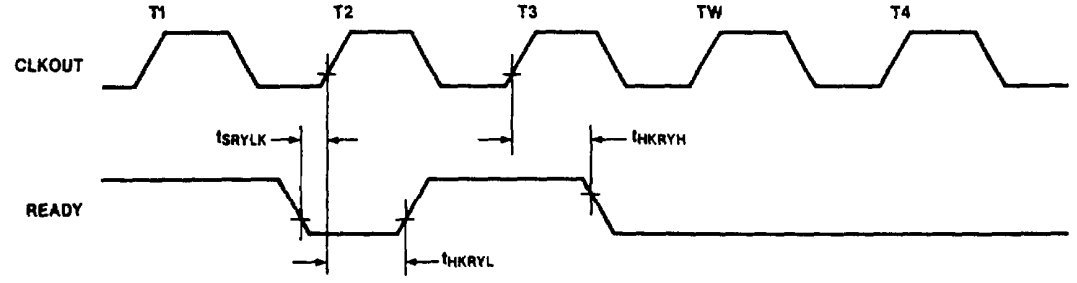
Reset Timing



Ready Timing, No Wait States



Ready Timng, Wait States



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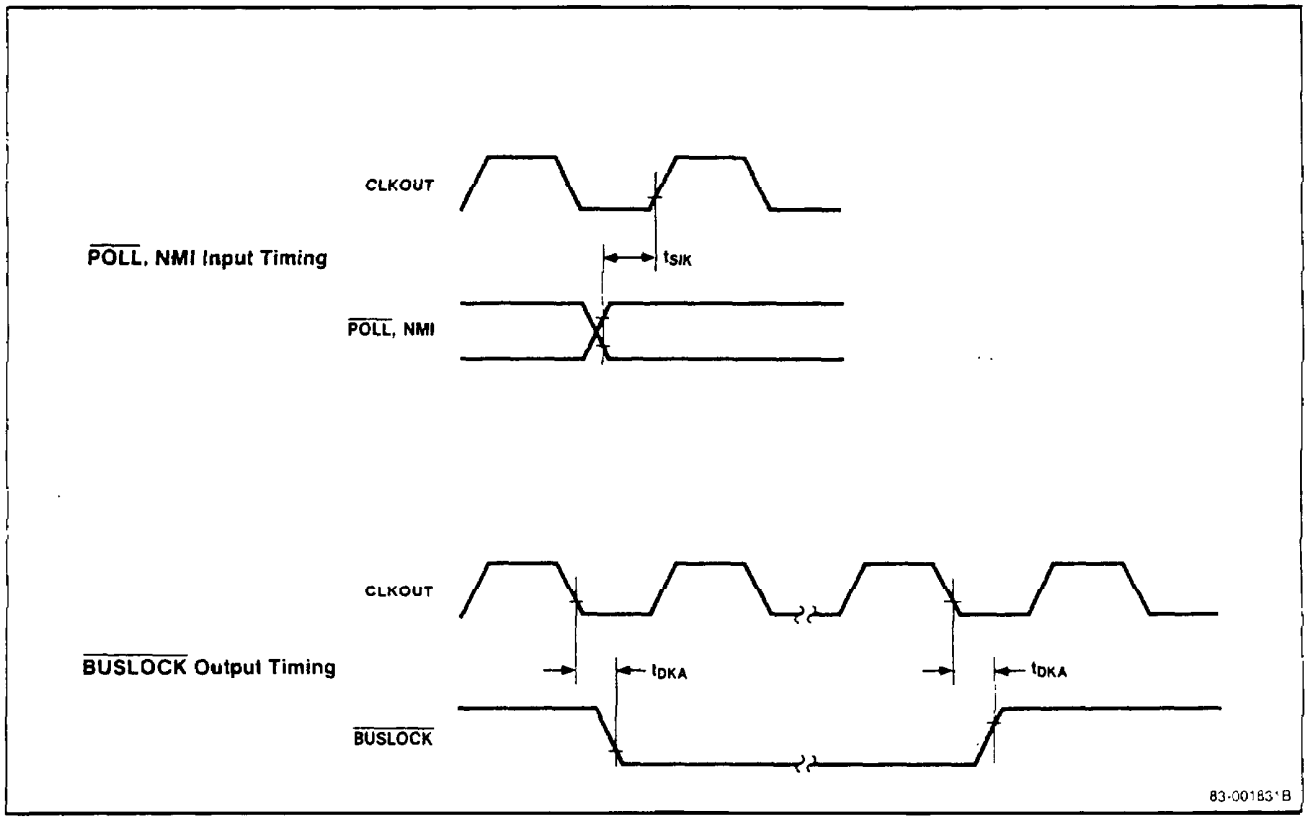
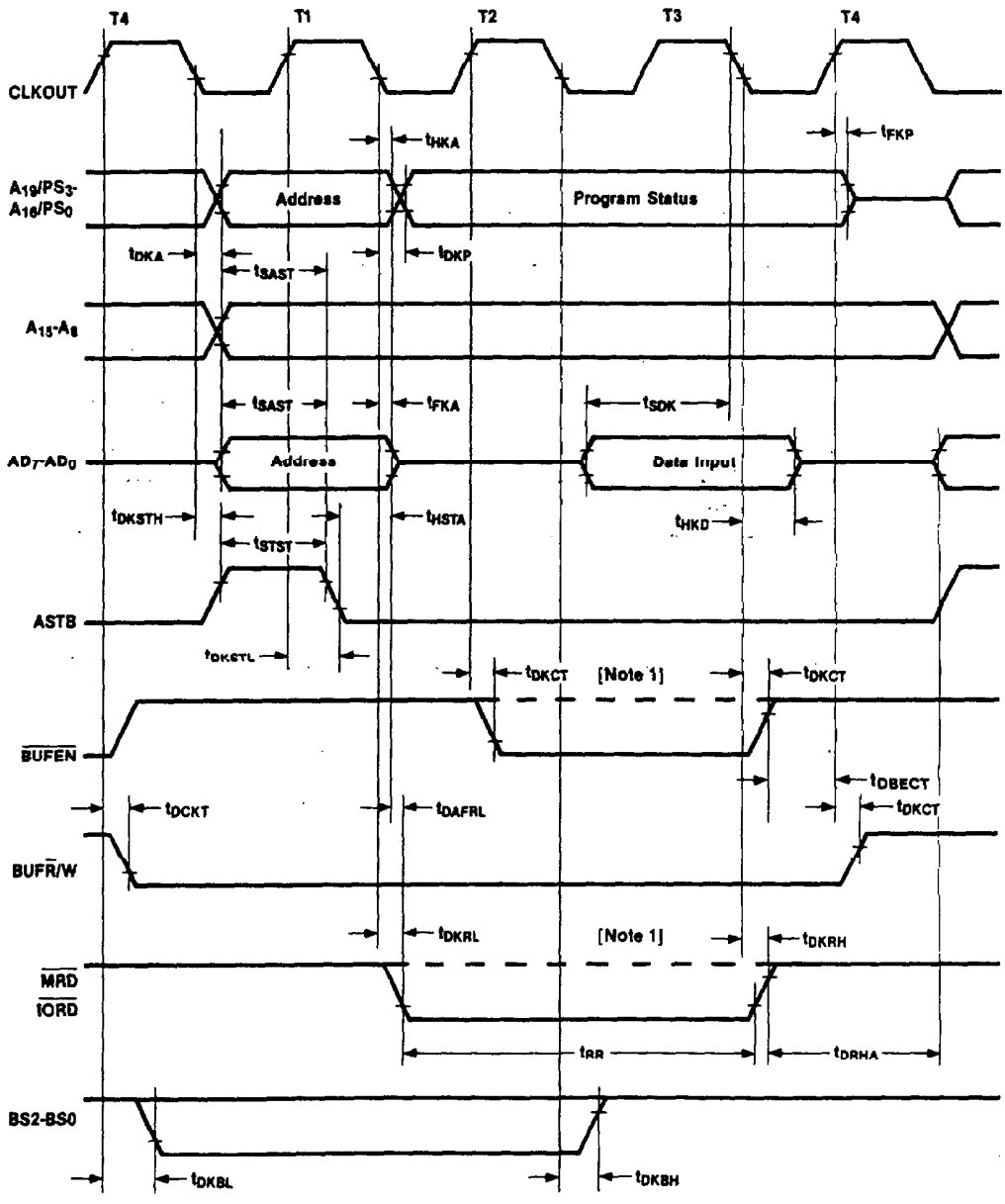
Timing Waveforms (cont)

Poll, NMI, and Buslock Timing



Timing Waveforms (cont)

Read Timing

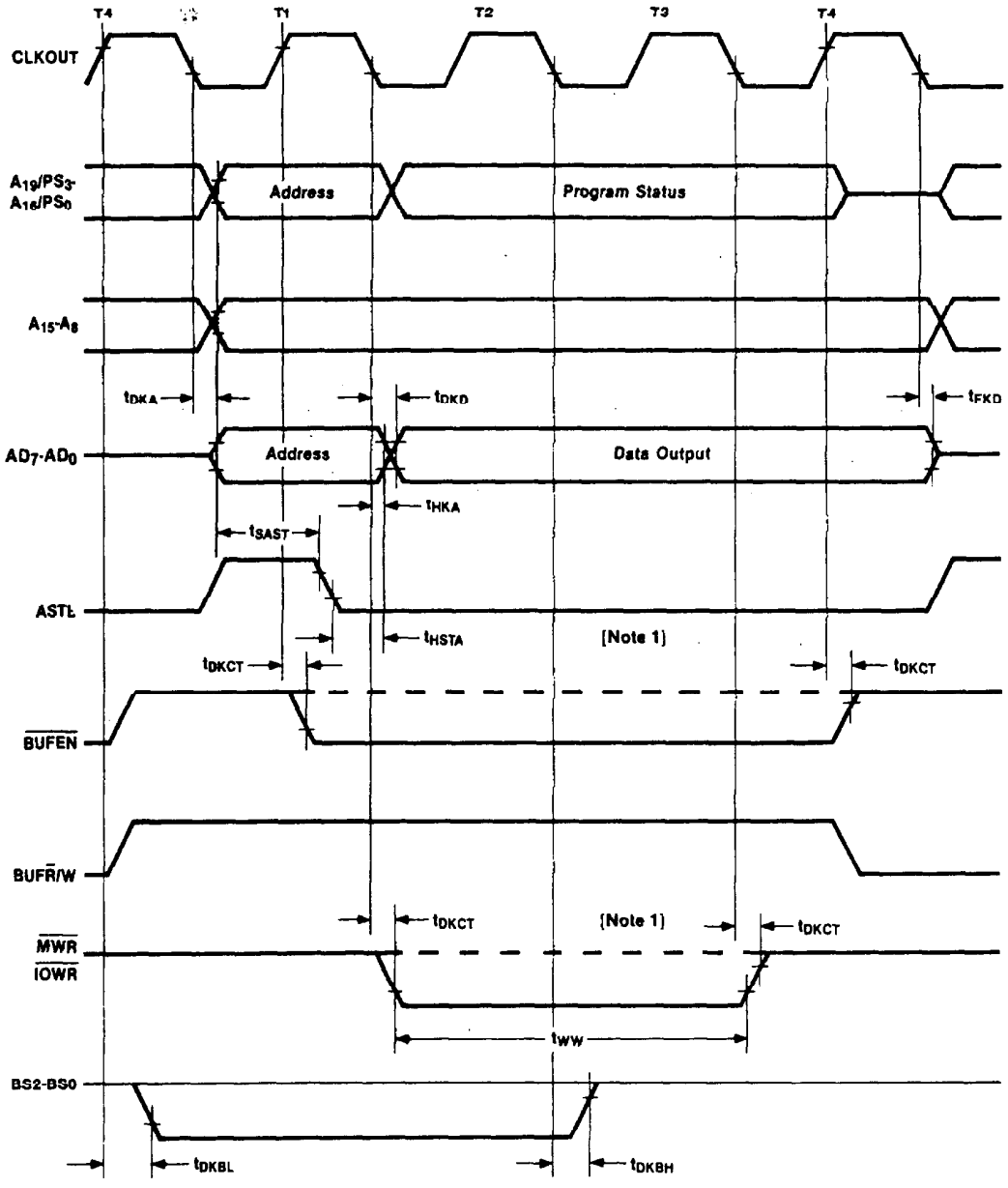


Note:
[1] Except internal I/O accesses.

83-001848B

Timing Waveforms (cont)

Write Timing

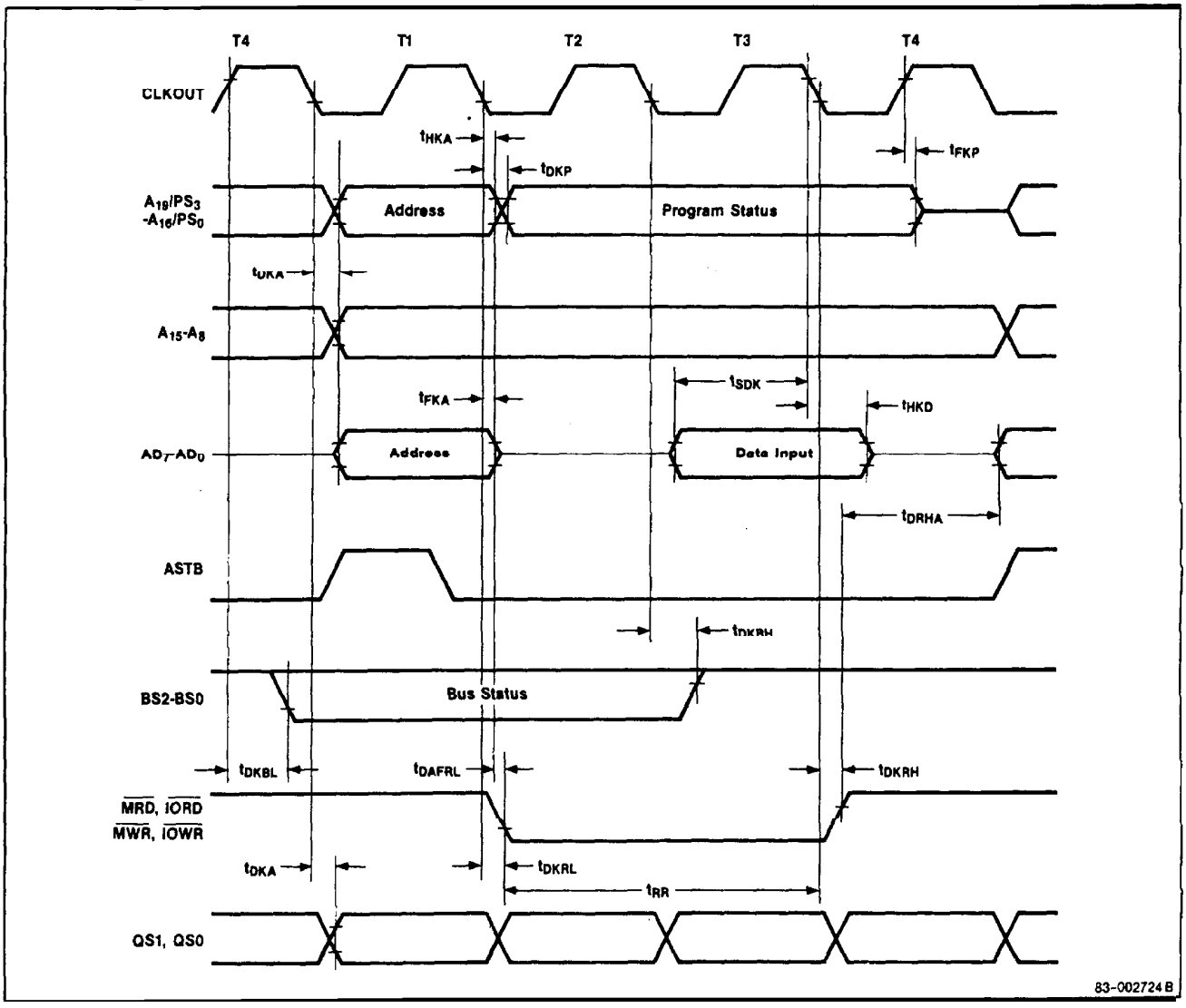


Note:
[1] Except internal I/O accesses.

83-001846B

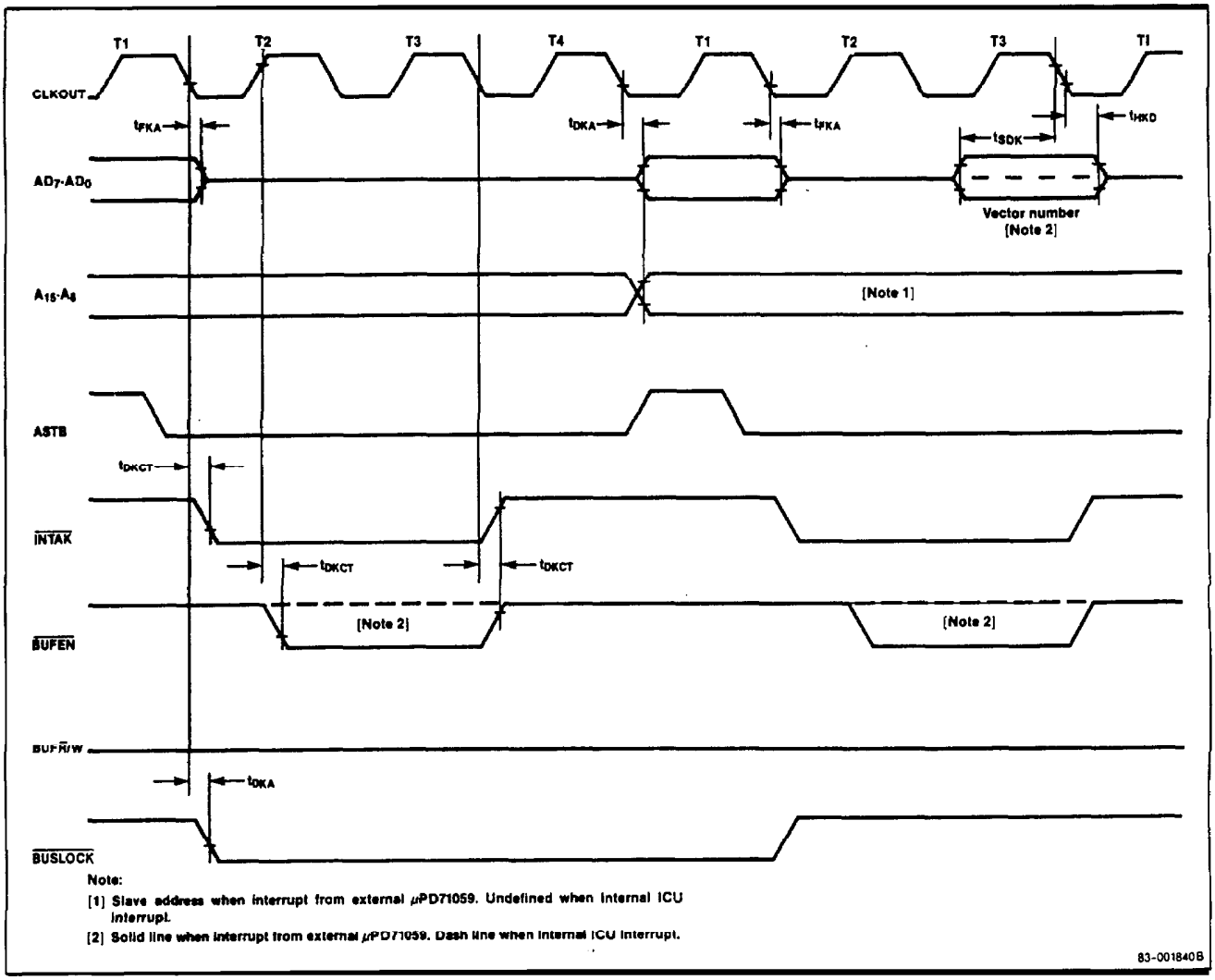
Timing Waveforms (cont)

Status Timing



Timing Waveforms (cont)

Interrupt Acknowledge Timing



Note:

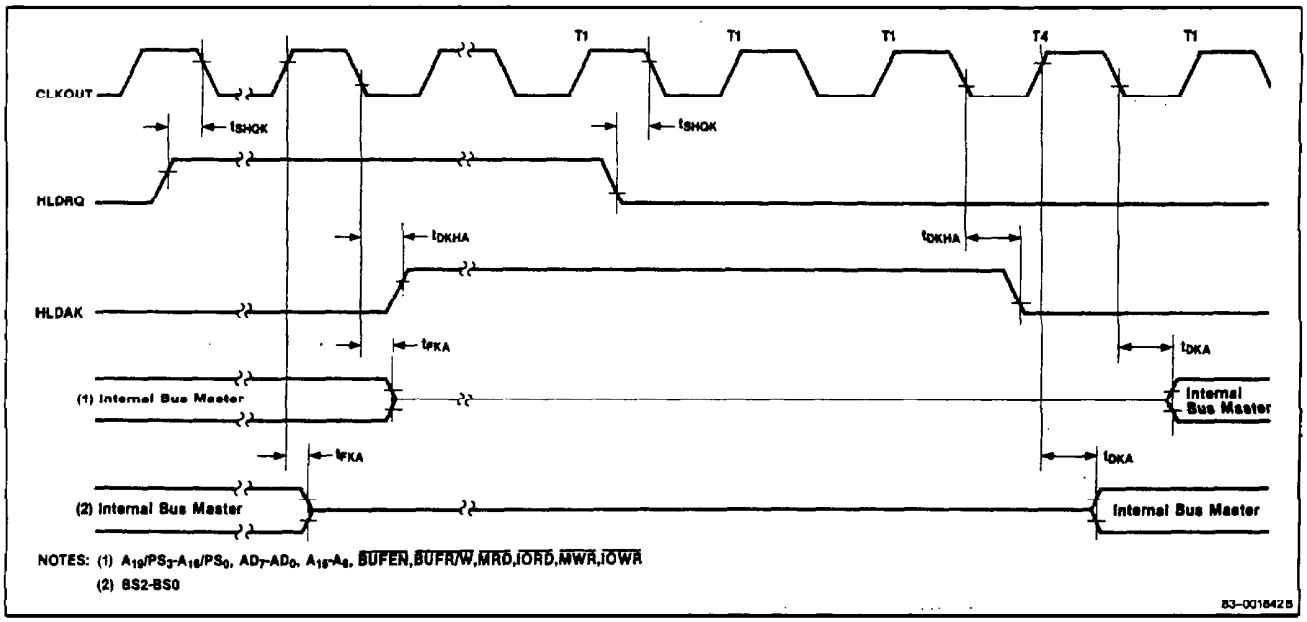
[1] Slave address when interrupt from external μPD71059. Undefined when internal ICU interrupt.

[2] Solid line when interrupt from external μPD71059. Dash line when internal ICU interrupt.

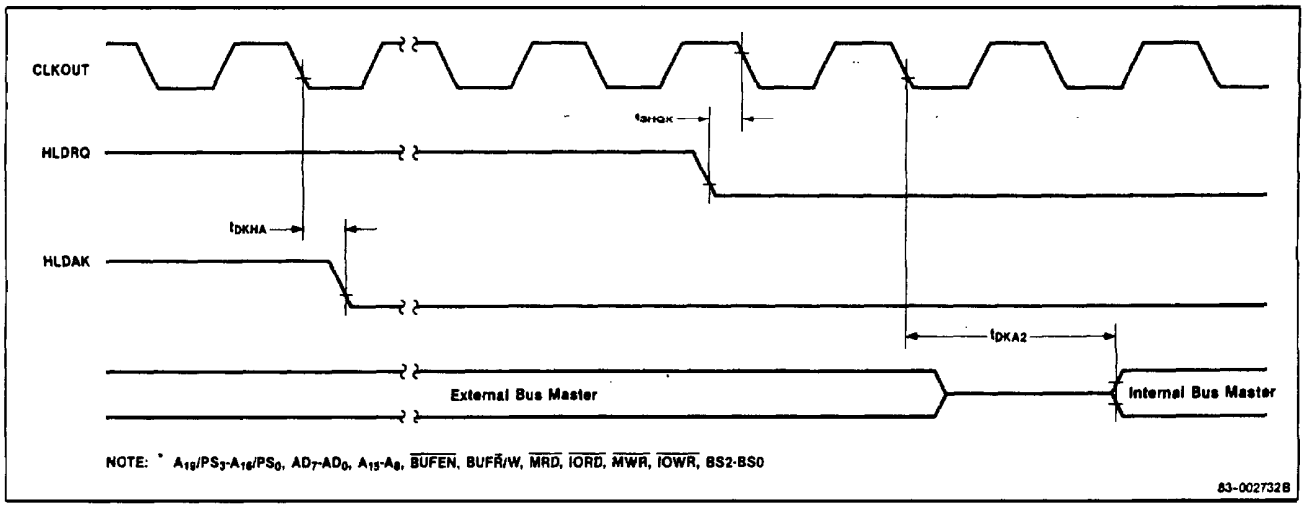
83-001840B

Timing Waveforms (cont)

Timing, Normal Operation



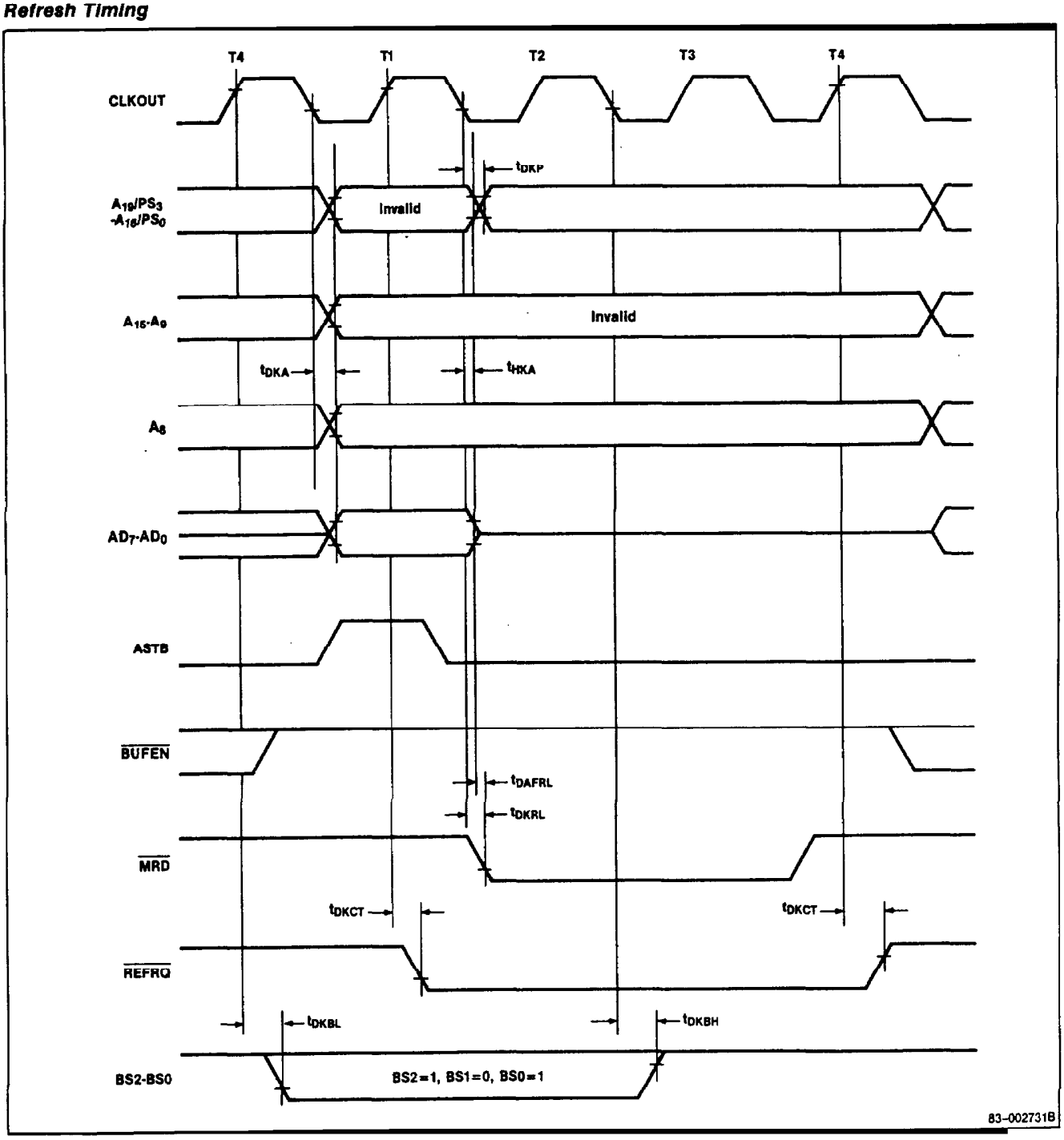
Timing, Bus Wait



3

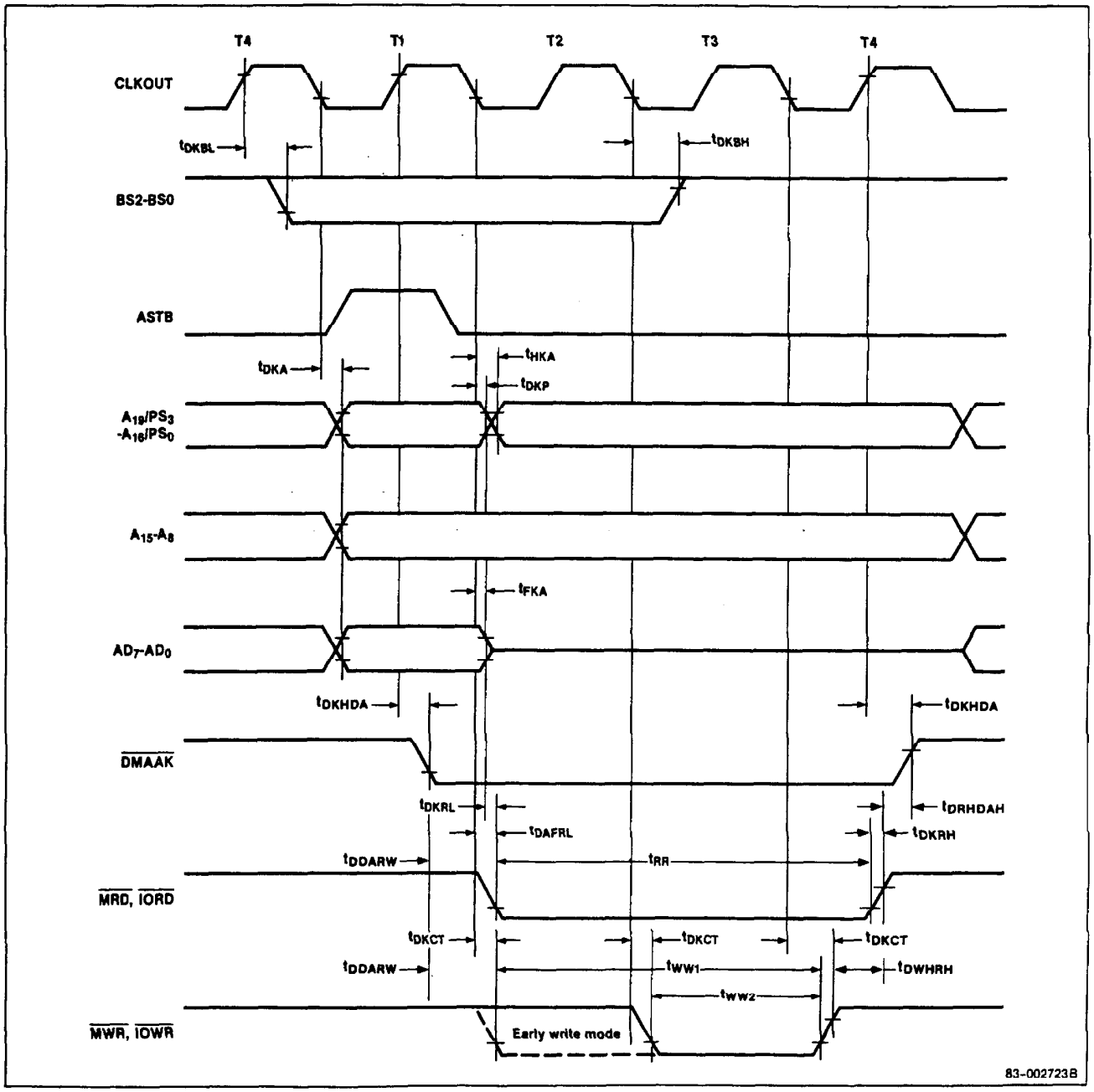
Timing Waveforms (cont)

Refresh Timing



Timing Waveforms (cont)

DMAU, DMA Transfer Timing

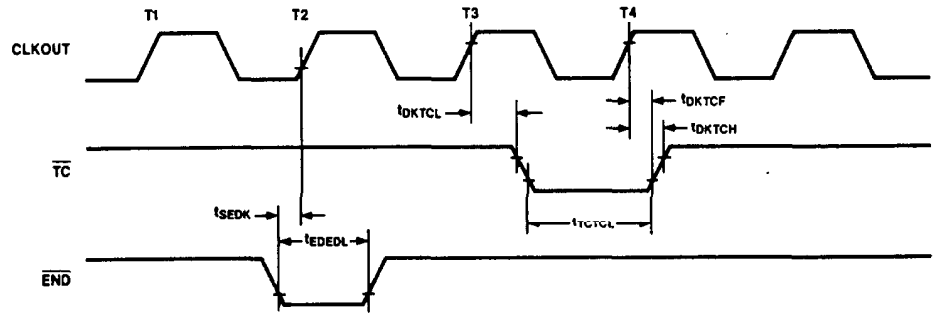


3

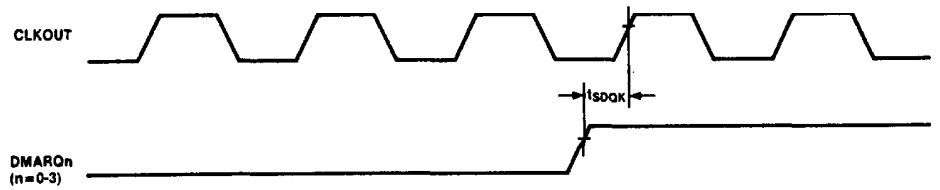
Timing Waveforms (cont)

DMA Timing

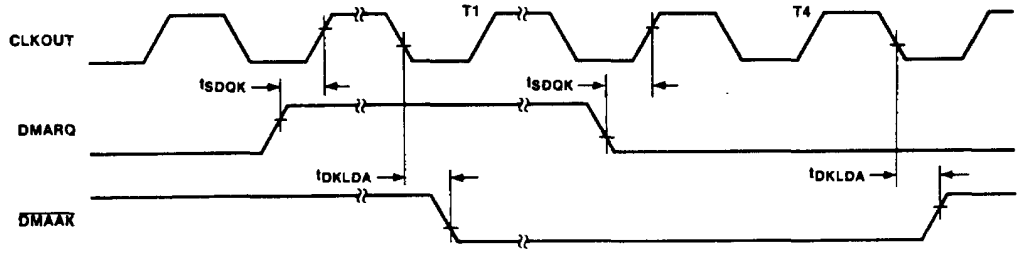
$\overline{END}$/$\overline{TC}$ Timing



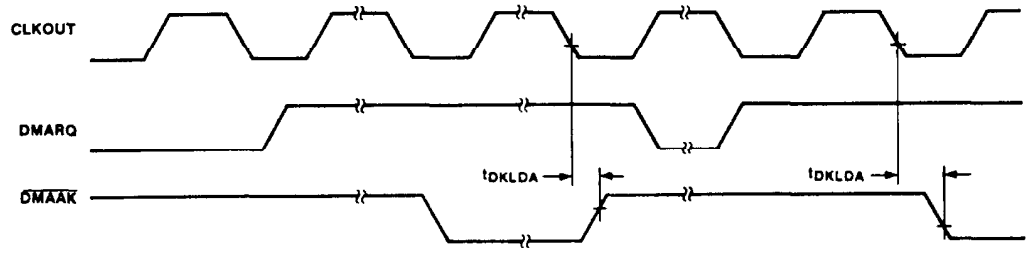
DMA Request Timing



Cascade Mode, Normal Operation



Cascade Mode, Refresh Cycle Insertion



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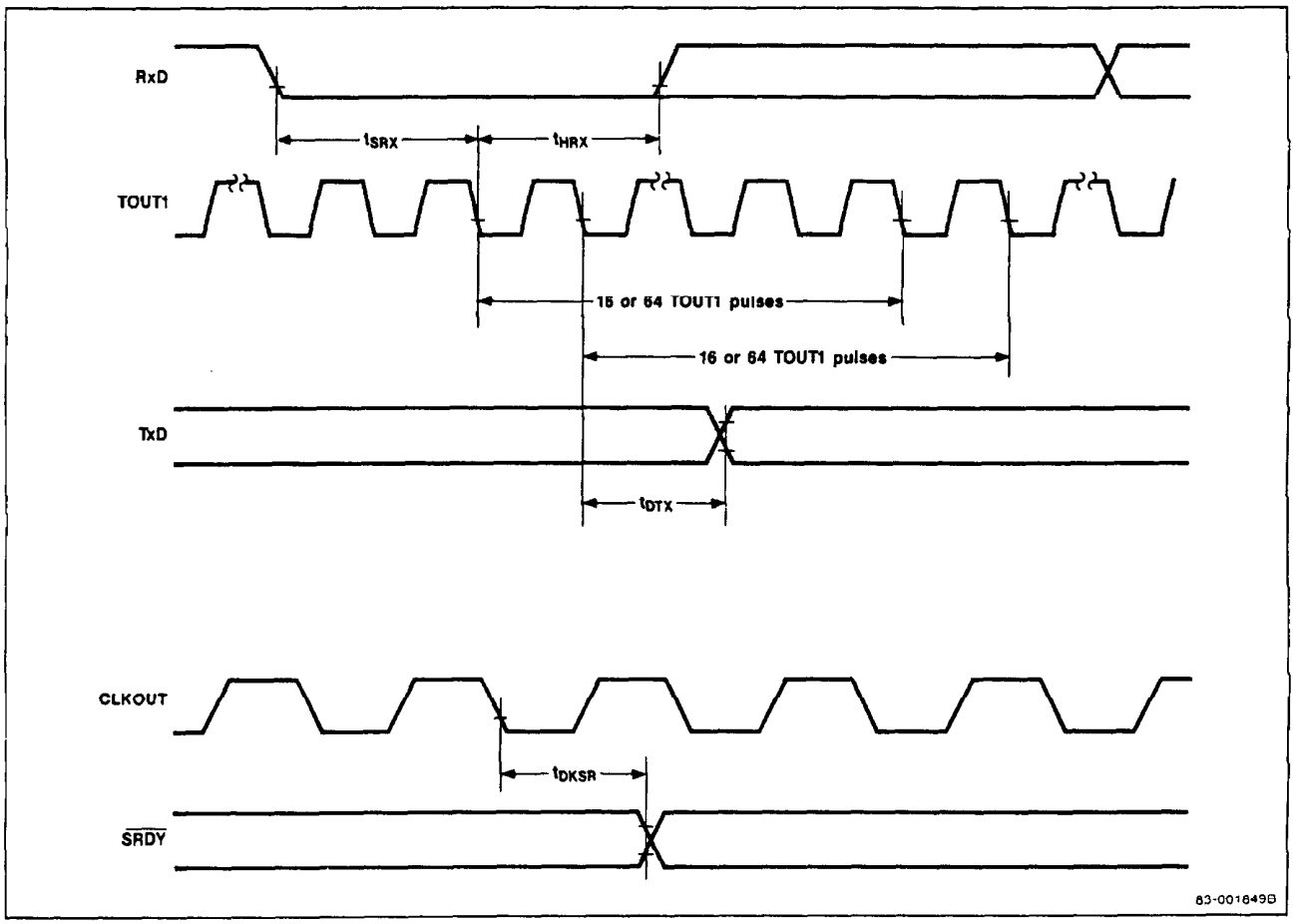
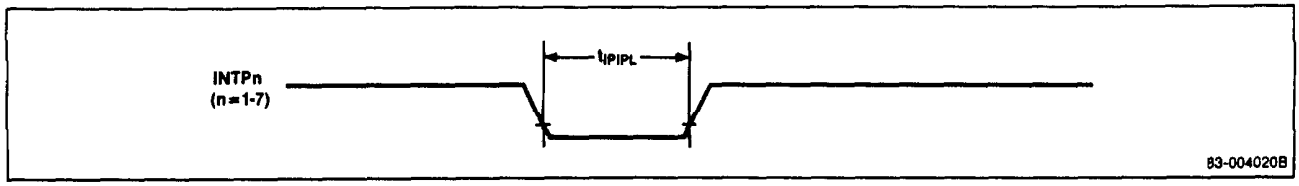
Timing Waveforms (cont)

SCU Timing

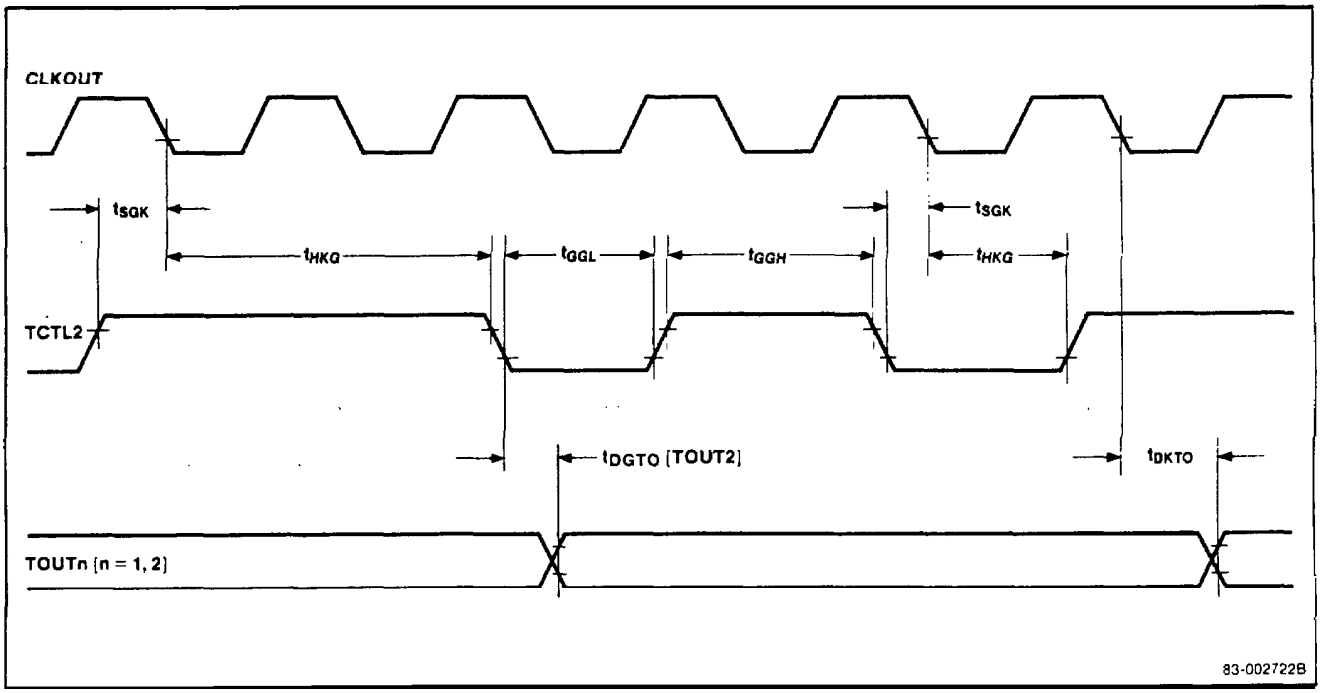


ICU Timing

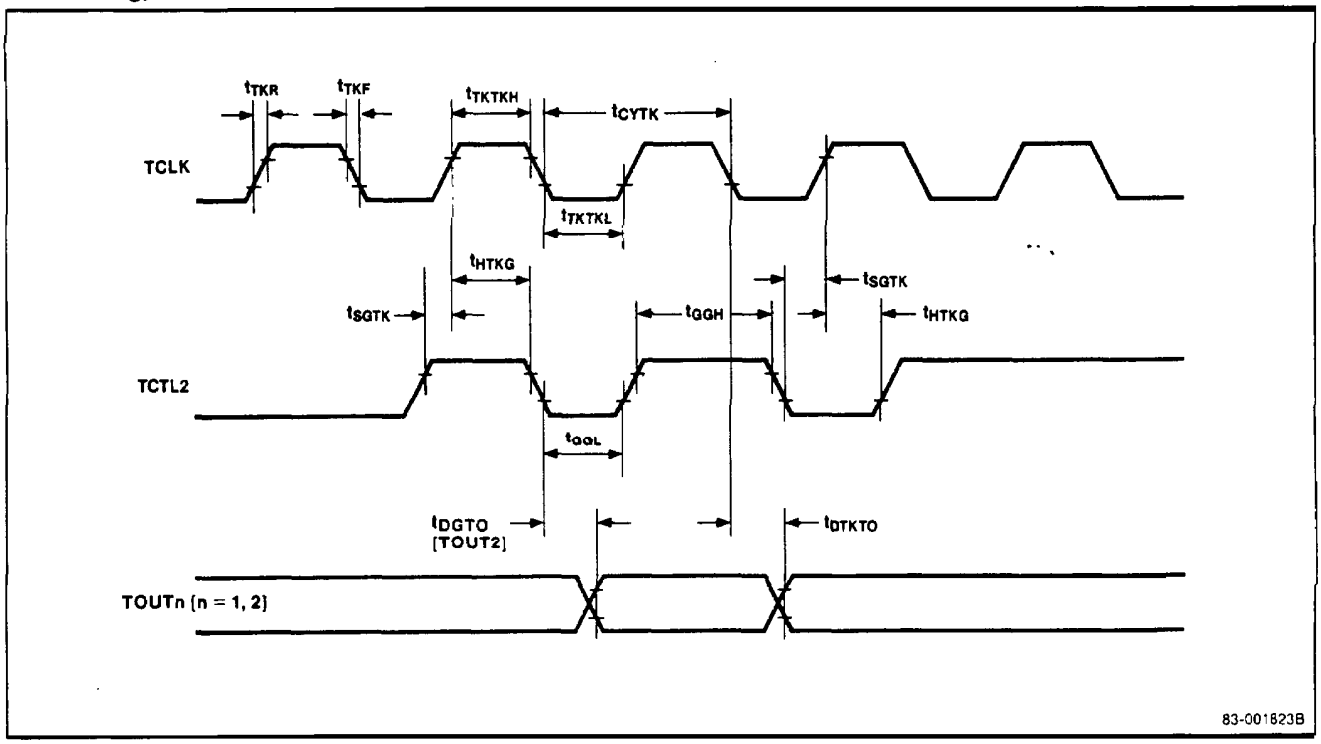


Timing Waveforms (cont)

TCU, Internal Clock Source



TCU Timing, TCLK Source



Functional Description

Refer to the μPD70208 block diagram for an overview of the ten major functional blocks listed below.

- Central processing unit (CPU)
- Clock generator (CG)
- Bus interface unit (BIU)
- Bus arbitration unit (BAU)
- Refresh control unit (RCU)
- Wait control unit (WCU)
- Timer/counter unit (TCU)
- Serial control unit (SCU)
- Interrupt control unit (ICU)
- DMA control unit (DMAU)

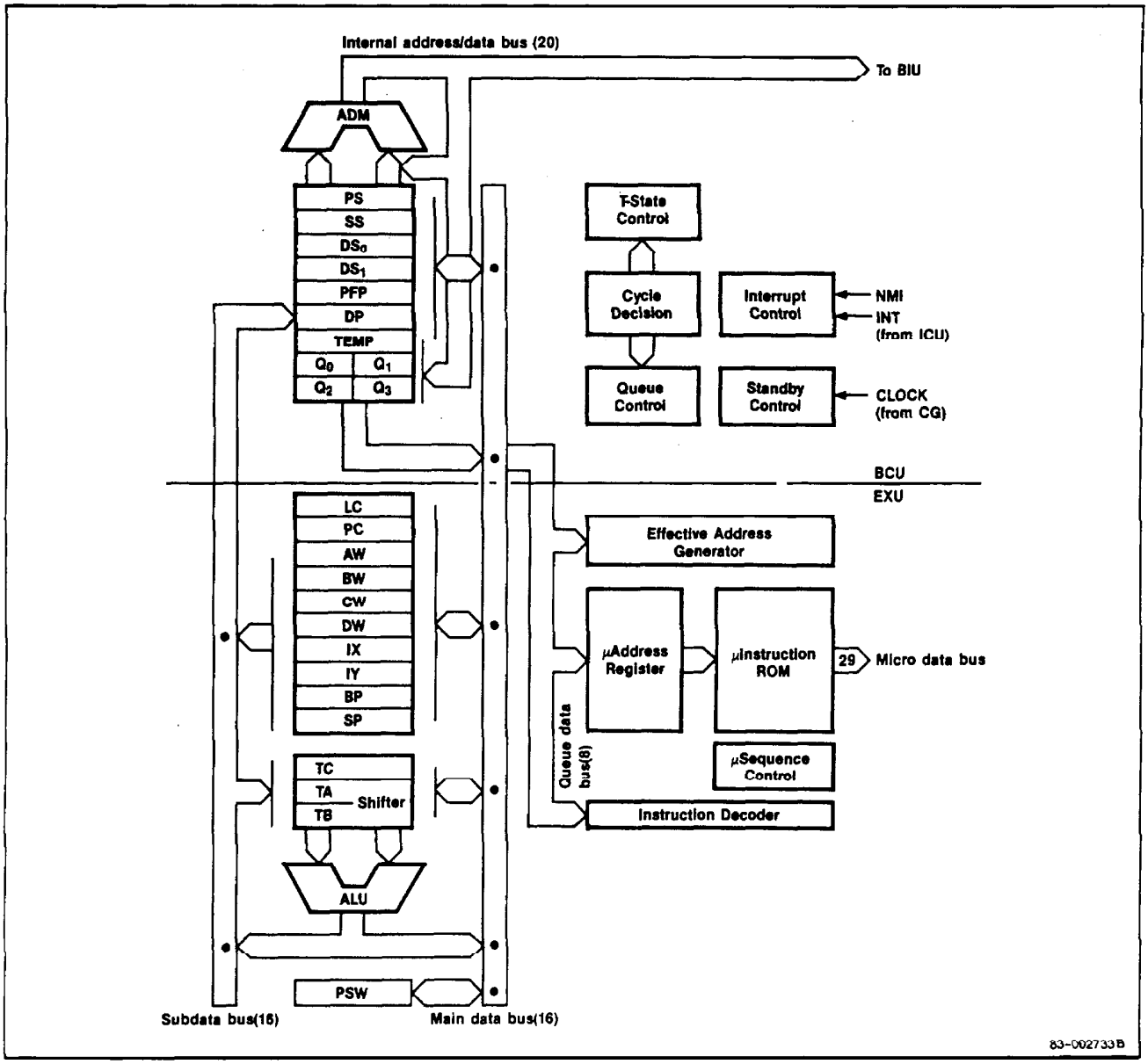
Central Processing Unit

The μPD70208 CPU functions similarly to the CPU of the μPD70108 CMOS microprocessor. However, because the μPD70208 has internal peripheral devices, its bus architecture has been modified to permit sharing the bus with internal peripherals. The μPD70208 CPU is object code compatible with both the μPD70108/μPD70116 and the μPD8086/μPD8088 microprocessors.

Figure 1 is the μPD70208 CPU block diagram. A listing of the μPD70208 instruction set is at the end of this data sheet.

3

Figure 1. μPD70208 CPU Block Diagram



Register Configuration

Program Counter [PC]. The program counter is a 16-bit binary counter that contains the program segment offset of the next instruction to be executed. The PC is incremented each time the microprogram fetches an instruction from the instruction queue. The contents of the PC are replaced whenever a branch, call, return, or break instruction is executed and during interrupt processing. At this time, the contents of the PC are the same as the prefetch pointer (PFP).

Prefetch Pointer [PFP]. The prefetch pointer is a 16-bit binary counter that contains the program segment offset of the next instruction to be fetched for the instruction queue. Because instruction queue prefetch is independent of instruction execution, the contents of the PFP and PC are not always identical. The PFP is updated each time the bus interface unit (BIU) fetches an instruction for the instruction queue. The contents of the PFP are replaced whenever a branch, call, return or break instruction is executed and during interrupt processing. At this time, the contents of the PFP and PC are the same.

Segment Registers [PS, SS, DS_0, DS_1]. The μPD70208 memory address space is divided into 64K-byte logical segments. A memory address is determined by the sum of a 20-bit base address (obtained from a segment register) and a 16-bit offset known as the effective address (EA). I/O address space is not segmented and no segment register is used. The four segment registers are program segment (PS), stack segment (SS), data segment 0 (DS_0), and data segment 1 (DS_1). The following table lists their offsets and overrides.

Default Segment Register	Offset	Override
PS	PFP register	Invalid
SS	SP register	Invalid
SS	Effective address (BP-based)	PS, DS_0, DS_1
DS_0	Effective address (non BP-based)	PS, SS, DS_1
DS_0	IX register (1)	PS, SS, DS_1
DS_1	IY register (2)	Invalid

Note:

(1) Includes source block transfer, output, BCD string, and bit field extraction.

(2) Includes destination block transfer, input, BCD string, and bit field insertion.

General-Purpose Registers. The μPD70208 CPU contains four 16-bit general-purpose registers (AW, BW, CW, DW), each of which can be used as a pair of 8-bit registers by dividing into upper and lower bytes (AH, AL, BH, BL, CH, CL, DH, DL). General-purpose registers may also be specified implicitly in an instruction. The implicit assignments are:

- AW — Word multiplication/division, word I/O, data conversion
- AL — Byte multiplication/division, byte I/O, BCD rotation, data conversion, translation
- AH — Byte multiplication/division
- BW — Translation
- CW — Loop control, repeat prefix
- CL — Shift/rotate bit counts, BCD operations
- DW — Word multiplication/division, indirect I/O addressing

Pointer [SP, BP] and Index Registers [IX, IY]. These registers serve as base pointers or index registers when accessing memory using one of the base, indexed, or base indexed addressing modes. Pointer and index registers can also be used as operands for word data transfer, arithmetic, and logical instructions. These registers are implicitly selected by certain instructions as follows.

- SP — Stack operations, interrupts
- IX — Source block transfer, BCD string operations, bit field extraction
- IY — Destination block transfer, BCD string operations, bit field insertion

Program Status Word [PSW]

The program status word consists of six status flags and four control flags.

Status Flags

- V (Overflow)
- S (Sign)
- Z (Zero)
- AC (Auxiliary Carry)
- P (Parity)
- CY (Carry)

Control Flags

- MD (Mode)
- DIR (Direction)
- IE (Interrupt Enable)
- BRK (Break)

When pushed onto the stack, the word image of the PSW is as follows:

15							8
MD	1	1	1	V	DIR	IE	BRK

7							0
S	Z	0	AC	0	P	1	CY

The status flags are set and cleared automatically depending upon the result of the previous instruction execution. Instructions are provided to set, clear, and complement certain status and control flags. Other flags can be manipulated by using the POP PSW instruction.

Between execution of the BRKEM and RETEM instructions, the native mode RETI and POP PSW instructions can modify the MD bit. Care must be exercised by emulation mode programs to prevent inadvertent alteration of this bit.

CPU Architectural Features

The major architectural features of the μPD70208 CPU are:

- Dual data buses
- Effective address generator
- Loop counter
- PC and PFP

Dual Data Buses. To increase performance, dual data buses (figure 2) have been employed in the CPU to fetch operands in parallel and avoid the bottleneck of a single bus. For two-operand instructions and effective address calculations, the dual data bus approach is 30 percent faster than single-bus systems.

Effective Address Generator. Effective address (EA) calculation requires only two clocks regardless of the addressing mode complexity due to the hardware effective address generator (figure 3). When compared with microprogrammed methods, the hardware approach saves between 3 and 10 clock cycles during effective address calculation.

Figure 2. Dual Data Buses

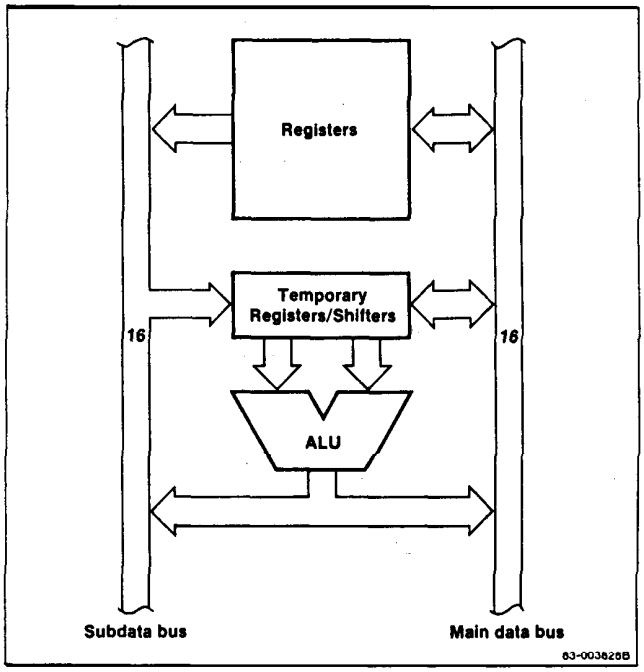
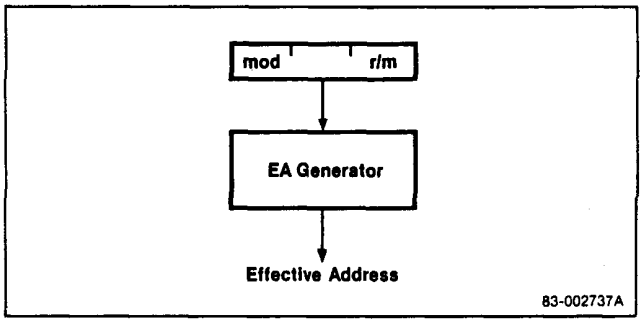


Figure 3. Effective Address Generator



Loop Counter and Shifters. A dedicated loop counter is used to count the iterations of block transfer and multiple shift instructions. This logic offers a significant performance advantage over architectures that control block transfers and multiple shifts using microprogramming. Dedicated shift registers also speed up the execution of the multiply and divide instructions. Compared with microprogrammed methods, multiply and divide instructions execute approximately four times faster.

3

Program Counter and Prefetch Pointer. The functions of instruction execution and queue prefetch are decoupled in the μPD70208. By avoiding a single-instruction pointer and providing separate PC and PFP registers, the execution time of control transfers and the interrupt response latency can be minimized. Several clocks are saved by avoiding the need to readjust an instruction pointer to account for prefetching before computing the new destination address.

Enhanced Instruction Set

In addition to the μPD8086/88 instruction set, the μPD70208 has added the following enhanced instructions.

Instruction	Function
PUSH imm	Push immediate data onto stack
PUSH R	Push all general registers onto stack
POP R	Pop all general registers from stack
MUL imm	Multiply register/memory by immediate data
SHL imm8	Shift/rotate by immediate count
SHR imm8	
SHRA imm8	
ROL imm8	
ROR imm8	
ROLC imm8	
RORC imm8	
CHKIND	Check array index
INM	Input multiple
OUTM	Output multiple
PREPARE	Prepare new stack frame
DISPOSE	Dispose current stack frame

Unique Instruction Set

In addition to the μPD70208 enhanced instruction set, the following unique instructions are supported.

Instruction	Function
INS	Insert bit field
EXT	Extract bit field
ADD4S	BCD string addition
SUB4S	BCD string subtraction
CMP4S	BCD string comparison
ROL4	Rotate BCD digit left
ROR4	Rotate BCD digit right
TEST1	Test bit
SET1	Set bit
CLR1	Clear bit
NOT1	Complement bit
REPC	Repeat while carry set
REPNC	Repeat while carry cleared
FPO2	Floating point operation 2

Bit Fields. Bit fields are data structures that range in length from 1 to 16 bits. Two separate operations on bit fields, insertion and extraction, with no restrictions on the position of the bit field in memory are supported. Separate segment, byte offset, and bit offset registers are used for bit field insertion and extraction. Because of their power and flexibility, these instructions are highly effective for graphics, high-level languages, and data packing/unpacking applications.

Insert bit field (INS) copies the bit field of specified length (0 = 1 bit, 15 = 16 bits) from the AW register to the bit field addressed by DS1:IY:reg8 (figure 4). The bit field length can be located in any byte register or supplied as an immediate value. The value in reg8 is a bit field offset. A content of 0 selects bit 0 and 15 selects bit 15 of the word DS0:IX points to. Following execution, the IY and bit offset register are updated to point to the start of the next bit field.

Bit field extraction (EXT) copies the bit field of specified length (0 = 1 bit, 15 = 16 bits) from the bit field addressed by DS0:IX:reg8 to the AW register (figure 5). If the bit field is less than 16 bits, it is right justified with a zero fill. The bit field length can be located in any byte register or supplied as immediate data. The value in reg8 is a bit field offset. A content of 0 selects bit 0 and 15 selects bit 15 of the word DS0:IX points to. Following execution, the IX and bit offset register are updated to point to the start of the next bit field.

Packed BCD Strings. These instructions are provided to efficiently manipulate packed BCD data as strings (length from 1 to 254 digits) or as a byte data type with a single instruction.

BCD string arithmetic is supported by the ADD4S, SUB4S, and CMP4S instructions. These instructions allow the source string (addressed by DS0:IX) and the destination string (addressed by DS1:IY) to be manipulated with a single instruction. When the number of BCD digits is even, the Z and CY flags are set according to the result of the operation. If the number of digits is odd, the Z flag will not be correctly set unless the upper 4 bits of the result are zero. The CY flag will not be correctly set unless there is a carry out of the upper 4 bits of the result.

The two BCD rotate instructions (ROR4, ROL4) perform rotation of a single BCD digit in the lower half of the AL register through the register or memory operand.

Bit Manipulation. Four bit manipulation instructions have been added to the μPD70208 instruction set. The ability to test, set, clear, or complement a single bit in a register or memory operand increases code readability as well as performance over the logical operations traditionally used to manipulate bit data.

Figure 4. Bit Field Insertion

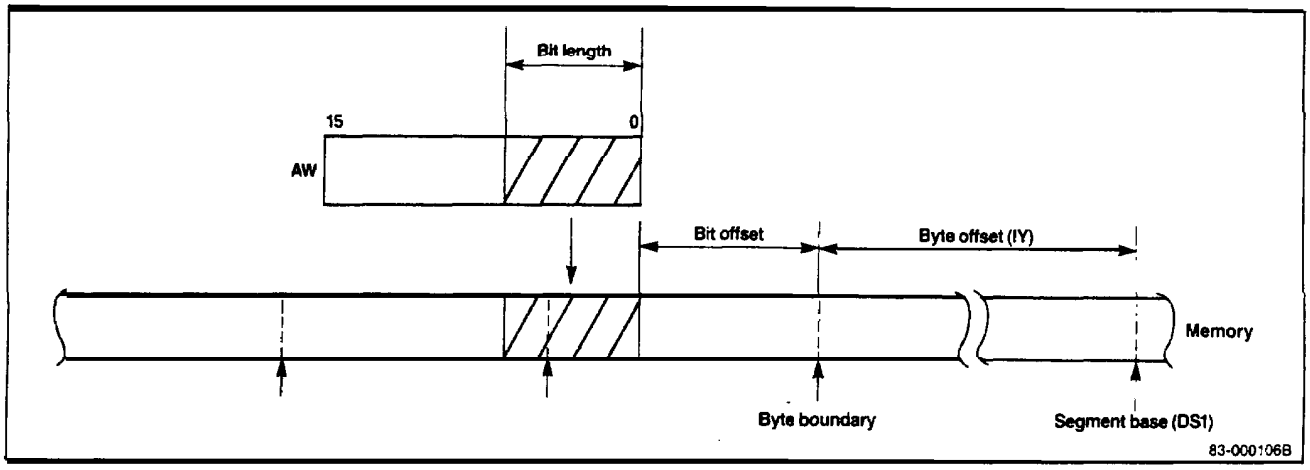
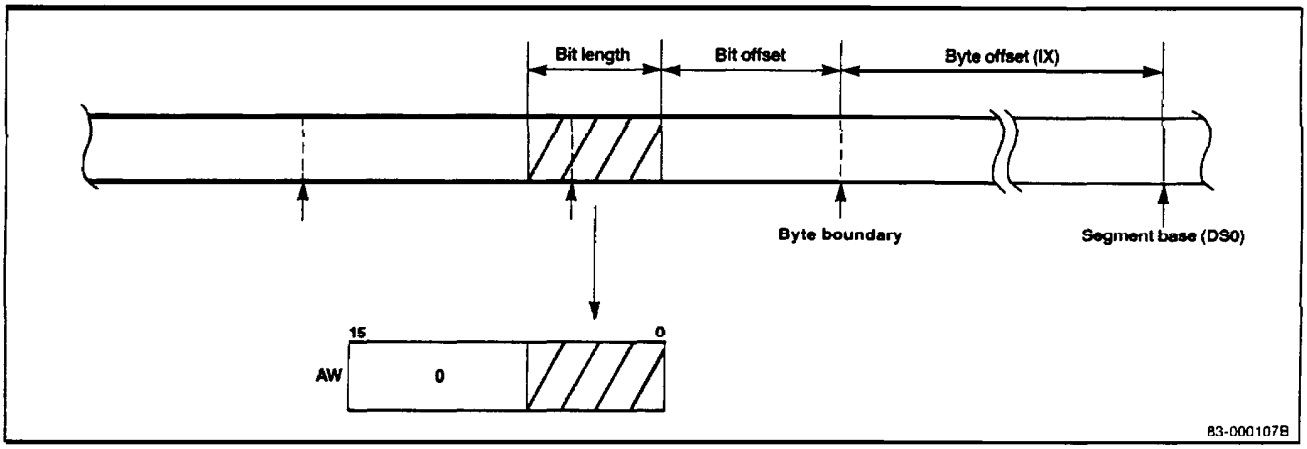


Figure 5. Bit Field Extraction



Repeat Prefixes. Two repeat prefixes (REPC, REPNC) allow conditional block transfer instructions to use the state of the CY flag as a terminating condition. The use of these prefixes allows inequalities to be used when working on ordered data, increasing the performance of searching and sorting algorithms.

Floating Point Operation Instructions. Two floating point operation (FPO) instruction types are recognized by the μPD70208 CPU. These instructions are detected by the CPU, which performs any auxiliary processing such as effective address calculation and the initial bus cycle if specified by the instruction. It is the responsibility of the external coprocessor to latch the address information and data (if a read cycle) from the bus and complete the execution of the instruction.

8080 Emulation Mode. The μPD70208 CPU can operate in either of two modes; see figure 6. Native mode allows the execution of the μPD8086/88, enhanced and unique instructions. The other operating mode is 8080 emulation mode, which allows the entire μPD8080AF instruction set to be executed. A mode (MD) flag is provided to distinguish between the two operating modes. Native mode is active when MD is 1 and 8080 emulation mode is active when MD is 0.

Two instructions are provided to switch from native to 8080 emulation mode and return back. Break for emulation (BRKEM) operates similarly to a BRK instruction, except that after the PSW has been pushed on the native mode stack, the MD flag is cleared.

During 8080 emulation mode, the registers and flags of the 8080 are mapped onto the native mode registers and flags as shown below. Note that PS, SS, DS_0, DS_1, IX, IY, AH, and the upper half of the PSW registers are inaccessible to 8080 programs.

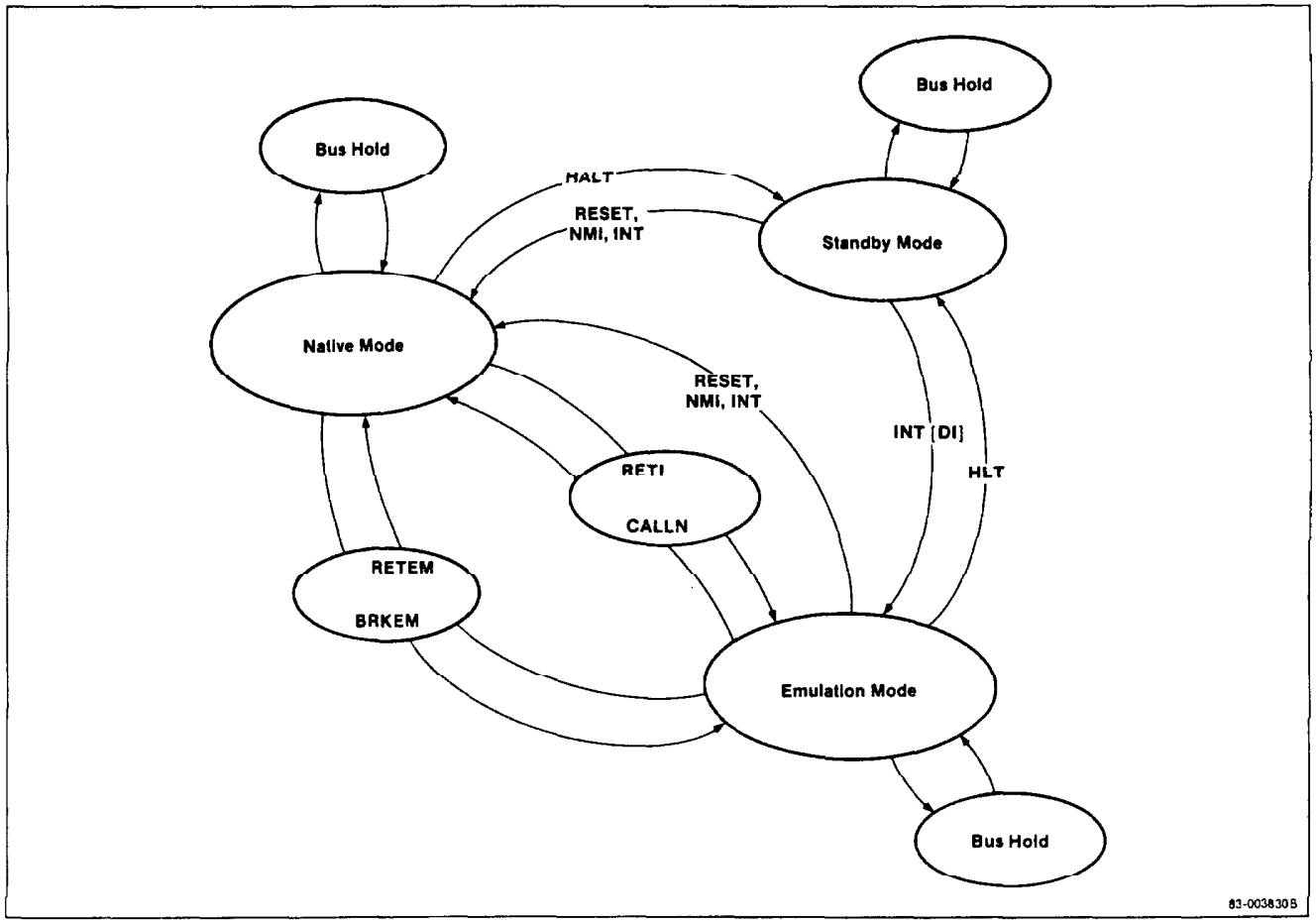
	μPD8080AF	μPD70208
Registers	A	AL
	B	CH
	C	CL
	D	DH
	E	DL
	H	BH
	L	BL
	SP	BP
	PC	PC
Flags	C	CY
	Z	Z
	S	S
	P	P
	AC	AC

During 8080 emulation mode, the BP register functions as the 8080 stack pointer. The use of separate stack pointers prevents inadvertent damage to the native stack pointer by emulation mode programs.

The 8080 emulation mode PC is combined with the PS register to form the 20-bit physical address. All emulation mode data references use DS0 as the segment register. For compatibility with older 8080 software these registers must be equal. By using different segment register contents, separate 64K-byte code and data spaces are possible.

Either an NMI or maskable interrupt will cause the 8080 emulation mode to be suspended. The CPU pushes the PS, PC, and PSW registers on the native mode stack, sets the MD bit (indicating native mode), and enters the specified interrupt handler. When the return from *interrupt (RETI) instruction is executed, the PS, PC,* and PSW (containing MD=0) are popped from the native stack and execution in 8080 emulation mode continues. Reset will also force a return to native mode.

Figure 6. μPD70208 Modes



The 8080 emulation mode programs also have the capability to invoke native mode interrupt handlers by means of the call native (CALLN) instruction. This instruction operates the same as the BRK instruction except that the saved PSW indicates 8080 emulation mode.

To exit 8080 emulation mode, the return from emulation (RETEM) instruction pops the PS, PC, and PSW from the native mode stack and execution continues with the instruction following the BRKEM instruction. Nesting of 8080 emulation modes is prohibited.

Interrupt Operation

The μPD70208 supports a number of external interrupts and software exceptions. External interrupts are events asynchronous to program execution. On the other hand, exceptions always occur as a result of program execution.

The two types of external interrupts are:

- Nonmaskable interrupt (NMI)
- Maskable interrupt (INT)

The six software exceptions are:

- Divide error (DIV, DIVU instructions)
- Array bound error (CHKIND instruction)
- Break on overflow (BRKV instruction)
- Break (BRK, BRK3 instructions)
- Single step (BRK bit in PSW set)
- Mode switch (BRKEM, CALLN instructions)

Interrupt vectors are determined automatically for exceptions and the NMI interrupt or supplied by hardware for maskable interrupts. The 256 interrupt vectors are stored in a table (figure 7) located at address 00000H. Vectors 0 to 5 are predetermined and vectors 6 to 31 are reserved. Interrupt vectors 32 to 255 are available for use by application software.

Each vector is made up of two words. The word located at the lower address contains the new PC for the interrupt handler. The word at the next-higher address is the new PS value for the interrupt handler. These must be initialized by software at the start of a program.

Standby Mode

The μPD70208 CPU has a low-power standby mode, which can dramatically reduce power consumption during idle periods. Standby mode is entered by simply executing a native or 8080 emulation HALT instruction; no external hardware is required. All other peripherals such as the timer/counter unit, refresh control unit, and DMA control unit continue to operate as programmed.

During standby mode, the clock is distributed only to the circuits required to release the standby mode. When a RESET, NMI, or INT event is detected, the standby mode is released. Both NMI and unmaskable interrupts are processed before control returns to the instruction following the HALT. In the case of the INT input being masked, execution will begin with the instruction immediately following the HALT instruction without an intervening interrupt acknowledge bus cycle. When maskable interrupts are again enabled, the interrupt will be serviced.

Output signal states in the standby mode are listed below.

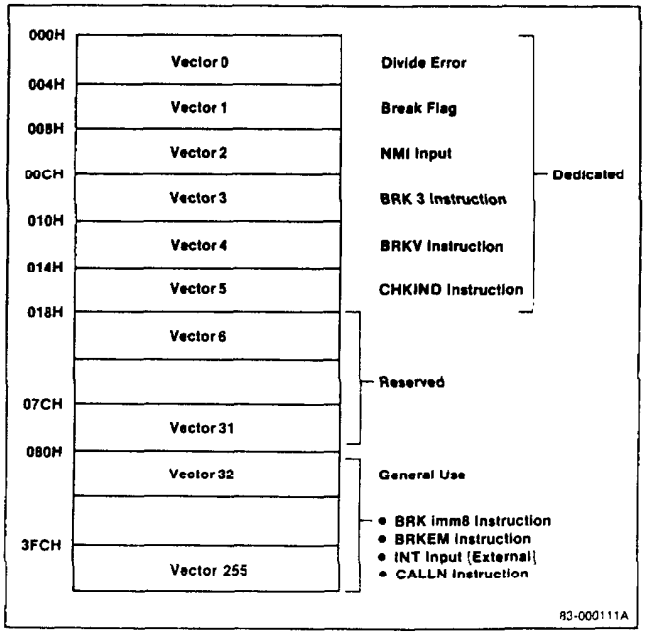
Output Signal	Status in Standby Mode
$\overline{INTAK}$, $\overline{BUFEN}$, $\overline{MRD}$, $\overline{MWR}$, $\overline{IOWR}$, $\overline{IORD}$	High level
BS_2-BS_0 (Note 2)	High level
QS_1-QS_0, ASTB	Low level
$\overline{BUSLOCK}$	High level (low level if the HALT instruction follows the BUSLOCK prefix)
$\overline{BUFR}$/W, A_{19}-A_{16}/PS_3-PS_0, A_{15}-A_8, AD_7-AD_0	High or low level

Note:

(1) Output pin states during refresh and DMA bus cycles will be as defined for those operations.

(2) Halt status is presented prior to entering the passive state.

Figure 7. Interrupt Vector Table



Clock Generator

The clock generator (CG) generates a clock signal half the frequency of a parallel-resonant, fundamental mode crystal connected to pins X1 and X2. Figure 8 shows the recommended circuit configuration. Capacitors C1 and C2 are required for frequency stability. Their values can be calculated from the load capacitance (CL) specified by the crystal manufacturer.

$$C1 = C2 = 2\,(CL - CS)$$

CS is any stray capacitance in parallel with the crystal, such as the μPD70208 input capacitance.

External clock sources (figure 9) are also accommodated by applying the external clock to the X1 pin and its complement to the X2 pin. The CG distributes the clock to the CLKOUT pin and to each functional block of the μPD70208. The generated clock signal has a 50-percent duty cycle.

Bus Interface Unit

The bus interface unit (BIU) controls the external address, data, and control buses for the three internal bus masters: CPU, DMA control unit (DMAU), and refresh control unit (RCU). The BIU is also responsible for synchronization of the $\overline{\text{RESET}}$ and READY inputs with the clock. The synchronized reset signal is used internally by the μPD70208 and provided externally at the RESOUT pin as a system-wide reset. The synchronized READY signal is combined with the output of the wait control unit (WCU) and is distributed internally to the CPU, DMAU, and RCU. Figure 10 shows the synchronization of $\overline{\text{RESET}}$ and READY.

Figure 8. Crystal Configuration

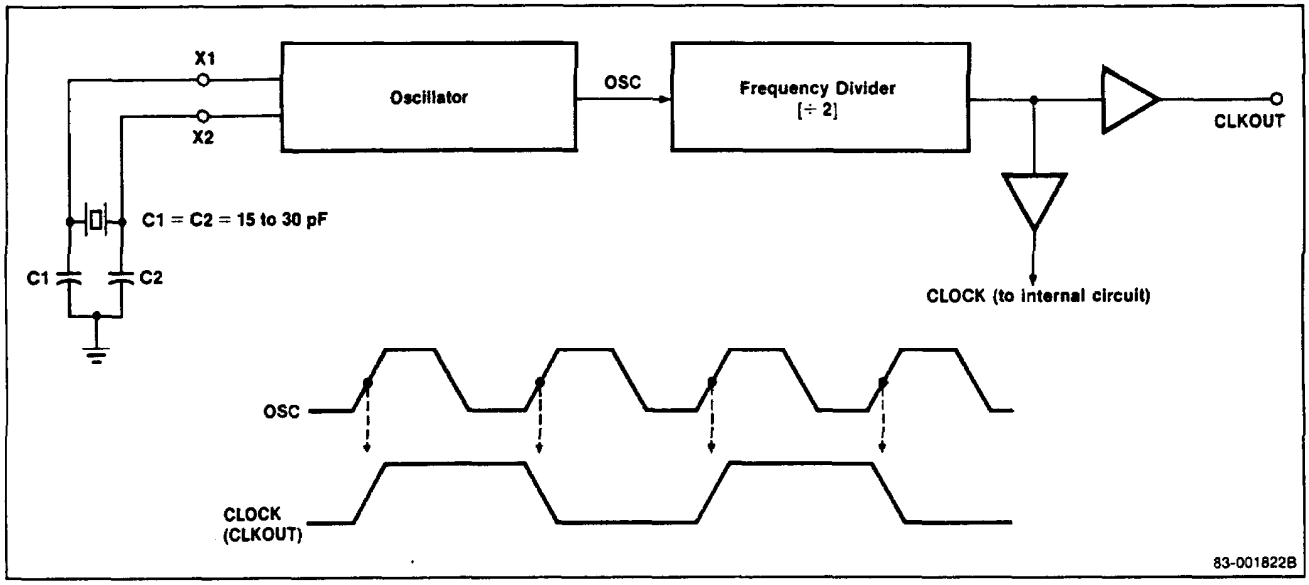


Figure 9. External Oscillator Configuration

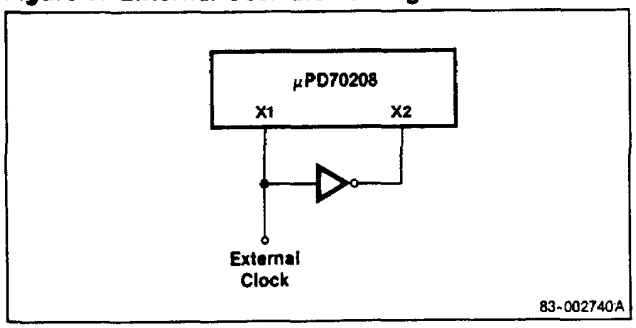
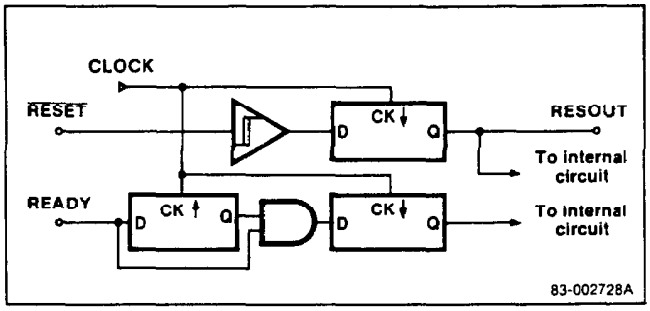


Figure 10. $\overline{\text{RESET}}$/READY Synchronization



Bus Arbitration Unit

The bus arbitration unit (BAU) arbitrates the local bus between the internal CPU, DMAU, and RCU bus requesters and an external bus master. The BAU bus priorities from the highest priority requester to the lowest are:

- RCU (Demand mode)
  DMAU
  HLDRQ
  CPU
  RCU (Normal mode)

Note that RCU requests the bus at either the highest or lowest priority depending on the status of the refresh request queue. Bus masters other than the CPU are prohibited from using the bus when the CPU is executing an instruction containing a BUSLOCK prefix. Therefore, caution should be exercised when using the BUSLOCK prefix with instructions having a long execution time.

If a bus master with higher priority than the current bus master requests the bus, the BAU inactivates the current bus master's acknowledge signal. When the BAU sees the bus request from the current master go inactive, the BAU gives control of the bus to the higher priority bus master. The BAU performs bus switching between internal bus masters without the introduction of idle bus cycles, enhancing system throughput.

System I/O Area

The I/O address space from addresses FF00H to FFFFH is reserved for use as the system I/O area. Located in this area are the 12 μPD70208 registers that determine the I/O addressing, enable/disable peripherals, and control pin multiplexing.

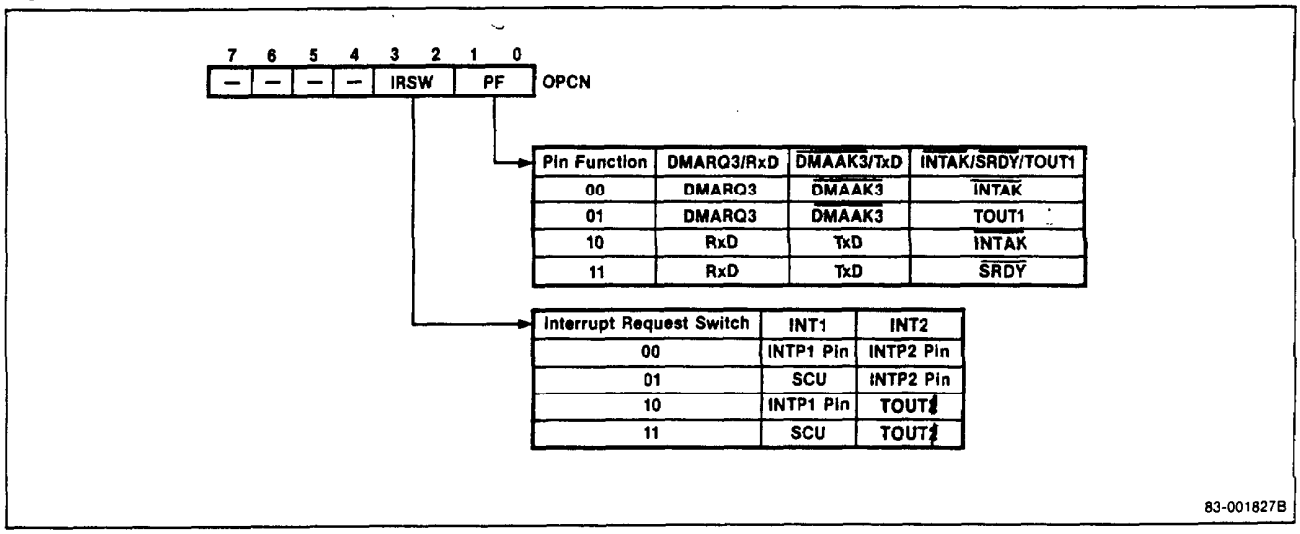
I/O Address	Register	Operation
FFFFH	Reserved	—
FFFEH	OPCN	Read/Write
FFFDH	OPSEL	Read/Write
FFFCH	OPHA	Read/Write
FFFBH	DULA	Read/Write
FFFAH	IULA	Read/Write
FFF9H	TULAL	Read/Write
FFF8H	SULA	Read/Write
FFF7H	Reserved	—
FFF6H	WCY2	Read/Write
FFF5H	WCY1	Read/Write
FFF4H	WMB	Read/Write
FFF3H	Reserved	—
FFF2H	RFC	Read/Write
FFF1H	Reserved	—
FFF0H	TCKS	Read/Write

On-Chip Peripheral Connection Register

The on-chip peripheral connection (OPCN) register controls multiplexing of the μPD70208 multiplexed pins. Figure 11 shows the format of the OPCN register. The interrupt request switch (IRSW) field controls multiplexing of ICU interrupt inputs INT1 and INT2. The output of an internal peripheral or an external interrupt source can be selected as the INT1 and INT2 inputs to the ICU.

The pin function (PF) field in the OPCN selects one of four possible states for the DMARQ3/RxD, $\overline{\text{DMAAK3}}$/TxD, and $\overline{\text{INTAK}}$/$\overline{\text{SRDY}}$/TOUT1 pins. Bit 0 of the

Figure 11. OPCN Register Format

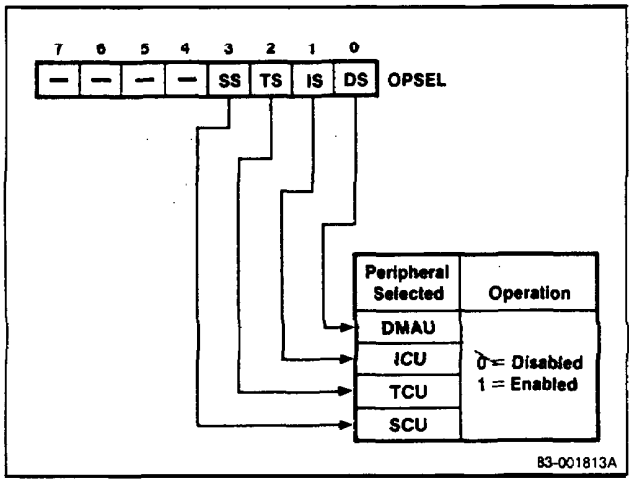


OPCN controls the function of the $\overline{INTAK}$/$\overline{SRDY}$/TOUT1 pin. If cleared, $\overline{INTAK}$ will appear on this output pin. If bit 0 is set, either TOUT1 or $\overline{SRDY}$ will appear at the output depending on the state of bit 1. If bit 1 is cleared, DMA channel 3 I/O signals will appear on the DMARQ3/RxD and $\overline{DMAAK3}$/TxD pins. If the SCU is to be used, bit 1 of the PF field must be set.

On-Chip Peripheral Selection Register

The on-chip peripheral selection (OPSEL) register is used to enable or disable the μPD70208 internal peripherals. Figure 12 shows the format of the OPSEL register. Any of the four (DMAU, TCU, ICU, SCU) peripherals can be independently enabled or disabled by setting or clearing the appropriate OPSEL bit.

Figure 12. OPSEL Register Format



Internal Peripheral Relocation Registers

The five internal peripheral relocation registers (figure 13) are used to fix the I/O addresses of the DMAU, ICU, TCU, and SCU. The on-chip peripheral high-address (OPHA) register is common to all four internal peripherals and fixes the high-order byte of the 16-bit I/O address. The individual DMAU low-address (DULA) register, ICU low-address (IULA) register, TCU low-address (TULA) register, and the SCU low-address (SULA) register select the low-order byte of the I/O addresses for the DMAU, ICU, TCU, and SCU peripherals.

The contents of the OPHA register are:

OPHA

7							0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

The formats for the individual internal peripheral registers appear below. Since address checking is not performed, do not overlap two peripheral I/O address spaces.

DULA

7							0
A_7	A_6	A_5	A_4	—	—	—	—

IULA

7							0
A_7	A_6	A_5	A_4	A_3	A_2	—	—

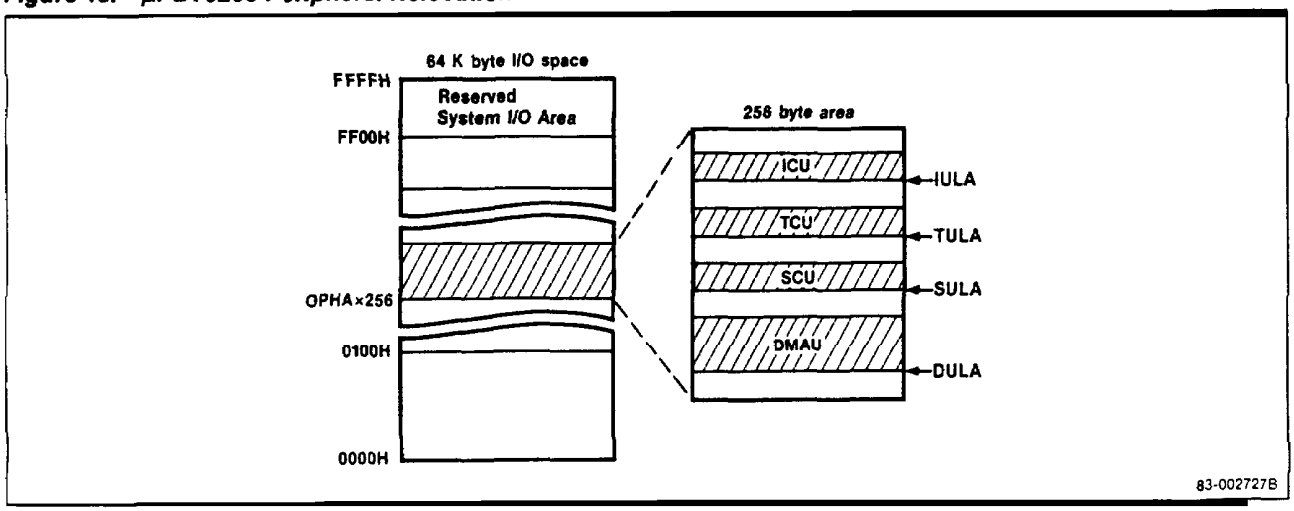
TULA

7							0
A_7	A_6	A_5	A_4	A_3	A_2	—	—

SULA

7							0
A_7	A_6	A_5	A_4	A_3	A_2	—	—

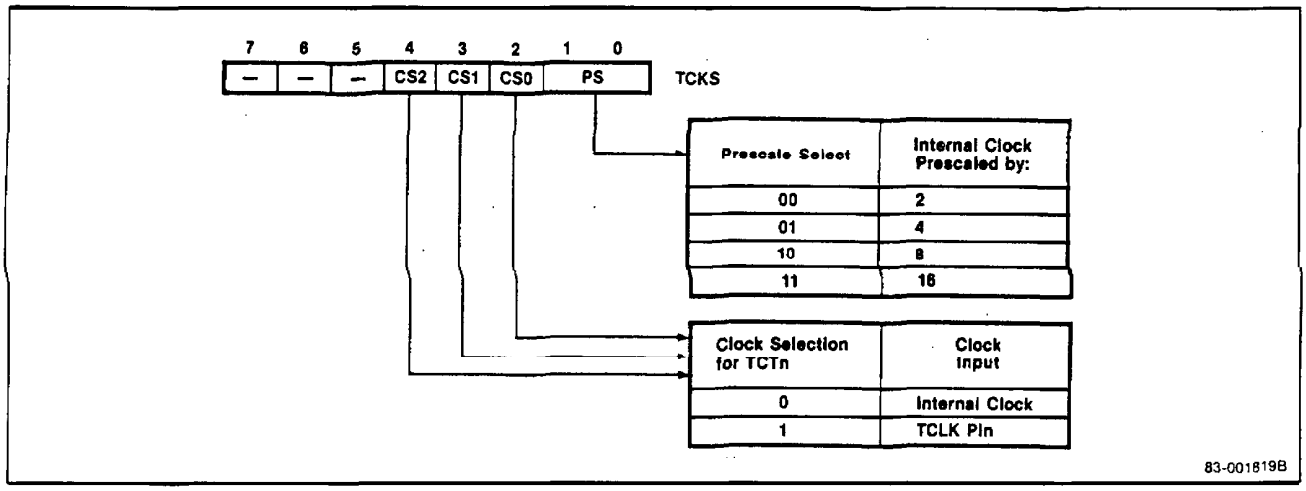
Figure 13. μPD70208 Peripheral Relocation



Timer Clock Selection Register

The timer clock selection (TCKS) register selects the clock source for each of the timer/counters as well as the divisor for the internal clock prescaler. Figure 14 shows the format of the TCKS register. The clock source for each timer/counter is independently selected from either the prescaled CLKOUT signal or from an external clock source (TCLK). The internal clock is derived from the CLKOUT signal and can be divided by 2, 4, 8, or 16 before being presented to the clock select logic.

Figure 14. Timer Clock Selection Register



Refresh Control Unit

The refresh control unit (RCU) refreshes external dynamic RAM devices by outputting a 9-bit row address on address lines A_8-A_0 and performing a memory read bus cycle. External logic can distinguish a refresh bus cycle by monitoring the refresh request ($\overline{REFRQ}$) pin. Following each refresh bus cycle, the refresh row counter is incremented.

The refresh control (RFC) register in the system I/O area contains two fields. The refresh enable field enables or disables the refreshing function. The refresh timer (RTM) field selects a refresh interval to match the dynamic memory refresh requirements. Figure 15 shows the format for the RFC register.

To minimize the impact of refresh on the system bus bandwidth, the μPD70208 utilizes a refresh request queue to store refresh requests and perform refresh bus cycles in otherwise idle bus cycles.

The RCU normally requests the bus as the lowest-priority bus requester (normal mode). However, if seven refresh requests are allowed to accumulate in the RCU refresh request queue, the RCU will change to the highest-priority bus requester (demand mode). The RCU will then perform back-to-back refresh cycles until three requests remain in the queue. This guarantees the integrity of the DRAM system while maximizing performance.

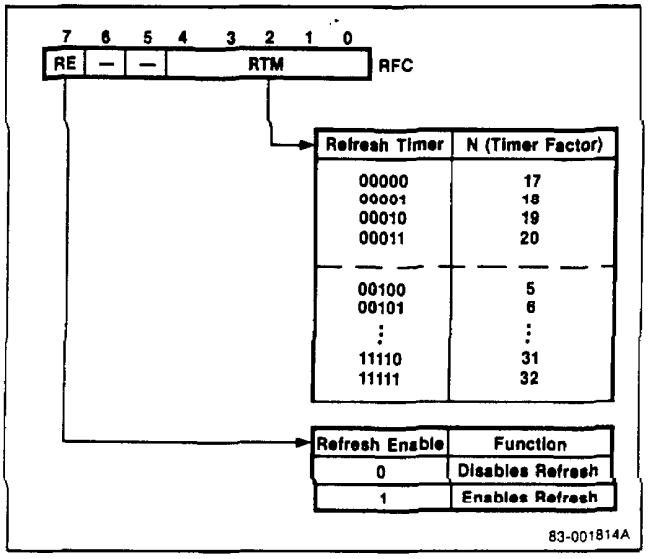
The refresh count interval can be calculated as follows:

$$\text{Refresh interval} = 8 \times N \times t_{CYK}$$

where N is the timer factor selected by the RTM field.

When the μPD70208 is reset, the RE field in the RFC register is unaffected and the RTM field is set to 01000 (N = 9). No refresh bus cycles occur while $\overline{RESET}$ is asserted.

Figure 15. Refresh Control Register



Wait Control Unit

The wait control unit (WCU) inserts from zero to three wait states into a bus cycle in order to compensate for the varying access times of memory and I/O devices. The number of wait states for CPU, DMAU, and RCU bus cycles is separately programmable. In addition, the memory address space is divided into three independent partitions to accommodate a wide range of system designs. $\overline{\text{RESET}}$ initializes the WCU to insert three wait states in all bus cycles. This allows operation with slow memory and peripheral devices before the initialization of the WCU registers.

The three system I/O area registers that control the WCU are wait cycle 1 (WCY1), wait cycle 2 (WCY2), and wait state memory boundary (WMB). The WCU always inserts wait states corresponding to the wait count programmed in WCY1 or WCY2 registers into a bus cycle, regardless of the state of the external READY input. After the programmed number of wait states occurs, the WCU will insert Tw states as long as the READY pin remains inactive. When READY is again asserted, the bus cycle continues with T4 as the next cycle. The μPD70208 internal peripherals never require wait states; four clock cycles will terminate an internal peripheral bus cycle.

CPU Wait States

The WMB register divides the 1M-byte memory address space into three independent partitions: lower, middle, and upper. Figure 16 shows the WMB register format.

Initialization software can then set the number of wait states for each memory partition and the I/O partition via the WCY1 register (figure 17).

DMA and Refresh Wait States

The WCY2 register (figure 18) specifies the number of wait states to be automatically inserted in DMA and refresh bus cycles.

Figure 16. Wait State Memory Boundary Register

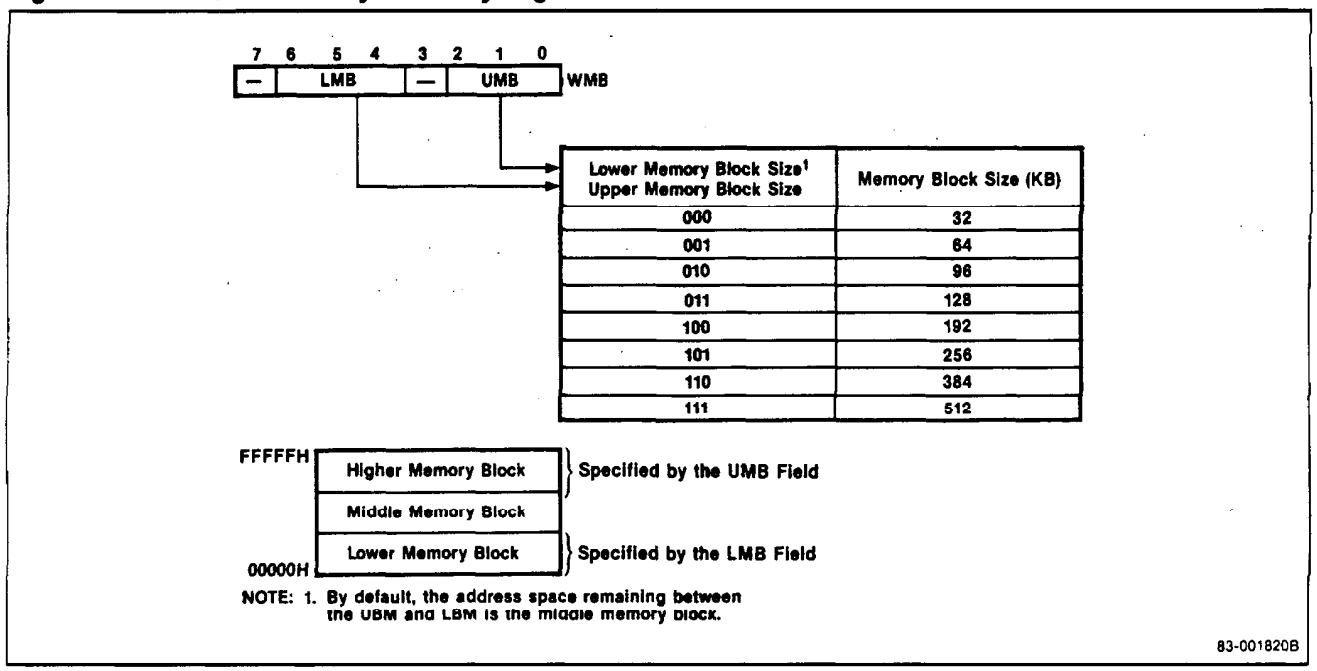


Figure 17. Wait Cycle 1 Register

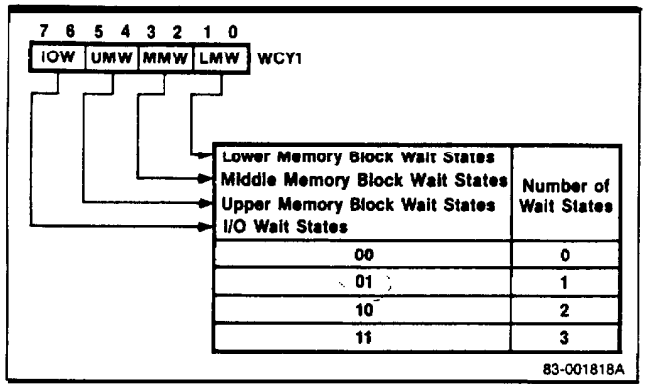
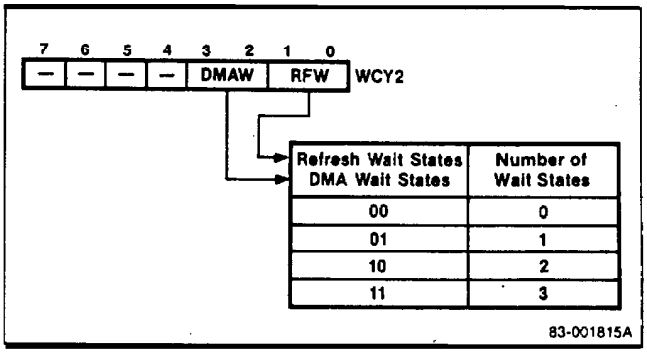


Figure 18. Wait Cycle 2 Register



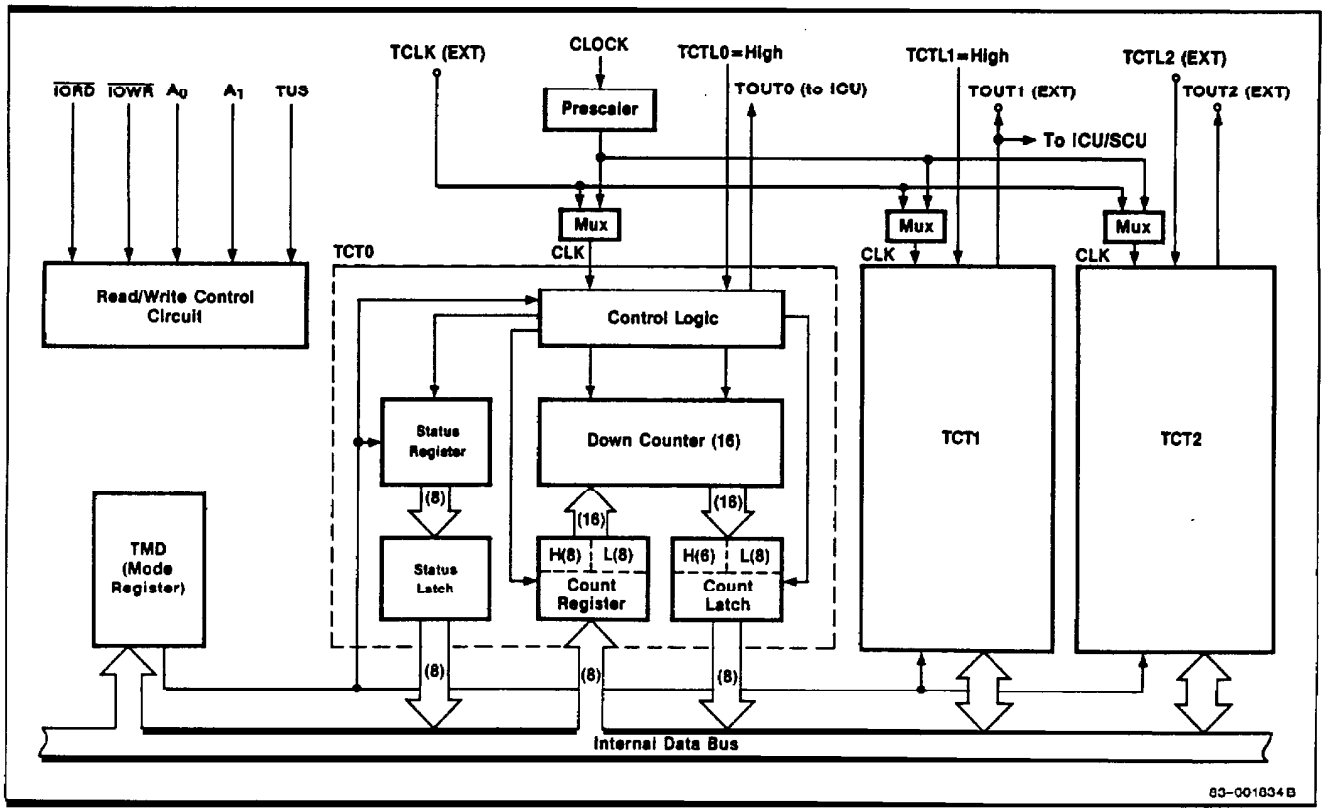
Timer/Counter Unit

The timer/counter unit (TCU) provides a set of three independent 16-bit timer/counters. The output signal of timer/counter 0 is hardwired internally as an interrupt source. The output of timer/counter 1 is available internally as an interrupt source, used as a baud rate generator, or used as an external output. The timer/counter 2 output is available as an external output. Due to mode restrictions, the TCU is a subset of the μPD71054 Programmable Timer/Counter. Figure 19 shows the internal block diagram of the TCU.

The TCU has the following features:

- Three 16-bit timer/counters
- Six programmable count modes
- Binary/BCD counting
- Multiple latch command
- Choice of two clock sources

Figure 19. TCU Block Diagram



Because $\overline{RESET}$ leaves the TCU in an uninitialized state, each timer/counter must be initialized by specifying an operating mode and a count. Once programmed, a timer/counter will continue to operate in that mode until another mode is selected. When the count has been written to the counter and transferred to the down counter, a new count operation starts. Both the current count and the counter status can be read while count operations are in progress.

TCU Commands

The TCU is programmed by issuing I/O instructions to the I/O port addresses programmed in the OPHA and TULA registers. The individual TCU registers are selected by address bits A_1 and A_0 as follows.

A_1	A_0	Register	Operation
0	0	TCT0 TST0	Read/Write Read
0	1	TCT1 TST1	Read/Write Read
1	0	TCT2 TST2	Read/Write Read
1	1	TMD	Write

The timer mode (TMD) register selects the operating mode for each timer/counter and issues the latch command for one or more timer/counters. Figure 20 shows the format for the TMD register.

Writes to the timer/counter 2-0 (TCT2-TCT0) registers stores the new count in the appropriate timer/counter. The count latch command is used before reading count data in order to latch the current count and prevent inaccuracies.

The timer status 2-0 (TST2-TST0) registers contain status information for the specified counter (figure 21). The latch command is used to latch the appropriate counter status before reading status information. If both status and counter data are latched for a counter, the first read operation returns the status data and subsequent read operations obtain the count data.

Count Modes

There are six programmable timer/counter modes. The timing waveforms for these modes are in figure 22.

Mode 0 [Interrupt on End of Count]. In this mode, TOUT changes from the low to high level when the specified count is reached. This mode is available on all timer/counters.

Mode 1 [Retriggerable One-Shot]. In mode 1, a low-level one-shot pulse, triggered by TCTL2 is output from the TOUT2 pin. This mode is available only on timer/counter 2.

Mode 2 [Rate Generator]. In mode 2, TOUT cyclically goes low for one clock period when the counter reaches the 0001H count. A counter in this mode operates as a frequency divider. All timer/counters can operate using mode 2.

Mode 3 [Square-Wave Generator]. Mode 3 is a frequency divider similar to mode 2, but the output has a symmetrical duty cycle. This mode is available on all three timer/counters. For counts of N = 2, use mode 2.

Mode 4 [Software-Triggered Strobe]. In mode 4, when the specified count is reached, TOUT goes low for the duration of one clock pulse. Mode 4 is available on all timer/counters.

Mode 5 [Hardware-Triggered Strobe]. Mode 5 is similar to mode 4 except that operation is triggered by the TCTL2 input and can be retriggered. This mode is available only on timer/counter 2.

Serial Control Unit

The serial control unit (SCU) is a single asynchronous serial channel that performs serial communication between the μPD70208 and an external serial device. The SCU is similar to the μPD71051 Serial Control Unit except for the lack of synchronous communication protocols. Figure 23 is the block diagram of the SCU.

The SCU has the following features.

- Full-duplex asynchronous serial controller
- Clock rate divisor (x16, x64)
- Baud rates to 38.4 kb/s supported
- 7-, 8-bit character lengths
- 1-, 2-bit stop bit lengths
- Break transmission and detection
- Full-duplex, double-buffered transmitter/receiver
- Even, odd, or no parity
- Parity, overrun, and framing error detection
- Receiver full and transmitter empty interrupts

The SCU contains four separately addressable registers for reading/writing data, reading status, and controlling operation of the SCU. The serial receive buffer (SRB) and the serial transmit buffer (STB) store the incoming and outgoing character data. The serial status (SST) register allows software to determine the current state of both the transmitter and receiver. The serial command (SCM) and serial mode (SMD) registers determine the operating mode of the SCU while the serial interrupt mask (SIMK) register allows software control of the SCU receive and transmit interrupts.

Figure 20. Timer Mode Register

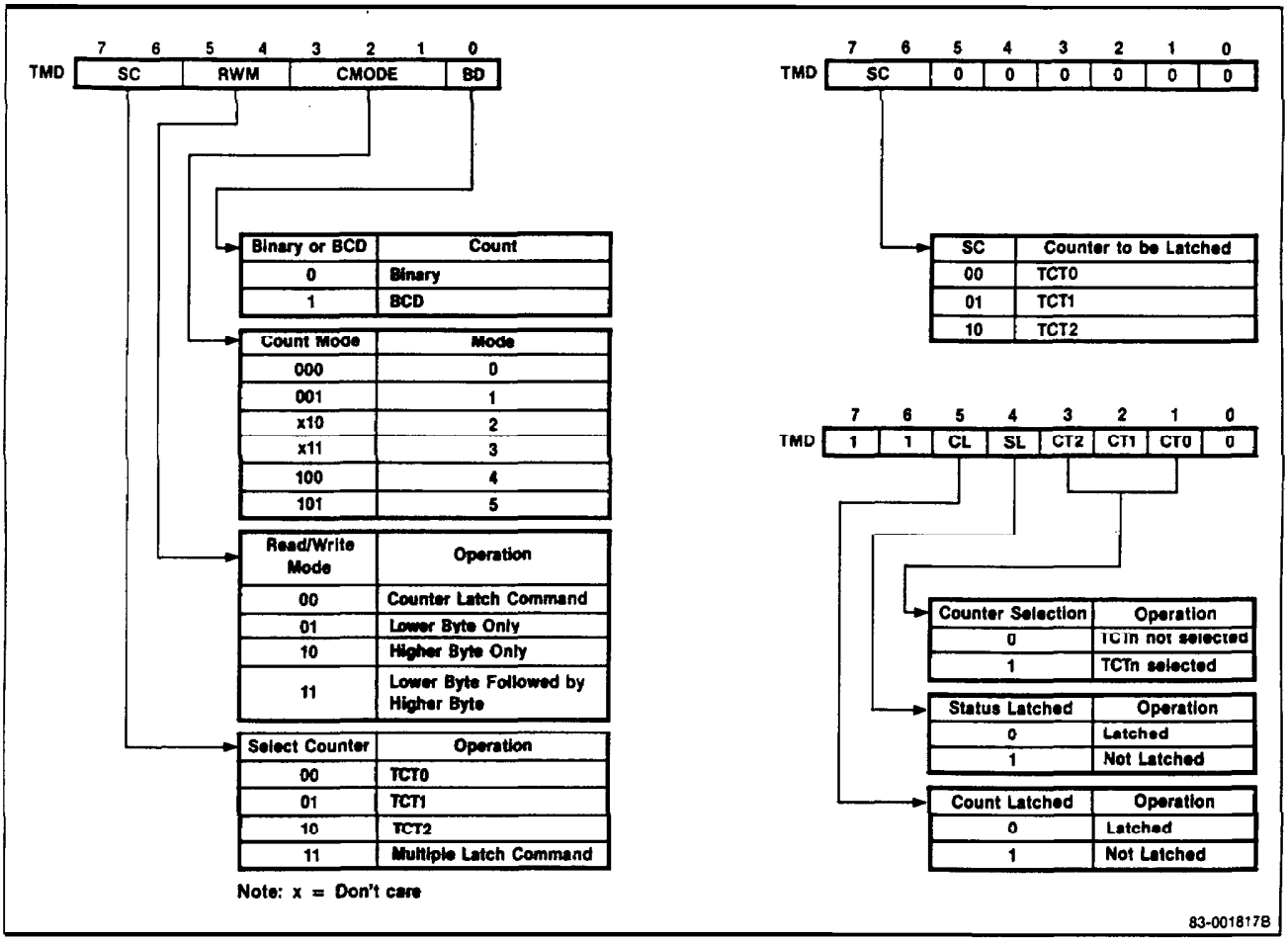


Figure 21. TCU Status Register

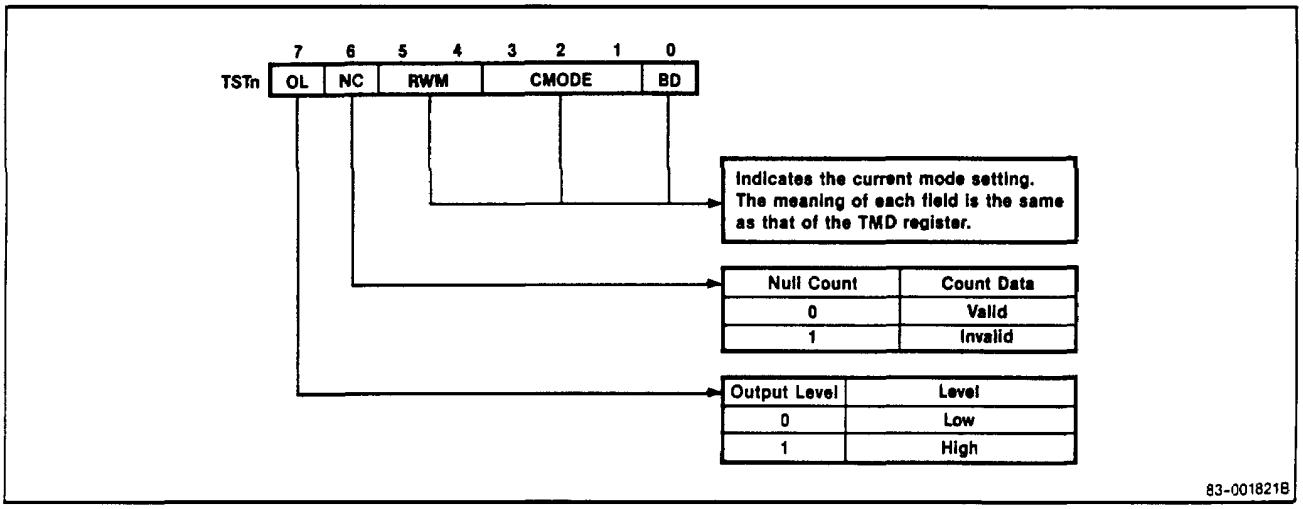


Figure 22. TCU Waveforms (Sheet 1 of 3)

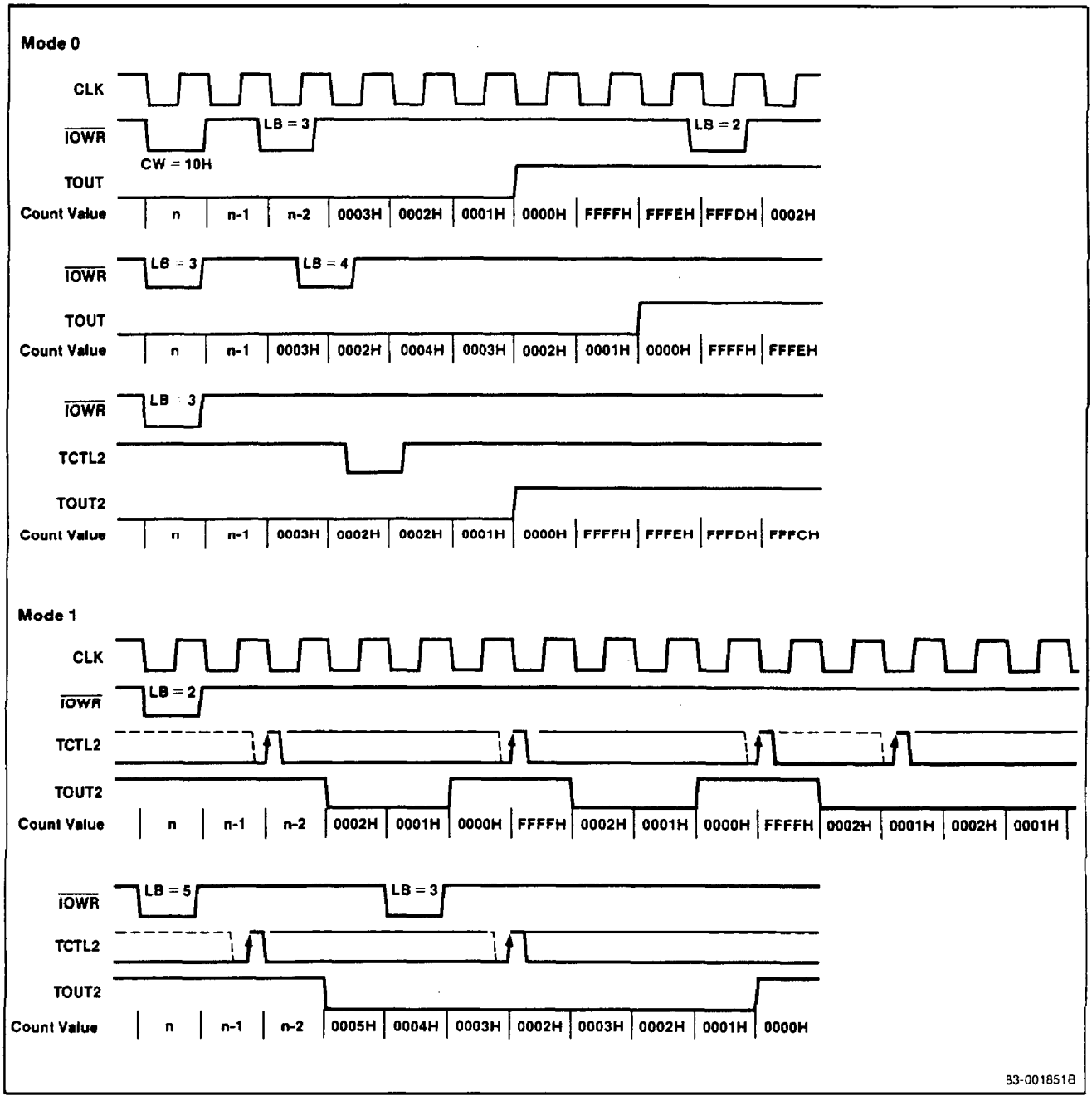
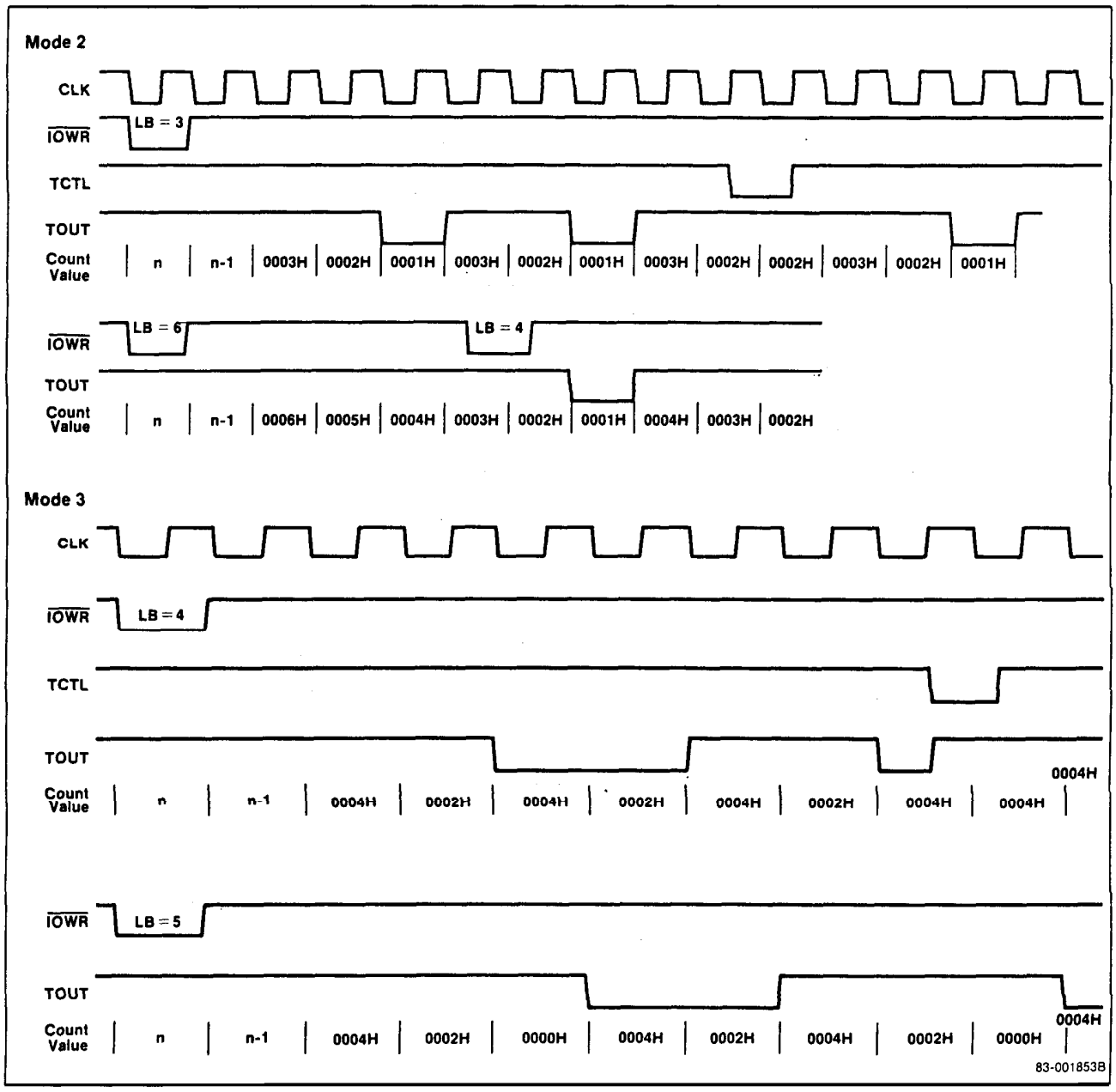


Figure 22. TCU Waveforms (Sheet 2 of 3)



3

Figure 22. TCU Waveforms (Sheet 3 of 3)

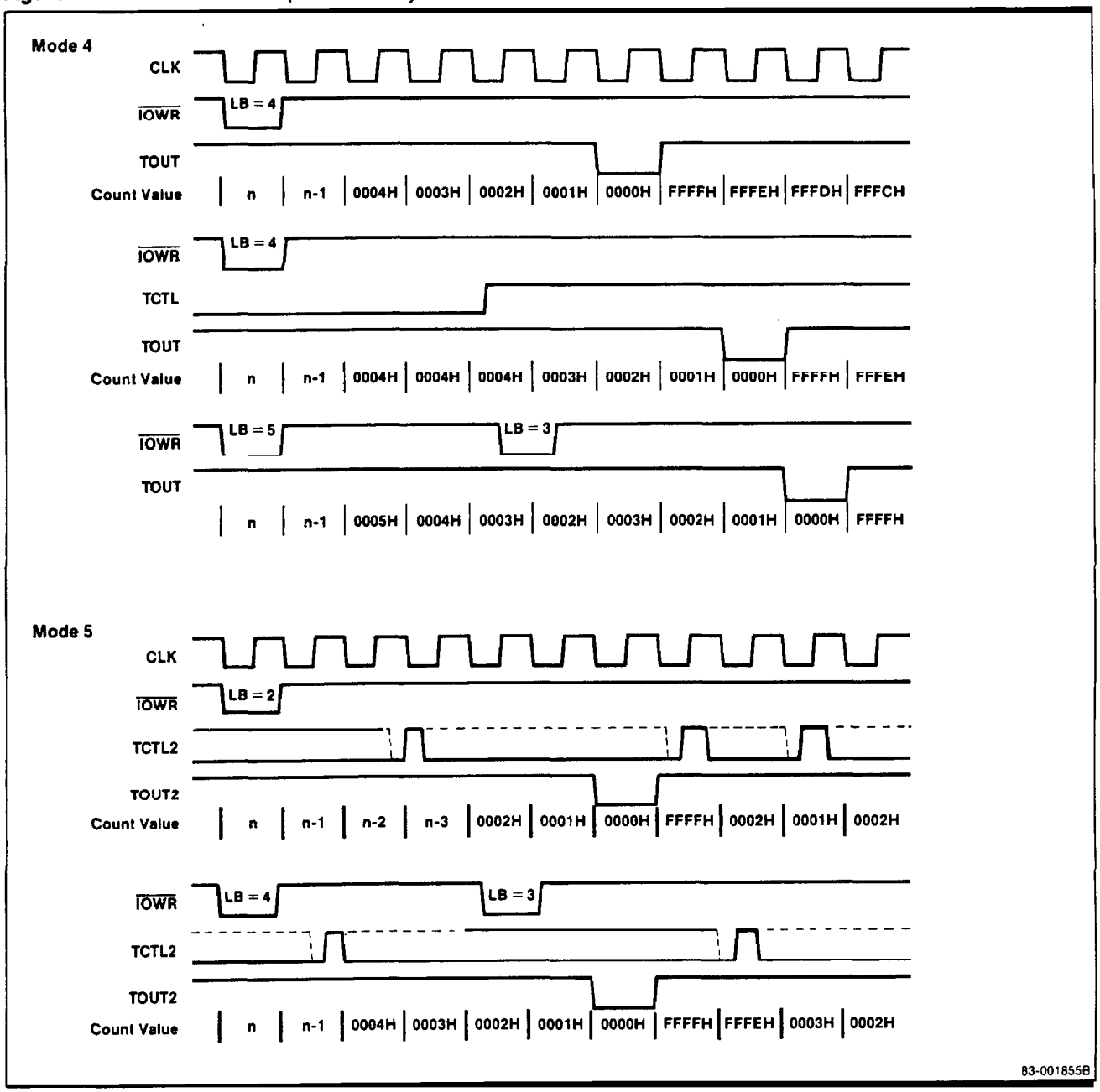
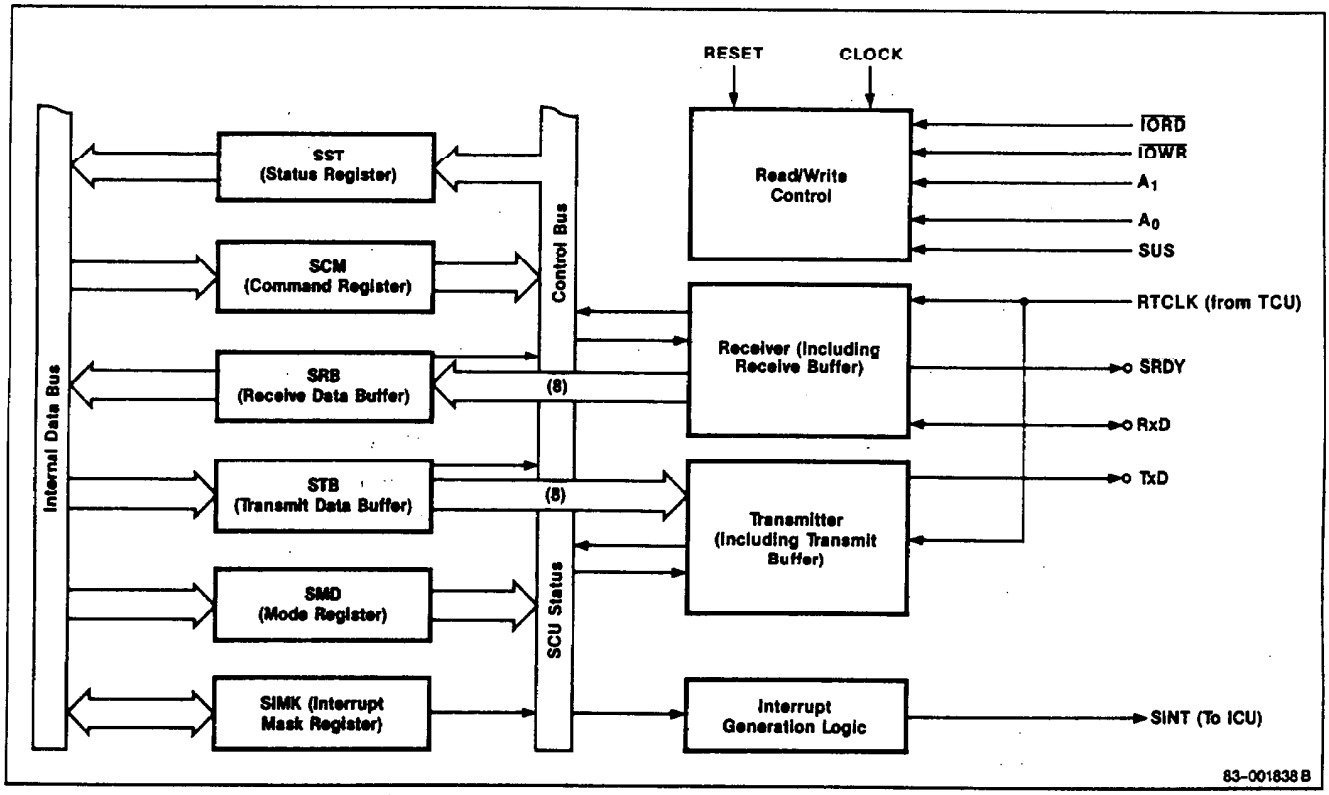


Figure 23. SCU Block Diagram



Receiver Operation

While the RxD pin is high, the SCU is in an idle state. A transition on RxD from high to low indicates the start of a new serial data reception. When a complete character has been received, it is transferred to the SRB; the receive buffer ready (RBRDY) bit in the SST register is set and (if unmasked) an interrupt is generated. The SST also latches any parity, overrun, or framing errors at this time.

The receiver detects a break condition when a null character with zero parity is received. The BRK bit is set for as long as the subsequent receive data is low and resets when RxD returns to a high level. The MRDY bit (SCM) and RBRDY (SST) are gated to form the output $\overline{SRDY}$. $\overline{SRDY}$ prevents overruns from occurring when the program is unable to process the input data. Software can control MRDY to prevent data from being sent from the remote transmitter while RBRDY can prevent the immediate overrun of a received character.

Transmitter Operation

TxD is kept high while the STB register is empty. When the transmitter is enabled and a character is written to the STB register, the data is converted to serial format and output on the TxD pin. The start bit indicates the start of the transmission and is followed by the character stream (LSB to MSB) and an optional parity bit. One or two stop bits are then appended, depending on the programmed mode. When the character has been transferred from the STB, the TRBDY bit in the SST is set and if unmasked, a transmit buffer empty interrupt is generated.

Serial data can be transmitted and received by polling the SST register and checking the TBRDY or RBRDY flags. Data can also be transmitted and received by SCU-generated interrupts to the interrupt control unit. The SCU generates an interrupt in either of these conditions:

(1) The receiver is enabled, the SRB is full, and receive interrupts are unmasked.

(2) The transmitter is enabled, the STB is empty, and transmit interrupts are unmasked.

SCU Registers and Commands

I/O instructions to the I/O addresses selected by the OPHA and SULA registers are used to read/write the SCU registers. Address bits A_1 and A_0 and the read/write lines select one of the six internal registers as follows:

A_1	A_0	Register	Operation
0	0	SRB STB	Read Write
0	1	SST SCM	Read Write
1	0	SMD	Write
1	1	SIMK	Read/Write

The SRB and STB are 8-bit registers. When the character length is 7 bits, the lower 7 bits of the SRB register are valid and bit 7 is cleared to 0. If programmed for 7-bit characters, bit 7 of the STB is ignored.

The SST register (figure 24) contains the status of the transmit and receive data buffers and the error flags. Error flags are persistent. Once an error flag is set, it remains set until a clear error flags command is issued.

Figure 25 shows the SCM and SMD registers. The SCM register stores the command word that controls transmission, reception, error flag reset, break transmission, and the state of the $\overline{SRDY}$ pin. The SMD register stores the mode word that determines serial characteristics such as baud rate divisor, parity, character length, and stop bit length.

Initialization software should first program the SMD register followed by the SCM register. Unlike the μPD71051, the SMD register can be modified at any time without resetting the SCU.

The SIMK register (figure 26) controls the occurrence of RBRDY and TBRDY interrupts. When an interrupt is masked, it is prevented from propagating to the interrupt control unit.

Figure 24. SST Register

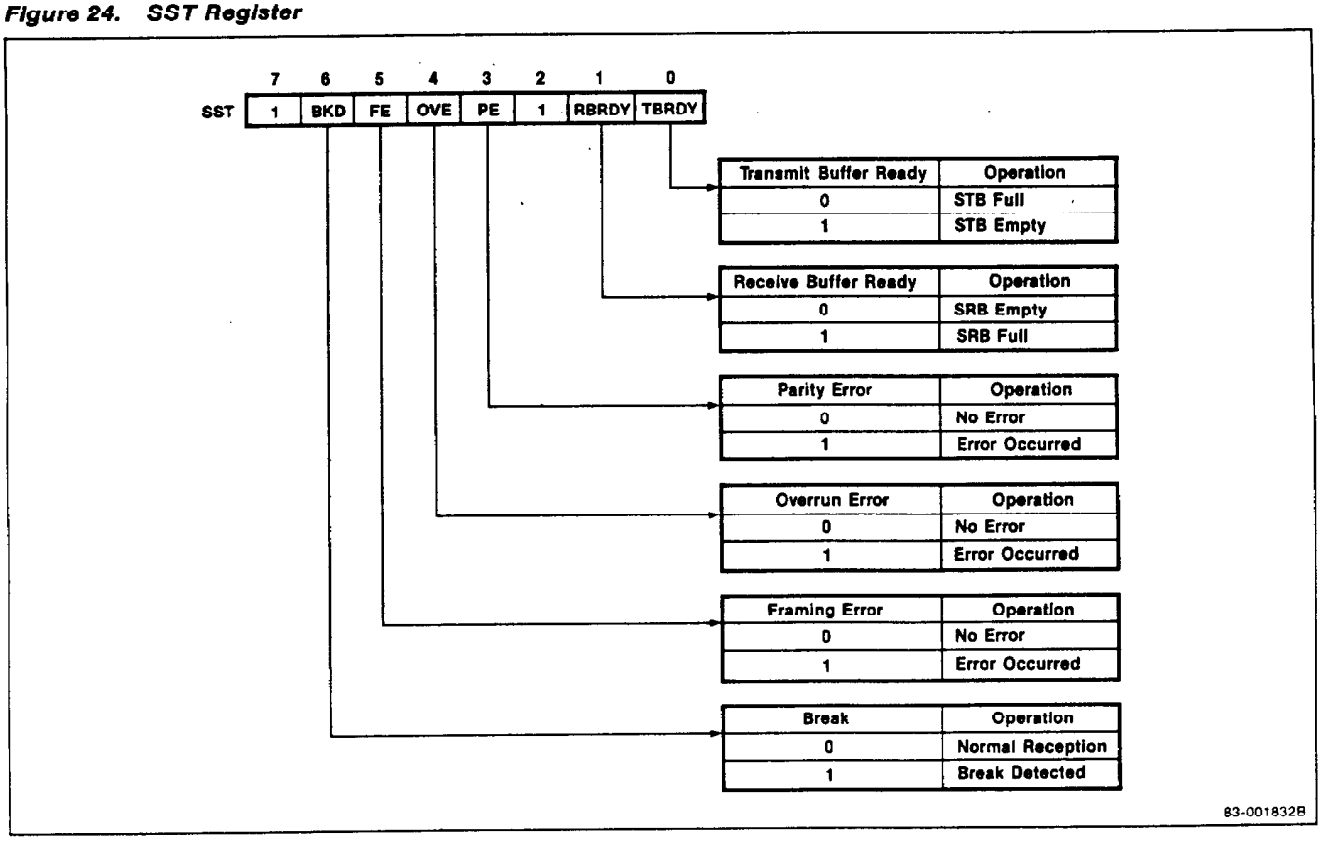


Figure 25. SCM and SMD Registers

SCM Register

	7	6	5	4	3	2	1	0
SCM	—	—	$\overline{MRDY}$	ECL	SBRK	RE	—	TE

Transmitter Enabled	Operation
0	Transmitter Disabled
1	Transmitter Enabled

Receiver Enabled	Operation
0	Receiver Disabled
1	Receiver Enabled

Send Break	Operation
0	Normal Operation
1	TxD = 0 (Break)

Error Clear	Operation
0	No Operation
1	Error Flag Clear

$\overline{MRDY}$	Mask Ready
0	$\overline{SRDY}$ = 1 (Mask)
1	Normal Operation of $\overline{SRDY}$ Output

SMD Register

	7	6	5	4	3	2	1	0
SMD	STL		PS		CL		BF	

Baud Rate Factor	Operation
0-	Illegal
10	RTCLK Frequency ÷ 16
11	RTCLK Frequency ÷ 64

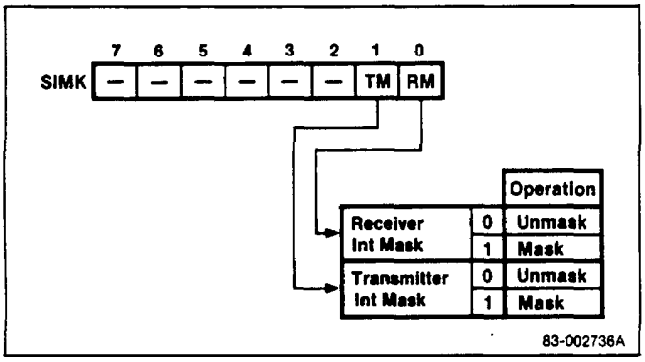
Character Length	Operation
0-	Illegal
10	7 Bit Characters
11	8 Bit Characters

Parity Select	Operation
-0	No Parity
01	Odd Parity
11	Even Parity

Stop Bit Length	Operation
-0	Illegal
01	1 Stop Bit
11	2 Stop Bits

83-001836B

Figure 26. SIMK Register



Interrupt Control Unit

The interrupt control unit (ICU) is a programmable interrupt controller equivalent to the μPD71059. The ICU arbitrates up to eight interrupt inputs, generates a CPU interrupt request, and outputs the interrupt vector number on the internal data bus during an interrupt acknowledge cycle. Cascading up to seven external slave μPD71059s permits the μPD70208 to support up to 56 interrupt sources. Figure 27 is the block diagram for the ICU.

The ICU has the following features.

- Eight interrupt request inputs
- Cascadable with μPD71059 Interrupt Controllers
- Programmable edge- or level-triggered interrupts (TCU, edge-triggered interrupts only)
- *Individually maskable interrupt requests*
- Programmable interrupt request priority
- Polling mode

ICU Registers

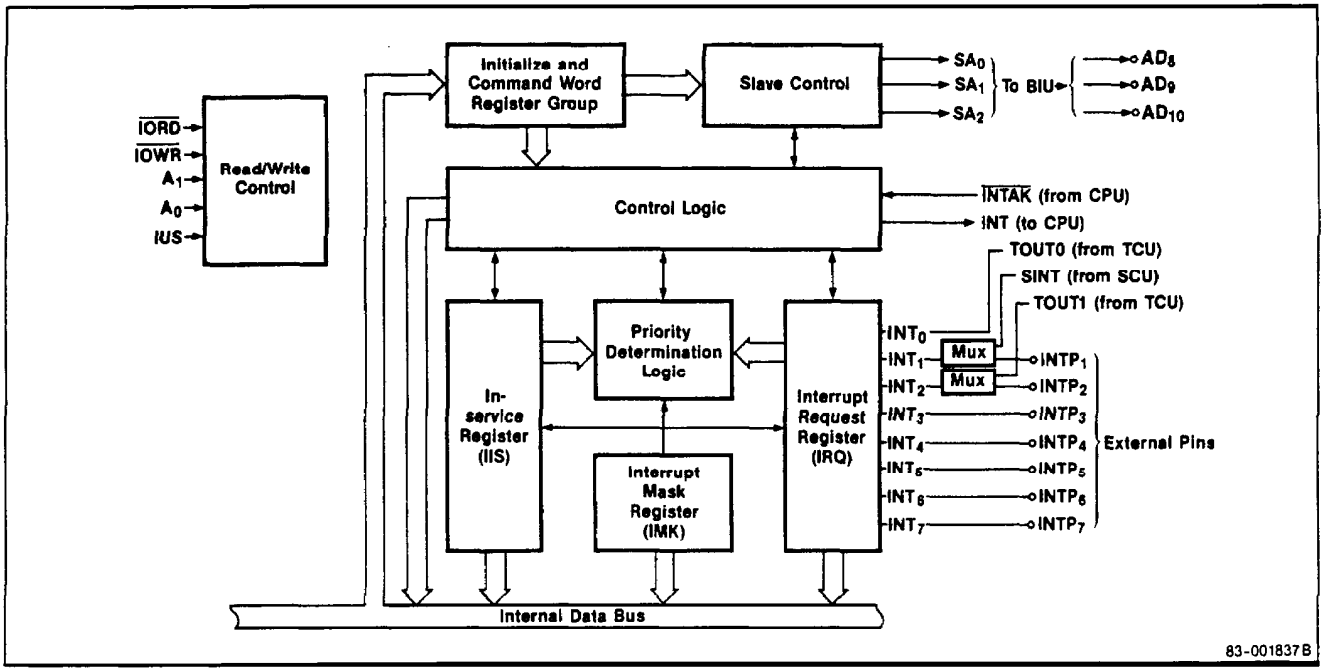
Use I/O instructions to the I/O addresses selected by the OPHA and IULA registers to read from and write to the ICU registers. Address bit A_0 and the command word selects an ICU internal register.

	A_0	Other Condition	Operation
Read	0	IMD selects IRQ	CPU ← IRQ data
	0	IMD selects IIS	CPU ← IIS data
	0	Polling phase	CPU ← Polling data
	1	—	CPU ← IMKW
Write	0	D4 = 1	CPU → IIW1
	0	D4 = 0 and D3 = 0	CPU → IPFW
	0	D4 = 0 and D3 = 1	CPU → IMDW
	1	During initialization	CPU → IIW2
	1		CPU → IIW3
	1		CPU → IIW4
	1	After initialization	CPU → IMKW

Note:

(1) In polling phase, polling data has priority over the contents of the IRQ or IIS register when read.

Figure 27. ICU Block Diagram



Initializing the ICU

The ICU is always used to service maskable interrupts in a μPD70208 system. Prior to accepting maskable interrupts, the ICU must first be initialized (figure 28). Following initialization, command words from the CPU can change the interrupt request priorities, mask/unmask interrupt requests, and select the polling mode. Figures 29 and 30 list the ICU initialization and command words.

Interrupt initialization words 1-4 (IIW1-IIW4) initialize the ICU, indicate whether external μPD71059s are connected as slaves, select the base interrupt vector, and select edge- or level-triggered inputs for INT1-INT7. Interrupt sources from the TCU are fixed as edge-triggering. INT0 is internally connected to TOUT0, and INT2 may be connected to TOUT1 by the IRSW field in the OPCN.

The interrupt mask word (IMKW) contains programmable mask bits for each of the eight interrupt inputs. The interrupt priority and finish word (IPFW) is used by the interrupt handler to terminate processing of an interrupt or change interrupt priorities. The interrupt mode word (IMDW) selects the polling register, interrupt request (IRQ) or interrupt in service (IIS) register, and the nesting mode.

The initialization words are written in consecutive order starting with IIW1. IIW2 sets the interrupt vector. IIW3 specifies which interrupts are connected to slaves. IIW3 is only required in extended systems. The ICU will only expect to receive IIW3 if SNGL = 0 (bit D_1 of IIW1). IIW4 is only written if II4 = 1 (bit D_0 of IIW1).

μPD71059 Cascade Connection

To increase the number of maskable interrupts, up to seven slave μPD71059 Interrupt Controllers can be cascaded. During cascade operation (figure 31), each slave μPD71059 INT output is routed to one of the μPD70208 INTP inputs. During the second interrupt acknowledge bus cycle, the ICU places the slave address on address lines A_{10}-A_8. Each slave compares this address with the slave address programmed using interrupt initialization word 3 (IIW3). If the same, the slave will place the interrupt vector on pins AD_7-AD_0 during the second interrupt acknowledge bus cycle.

Figure 28. Initialization Sequence

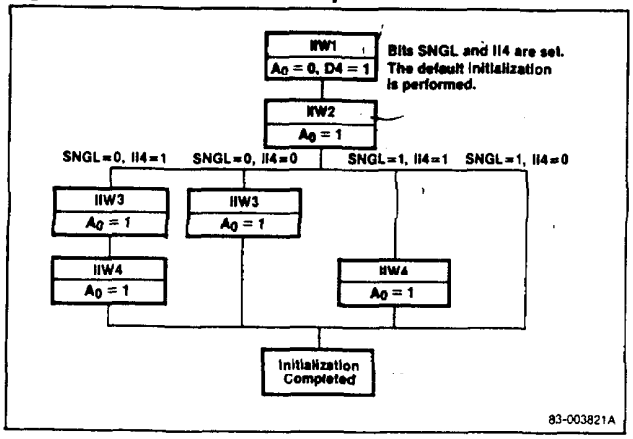


Figure 29. Interrupt Initialization Words 1-4

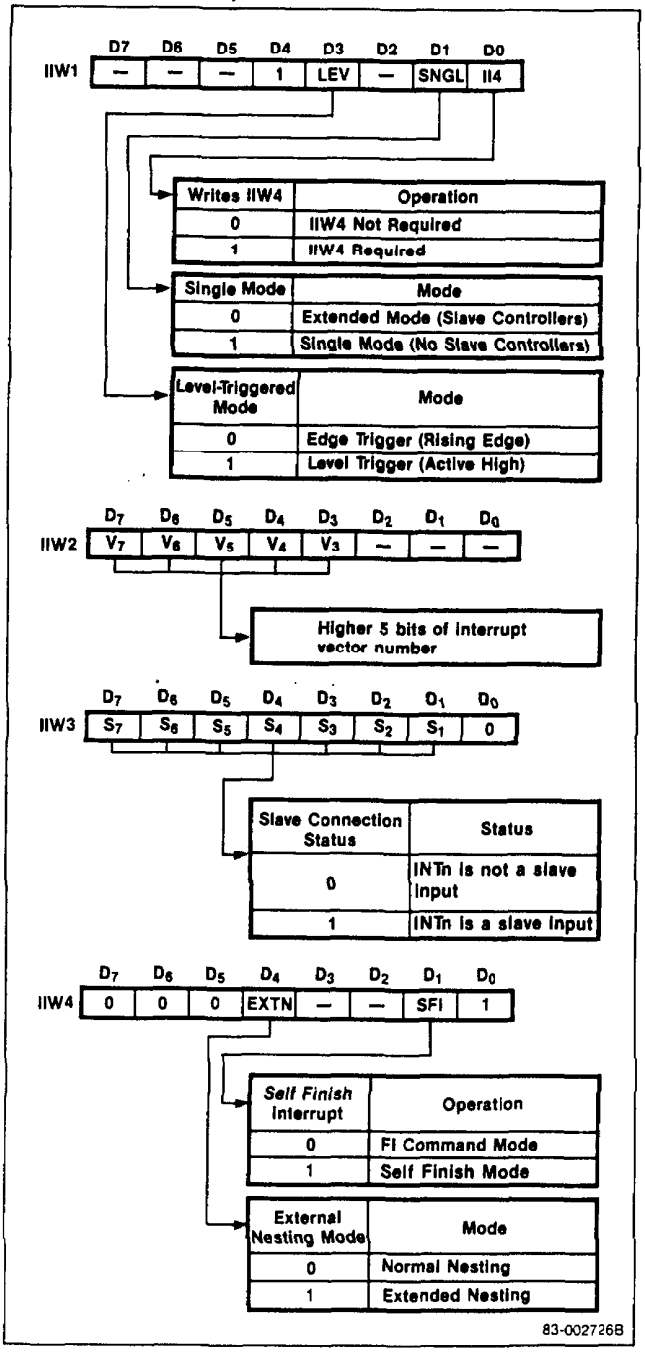


Figure 30. Command Words

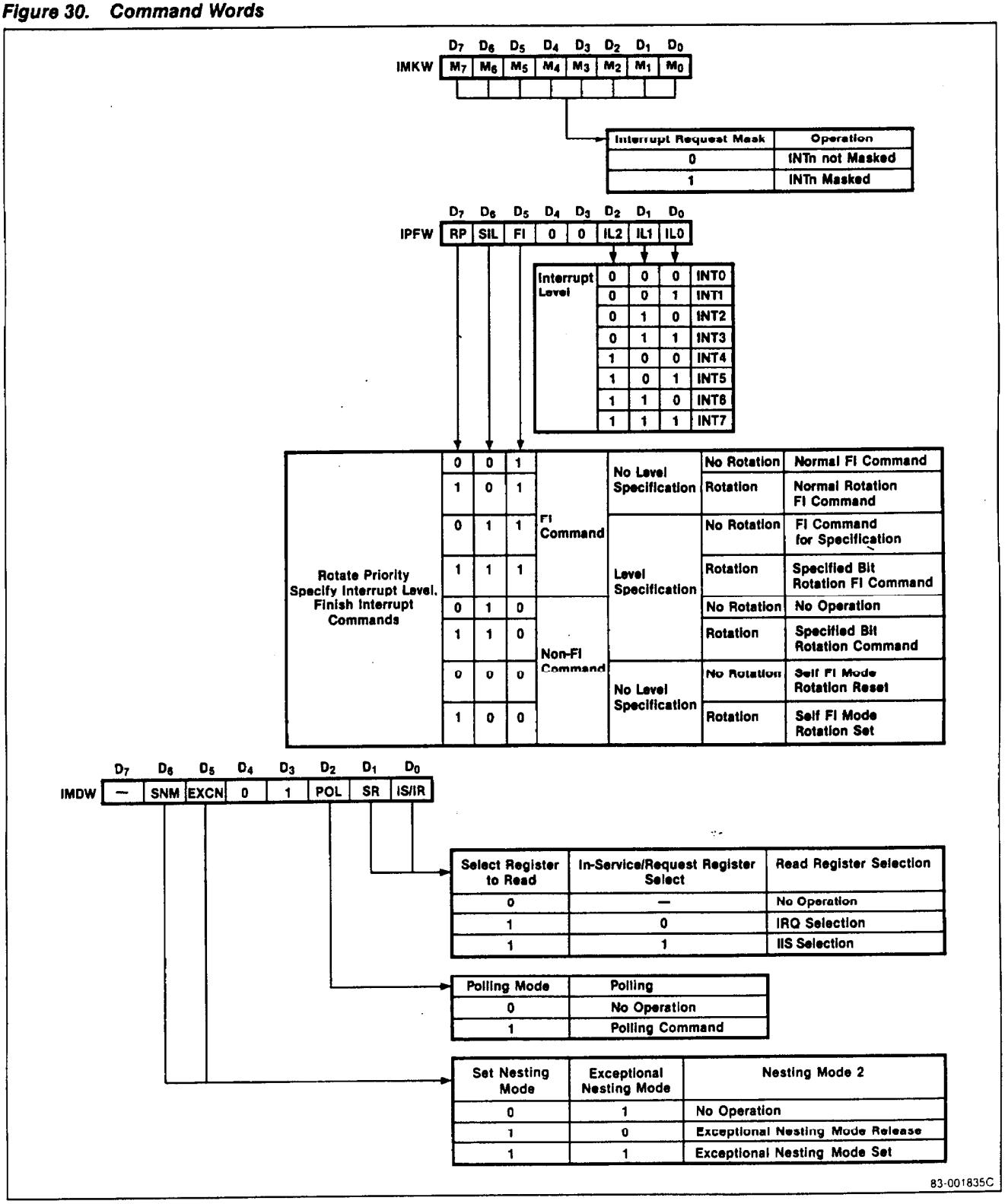
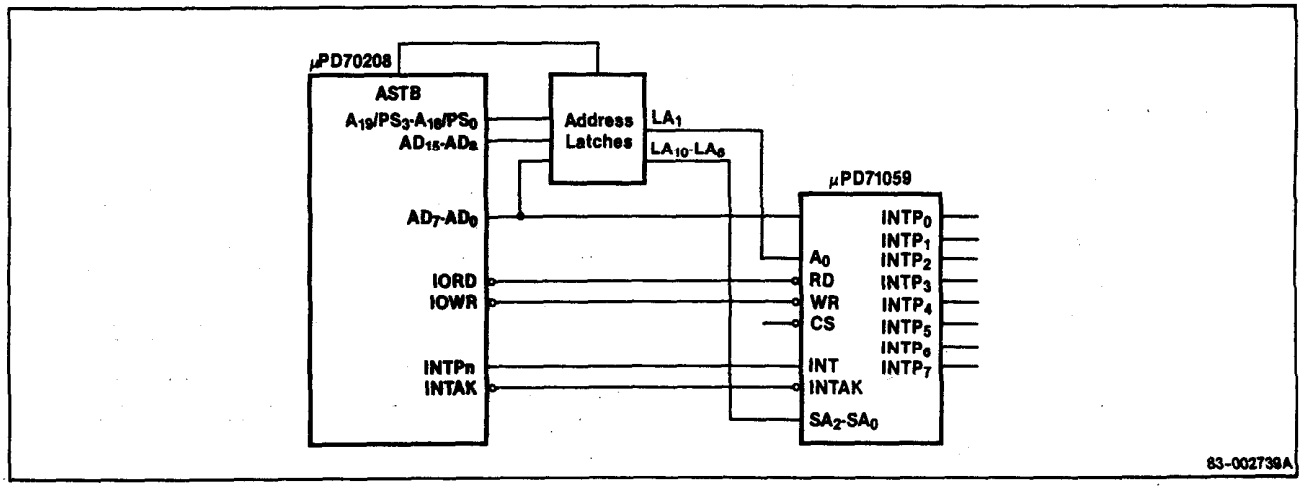


Figure 31. μPD71059 Cascade Connection



DMA Control Unit

The DMA Control Unit (DMAU) is a high-speed DMA controller compatible with the μPD71071 DMA Controller. The DMAU has four independent DMA channels and performs high-speed data transfers between memory and external peripheral devices at speeds as high as 2 megabytes/second in an 8-MHz system. Figure 32 is the block diagram for the DMAU.

The DMAU has the following features.

- Four independent DMA channels
- Cascade mode for slave μPD71071 DMA controllers
- 20-bit address registers
- 16-bit transfer count register
- Single, demand, and block transfer modes
- Bus release and bus hold modes
- Autoinitialization
- Address increment/decrement
- Fixed/rotating channel priorities
- TC output at transfer end
- Forced termination of service by $\overline{END}$ input

DMAU Basic Operation

The DMAU operates in either a slave or master mode. In the slave mode, the DMAU samples the four DMARQ input pins every clock. If one or more inputs are active, the corresponding DMA request bits are set and the DMAU sends a bus request to the BAU while continuing to sample the DMA request inputs. After the BAU returns the DMA bus acknowledge signal, the DMAU stops DMA request sampling, selects the DMA channel with the highest priority, and enters the bus master mode to perform the DMA transfer. While in the bus master mode, the DMAU controls the external bus and performs DMA transfers based on the preprogrammed channel information.

Terminal Count

The DMAU ends DMA service when the terminal count condition is generated or when the $\overline{END}$ input is asserted. A terminal count (TC) is produced when the contents of the current count register becomes zero. If autoinitialization is not enabled when DMA service terminates, the mask bit of the channel is set and the DMARQ input of that channel is masked. Otherwise, the current count and address registers are reloaded from the base registers and new DMA transfers are again enabled.

DMA Transfer Type

The type of transfer the DMAU performs depends on the following conditions.

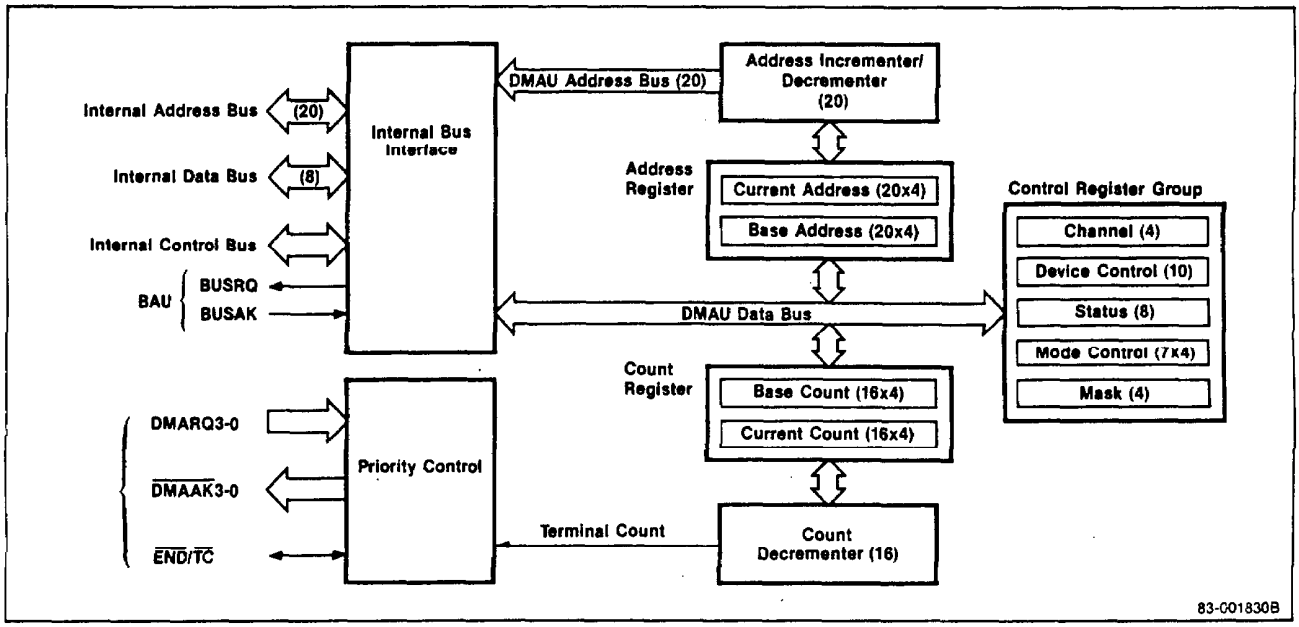
- Direction of the transfer (each channel)
- Transfer mode (each channel)
- Bus mode

Transfer Direction

All DMA transfers use memory as a reference point. Therefore, a DMA read operation transfers data from memory to an I/O port. A DMA write reads an I/O port and writes the data to memory. During memory-to-I/O transfer, the DMA mode (DMD) register is used to select the transfer directions for each channel and activate the appropriate control signals.

Operation	Transfer Direction	Activated Signals
DMA read	Memory → I/O	$\overline{IOWR}$, $\overline{MRD}$
DMA write	I/O → Memory	$\overline{IORD}$, $\overline{MWR}$
DMA verify		Addresses only; no transfer performed

Figure 32. DMAU Block Diagram

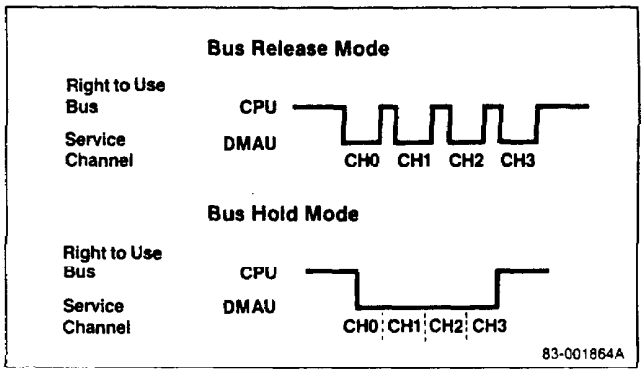


Bus Mode

The DMA device control (DDC) register selects operation in either the bus release or bus hold mode. The selected bus mode determines the DMAU conditions for return of the bus to the BAU. Figure 33 shows that in bus release mode, only one channel is serviced after the DMAU obtains the bus. When DMA service ends (termination conditions depend on the transfer mode), the DMAU returns the bus to the BAU regardless of the state of other DMA requests, and the DMAU reenters the slave mode. When the DMAU regains use of the bus, a new DMA operation can begin.

In bus hold mode, several channels can receive contiguous service without releasing the bus. If there is another valid DMA request when a channel's DMA service is finished, the new DMA service can begin immediately after the previous service without returning the bus to the BAU.

Figure 33. Bus Modes



Transfer Modes

The DMD register also selects either single, demand, or block transfer mode for each channel. The conditions for the termination of each transfer characterize each transfer mode. The following table shows the various transfer modes and termination conditions.

Transfer Mode	Termination Conditions
Single	After each byte/word transfer
Demand	$\overline{END}$ input Terminal count Inactive DMARQ DMARQ of a higher priority channel *becomes active (bus hold mode)*
Block	$\overline{END}$ input Terminal count

The operation of single, demand, and block mode transfers depends on whether the DMAU is in bus release or bus hold mode. Figure 34 shows the operation flow for the six possible transfer and bus mode operations in DMA transfer.

Single-Mode Transfer. In bus release mode, when a channel completes transfer of a single byte, the DMAU enters the slave mode regardless of the state of DMA request inputs. In this manner, other lower-priority bus masters will be able to access the bus.

In bus hold mode, when a channel completes transfer of a single byte, the DMAU terminates the channel's service even if the DMARQ request signal is asserted. The DMAU will then service any other requesting channel. If there are no requests from any other DMA channels, the DMAU releases the bus and enters the slave state.

Demand-Mode Transfer. In bus release mode, the currently active channel continues to transfer data as long as the DMA request of that channel is active, even though other DMA channels are issuing higher-priority requests. When the DMA request of the serviced channel becomes inactive, the DMAU releases the bus and enters the slave state.

In bus hold mode, when the active channel completes a single transfer, the DMAU checks the other DMA request lines without ending the current service. If there is a higher-priority DMA request, the DMAU stops the service of the current channel and starts servicing the highest-priority channel requesting service. If there is no higher request than the current one, the DMAU continues to service the currently active channel. Lower-priority DMA requests are honored without releasing the bus after the current channel service is complete.

Block-Mode Transfer. In bus release mode, the current channel continues DMA transfers until a terminal count or the external END input becomes active. During this time, the DMAU ignores all other DMA requests. After completion of the block transfer, the DMAU releases the bus and enters the slave state, even if DMA requests from other channels are active.

In bus hold mode, the current channel transfers data until an internal or external END signal becomes active. When the service is complete, the DMAU checks all DMA requests without releasing the bus. If there is an active request, the DMAU immediately begins servicing the request. The DMAU releases the bus after it honors all DMA requests or a higher-priority bus master requests the bus.

Byte Transfer

The DMD register can specify only byte DMA transfers for each channel. Depending on the mode selected, the address register can either increment or decrement whereas the count register is always decremented.

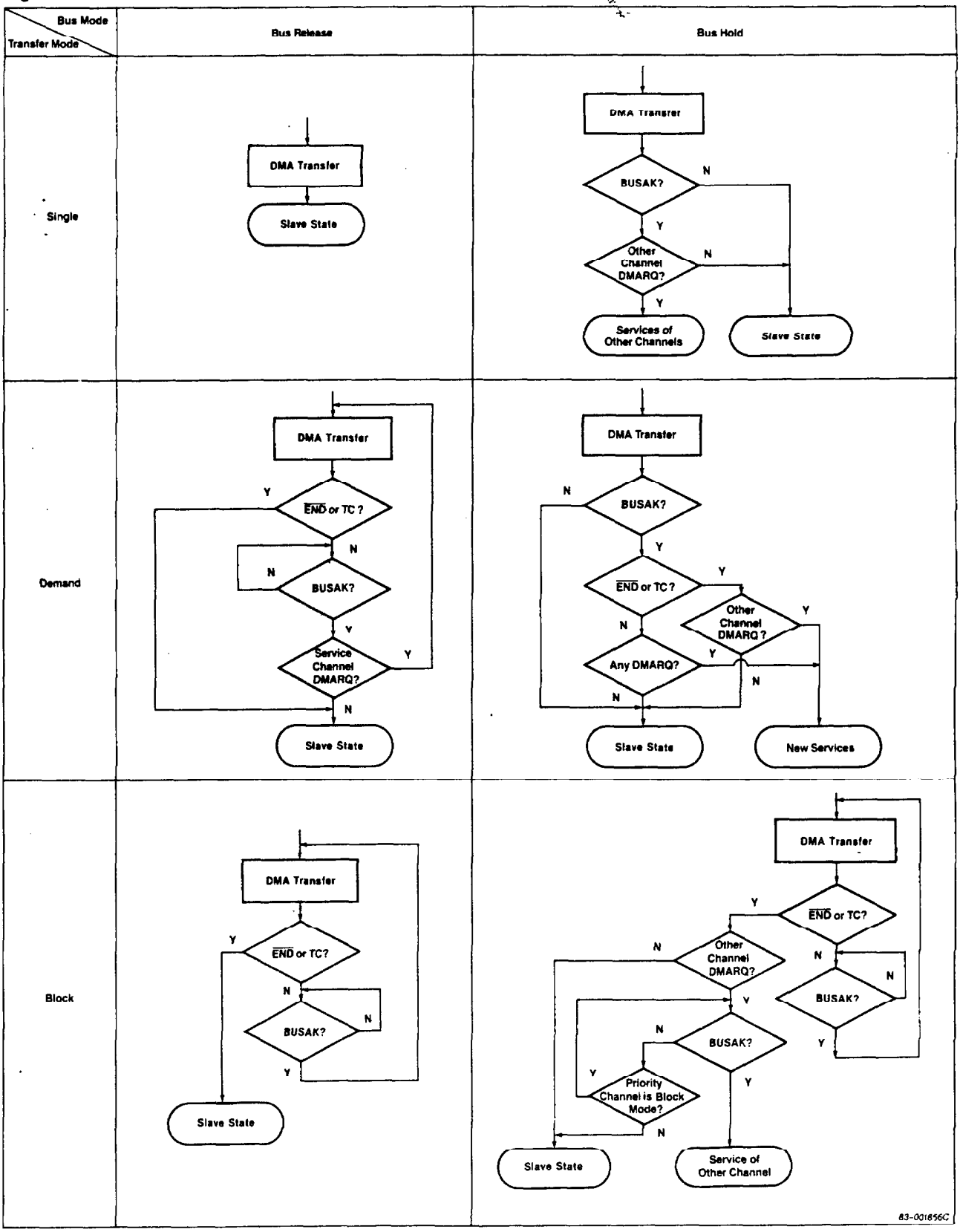
Autoinitialize

When the DMD register selects autoinitialize for a channel, the DMAU automatically reinitializes the address and count registers when $\overline{END}$ is asserted or the terminal count condition is reached. The contents of the base address and base count registers are transferred to the current address and current count registers, and the applicable bit of the mask register remains cleared.

Channel Priority

Each of the four DMAU channels is assigned a priority. When multiple DMA requests from several channels occur simultaneously, the channel with the highest priority will be serviced first. The DDC register selects one of two priority schemes: fixed or rotating (figure 35). In fixed priority, channel 0 is assigned the highest priority and channel 3, the lowest. In rotating priority, priority order is rotated after each service so that the channel last serviced receives the lowest priority. This method prevents the exclusive servicing of higher-priority channels and the lockout of lower-priority DMA channels.

Figure 34. Transfer Modes



Cascade Connection

Slave μPD71071 DMA Controllers can be cascaded to easily expand the system DMA channel capacity to 16 DMA channels. Figure 36 shows an example of cascade connection. During cascade operation, the DMAU acts as a mediator between the BAU and the slave μPD71071s. All other bus outputs are disabled while a slave DMA controller is active.

The DMAU always operates in the bus hold mode while a cascade channel is in service, even when the bus release mode is programmed. Other DMA requests are held pending while a slave μPD71071 channel is in service. When the cascaded μPD71071 ends service and moves into the slave state, the DMAU also moves to the slave state and releases the bus. At this time, all bits of the DMAU request register are cleared. The DMAU continues to operate normally with the other noncascaded channels.

Figure 35. Priority Order

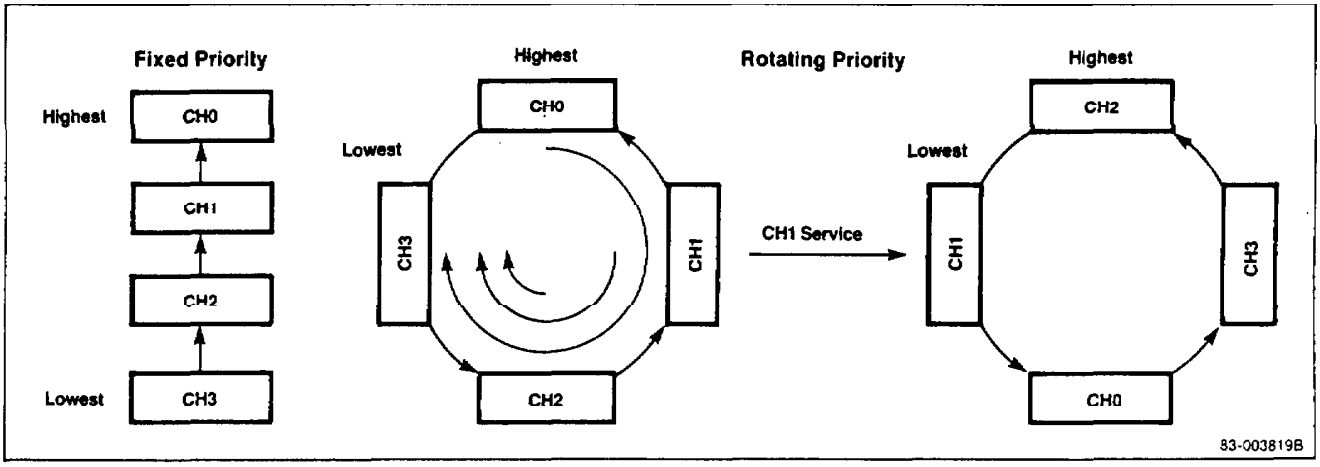
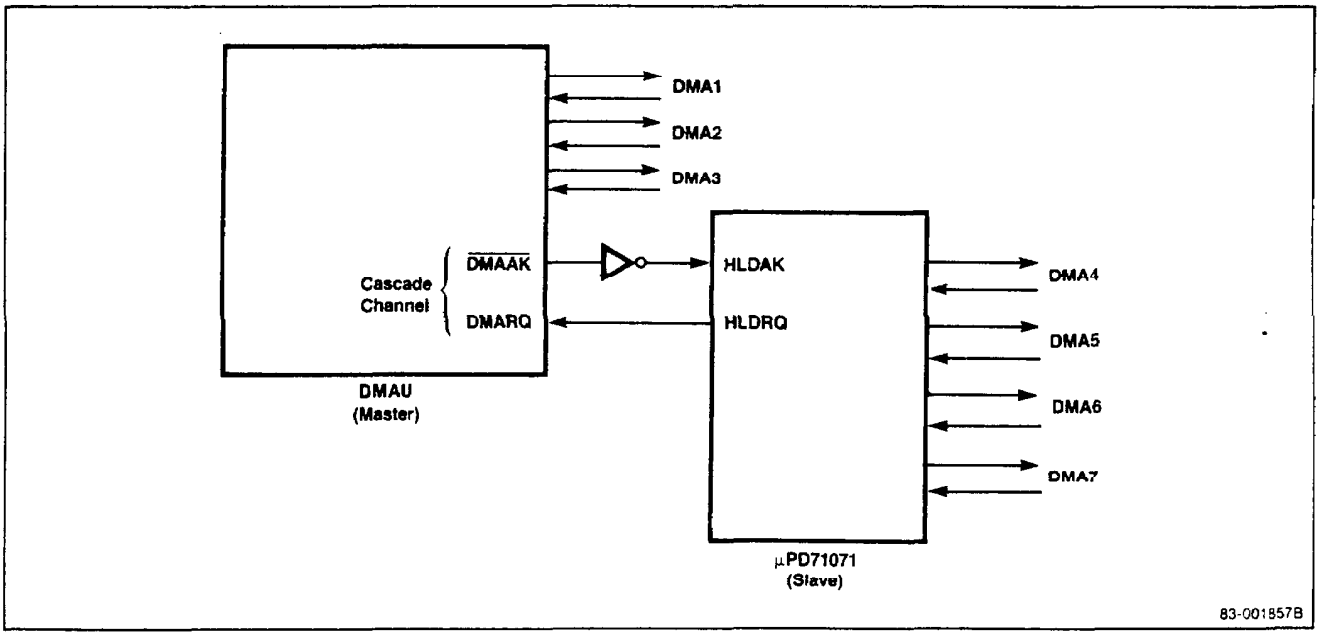


Figure 36. μPD71071 Cascade Example



Bus Waiting Operation

The DMAU will automatically perform a bus waiting operation (figure 37) whenever the RCU refresh request queue fills. When the DMA bus acknowledge goes inactive, the DMAU enters the bus waiting mode and inactivates the DMA bus request signal. Control of the bus is then transferred to the higher-priority RCU by the BAU.

Two clocks later, the DMAU reasserts its internal DMA bus request. The bus waiting mode is continued until *the DMA bus acknowledge signal again becomes* active and the interrupted DMA service is immediately restarted.

Programming the DMAU

To prepare a channel for DMA transfer, the following characteristics must be programmed.

- Starting address for the transfer
- Transfer count
- DMA operating mode
- Transfer size (byte/word)

The contents of the OPHA and DULA registers determine the base I/O port address of the DMAU. Addresses A_3-A_0 are used to select a particular register as follow:

A_3	A_2	A_1	A_0	Register	Operation
0	0	0	0	DICM	Write
0	0	0	1	DCH	Read/Write
0	0	1	0	DBC/DCC (low)	Read/Write
0	0	1	1	DBC/DCC (high)	Read/Write
0	1	0	0	DBA/DCA (low)	Read/Write
0	1	0	1	DBA/DCA (high)	Read/Write
0	1	1	0	DBA/DCA (upper)	Read/Write
0	1	1	1	Reserved	—
1	0	0	0	DDC (low)	Read/Write
1	0	0	1	DDC (high)	Read/Write
1	0	1	0	DMD	Read/Write
1	0	1	1	DST	Read
1	1	0	0	Reserved	—
1	1	0	1	Reserved	—
1	1	1	0	Reserved	—
1	1	1	1	DMK	Read/Write

Word I/O instructions can be used to read/write the register pairs listed below. All other registers are accessed via byte I/O instructions.

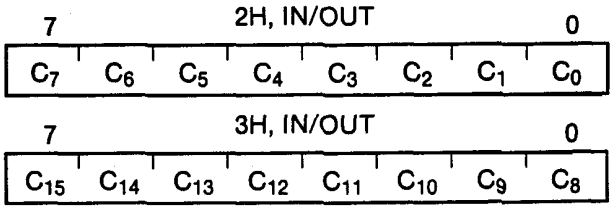
DBC/DCC
DBA/DCA (higher/lower only)
DDC

DMAU Registers

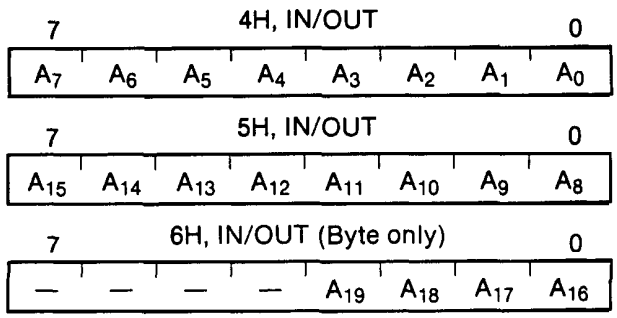
Initialize. The DMA initialize command (DICM) register (figure 38) is used to perform a software reset of the DMAU. The DICM is accessed using the byte OUT instruction.

Channel Register. Writes to the DMA channel (DCH) register (figure 39) select one of the four DMA channels for programming and also the base/current registers. Reads of the DCH register return the currently-selected channel and the register access mode.

Count Registers. When bit 2 of the DCH register is cleared, a write to the DMA count register updates both the DMA base count (DBC) and the DMA current count (DCC) registers with a new count. If bit 2 of the DCH register is set, a write to the DMA count register affects only the DBC register. The DBC register holds the initial count value until a new count is specified. If autoinitialization is enabled, this value is transferred to the DCC register when a terminal count or END condition occurs. For each DMA transfer, the current count register is decremented by one. The format of the DMA count register is shown below. The count value loaded into the DBC/DCC registers is one less than the desired transfer count.



Address Register. Use either byte or word I/O instructions with the lower two bytes (4H and 5H) of the DMA address register. However, *byte I/O instructions* must be used to access the high-order byte (6H) of this register. When bit 2 of the channel register is cleared, a write to the DMA address register updates both the DMA base address (DBA) and the DMA current address (DCA) registers with the new address. If bit 2 of the DCH register is set, a write to the DMA address register affects only the DBA register.



The DBA register holds the starting address value until a new address is specified. This value is transferred to the DCA register automatically if autoinitialization is selected. For each DMA transfer, the current address register is incremented/decremented by one.

Device Control Register. The DMA device control (DDC) register (figure 40) is used to to program the DMA transfer characteristics common to all DMA channels. It controls the bus mode, write timing, priority logic, and enable/disable of the DMAU.

Status Register. The DMA status (DST) register (figure 41) contains information about the current state of each DMA channel. Software can determine if a termination condition has been reached (TC_3-TC_0) or if a DMA service request is present (RQ_3-RQ_0). The byte IN instruction must be used to read this register.

Figure 37. Bus Waiting Operation

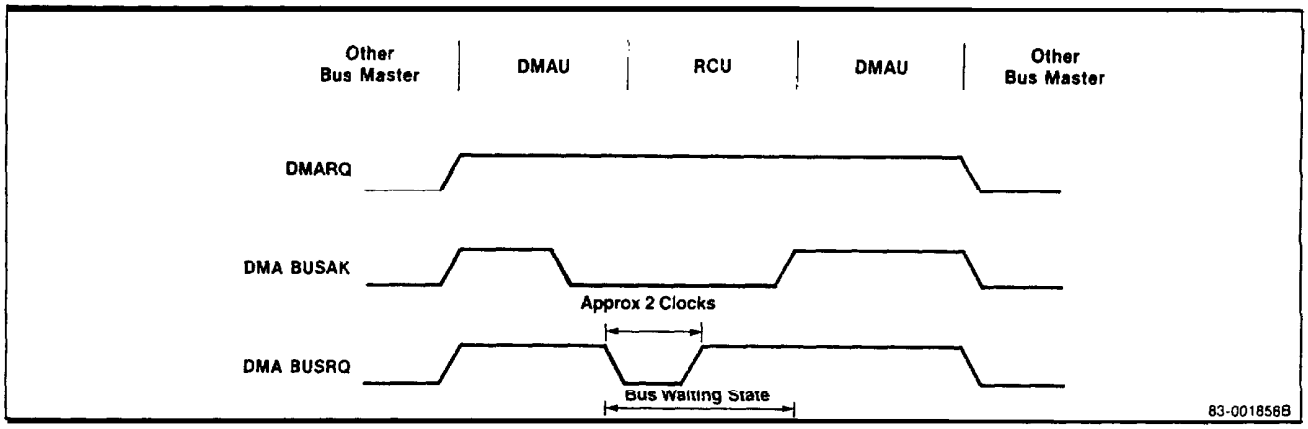


Figure 38. DMA Initialize Command Register

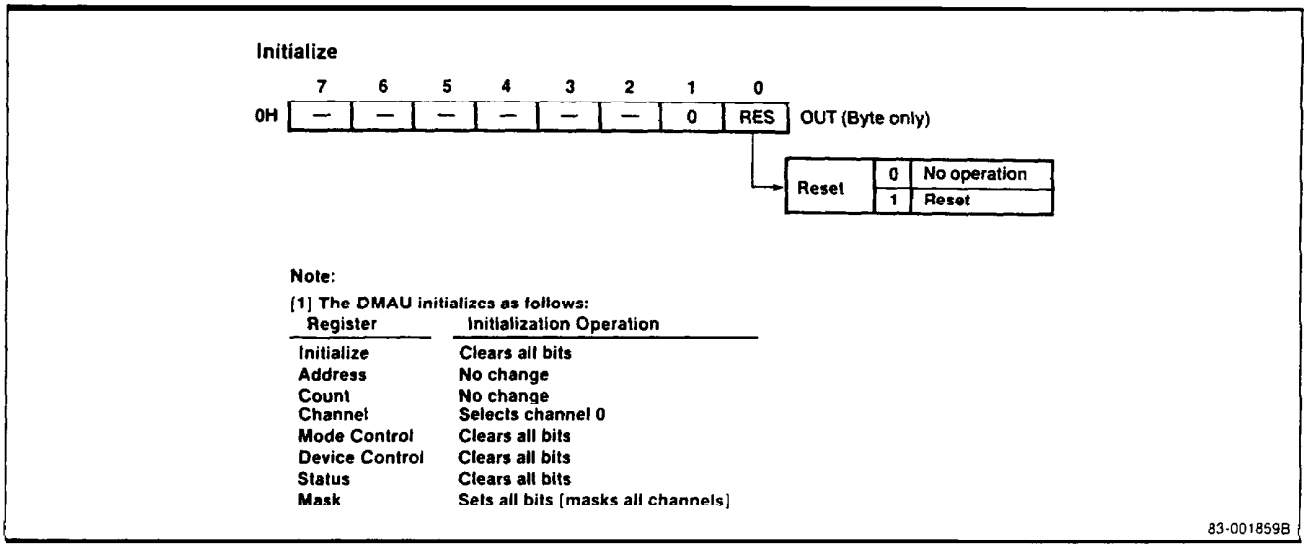


Figure 39. DMA Channel Register

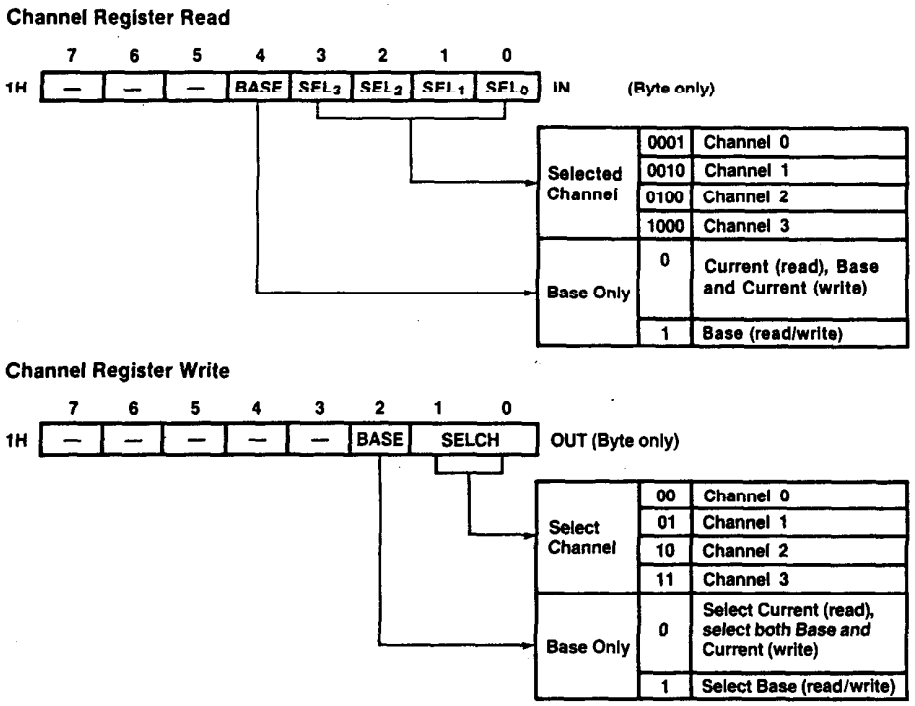
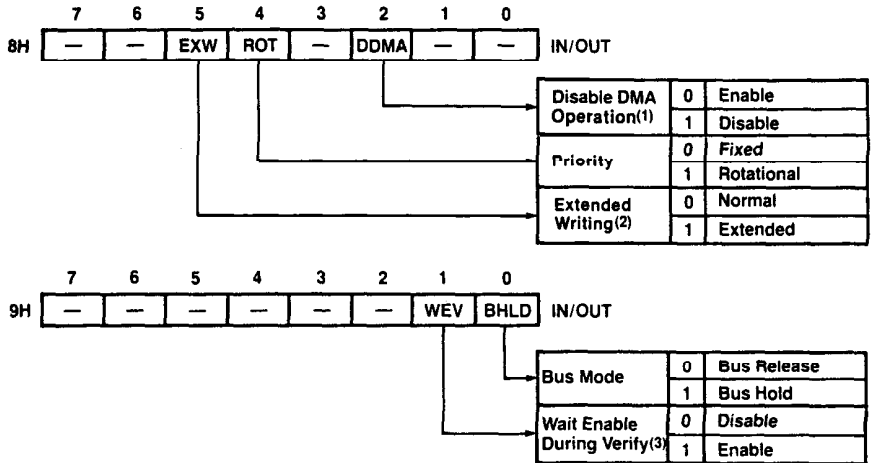


Figure 40. DMA Device Control Register



Note:

[1] Disables BUSRQ to the BAU to prevent incorrect DMA operation while the DMAU registers are being initialized or modified.

[2] When EXW is 0, the write signal becomes active [normal write] during T3 and TW [see timing waveforms]. When 1, the write signal becomes active during T2, T3, and TW [like the read signal].

[3] Wait states are generated by the READY signal during a verify transfer.

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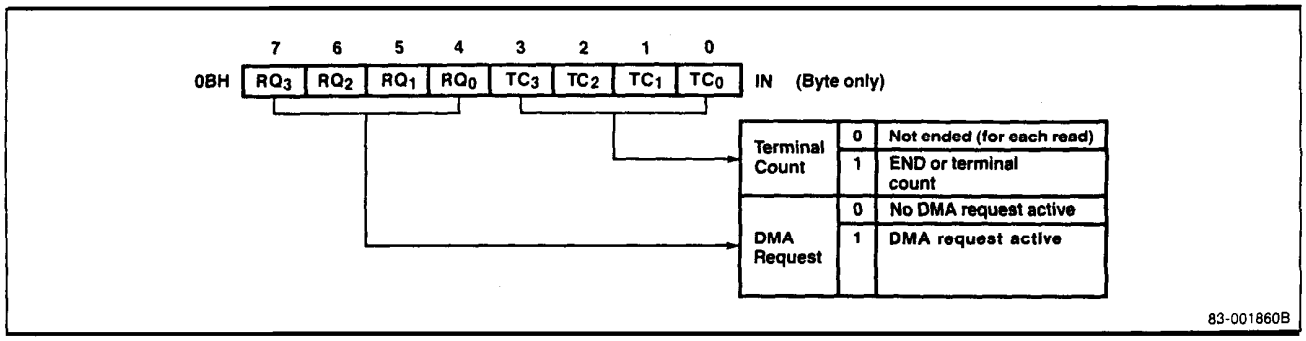
Figure 41. DMA Status Register



Mode Control Register. The DMA mode (DMD) register (figure 42) selects the operating mode for each DMA channel. The DCH register selects which DMD register will be accessed. A byte IN/OUT instruction must be used to access this register.

Mask Register Read/Write. The DMA mask (DMK) register (figure 43) allows software to individually enable and disable DMA channels. The DMK register can only be accessed via byte I/O instructions.

Reset

The falling edge of the $\overline{RESET}$ signal resets the μPD70208. The signal must be held low for at least four clock cycles to be recognized as valid.

CPU Reset State Register	Reset Value
PFP	0000H
PC	0000H
PS	FFFFH
SS	0000H
DS0	0000H
DS1	0000H
PSW	F002H
AW, BW, CW, DW, IX, IY, BP, SP	Undefined
Instruction queue	Cleared

When $\overline{RESET}$ returns to the high level, the CPU will start fetching instructions from physical address FFFF0H.

Internal Peripheral Devices

Internal peripheral devices initialized on reset are listed in the following table. I/O devices not listed are not initialized on reset and must be initialized by software.

	Register	Reset Value
System I/O area	OPCN	----0000
	OPSEL	----0000
	WCY1	11111111
	WCY2	----1111
	TCKS	---00000
	RFC	x--01000
SCU	SMD	01001011
	SCM	--0000-0
	SIMK	------11
	SST	10000100
	DCH	---00001
	DMD	000000-0
DMAU	DDC (low)	--00-0--
	DDC (high)	------00
	DST	xxxx0000
	DMK	----1111

Symbols: x = unaffected; 0 = cleared; 1 = set; (-) = unused

Output Pin Status

The following table lists output pin status during reset.

Signal	Status
$\overline{INTAK}$, $\overline{BUFEN}$, $\overline{BUFR}$/W, $\overline{MRD}$, $\overline{MWR}$, $\overline{END}$/$\overline{TC}$, $\overline{IOWR}$, $\overline{IORD}$, $\overline{REFRQ}$, BS_2-BS_0, $\overline{BUSLOCK}$, RESOUT, $\overline{DMAAK3}$-$\overline{DMAAK0}$	High level
QS_1-QS_0, ASTB, HLDAK	Low level
A_{19}-A_{16}/PS_3-PS_0, TOUT2	High or low level
A_{15}-A_8, AD_7-AD_0	High impedance
CLKOUT	Continues to supply clock

Figure 42. DMA Mode Register

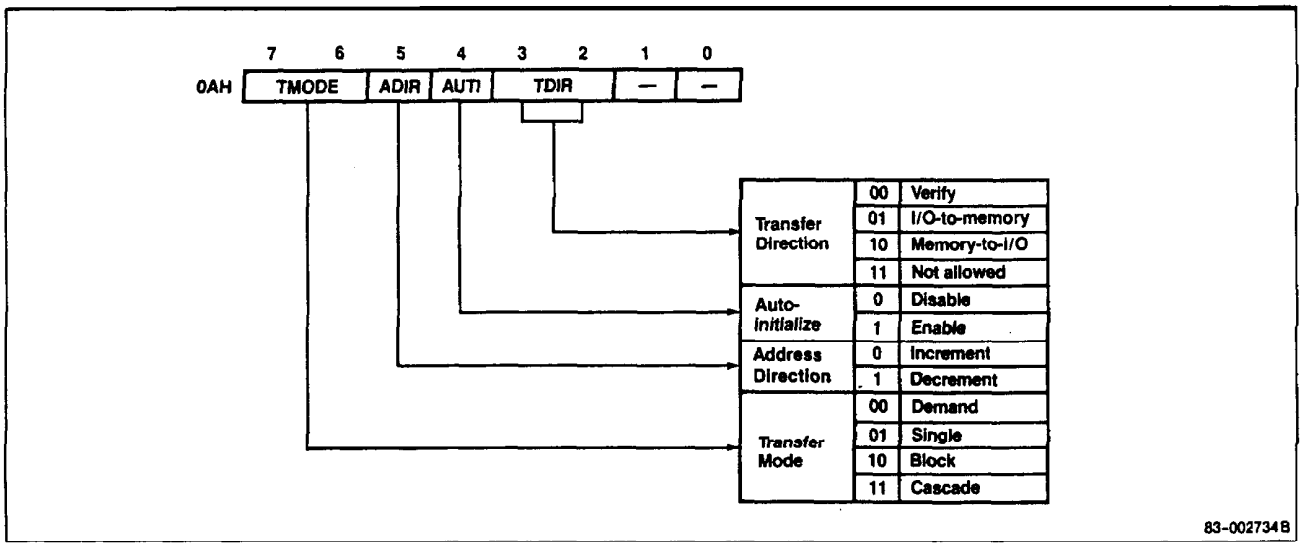
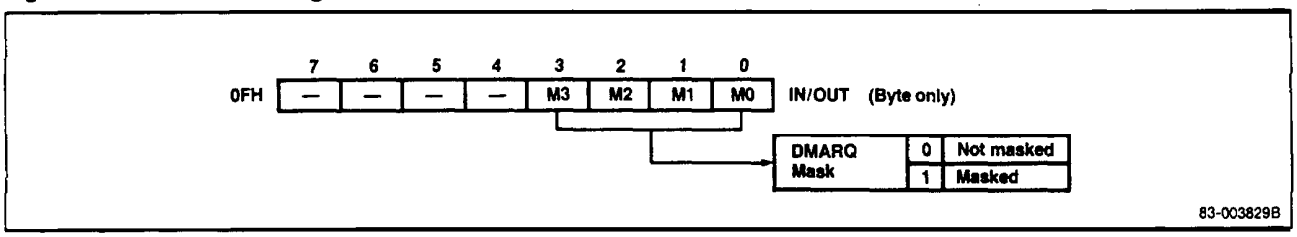


Figure 43. DMA Mask Register



Instruction Set

Symbols

Preceding the instruction set, several tables explain symbols, abbreviations, and codes.

Clocks

In the Clocks column of the instruction set, the numbers cover these operations: instruction decoding, effective address calculation, operand fetch, and instruction execution.

Clock timings assume the instruction has been prefetched and is present in the four-byte instruction queue. Otherwise, add four clocks for each byte not present.

For instructions that reference memory operands, the number on the left side of the slash (/) is for byte operands and the number on the right side is for word operands.

For conditional control transfer or branch instructions, the number on the left side of the slash is applicable if the transfer or branch takes place. The number on the right side is applicable if it does not take place.

If a range of numbers is given, the execution time depends on the operands involved.

Symbols

Symbol	Meaning
acc	Accumulator (AW or AL)
disp	Displacement (8 or 16 bits)
dmem	Direct memory address
dst	Destination operand or address
ext-disp8	16-bit displacement (sign-extension byte + 8-bit displacement)
far_label	Label within a different program segment
far_proc	Procedure within a different program segment
fp_op	Floating point instruction operation
imm	8- or 16-bit immediate operand
imm3/4	3/4-bit immediate bit offset
imm8	8-bit immediate operand
imm16	16-bit immediate operand
mem	Memory field (000 to 111): 8- or 16-bit memory location

Symbols

Symbol	Meaning
mem8	8-bit memory location
mem16	16-bit memory location
mem32	32-bit memory location
memptr16	Word containing the destination address within the current segment
memptr32	Double word containing a destination address in another segment
mod	Mode field (00 to 10)
near_label	Label within the current segment
near_proc	Procedure within the current segment
offset	Immediate offset data (16 bits)
pop_value	Number of bytes to discard from the stack
reg	Register field (000 to 111); 8- or 16-bit general-purpose register
reg8	8-bit general-purpose register
reg16	16-bit general-purpose register
regptr	16-bit register containing a destination address within the current segment
regptr16	Register containing a destination address within the current segment
seg	Immediate segment data (16 bits)
short_label	Label between −128 and +127 bytes from the end of the current instruction
sr	Segment register
src	Source operand or address
temp	Temporary register (8/16/32 bits)
tmpcy	Temporary carry flag (1 bit)
AC	Auxiliary carry flag
AH	Accumulator (high byte)
AL	Accumulator (low byte)
AND	Logical product
AW	Accumulator (16 bits)
BH	BW register (high byte)
BL	BW register (low byte)
BP	BP register
BRK	Break flag
BW	BW register (16 bits)
CH	CW register (high byte)
CL	CW register (low byte)
CW	CW register (16 bits)
CY	Carry flag
DH	DW register (high byte)
DIR	Direction flag
DL	DW register (low byte)

3

Symbols (cont)

Symbol	Meaning
DS0	Data segment 0 register (16 bits)
DS1	Data segment 1 register (16 bits)
DW	DW register (16 bits)
IE	Interrupt enable flag
IX	Index register (source) (16 bits)
IY	Index register (destination) (16 bits)
MD	Mode flag
OR	Logical sum
P	Parity flag
PC	Program counter (16 bits)
PS	Program segment register (16 bits)
PSW	Program status word (16 bits)
R	Register set
S	Sign extend operand field S = 0 No sign extension S = 1 Sign extend immediate byte operand
S	Sign flag
SP	Stack pointer (16 bits)
SS	Stack segment register (16 bits)
V	Overflow flag
W	Word/byte field (0 to 1)
X, XXX, YYY, ZZZ	Data to identify the instruction code of the external floating point arithmetic chip
XOR	Exclusive logical sum
XXH	Two-digit hexadecimal value
XXXXH	Four-digit hexadecimal value
Z	Zero flag
( )	Values in parentheses are memory contents
←	Transfer direction
+	Addition
−	Subtraction
x	Multiplication
÷	Division
%	Modulo

Flag Operations

Symbol	Meaning
(blank)	No change
0	Cleared to 0
1	Set to 1
x	Set or cleared according to result
u	Undefined
R	Restored to previous state

Memory Addressing Modes

mem	mod = 00	mod = 01	mod = 10
000	BW + IX	BW + IX + disp8	BW + IX + disp16
001	BW + IY	BW + IY + disp8	BW + IY + disp16
010	BP + IX	BP + IX + disp8	BP + IX + disp16
011	BP + IY	BP + IY + disp8	BP + IY + disp16
100	IX	IX + disp8	IX + disp16
101	IY	IY + disp8	IY + disp16
110	Direct	BP + disp8	BP + disp16
111	BW	BW + disp8	BW + disp16

Register Selection (mod = 11)

reg	W = 0	W = 1
000	AL	AW
001	CL	CW
010	DL	DW
011	BL	BW
100	AH	SP
101	CH	BP
110	DH	IX
111	BH	IY

Segment Register Selection

sr	Segment Register
00	DS1
01	PS
10	SS
11	DS0

Instruction Set

Mnemonic	Operand	Opcode 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Clocks	Bytes	Flags AC	CY	V	P	S	Z
Data Transfer Instructions																									
MOV	reg, reg	1	0	0	0	1	0	1	W	1	1	reg				reg		2	2						
	mem, reg	1	0	0	0	1	0	0	W	mod		reg				mem		7/11	2-4						
	reg, mem	1	0	0	0	1	0	1	W	mod		reg				mem		10/14	2-4						
	mem, imm	1	1	0	0	0	1	1	W	mod		reg				mem		9/13	3-6						
	reg, imm	1	0	1	1	W		reg										4	2-3						
	acc, dmem	1	0	1	0	0	0	0	W									10/14	3						
	dmem, acc	1	0	1	0	0	0	1	W									9/13	3						
	sr, reg16	1	0	0	0	1	1	1	0	1	1	0	sr			reg		2	2						
	sr, mem16	1	0	0	0	1	1	1	0	mod		0	sr			mem		14	2-4						
	reg16, sr	1	0	0	0	1	1	0	0	1	1	0	sr			reg		2	2						
	mem16, sr	1	0	0	0	1	1	0	0	mod		0	sr			mem		12	2-4						
	DS0, reg16, mem32	1	1	0	0	0	1	0	1	mod		reg				mem		25	2-4						
	DS1, reg16, mem32	1	1	0	0	0	1	0	0	mod		reg				mem		25	2-4						
	AH, PSW	1	0	0	1	1	1	1	1									2	1						
	PSW, AH	1	0	0	1	1	1	1	0									3	1	x	x		x	x	x
LDEA	reg16, mem16	1	0	0	0	1	1	0	1	mod		reg				mem		4	2-4						
TRANS	src_table	1	1	0	1	0	1	1	1									9	1						
XCH	reg, reg	1	0	0	0	0	1	1	W	1	1	reg				reg		3	2						
	mem, reg	1	0	0	0	0	1	1	W	mod		reg				mem		13/21	2-4						
	AW, reg16	1	0	0	1	0		reg										3	1						
Repeat Prefixes																									
REPC		0	1	1	0	0	1	0	1									2	1						
REPNC		0	1	1	0	0	1	0	0									2	1						
REP REPE REPZ		1	1	1	1	0	0	1	1									2	1						
REPNE REPNZ		1	1	1	1	0	0	1	0									2	1						
Block Transfer Instructions																									
MOVBK	dst, src	1	0	1	0	0	1	0	W									1 9 (9) + 8n (W = 0) 9 (17) + 16n (W = 1)							
CMPBK	dst, src	1	0	1	0	0	1	1	W									1 7 (13) + 14n (W = 0) 7 (21) + 22n (W = 1)		x	x	x	x	x	x
CMPM	dst	1	0	1	0	1	1	1	W									1 7 (7) + 10n (W = 0) 7 (11) + 14n (W = 1)		x	x	x	x	x	x
LDM	src	1	0	1	0	1	1	0	W									1 7 (7) + 9n (W = 0) 7 (11) + 13n (W = 1)							
STM	dst	1	0	1	0	1	0	1	W									1 5 (5) + 4n (W = 0) 5 (9) + 8n (W = 1)							

n = number of transfers
String instruction execution clocks for a single instruction execution are in parentheses.

3

Instruction Set (cont)

Mnemonic	Operand	Opcode 7 6 5 4 3 2 1 0	Opcode 7 6 5 4 3 2 1 0	Clocks	Bytes	Flags AC CY V P S Z
I/O Instructions						
IN	acc, imm8	1 1 1 0 0 1 0 W		9/13	2	
	acc, DW	1 1 1 0 1 1 0 W		8/12	1	
OUT	imm8, acc	1 1 1 0 0 1 1 W		8/12	2	
	DW, acc	1 1 1 0 1 1 1 W		8/12	1	
INM	dst, DW	0 1 1 0 1 1 0 W		9 (10) + 8n (W = 0) 9 (18) + 16n (W = 1)	1	
OUTM	DW, src	0 1 1 0 1 1 1 W		9 (10) + 8n (W = 0) 9 (18) + 16n (W = 1)	1	
		n = number of transfers String instruction execution clocks for a single instruction execution are in parentheses.				
BCD Instructions						
ADJBA		0 0 1 1 0 1 1 1		7	1	x x u u u u
ADJ4A		0 0 1 0 0 1 1 1		3	1	x x u x x x
ADJBS		0 0 1 1 1 1 1 1		7	1	x x u u u u
ADJ4S		0 0 1 0 1 1 1 1		3	1	x x u x x x
ADD4S	dst, src	0 0 0 0 1 1 1 1	0 0 1 0 0 0 0 0	7 + 19n	2	u x u u u x
SUB4S	dst, src	0 0 0 0 1 1 1 1	0 0 1 0 0 0 1 0	7 + 19n	2	u x u u u x
CMP4S	dst, src	0 0 0 0 1 1 1 1	0 0 1 0 0 1 1 0	7 + 19n	2	u x u u u x
ROL4	reg8	0 0 0 0 1 1 1 1 1 1 0 0 0 reg	0 0 1 0 1 0 0 0	13	3	
	mem8	0 0 0 0 1 1 1 1 mod 0 0 0 mem	0 0 1 0 1 0 0 0	25	3-5	
ROR4	reg8	0 0 0 0 1 1 1 1 1 1 0 0 0 reg	0 0 1 0 1 0 1 0	17	3	
	mem8	0 0 0 0 1 1 1 1 mod 0 0 0 mem	0 0 1 0 1 0 1 0	29	3-5	
		n = number of BCD digits divided by 2				
Data Type Conversion Instructions						
CVTBD		1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0	15	2	u u u x x x
CVTDB		1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0	7	2	u u u x x x
CVTBW		1 0 0 1 1 0 0 0		2	1	
CVTWL		1 0 0 1 1 0 0 1		4/5	1	
Arithmetic Instructions						
ADD	reg, reg	0 0 0 0 0 0 1 W	1 1 reg reg	2	2	x x x x x x
	mem, reg	0 0 0 0 0 0 0 W	mod reg mem	13/21	2-4	x x x x x x
	reg, mem	0 0 0 0 0 0 1 W	mod reg mem	10/14	2-4	x x x x x x
	reg, imm	1 0 0 0 0 0 S W	1 1 0 0 0 reg	4	3 4	x x x x x x
	mem, imm	1 0 0 0 0 0 S W	mod 0 0 0 mem	15/23	3-6	x x x x x x
	acc, imm	0 0 0 0 0 1 0 W		4	2-3	x x x x x x

Instruction Set (cont)

Mnemonic	Operand	Opcode 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Clocks	Bytes	Flags AC	CY	V	P	S	Z
Arithmetic Instructions (cont)																									
ADDC	reg, reg	0	0	0	1	0	0	1	W	1	1		reg			reg		2	2	x	x	x	x	x	x
	mem, reg	0	0	0	1	0	0	0	W	mod			reg			mem		13/21	2-4	x	x	x	x	x	x
	reg, mem	0	0	0	1	0	0	1	W	mod			reg			mem		10/14	2-4	x	x	x	x	x	x
	reg, imm	1	0	0	0	0	0	S	W	1	1	0	1	0		reg		4	3-4	x	x	x	x	x	x
	mem, imm	1	0	0	0	0	0	S	W	mod		0	1	0		mem		15/23	3-6	x	x	x	x	x	x
	acc, imm	0	0	0	1	0	1	0	W									4	2-3	x	x	x	x	x	x
SUB	reg, reg	0	0	1	0	1	0	1	W	1	1		reg			reg		2	2	x	x	x	x	x	x
	mem, reg	0	0	1	0	1	0	0	W	mod			reg			mem		13/21	2-4	x	x	x	x	x	x
	reg, mem	0	0	1	0	1	0	1	W	mod			reg			mem		10/14	2-4	x	x	x	x	x	x
	reg, imm	1	0	0	0	0	0	S	W	1	1	1	0	1		reg		4	3-4	x	x	x	x	x	x
	mem, imm	1	0	0	0	0	0	S	W	mod		1	0	1		mem		15/23	3-6	x	x	x	x	x	x
	acc, imm	0	0	1	0	1	1	0	W									4	2-3	x	x	x	x	x	x
SUBC	reg, reg	0	0	0	1	1	0	1	W	1	1		reg			reg		2	2	x	x	x	x	x	x
	mem, reg	0	0	0	1	1	0	0	W	mod			reg			mem		13/21	2-4	x	x	x	x	x	x
	reg, mem	0	0	0	1	1	0	1	W	mod			reg			mem		10/14	2-4	x	x	x	x	x	x
	reg, imm	1	0	0	0	0	0	S	W	1	1	0	1	1		reg		4	3-4	x	x	x	x	x	x
	mem, imm	1	0	0	0	0	0	S	W	mod		0	1	1		mem		15/23	3-6	x	x	x	x	x	x
	acc, imm	0	0	0	1	1	1	0	W									4	2-3	x	x	x	x	x	x
INC	reg8	1	1	1	1	1	1	1	0	1	1	0	0	0		reg		2	2	x		x	x	x	x
	mem	1	1	1	1	1	1	1	W	mod		0	0	0		mem		13/21	2-4	x		x	x	x	x
	reg16	0	1	0	0	0		reg										2	1	x		x	x	x	x
DEC	reg8	1	1	1	1	1	1	1	0	1	1	0	0	1		reg		2	2	x		x	x	x	x
	mem	1	1	1	1	1	1	1	W	mod		0	0	1		mem		13/21	2-4	x		x	x	x	x
	reg16	0	1	0	0	1		reg										2	1	x		x	x	x	x
MULU	reg	1	1	1	1	0	1	1	W	1	1	1	0	0		reg		21-30	2	u	x	x	u	u	u
	mem	1	1	1	1	0	1	1	W	mod		1	0	0		mem		26/39	2-4	u	x	x	u	u	u
MUL	reg	1	1	1	1	0	1	1	W	1	1	1	0	1		reg		33-47	2	u	x	x	u	u	u
	mem	1	1	1	1	0	1	1	W	mod		1	0	1		mem		38-56	2-4	u	x	x	u	u	u
	reg16,reg16,imm8	0	1	1	0	1	0	1	1	1	1		reg			reg		28-34	3	u	x	x	u	u	u
	reg16,mem16,imm8	0	1	1	0	1	0	1	1	mod			reg			mem		37-43	3-5	u	x	x	u	u	u
	reg16,reg16,imm16	0	1	1	0	1	0	0	1	1	1		reg			reg		36-42	4	u	x	x	u	u	u
	reg16,mem16,imm16	0	1	1	0	1	0	0	1	mod			reg			mem		45-51	4-6	u	x	x	u	u	u
DIVU	reg	1	1	1	1	0	1	1	W	1	1	1	1	0		reg		19/25	2	u	u	u	u	u	u
	mem	1	1	1	1	0	1	1	W	mod		1	1	0		mem		24/34	2-4	u	u	u	u	u	u
DIV	reg	1	1	1	1	0	1	1	W	1	1	1	1	1		reg		29-43	2	u	u	u	u	u	u
	mem	1	1	1	1	0	1	1	W	mod		1	1	1		mem		34-52	2-4	u	u	u	u	u	u

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Instruction Set (cont)

Mnemonic	Operand	Opcode 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Clocks	Bytes	Flags AC	CY	V	P	S	Z
Comparison Instructions																									
CMP	reg, reg	0	0	1	1	1	0	1	W	1	1		reg				reg	2	2	x	x	x	x	x	x
	mem, reg	0	0	1	1	1	0	0	W	mod			reg				mem	10/14	2-4	x	x	x	x	x	x
	reg, mem	0	0	1	1	1	0	1	W	mod			reg				mem	10/14	2-4	x	x	x	x	x	x
	reg, imm	1	0	0	0	0	0	S	W	1	1	1	1	1		reg		4	3-4	x	x	x	x	x	x
	mem, imm	1	0	0	0	0	0	S	W	mod			1	1	1	mem		12/16	3-6	x	x	x	x	x	x
	acc, imm	0	0	1	1	1	1	0	W									4	2-3	x	x	x	x	x	x
Logical Instructions																									
NOT	reg	1	1	1	1	0	1	1	W	1	1	0	1	0		reg		2	2						
	mem	1	1	1	1	0	1	1	W	mod		0	1	0		mem		13/21	2-4						
NEG	reg	1	1	1	1	0	1	1	W	1	1	0	1	1		reg		2	2	x	x	x	x	x	x
	mem	1	1	1	1	0	1	1	W	mod		0	1	1		mem		13/21	2-4	x	x	x	x	x	x
TEST	reg, reg	1	0	0	0	0	1	0	W	1	1		reg			reg		2	2	u	0	0	x	x	x
	mem, reg	1	0	0	0	0	1	0	W	mod			reg			mem		9/13	2-4	u	0	0	x	x	x
	reg, imm	1	1	1	1	0	1	1	W	1	1	0	0	0		reg		4	3-4	u	0	0	x	x	x
	mem, imm	1	1	1	1	0	1	1	W	mod			0	0	0	mem		10/14	3-6	u	0	0	x	x	x
	acc, imm	1	0	1	0	1	0	0	W									4	2-3	u	0	0	x	x	x
AND	reg, reg	0	0	1	0	0	0	1	W	1	1		reg			reg		2	2	u	0	0	x	x	x
	mem, reg	0	0	1	0	0	0	0	W	mod			reg			mem		13/21	2-4	u	0	0	x	x	x
	reg, mem	0	0	1	0	0	0	1	W	mod			reg			mem		10/14	2-4	u	0	0	x	x	x
	reg, imm	1	0	0	0	0	0	0	W	1	1	1	0	0		reg		4	3-4	u	0	0	x	x	x
	mem, imm	1	0	0	0	0	0	0	W	mod			1	0	0	mem		15/23	3-6	u	0	0	x	x	x
	acc, imm	0	0	1	0	0	1	0	W									4	2-3	u	0	0	x	x	x
OR	reg, reg	0	0	0	0	1	0	1	W	1	1		reg			reg		2	2	u	0	0	x	x	x
	mem, reg	0	0	0	0	1	0	0	W	mod			reg			mem		13/21	2-4	u	0	0	x	x	x
	reg, mem	0	0	0	0	1	0	1	W	mod			reg			mem		10/14	2-4	u	0	0	x	x	x
	reg, imm	1	0	0	0	0	0	0	W	1	1	0	0	1		reg		4	3-4	u	0	0	x	x	x
	mem, imm	1	0	0	0	0	0	0	W	mod			0	0	1	mem		15/23	3-6	u	0	0	x	x	x
	acc, imm	0	0	1	0	0	1	0	W									4	2-3	u	0	0	x	x	x
XOR	reg, reg	0	0	1	1	0	0	1	W	1	1		reg			reg		2	2	u	0	0	x	x	x
	mem, reg	0	0	1	1	0	0	0	W	mod			reg			mem		13/21	2-4	u	0	0	x	x	x
	reg, mem	0	0	1	1	0	0	1	W	mod			reg			mem		10/14	2-4	u	0	0	x	x	x
	reg, imm	1	0	0	0	0	0	0	W	1	1	1	1	0		reg		4	3-4	u	0	0	x	x	x
	mem, imm	1	0	0	0	0	0	0	W	mod			1	1	0	mem		15/23	3-6	u	0	0	x	x	x
	acc, imm	0	0	1	0	0	1	0	W									4	2-3	u	0	0	x	x	x

Instruction Set (cont)

Mnemonic	Operand	Opcode 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Clocks	Bytes	Flags AC	CY	V	P	S	Z
Bit Manipulation Instructions																									
INS	reg8, reg8	0	0	0	0	1	1	1	1	0	0	1	1	0	0	0	1	35-133	3						
		1	1		reg			reg																	
	reg8, imm8	0	0	0	0	1	1	1	1	0	0	1	1	1	0	0	1	35-133	4						
		1	1	0	0	0		reg																	
EXT	reg8, reg8	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	1	34-59	3						
		1	1		reg			reg																	
	reg8, imm8	0	0	0	0	1	1	1	1	0	0	1	1	1	0	1	1	34-59	4						
		1	1	0	0	0		reg																	
TEST1	reg, CL	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	W	3	3	u	0	0	u	u	x
		1	1	0	0	0		reg																	
	mem, CL	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	W	7/11	3-5	u	0	0	u	u	x
		mod		0	0	0		mem																	
	reg, imm3/4	0	0	0	0	1	1	1	1	0	0	0	1	1	0	0	W	4	4	u	0	0	u	u	x
		1	1	0	0	0		reg																	
	mem, imm3/4	0	0	0	0	1	1	1	1	0	0	0	1	1	0	0	W	8/12	4-6	u	0	0	u	u	x
		mod		0	0	0		mem																	
SET1	reg, CL	0	0	0	0	1	1	1	1	0	0	0	1	0	1	0	W	4	3						
		1	1	0	0	0		reg																	
	mem, CL	0	0	0	0	1	1	1	1	0	0	0	1	0	1	0	W	10/18	3-5						
		mod		0	0	0		mem																	
	reg, imm3/4	0	0	0	0	1	1	1	1	0	0	0	1	1	1	0	W	5	4						
		1	1	0	0	0		reg																	
	mem, imm3/4	0	0	0	0	1	1	1	1	0	0	0	1	1	1	0	W	11/19	4-6						
		mod		0	0	0		mem																	
	CY	1	1	1	1	1	0	0	1									2	1		1				
	DIR	1	1	1	1	1	1	0	1									2	1						
CLR1	reg, CL	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	W	5	3						
		1	1	0	0	0		reg																	
	mem, CL	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	W	11/19	3-5						
		mod		0	0	0		mem																	
	reg, imm3/4	0	0	0	0	1	1	1	1	0	0	0	1	1	0	1	W	6	4						
		1	1	0	0	0		reg																	
	mem, imm3/4	0	0	0	0	1	1	1	1	0	0	0	1	1	0	1	W	12/20	4-6						
		mod		0	0	0		mem																	
	CY	1	1	1	1	1	0	0	0									2	1		0				
	DIR	1	1	1	1	1	1	0	0									2	1						
NOT1	reg, CL	0	0	0	0	1	1	1	1	0	0	0	1	0	1	1	W	4	3						
		1	1	0	0	0		reg																	
	mem, CL	0	0	0	0	1	1	1	1	0	0	0	1	0	1	1	W	10/18	3-5						
		mod		0	0	0		mem																	
	reg, imm3/4	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	W	5	4						
		1	1	0	0	0		reg																	
	mem, imm3/4	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	W	11/19	4-6						
		mod		0	0	0		mem																	
	CY	1	1	1	1	0	1	0	1									2	1		x				

Instruction Set (cont)

Mnemonic	Operands	Opcode 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Clocks	Bytes	Flags AC	CY	V	P	S	Z
Shift/Rotate Instructions																									
SHL	reg, 1	1	1	0	1	0	0	0	W	1	1	1	0	0		reg		2	2	u	x	x	x	x	x
	mem, 1	1	1	0	1	0	0	0	W	mod			1	0	0	mem		13/21	2-4	u	x	x	x	x	x
	reg, CL	1	1	0	1	0	0	1	W	1	1	1	0	0		reg		7 + n	2	u	x	u	x	x	x
	mem, CL	1	1	0	1	0	0	1	W	mod			1	0	0	mem		16/24 + n	2-4	u	x	u	x	x	x
	reg, imm8	1	1	0	0	0	0	0	W	1	1	1	0	0		reg		7 + n	3	u	x	u	x	x	x
	mem, imm8	1	1	0	0	0	0	0	W	mod			1	0	0	mem		16/24 + n	3-5	u	x	u	x	x	x
SHR	reg, 1	1	1	0	1	0	0	0	W	1	1	1	0	1		reg		2	2	u	x	x	x	x	x
	mem, 1	1	1	0	1	0	0	0	W	mod			1	0	1	mem		13/21	2-4	u	x	x	x	x	x
	reg, CL	1	1	0	1	0	0	1	W	1	1	1	0	1		reg		7 + n	2	u	x	u	x	x	x
	mem, CL	1	1	0	1	0	0	1	W	mod			1	0	1	mem		16/24 + n	2-4	u	x	u	x	x	x
	reg, imm8	1	1	0	0	0	0	0	W	1	1	1	0	1		reg		7 + n	3	u	x	u	x	x	x
	mem, imm8	1	1	0	0	0	0	0	W	mod			1	0	1	mem		16/24 + n	3-5	u	x	u	x	x	x
SHRA	reg, 1	1	1	0	1	0	0	0	W	1	1	1	1	1		reg		2	2	u	x	0	x	x	x
	mem, 1	1	1	0	1	0	0	0	W	mod			1	1	1	mem		13/21	2-4	u	x	0	x	x	x
	reg, CL	1	1	0	1	0	0	1	W	1	1	1	1	1		reg		7 + n	2	u	x	u	x	x	x
	mem, CL	1	1	0	1	0	0	1	W	mod			1	1	1	mem		16/24 + n	2-4	u	x	u	x	x	x
	reg, imm8	1	1	0	0	0	0	0	W	1	1	1	1	1		reg		7 + n	3	u	x	u	x	x	x
	mem, imm8	1	1	0	0	0	0	0	W	mod			1	1	1	mem		16/24 + n	3-5	u	x	u	x	x	x
ROL	reg, 1	1	1	0	1	0	0	0	W	1	1	0	0	0		reg		2	2		x	x			
	mem, 1	1	1	0	1	0	0	0	W	mod			0	0	0	mem		13/21	2-4		x	x			
	reg, CL	1	1	0	1	0	0	1	W	1	1	0	0	0		reg		7 + n	2		x	u			
	mem, CL	1	1	0	1	0	0	1	W	mod			0	0	0	mem		16/24 + n	2-4		x	u			
	reg, imm	1	1	0	0	0	0	0	W	1	1	0	0	0		reg		7 + n	3		x	u			
	mem, imm	1	1	0	0	0	0	0	W	mod			0	0	0	mem		16/24 + n	3-5		x	u			
ROR	reg, 1	1	1	0	1	0	0	0	W	1	1	0	0	1		reg		2	2		x	u			
	mem, 1	1	1	0	1	0	0	0	W	mod			0	0	1	mem		13/21	2-4		x	x			
	reg, CL	1	1	0	1	0	0	1	W	1	1	0	0	1		reg		7 + n	2		x	u			
	mem, CL	1	1	0	1	0	0	1	W	mod			0	0	1	mem		16/24 + n	2-4		x	u			
	reg, imm8	1	1	0	0	0	0	0	W	1	1	0	0	1		reg		7 + n	3		x	u			
	mem, imm8	1	1	0	0	0	0	0	W	mod			0	0	1	mem		16/24 + n	3-5		x	u			
ROLC	reg, 1	1	1	0	1	0	0	0	W	1	1	0	1	0		reg		2	2		x	x			
	mem, 1	1	1	0	1	0	0	0	W	mod			0	1	0	mem		13/21	2-4		x	x			
	reg, CL	1	1	0	1	0	0	1	W	1	1	0	1	0		reg		7 + n	2		x	u			
	mem, CL	1	1	0	1	0	0	1	W	mod			0	1	0	mem		16/24 + n	2-4		x	u			
	reg, imm8	1	1	0	0	0	0	0	W	1	1	0	1	0		reg		7 + n	3		x	u			
	mem, imm8	1	1	0	0	0	0	0	W	mod			0	1	0	mem		16/24 + n	3-5		x	u			

n = number of shifts

Instruction Set (cont)

Mnemonic	Operands	Opcode 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Clocks	Bytes	Flags AC	CY	V	P	S	Z
Shift Rotate Instructions (cont)																									
RORC	reg, 1	1	1	0	1	0	0	0	W	1	1	0	1	1	reg			2	2		x	x			
	mem, 1	1	1	0	1	0	0	0	W	mod		0	1	1	mem			13/21	2-4		x	x			
	reg, CL	1	1	0	1	0	0	1	W	1	1	0	1	1	reg			7 + n	2		x	u			
	mem, CL	1	1	0	1	0	0	1	W	mod		0	1	1	mem			16/24 + n	2-4		x	u			
	reg, imm8	1	1	0	0	0	0	0	W	1	1	0	1	1	reg			7 + n	3		x	u			
	mem, imm8	1	1	0	0	0	0	0	W	mod		0	1	1	mem			16/24 + n	3-5		x	u			
		n = number of shifts																							
Stack Manipulation Instructions																									
PUSH	mem16	1	1	1	1	1	1	1	1	mod		1	1	0	mem			23	2-4						
	reg16	0	1	0	1	0	reg											10	1						
	sr	0	0	0	sr		1	1	0									10	1						
	PSW	1	0	0	1	1	1	0	0									10	1						
	R	0	1	1	0	0	0	0	0									65	1						
	imm	0	1	1	0	1	0	S	0									9-10	2-3						
POP	mem16	1	0	0	0	1	1	1	1	mod		0	0	0	mem			25	2-4						
	reg16	0	1	0	1	1	reg											12	1						
	sr	0	0	0	sr		1	1	1									12	1						
	PSW	1	0	0	1	1	1	0	1									12	1	R	R	R	R	R	R
	R	0	1	1	0	0	0	0	1									75	1						
PREPARE	imm16, imm8	1	1	0	0	1	0	0	0	*imm8 = 0 : 16 imm8 > 1 : 21 + 16 (imm8 − 1)								*	4						
DISPOSE		1	1	0	0	1	0	0	1									10	1						
Control Transfer Instructions																									
CALL	near_proc	1	1	1	0	1	0	0	0									20	3						
	regptr	1	1	1	1	1	1	1	1	1	1	0	1	0	reg			18	1						
	memptr16	1	1	1	1	1	1	1	1	mod		0	1	0	mem			31	2-4						
	far_proc	1	0	0	1	1	0	1	0									29	5						
	memptr32	1	1	1	1	1	1	1	1	mod		0	1	1	mem			47	2-4						
RET		1	1	0	0	0	0	1	1									19	1						
	pop_value	1	1	0	0	0	0	1	0									24	3						
		1	1	0	0	1	0	1	1									29	1						
	pop_value	1	1	0	0	1	0	1	0									32	3						
BR	near_label	1	1	1	0	1	0	0	1									13	3						
	short_label	1	1	1	0	1	0	0	1									12	2						
	reg	1	1	1	1	1	1	1	1	1	1	1	0	0	reg			11	2						
	memptr16	1	1	1	1	1	1	1	1	mod		1	0	0	mem			23	2-4						
	far_label	1	1	1	0	1	0	1	0									15	5						
	memptr32	1	1	1	1	1	1	1	1	mod		1	0	1	mem			34	2-4						
BV	near_label	0	1	1	1	0	0	0	0									14/4	2						
BNV	near_label	0	1	1	1	0	0	0	1									14/4	2						

3

Instruction Set (cont)

Mnemonic	Operands	Opcode 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Clocks	Bytes	Flags AC	CY	V	P	S	Z
Control Transfer Instructions (cont)																									
BC, BL	near_label	0	1	1	1	0	0	1	0									14/4	2						
BNC, BNL	near_label	0	1	1	1	0	0	1	1									14/4	2						
BE, BZ	near_label	0	1	1	1	0	1	0	0									14/4	2						
BNE, BNZ	near_label	0	1	1	1	0	1	0	1									14/4	2						
BNH	near_label	0	1	1	1	0	1	1	0									14/4	2						
BH	near_label	0	1	1	1	0	1	1	1									14/4	2						
BN	near_label	0	1	1	1	1	0	0	0									14/4	2						
BP	near_label	0	1	1	1	1	0	0	1									14/4	2						
BPE	near_label	0	1	1	1	1	0	1	0									14/4	2						
BPO	near_label	0	1	1	1	1	0	1	1									14/4	2						
BLT	near_label	0	1	1	1	1	1	0	0									14/4	2						
BGE	near_label	0	1	1	1	1	1	0	1									14/4	2						
BLE	near_label	0	1	1	1	1	1	1	0									14/4	2						
BGT	near_label	0	1	1	1	1	1	1	1									14/4	2						
DBNZNE	near_label	1	1	1	0	0	0	0	0									14/5	2						
DBNZE	near_label	1	1	1	0	0	0	0	1									14/5	2						
DBNZ	near_label	1	1	1	0	0	0	1	0									13/5	2						
BCWZ	near_label	1	1	1	0	0	0	1	1									13/5	2						
Interrupt Instructions																									
BRK	3	1	1	0	0	1	1	0	0									50	1						
	imm8	1	1	0	0	1	1	0	1									50	2						
BRKV	imm8	1	1	0	0	1	1	1	1									52/3	1						
RETI		1	1	0	0	1	1	1	0									39	1	R	R	R	R	R	R
CHKIND	reg16, mem32	0	1	1	0	0	0	1	0	mod			reg			mem		72-75/25	2-4						
BRKEM	imm8	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	50	3						
CPU Control Instructions																									
HALT		1	1	1	1	0	1	0	0									2	1						
BUSLOCK		1	1	1	1	0	0	0	0									2	1						
FPO1	fp_op	1	1	0	1	1	X	X	X	1	1	Y	Y	Y	Z	Z	Z	2	2						
	fp_op, mem	1	1	0	1	1	X	X	X	mod		Y	Y	Y		mem		14	2-4						
FPO2	fp_op	0	1	1	0	0	1	1	X	1	1	Y	Y	Y	Z	Z	Z	2	2						
	fp_op, mem	0	1	1	0	0	1	1	X	mod		Y	Y	Y		mem		14	2-4						
POLL		1	0	0	1	1	0	1	1	n = number of times POLL pin is sampled.								2 + 5n	1						
NOP		1	0	0	1	0	0	0	0									3	1						
DI		1	1	1	1	1	0	1	0									2	1						
EI		1	1	1	1	1	0	1	1									2	1						
DS0:, DS1:, PS:, and SS: (segment override prefixes)		0	0	1	seg		1	1	0									2	1						
8080 Instruction Set Enhancements																									
RETEM		1	1	1	0		1	1	0	1	1	1	1	1	1	1	0	1	39	2	R	R	R	R	R	R
CALLN	imm8	1	1	1	0		1	1	0	1	1	1	1	0	1	1	0	1	58	3						

7 APPENDIX E

16C452 Datasheet Reprint

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ST16C452
ST16C452PS

DUAL UART WITH PARALLEL PRINTER PORT

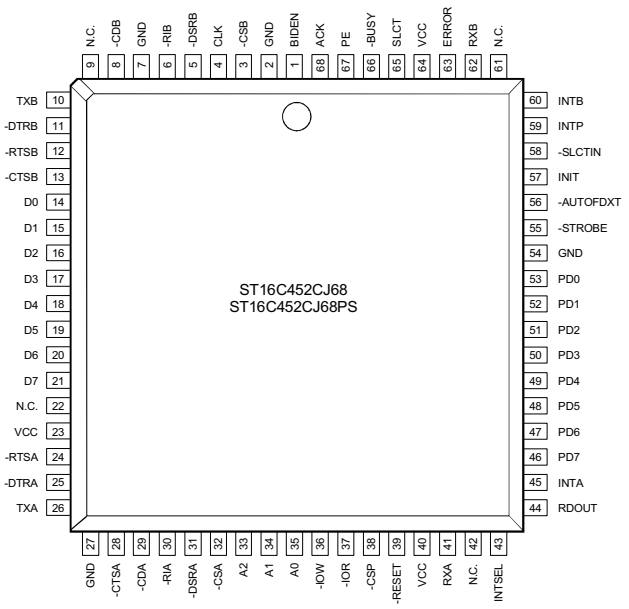
DESCRIPTION

The ST16C452/ST16C452PS (452/452PS) is a dual universal asynchronous receiver and transmitter (UART) with an added bi-directional parallel port that is directly compatible with a CENTRONICS type printer. The parallel port is designed such that the user can configure it as general purpose I/O interface, or for connection to other printer devices. The 452/452PS provides enhanced UART functions, a modem control interface, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status. The system interrupts and control may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. A programmable baud rate generator is provided to select transmit and receive clock rates from 50 bps to 1.5 Mbps. The 452/452PS is available in a 68 pin PLCC package. The 452/452PS is compatible with the 16C450. The 452 is available in two versions, the ST16C452 and the ST16C452PS. The ST16C452 provides single hardware pin to control the printer port data direction while the 452PS provides an additionally software control bit to control the printer port data direction to become compatible PS/2 operating system.
The 452/452PS is fabricated in an advanced CMOS process with low power consumption.

FEATURES

- Pin to pin and functional compatible to TL16C452
- Software compatible with ST16C450, NS16C450
- 1.5 Mbps transmit/receive operation (24MHz)
- Independent transmit and receive control
- Modem and printer status registers
- UART port and printer port Bi-directional
- Printer port direction set by single control bit or 8 bit pattern (AA/55)
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Internal loop-back diagnostics
- TTL compatible inputs, outputs
- Low Power

PLCC Package

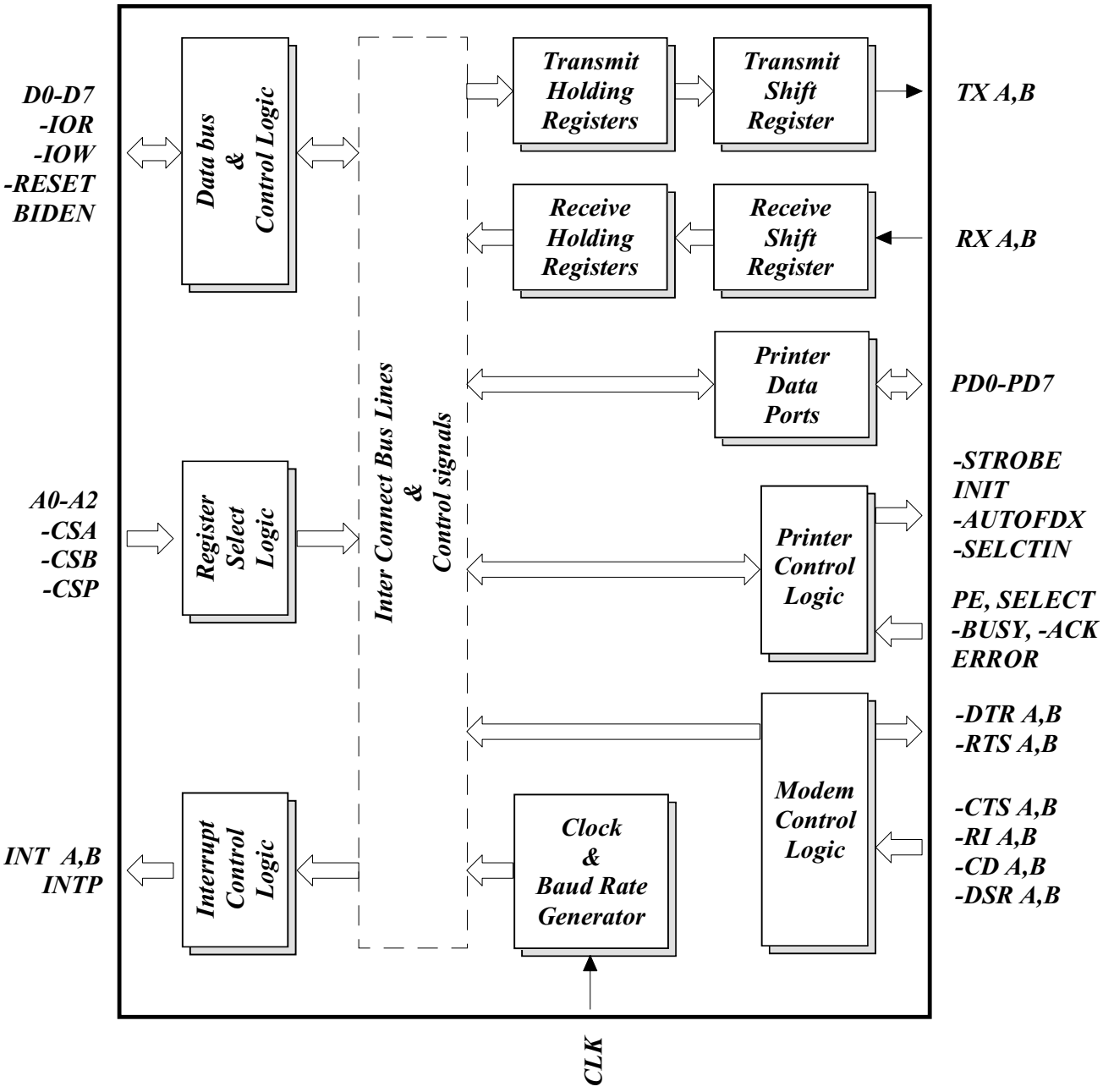


ORDERING INFORMATION

Part number	Pin	Package	Operating temperature
ST16C452CJ68	68	PLCC	0° C to + 70° C
ST16C452CJ68PS	68	PLCC	0° C to + 70° C
ST16C452IJ68	68	PLCC	-40° C to + 85° C
ST16C452IJ68PS	68	PLCC	-40° C to + 85° C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 • (510) 668-7000 • FAX (510) 668-7017

Figure 1, Block Diagram



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
A0	35	I	Address-0 Select Bit - Internal registers address selection.
A1	34	I	Address-1 Select Bit - Internal registers address selection.
A2	33	I	Address-2 Select Bit - Internal registers address selection.
-ACK	68	I	Acknowledge (with internal pull-up) - General purpose input or line printer acknowledge (active low). a logic 0 from the printer, indicates successful data transfer to the print buffer.
-AutoFDXT	56	I/O	General purpose I/O (open drain, with internal pull-up) or automatic line feed (open drain input with internal pull-up). When this signal is low the printer should automatically line feed after each line is printed.
BIDEN	1	I	Bi-Direction Enable - PD7-PD0 direction select. A logic 0 sets the parallel port for I/O Select Register Control. A logic 1 sets the parallel port for Control Register Bit-5 Control.
BUSY	66	I	Busy (with internal pull-up) - General purpose input or line printer busy (active high). can be used as an output from the printer to indicate printer is not ready to accept data.
CLK	4	I	Clock Input. - An external clock must be connected to this pin to clock the baud rate generator and internal circuitry (see Programmable Baud Rate Generator).
-CSA	32	I	Chip Select A - A logic 0 at this pin enables the serial channel-A UART registers for CPU data transfers.
-CSB	3	I	Chip Select B - A logic 0 at this pin enables the serial channel-B UART registers for CPU data transfers.
-CSP	38	I	Printer Port Chip Select - (active low). A logic 0 at this pin enables the parallel printer port registers and/or PD7-PD0 for external CPU data transfers.
D0-D7	14-21	I/O	Data Bus (Bi-directional) - These pins are the eight bit, three state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
-ERROR	63	I	Error, Printer (with internal pull-up) - General purpose input or line printer error. This pin may be connected to the active low (logic 0) output of a printer to indicate an error condition.
GND	2,7,54 27	Pwr	Signal and Power Ground.
INIT	57	I/O	Initialize (open drain, with internal pull-up) - General purpose I/O signal. This pin may be connected for initialization service of a connected line printer. Generally when this signal is a logic 0, any connected printer will be initialized.
INT A/B	45,60	O	Interrupt output A/B (three state active high) - These pins provide individual channel interrupts, INT A-B. INT A-B are enabled when MCR bit-3 is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected.
-INTP	59	O	Printer Interrupt, - This pin can be used to signal the interrupt status of a connected printer. This pin basically tracks the -ACK input pin, When INTSEL is a logic 0 and interrupts are enabled by bit-4 in the control register. A latched mode can be selected by setting INTSEL to a logic 1. In this case the interrupt -INTP is generated normally but does not return to the inactive state until the trailing edge of the read cycle (-IOR pin). -INTP is three stated until CON bit-4 is set to a logic 1.
INTSEL	43	I	Interrupt Select mode - This pin selects the interrupt type for the printer port (-INTP). When this pin is a logic 0, the external -ACK signal state is generally followed, minus some minor propagation delay. Making this pin a logic 1 or connecting it to VCC will set the interrupt latched mode. In this case the printer interrupt (-INTP) will not return to a logic 1 until the trailing edge of -IOR (end of the external CPU read cycle).
-IOR	37	I	Read strobe.- A logic 0 transition on this pin will place the contents of an Internal register defined by address bits A0-A2 for either UART channels A/B or A0-A1 for the printer

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			port, onto D0-D7 data bus for a read cycle by an external CPU.
-IOW	36	I	Write strobe.- A logic 0 transition on this pin will transfer the data on the internal data bus (D0-D7), as defined by either address bits A0-A2 for UART channels A/B or A0-A1 for the printer port, into an internal register during a write cycle from an external CPU.
PD7-PD0	46-53	I/O	Printer Data port (Bi-directional three state) - These pins are the eight bit, three state data bus for transferring information to or from an external device (usually a printer). D0 is the least significant bit. PD7-PD0 are latched during a write cycle (output mode).
PE	67	I	Paper Empty - General purpose input or line printer paper empty (Internal pull-up). This pin can be connected to provide a printer out of paper indication.
RDOUT	44	O	Read Out (active high) - This pin goes to a logic 1 when the external CPU is reading data from the 452/452PS. This signal can be used to enable/disable external transceivers or other logic functions.
-RESET	39	I	Master Reset (active low) - a logic 0 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See ST16C452/452PS External Reset Conditions for initialization details.)
N.C.	9,61		Not Used. Should be left open.
SLCT	65	I	Select (with internal pull-up) - General purpose input or line printer select status. Normally this pin is connected to a printer output (active low) that indicates the ready status of a printer, i.e., on-line and/or on-line and ready.
-SLCTIN	58	I/O	Select In (open drain, with internal pull-up) - General purpose I/O or line printer select. This pin can be read via Bit-3 in the printer command register, or written via bit-3 in the printer control register. As this pin is open-drain, it can be wire-or'd with other outputs. Normally this signal is

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			connected with a printer to select the printer with an active low.
-STROBE	55	I/O	Strobe (open drain, with internal pull-up) - General purpose I/O or data strobe output. Normally this output is connected to a printer and indicates that valid data is available at the printer port (PD0-PD7).
N.C.	22,42		Not Used. Should be left open.
VCC	23,40,64	Pwr	Power supply input.
-CD A/B	29,8	I	Carrier Detect (active low) - These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
-CTS A/B	28,13	I	Clear to Send (active low) - These inputs are associated with individual UART channels, A through B. A logic 0 on this pin(s) indicates the modem or data set is ready to accept transmit data from the 452/452PS for the given channel. Status can be tested by reading MSR bit-4 for that channel(s). -CTS has no effect on the transmit or receive operation.
-DSR A/B	31,5	I	Data Set Ready (active low) - These inputs are associated with individual UART channels, A through B. A logic 0 on this pin(s) indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation.
-DTR A/B	25,11	O	Data Terminal Ready (active low) - These outputs are associated with individual UART channels, A through B. A logic 0 on this pin(s) indicates that the 452/452PS is powered-on and ready. This pin can be controlled via the modem control register for channel(s) A-B. Writing a logic 1 to MCR bit-0 will set the -DTR output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR bit-0, or after a reset. This pin has no effect on the UART's transmit or receive operation.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
-RI A/B	30,6	I	Ring Indicator (active low) - These inputs are associated with individual UART channels, A through B. A logic 0 on this pin(s) indicates the modem has received a ringing signal from the telephone line(s). A logic 1 transition on this input pin will generate an interrupt for the ringing channel(s). This pin does not have any effect on the transmit or receive operation.
-RTS A/B	24,12	O	Request to Send (active low) - These outputs are associated with individual UART channels, A through B. A logic 0 on the -RTS pin(s) indicates the transmitter has data ready and waiting to send for the given channel(s). Writing a logic 1 in the modem control register (MCR bit-1) will set this pin to a logic 0 indicating data is available. After a reset this pin will be set to a logic 1. This pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Receive Data Input, RX A-B. - These inputs are associated with individual serial channel(s) to the 452. The RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the RX input pins are disabled and TX data is internally connected to the UART RX Inputs, internally.
TX A/B	26,10	O	Transmit Data, TX A-B - These outputs are associated with individual serial transmit channel(s) from the 452/452PS. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the TX output pins are disabled and TX data is internally connected to the UART RX Inputs.

GENERAL DESCRIPTION

The 452/452PS provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The 452/452PS represents such an integration with greatly enhanced features. The 452/452PS is fabricated with an advanced CMOS process.

The 452/452PS combines the package functions of a dual UART and a printer interface on a single integrated chip. The 452/452PS UART is indented to be software compatible with the ST16C450, and NS16C450 while the bi-directional printer interface mode is intended to operate with a CENTRONICS type parallel printer. However, the printer interface is designed such that it may be configured to operate with other parallel printer interfaces or used as a general purpose parallel interface. The 452 is available in two versions, the ST16C452 and the ST16C452PS. The ST16C452 provides single hardware pin to control the printer port data direction while the 452PS provides an additionally software control bit to control the printer port data direction to become compatible PS/2 operating system.

The 452/452PS is capable of operation to 1.5Mbps with a 24 MHz external clock input. With an external clock input of 1.8432 MHz the user can select data rates up to 115.2 Kbps.

FUNCTIONAL DESCRIPTIONS

Functional Modes

Two functional user modes are selectable for the 452/452PS package. The first of these provides the dual UART functions, while the other provides the functions of a parallel printer interface. These features are available through selection at the package interface select pins.

UART A-B Functions

The UART mode provides the user with the capability to transfer information between an external CPU and the 452/452PS package. A logic 0 on chip select pins -CSA or -CSB allows the user to configure, send data, and/or receive data via the UART channels A-B.

Printer Port Functions

The Printer mode provides the user with the capability to transfer information between an external CPU and the 452/452PS parallel printer port. A logic 0 on chip select pin -CSP allows the user to configure, send data, and/or receive data via the bi-directional parallel 8-bit data bus, PD0-PD7.

Internal Registers

The 452/452PS provides 11 internal registers for monitoring and control of the UART functions and another 6 registers for monitoring and controlling the printer port. These resisters are shown in Table 4 below. The UART registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user assessable scratchpad register (SPR). The printer port registers functions data holding registers (PR), I/O status register (SR), I/O select register (IOSEL), and a command and control register (COM/CON). Register functions are more fully described in the following paragraphs.

Table 4, INTERNAL REGISTER DECODE

A2	A1	A0	READ MODE	WRITE MODE
General Register Set (THR/RHR, IER/ISR, MCR/MSR, LCR/LSR, SPR): Note 1*				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
Baud Rate Register Set (DLL/DLM): Note *2				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
Printer Port Set (PR/SR/IOSEL/COM/CON): Note *3				
X	0	0	PORT REGISTER	PORT REGISTER
X	0	1	STATUS REGISTER	I/O SELECT REGISTER
X	1	0	COMMAND REGISTER	CONTROL REGISTER

Note 1* The General Register set is accessible only when CS A or CS B is a logic 0.
Note 2* The Baud Rate register set is accessible only when CS A or CS B is a logic 0 and LCR bit-7 is a logic 1.
Note 3*: Printer Port Register set is accessible only when -CSP is a logic 0 in conjunction with the states of the interface signal BIDEN and Printer Control Register bit-5 or IOSEL register.

Programmable Baud Rate Generator

The 452/452PS supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example a 33.6Kbps modem that employs data compression may require a 115.2Kbps input data rate. A 128.0Kbps ISDN modem that supports data compression may need an input data rate of 460.8Kbps. The 452/452PS can support a standard data rate of 921.6Kbps.

Single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 24 MHz, as required for supporting a 1.5Mbps data rate. The 452/452PS requires that an external clock source be connected to the CLK input pin to clock the internal baud rate generator for standard or custom rates. (see Baud Rate Generator Programming below).

The generator divides the input 16X clock by any divisor from 1 to 2^{16} -1. The 452/452PS divides the basic external clock by 16. The basic 16X clock provides table rates to support standard and custom applications using the same system design. The rate table is configured via the DLL and DLM internal register functions. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 below, shows the selectable baud rate table available when using a 1.8432 MHz external clock input.

Table 5, BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

Output Baud Rate	Output 16 x Clock Divisor (Decimal)	User 16 x Clock Divisor (HEX)	DLM Program Value (HEX)	DLL Program Value (HEX)
50	2304	900	09	00
110	1047	417	04	17
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1200	96	60	00	60
2400	48	30	00	30
4800	24	18	00	18
7200	16	10	00	10
9600	12	0C	00	0C
19.2k	6	06	00	06
38.4k	3	03	00	03
57.6k	2	02	00	02
115.2k	1	01	00	01

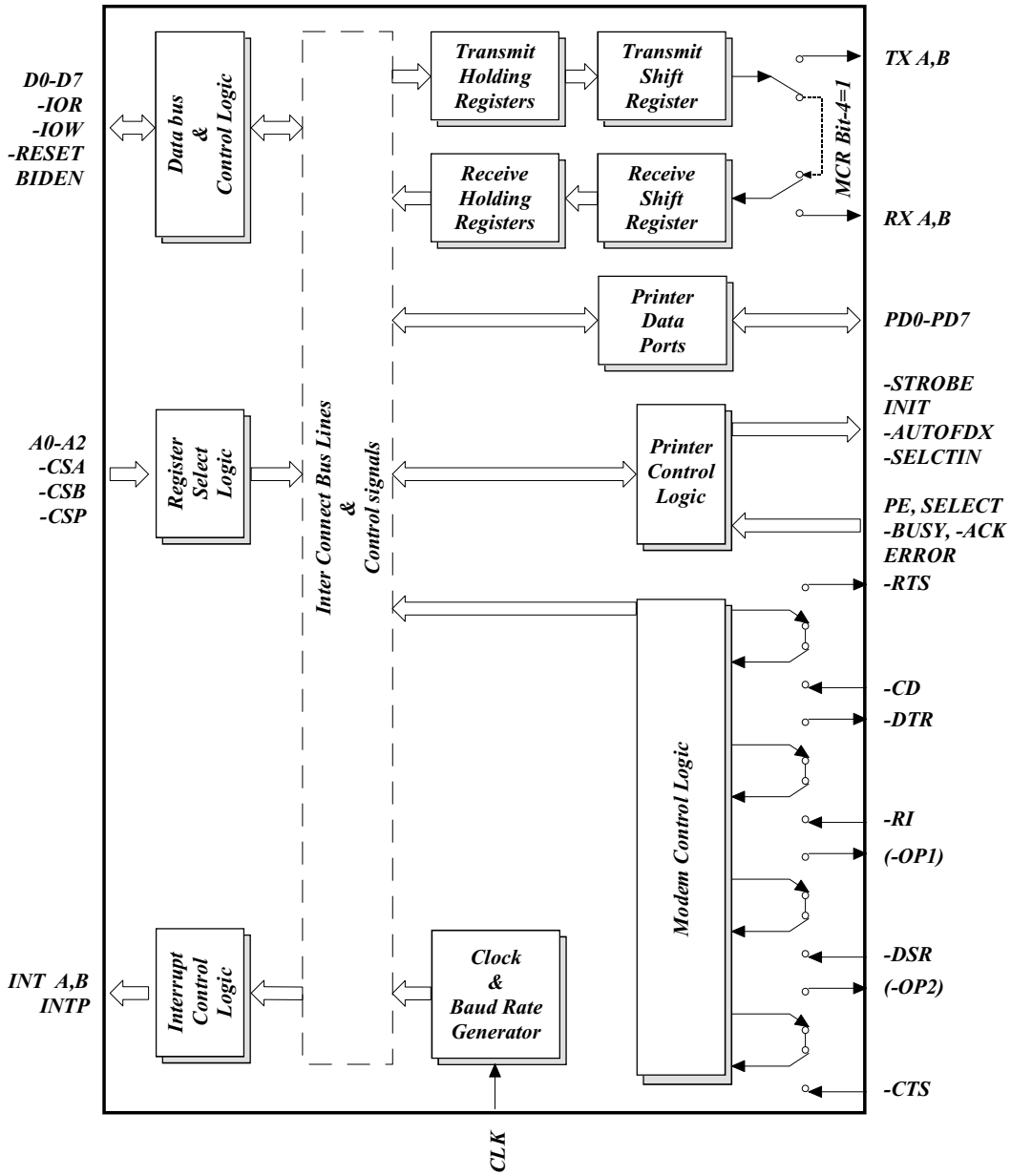
Loop-back Mode

The internal loop-back capability allows onboard diagnostics. In the loop-back mode the normal modem interface pins are disconnected and reconfigured for loop-back internally. MCR register bits 0-3 are used for controlling loop-back diagnostic testing. In the loop-back mode INT enable and MCR bit-2 in the MCR register (bits 2,3) control the modem -RI and -CD inputs respectively. MCR signals -DTR and -RTS (bits 0-1) are used to control the modem -CTS and -DSR inputs respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (See Figure 6). The -CTS, -DSR, -CD, and -RI are disconnected from their normal modem control inputs pins, and instead are connected internally to -DTR, -RTS, INT enable and MCR bit-2. Loop-back test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel data that is then made

available at the user data interface, D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Control Register (MCR bits 0-3) instead of the four Modem Status Register bits 4-7. The interrupts are still controlled by the IER.

Figure 6, INTERNAL LOOP-BACK MODE DIAGRAM



Printer Port

The 452/452PS contains a general purpose 8-bit parallel interface port that is designed to directly interface with a CENTRONICS Printer. A number of the control/interrupt signals and the 8-bit data bus have been designed as bi-directional data buses. This allows the interface to function with other device parallel data bus applications. Signal -ACK is used to generate an -INTP interface interrupt that would normally be connected to the user CPU. -INTP can be made to follow the -ACK signal, normal mode (see Figure 7) or it can be configured for the latch mode. In the latch mode the interrupt is not cleared until printer status register (SR) is read. Another signal (INIT) can be made to function as an outgoing or incoming interrupt, or combined with other interrupts to provide a common wire-or interrupt output. Interface signals -STROBE, -AutoFDXT, and -SLCTIN are bi-directional and can be used as combinations of input and/or output functions. The signals have internal pull-up resistors and can be wire-or'd. Normally, -STROBE is used to strobe PD0-PD7 bus data into a printer input buffer. -SLCTIN normally selects the printer while AutoFDXT signals the printer to auto-linefeed. Other signals provide similar printer functions but are not bi-directional. The printer functions for these signals are described in table 1, Symbol Description.

The interface provides a mode steering signal called BIDEN. BIDEN controls the bi-directional 8-bit data bus (PD0-PD7) direction, input or output. When BIDEN is a logic 1 a single control bit (D5) in the control register sets the input or output mode. Setting BIDEN to a logic 0 however sets an IBM interface compatible mode. In this mode the bus direction (input/output) is set by eight data bits in the IOSEL register. An AA (Hex) pattern sets the input mode while a 55 (hex) pattern sets the output mode. I/O direction is depicted in Table 6 below.

Table 6, PD0-PD7 I/O DIRECTION MODE SELECTION

PORT DIRECTION	BIDEN	CONTROL REGISTER (D5)	I/O SELECT REGISTER
Input mode	0	X (Note 4)	AA Hex
Output mode	0	X (Note 4)	55 Hex
Output mode	1	0	X (Note 4)
Input mode	1	1	X (Note 4)

Note: 4 = don't care

REGISTER FUNCTIONAL DESCRIPTIONS

The following table delineates the assigned bit functions for the eighteen 452/452PS internal registers. The assigned bit functions are more fully defined in the following paragraphs.

Table 7, ST16C452/452PS INTERNAL REGISTERS

A2 A1 A0	Register [Default] Note 5*	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
General Register Set: Note 1*									
0 0 0	RHR [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER [00]	0	0	0	0	Modem Status Interrupt	Receive Line Status interrupt	Transmit Holding Register interrupt	Receive Holding Register
0 1 0	ISR [01]	0	0	0	0	INT priority bit-2	INT priority bit-1	INT priority bit-0	INT status
0 1 1	LCR [00]	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR [00]	0	0	0	loop back	INT A/B enable	[X]	-RTS	-DTR
1 0 1	LSR [60]	0	THR & TSR empty	THR. empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR [X0]	CD	RI	DSR	CTS	delta -CD	delta -RI	delta -DSR	delta -CTS
1 1 1	SPR [FF]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Special Register Set: Note *2									
0 0 0	DLL [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM [XX]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

A2 A1 A0	Register [Default] Note 5*	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
Printer Port Register Set: Note 3*									
[X] 0 0	PR[00]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
[X] 0 0	PR[00]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
[X] 0 1	SR[4F]	-Busy	-ACK	PE	SLCT	Error State	-IRQ	logic "1"	logic "1"
[X] 0 1	IOSEL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
[X] 1 0	COM[E0]	logic "1"	logic "1"	logic "1"	-INTP Enable	-SLCTIN	INIT	-Auto FDXT	-STROBE
[X] 1 0	CON[00]	[X]	[X]	PD 0-7 IN/OUT	-INTP Enable	-SLCTIN	INIT	-Auto FDXT	-STROBE

Note 1* The General Register set is accessible only when CS A or CS B is a logic 0.
Note 2* The Baud Rate register set is accessible only when CS A or CS B is a logic 0 and LCR bit-7 is a logic 1.
Note 3*: Printer Port Register set is accessible only when -CSP is a logic 0 in conjunction with the states of the interface signal BIDEN and Printer Control Register bit-5 or IOSEL register.
Note 5* The value between the square brackets represents the register's initialized HEX value, X = N/A.

UART REGISTER DESCRIPTIONS

Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the transmit holding register empty flag is set (logic 0 = Buffer full).

The serial receive section also contains an 8-bit Receive Holding Register, RHR. Receive data is removed from the 452/452PS by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16x clock rate. After 7 1/2 clocks the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT A,B output pins.

IER BIT-0:
This interrupt will be issued when the RHR is full or is cleared when the RHR is empty.
Logic 0 = Disable the receiver ready interrupt. (normal default condition)
Logic 1 = Enable the receiver ready interrupt.

IER BIT-1:
This interrupt will be issued whenever the THR is empty and is associated with bit-1 in the LSR register.
Logic 0 = Disable the transmitter empty interrupt. (normal default condition)
Logic 1 = Enable the transmitter empty interrupt.

IER BIT-2:
This interrupt will be issued whenever a fully assembled receive character is transferred from the RSR to the RHR, i.e., data ready, LSR bit-0.
Logic 0 = Disable the receiver line status interrupt. (normal default condition)
Logic 1 = Enable the receiver line status interrupt.

IER BIT-3:
Logic 0 = Disable the modem status register interrupt. (normal default condition)
Logic 1 = Enable the modem status register interrupt.

IER BIT 4-7:
Not Used - initialized to a logic 0.

Interrupt Status Register (ISR)

The 452/452PS provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after rereading the interrupt status bits. The Interrupt Source Table 8 (below) shows the data values (bits 0-3) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels:

Table 8, INTERRUPT SOURCE TABLE

Priority Level	[ISR BITS] Bit-3	Bit-2	Bit-1	Bit-0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
Logic 1 = No interrupt pending. (normal default condition)

ISR BIT 1-3: (logic 0 or cleared is the default condition)
These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (See Interrupt Source Table).

ISR BIT 4-7: (logic 0 or cleared is the default condition)
Not Used - initialized to a logic 0.

Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR BIT 0-1: (logic 0 or cleared is the default condition)
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2: (logic 0 or cleared is the default condition)
The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	Word length	Stop bit length (Bit time(s))
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
Logic 0 = No parity. (normal default condition)
Logic 1 = A parity bit is generated during the transmission, receiver checks the data and parity for transmission errors.

LCR BIT-4:
If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.
Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted data. The receiver must be programmed to check the same format. (normal default condition)
Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted. The receiver must be programmed to check the same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = logic 0, parity is not forced. (normal default condition)
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

LCR Bit-5	LCR Bit-4	LCR Bit-3	Parity selection
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity odd parity
1	1	1	Forced even parity

LCR BIT-6:
When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR bit-6 to a logic 0.
Logic 0 = No TX break condition. (normal default condition)
Logic 1 = Forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition.

LCR BIT-7:
The internal baud rate counter latch and Enhance Feature mode enable.
Logic 0 = Divisor latch disabled. (normal default condition)
Logic 1 = Divisor latch and enhanced feature register enabled.

Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

MCR BIT-0:
Logic 0 = Force -DTR output to a logic 1. (normal default condition)
Logic 1 = Force -DTR output to a logic 0.

MCR BIT-1:
Logic 0 = Force -RTS output to a logic 1. (normal default condition)
Logic 1 = Force -RTS output to a logic 0.

MCR BIT-2:
This bit is used in the Loop-back mode only. In the loop-back mode this bit is use to write the state of the modem -RI interface signal.

*MCR BIT-3: (*Used to control the modem -CD signal in the loop-back mode.)
Logic 0 = Forces INT (A-B) outputs to the three state mode. (normal default condition) In the Loop-back mode, sets -CD internally to a logic 1.
Logic 1 = Forces the INT (A-B) outputs to the active mode. In the Loop-back mode, sets -CD internally to a logic 0.

MCR BIT-4:
Logic 0 = Disable loop-back mode. (normal default condition)
Logic 1 = Enable local loop-back mode (diagnostics).

MCR BIT 5-7:
Not Used - initialized to a logic 0.

Line Status Register (LSR)

This register provides the status of data transfers between. the 452/452PS and the CPU.

LSR BIT-0:
Logic 0 = No data in receive holding register. (normal default condition)
Logic 1 = Data has been received and is saved in the receive holding register.

LSR BIT-1:
Logic 0 = No overrun error. (normal default condition)
Logic 1 = Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the RHR is full. In this case the previous data in the shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the RHR, therefore the data in the RHR is not corrupted by the error.

LSR BIT-2:
Logic 0 = No parity error. (normal default condition)
Logic 1 = Parity error. The receive character does not have correct parity information and is suspect.

LSR BIT-3:
Logic 0 = No framing error. (normal default condition)
Logic 1 = Framing error. The receive character did not have a valid stop bit(s).

LSR BIT-4:
Logic 0 = No break condition. (normal default condition)
Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time).

LSR BIT-5:
This bit indicates that the 452/452PS is ready to accept new characters for transmission. This bit causes the 452/452PS to issue an interrupt to the CPU when the transmit holding register is empty and the interrupt enable is set.

Logic 0 = Transmit holding register is not empty. (normal default condition)
Logic 1 = Transmit holding register is empty. When this bit is a logic 1, the CPU can load new character into the Transmit Holding Register for transmission.

LSR BIT-6:
Logic 0 = Transmitter holding and shift registers are full.
Logic 1 = Transmitter holding and shift registers are empty (normal default condition).

LSR BIT-7:
Not Used - initialized to a logic 0.

Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device that the 452/452PS is connected to. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

MSR BIT-0:
Logic 0 = No -CTS Change (normal default condition)
Logic 1 = The -CTS input to the 452/452PS has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-1:
Logic 0 = No -DSR Change. (normal default condition)
Logic 1 = The -DSR input to the 452/452PS has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-2:
Logic 0 = No -RI Change. (normal default condition)
Logic 1 = The -RI input to the 452/452PS has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.

MSR BIT-3:
Logic 0 = No -CD Change. (normal default condition)
Logic 1 = Indicates that the -CD input to the has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-4:
Normally MSR bit-4 bit is the compliment of the -CTS input. However in the loop-back mode, this bit is equivalent to the RTS bit in the MCR register.

MSR BIT-5:
DSR (active high, logical 1). Normally this bit is the compliment of the -DSR input. In the loop-back mode, this bit is equivalent to the DTR bit in the MCR register.

MSR BIT-6:
RI (active high, logical 1). Normally this bit is the compliment of the -RI input. In the loop-back mode this bit is equivalent to MCR bit-2 in the MCR register.

MSR BIT-7:
CD (active high, logical 1). Normally this bit is the compliment of the -CD input. In the loop-back mode this bit is equivalent to MCR bit-3 in the MCR register.

Note: Whenever any MSR bit 0-3: is set to logic “1”, a MODEM Status Interrupt will be generated.

Scratchpad Register (SPR)

The ST16C452/452PS provides a temporary data register to store 8 bits of user information.

PRINTER PORT REGISTER DESCRIPTIONS

Port Register (PR)

PR BIT 0-7:

Printer Data port (Bi-directional) - These pins are the eight bit data bus for transferring information to or from an external device (usually a printer). D0 is the least significant bit. PD7-PD0 are latched during a write cycle (output mode).

I/O Select Register (IOSEL)

This bit is used in conjunction with the state of BIDEN to set the direction (input/output) of the PD7-PD0 data bus. This register is used only when BIDEN is a logic 0.

Logic 55 (Hex) + BIDEN 0 = PD7-PD0 are set for output mode

Logic AA (Hex) + BIDEN 0 = PD7-PD0 are set for input mode

Status Register (SR)

This register provides the printer port input logical states and the status of the interrupt -INTP based on the condition of the -ACK printer port interface signal. The logical state of these pins is dependent on external interface signals.

SR BIT 1-0:

Not Used - initialized to a logic 1.

SR BIT-2:

Logic 0 = an interrupt is pending

When INTSEL is a logic 0, SR bit-2 basically tracks the -ACK input interface pin (returns to a logic 1 when the -ACK input returns to a logic 1). However when INTSEL is a logic 1, the latched mode is selected, SR bit-2 goes to a logic 0 with the -ACK input but does not return to a logic 1 until the end of the read cycle, i.e., reading SR will set this bit to a logic 1.

Logic 1 = no interrupt is pending. (normal inactive state)

SR BIT-3:

Logic 0 = -ERROR input is a logic 0.

Logic 1 = -ERROR input is a logic 1. (normal inactive state)

SR BIT-4:

Logic 0 = SLCT input is a logic 0. (normal inactive state)

Logic 1 = SLCT input is a logic 1.

SR BIT-5:

Logic 0 = PE input is a logic 0. (normal inactive state)

Logic 1 = PE input is a logic 1.

SR BIT-6:

Logic 0 = -ACK input is a logic 0.

Logic 1 = -ACK input is a logic 1. (normal inactive state)

SR BIT-7:

Logic 0 = BUSY input is a logic 0

Logic 1 = BUSY input is a logic 1 (normal inactive state)

Command Register (COM)

This register provides the printer port input logical states and the status of the printer interrupt INIT, which is based on the state of CON bit-1.

COM BIT-0:

-STROBE is a bi-directional signal with an open source driver and internal pull-up so that it may be wire-or'd with other outputs. COM bit-1 is used to read status while CON bit 1 is used to set an output state. If it is to function as an input, CON bit-1 shall be set to a logic 1 first.

Logic 0 = -STROBE pin is a logic 1. (normal default condition)

Logic 1 = -STROBE pin is a logic 0.

COM BIT-1:

-AutoFDXT is a bi-directional signal with an open source driver and internal pull-up so that it may be wire-or'd with other outputs. COM bit-1 is used to read status while CON bit 1 is used to set an output state. If it is to function as an input, CON bit-1 shall be set to

a logic 1 first.
Logic 0 = -AutoFDXT pin is a logic 1. (normal default condition)
1= -AutoFDXT pin is a logic 0.

COM BIT-2:
INIT is a bi-directional signal with an open source driver and internal pull-up so that it may be wire-or'd with other outputs. COM bit-2 is used to read status while CON bit 2 is used to set an output state. If it is to function as an input, CON bit-1 shall be set to a logic 1 first.
Logic 0 = INIT pin is a logic 0. (normal default condition)
Logic 1 = INIT pin is a logic 1.

COM BIT-3:
-SLCTIN is a bi-directional signal with an open source driver and internal pull-up so that it may be wire-or'd with other outputs. COM bit-1 is used to read status while CON bit 1 is used to set an output state. If it is to function as an input, CON bit-1 shall be set to a logic 1 first.
Logic 0 = -SLCTIN pin is a logic 1 (normal default condition)
Logic 1 = -SLCTIN pin is a logic 0

COM BIT-4:
This bit allows the state of -INTP to be read back by the external CPU.
Logic 0 = Interrupt (-INTP output) is disabled (normal default condition)
Logic 1 = Interrupt (-INTP output) is enabled

COM BIT 5-7:
Not Used - initialized to a logic 1.

Control Register (CON)

This register provides control of the printer port output logical states and controls the printer interrupts INIT and -INTP. With the exception of PD 0-7 IN/OUT, the status of this register may be read by reading the COM register.

CON BIT-0:
The -STROBE output control bit is under software control, i.e., the hardware will not generate a strobe. It is up to software to return the state of -STROBE to the inactive (logic 1) state. The hardware driver is open drain so that -STROBE may be wire-or'd. The state of this bit can be read using COM bit-0.
Logic 0 = -STROBE output is set to a logic 1. (normal default condition)
Logic 1 = -STROBE output is set to a logic 0.

CON BIT-1:
The -AutoFDXT output control bit is set by software using CON bit-1. The hardware driver is open drain so that -AutoFDXT may be wire-or'd. The state of this bit can be read using COM bit-1.
Logic 0 = -AutoFDXT output is set to a logic 1. (normal default condition)
Logic 1 = -AutoFDXT output is set to a logic 0.

CON BIT-2:
The INIT output control bit is set by software using CON bit-2. The hardware driver is open drain so that INIT may be wire-or'd. The state of this bit can be read using COM bit-2.
Logic 0 = INIT output is set to a logic 0. (normal default condition)
Logic 1 = INIT output is set to a logic 1.

CON BIT-3:
The -SLCTIN output control bit is set by software using CON bit-3. The hardware driver is open drain so that -AutoFDXT may be wire-or'd. The state of this bit can be read using COM bit-3.
Logic 0 = -SLCTIN output is set to a logic 1. (normal default condition)
Logic 1 = -SLCTIN output is set to a logic 0.

CON BIT-4:
This bit enables or masks the printer interrupt output -INTP. The state of this bit can be read using COM bit-4.
Logic 0 = Disable -INTP output. (normal default condition)
Logic 1 = Enable -INTP output.

CON BIT-5:
This bit is used in conjunction with the state of BIDEN to set the direction (input/output) of the PD7-PD0 data bus.
Logic 0 + BIDEN 1 = PD7-PD0 are set for output mode (normal default condition)
Logic 1 + BIDEN 1 = PD7-PD0 are set for input mode

CON BIT 6-7:
Not Used - initialized to a logic 1.

ST16C452/452PS EXTERNAL RESET CONDITION

REGISTERS (UART)	RESET STATE
IER	BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

REGISTERS Printer Port	RESET STATE
IOSEL	IOSEL BITS-0-7=0
SR	SR BITS 0-1=1, BITS 2-7=input signals
COM	COM BITS 0-4=0, BITS 5-7=1
CON	CON BITS 0-5=0, BITS 6-7=1

SIGNALS	RESET STATE
TX A/B	High
-RTS A/B	High
-DTR A/B	High
INT A/B, P	Three state mode
PD0-PD7	Low, output mode
-STROBE	High, output mode
-AutoFDXT	High, output mode
INIT	Low, output mode
-SLCTIN	High, output mode

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T_{1w},T_{2w}	Clock pulse duration	17		17		ns	
T_{3w}	Oscillator/Clock frequency		8		24	MHz	
T_{6s}	Address setup time	5		0		ns	
T_{7d}	-IOR delay from chip select	10		10		ns	
T_{7w}	-IOR strobe width	35		25		ns	
T_{7h}	Chip select hold time from -IOR	0		0		ns	
T_{9d}	Read cycle delay	40		30		ns	
T_{12d}	Delay from -IOR to data		35		25	ns	
T_{12h}	Data disable time		25		15	ns	
T_{13d}	-IOW delay from chip select	10		10		ns	
T_{13w}	-IOW strobe width	40		25		ns	
T_{13h}	Chip select hold time from -IOW	0		0		ns	
T_{15d}	Write cycle delay	40		30		ns	
T_{16s}	Data setup time	20		15		ns	
T_{16h}	Data hold time	5		5		ns	
T_{17d}	Delay from -IOW to output		50		40	ns	100 pF load
T_{18d}	Delay to set interrupt from MODEM input		40		35	ns	100 pF load
T_{19d}	Delay to reset interrupt from -IOR		40		35	ns	100 pF load
T_{20d}	Delay from stop to set interrupt		1		1	Rclk	
T_{21d}	Delay from -IOR to reset interrupt		45		40	ns	100 pF load
T_{22d}	Delay from stop to interrupt		45		40	ns	
T_{23d}	Delay from initial INT reset to transmit start	8	24	8	24	Rclk	
T_{24d}	Delay from -IOW to reset interrupt		45		40	ns	
T_{39w}	-ACK pulse width	75		75		ns	
T_{40s}	PD7 - PD0 setup time	15		10		ns	
T_{41h}	PD7 - PD0 hold time	30		25		ns	
T_{42d}	Delay from -ACK low to interrupt low	10		5		ns	
T_{43d}	Delay from -IOR to reset interrupt	10		5		ns	
T_R	Reset pulse width	40		40		ns	
N	Baud rate devisor	1	2^{16}-1	1	2^{16}-1	Rclk	

ABSOLUTE MAXIMUM RATINGS

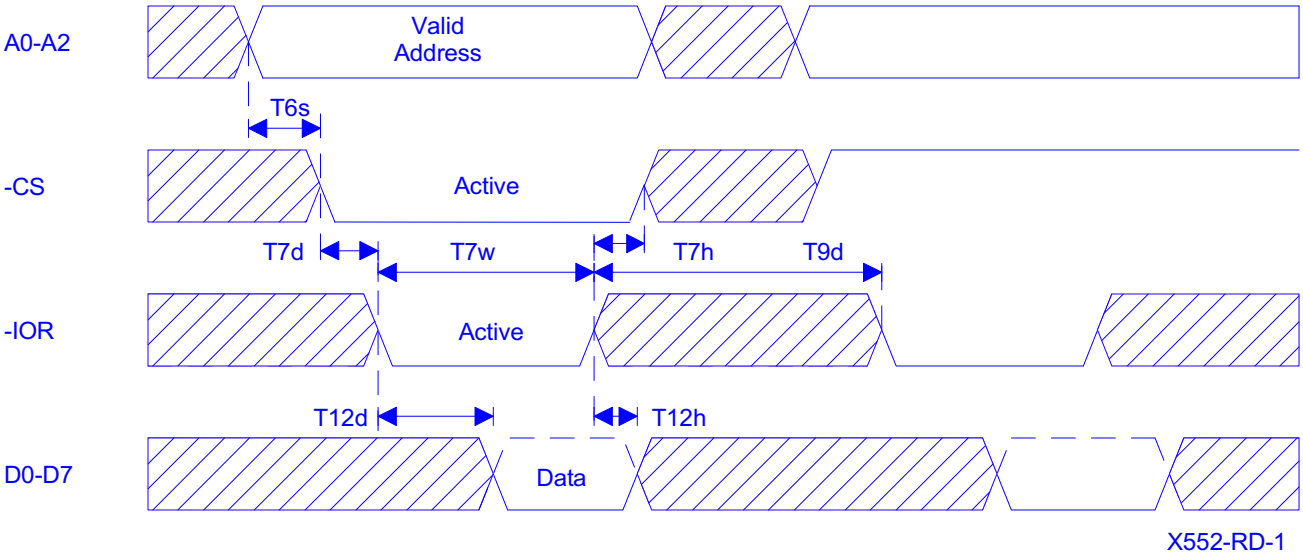
Supply range	7 Volts
Voltage at any pin	GND - 0.3 V to VCC +0.3 V
Operating temperature	-40° C to +85° C
Storage temperature	-65° C to 150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

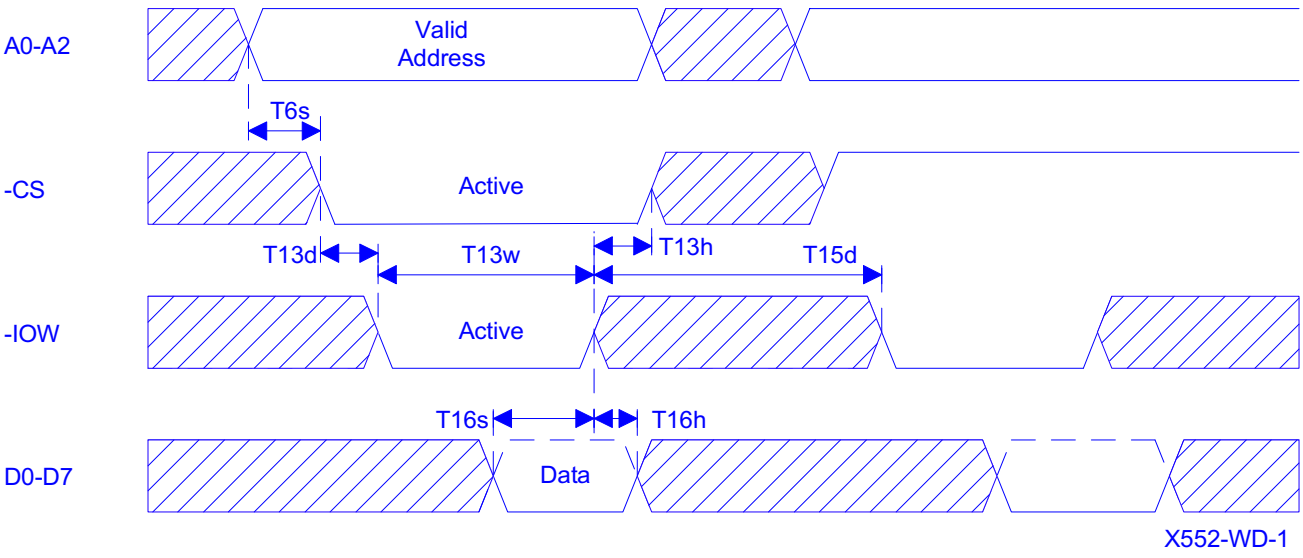
T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
V_{ILCK}	Clock input low level	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock input high level	2.4	VCC	3.0	VCC	V	
V_{IL}	Input low level	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input high level	2.0		2.2	VCC	V	
V_{OL}	Output low level on all outputs				0.4	V	I_{OL}= 4 mA
V_{OL}	Output low level on all outputs		0.4			V	I_{OL}= 4 mA
V_{OH}	Output high level			2.4		V	I_{OH}= -4 mA
V_{OH}	Output high level	2.0				V	I_{OH}= -1 mA
I_{IL}	Input leakage		±10		±10	µA	
I_{CL}	Clock leakage		±10		±10	µA	
I_{CC}	Avg power supply current		1.2		3	mA	
C_P	Input capacitance		5		5	pF	
R_{IN}	Internal pull-up resistance	9			22	kΩ	

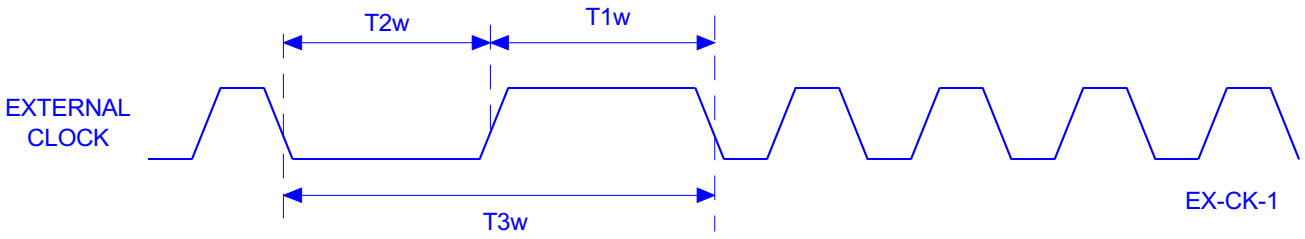
Note: See the Symbol Description Table, for a listing of pins having internal pull-up resistors.



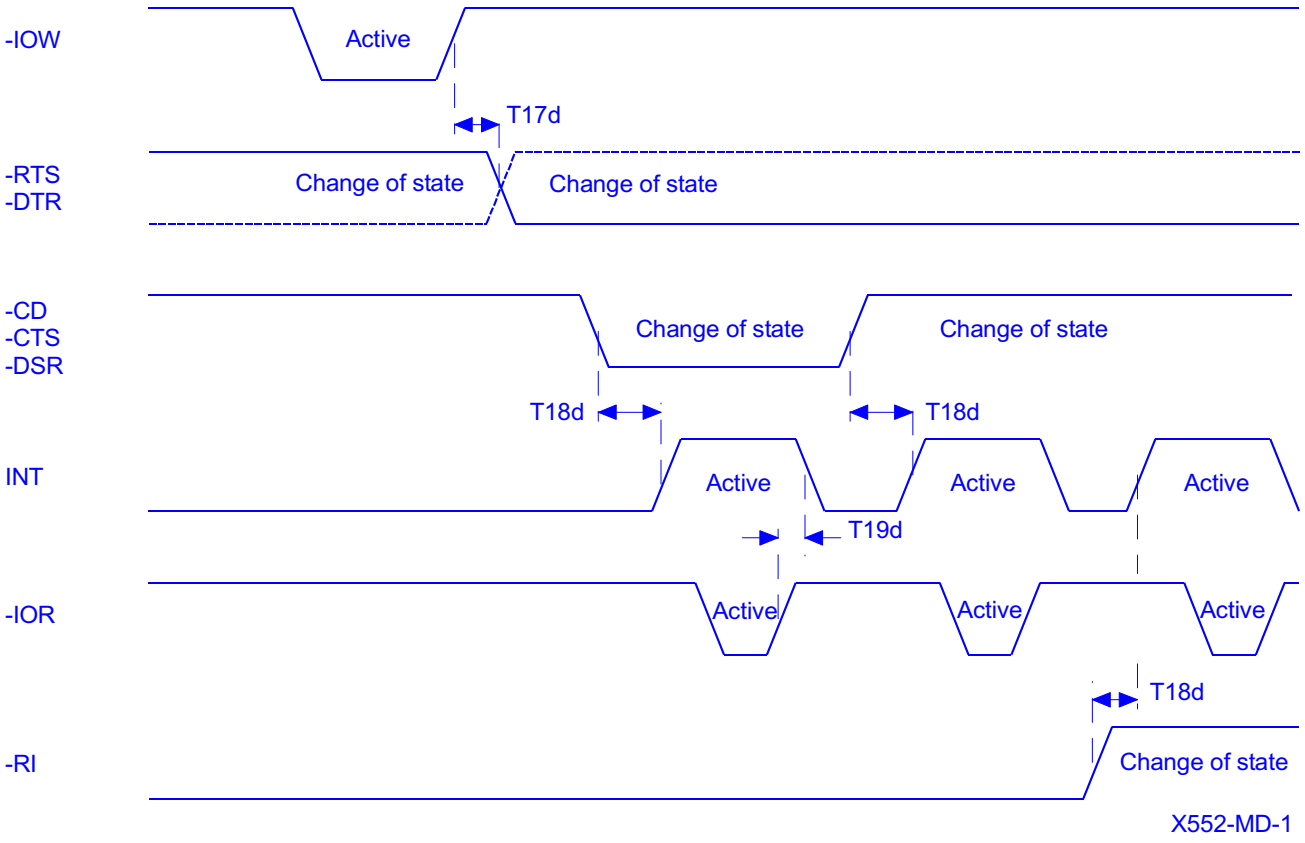
General read timing



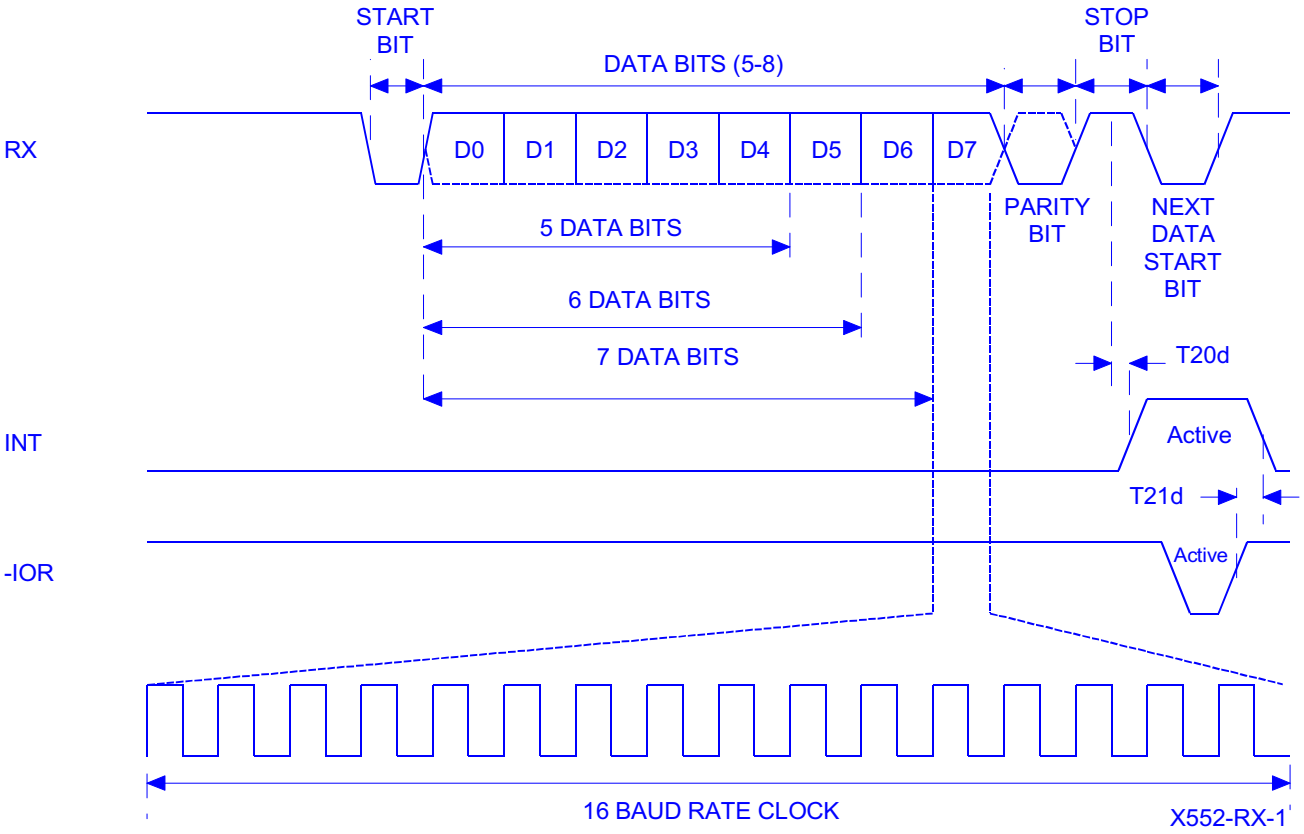
General write timing



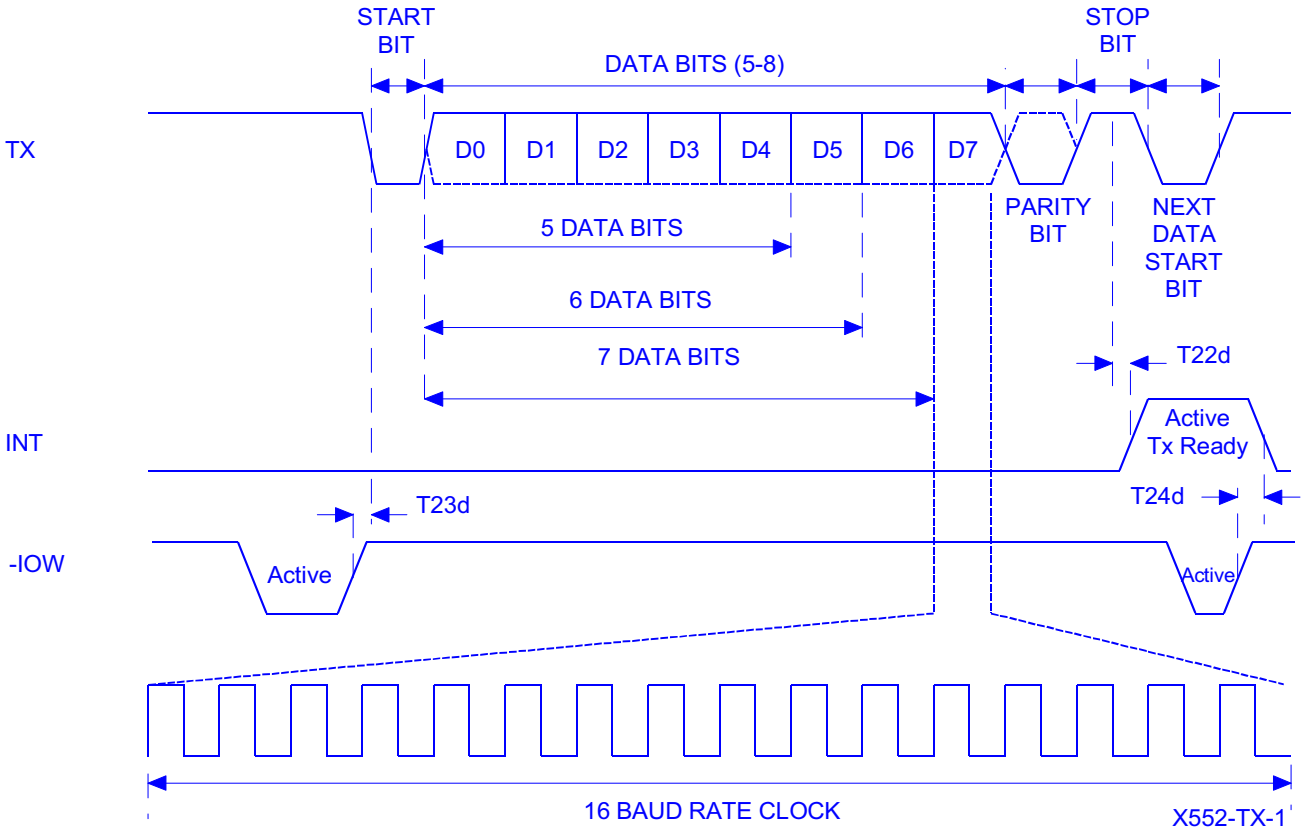
External clock timing



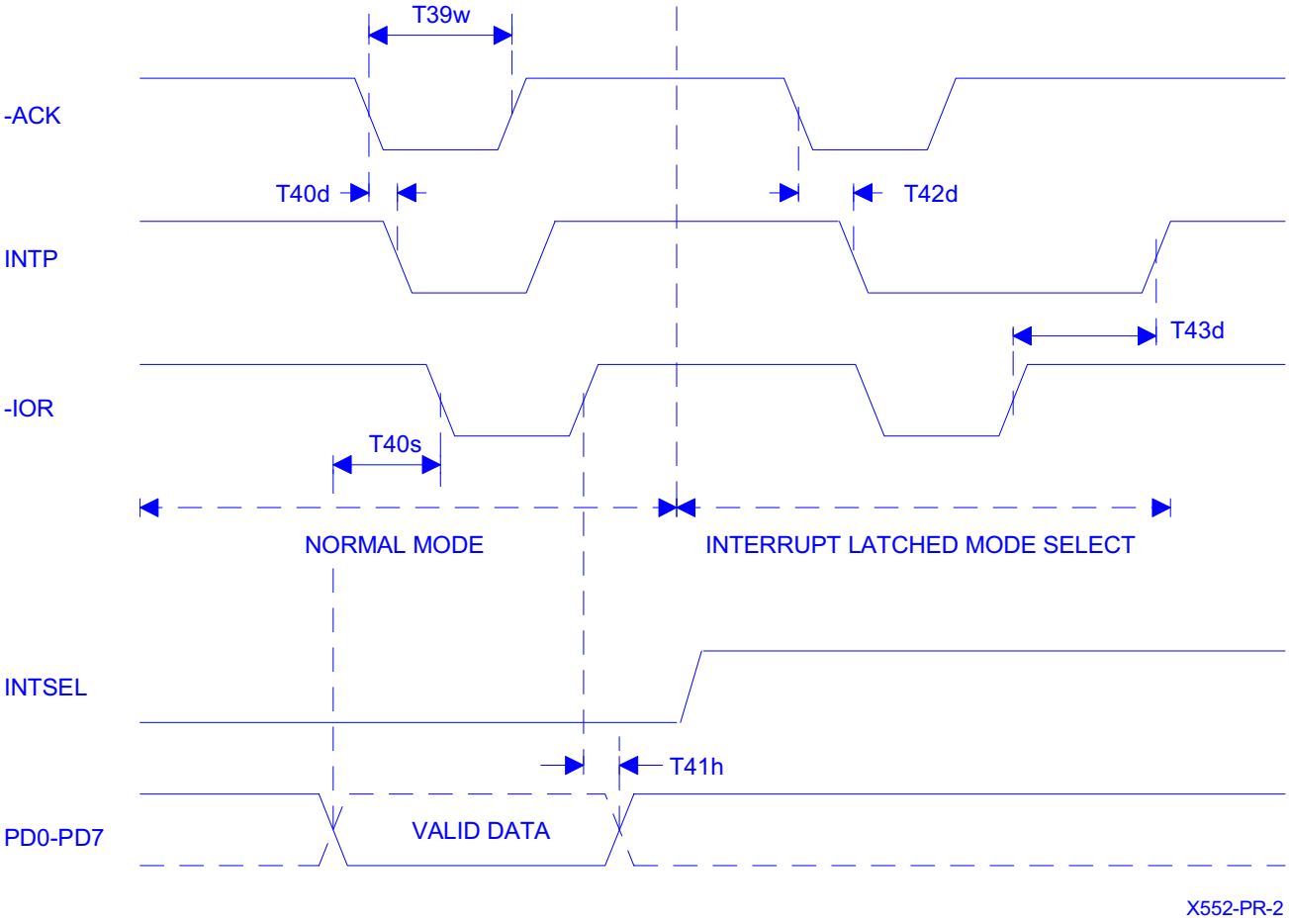
Modem input/output timing



Receive timing



Transmit timing

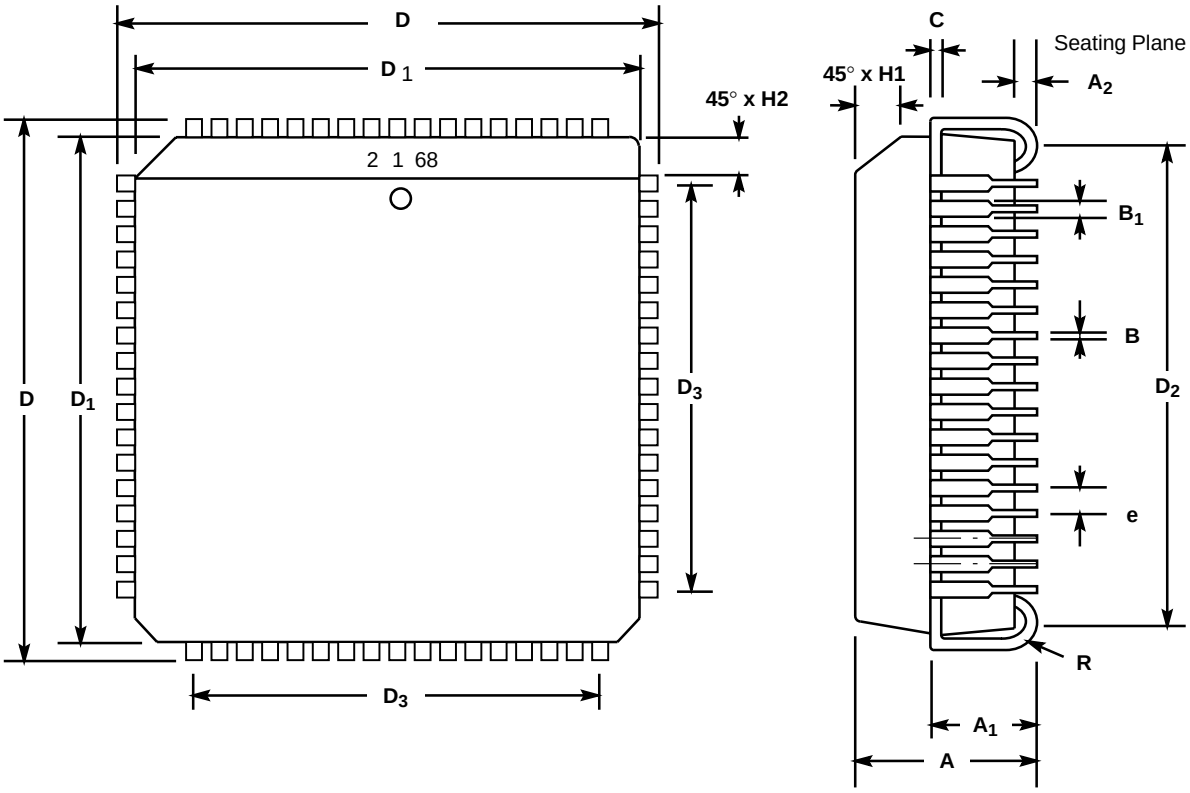


Printer port timing

Package Dimensions

68 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.200	4.19	5.08
A_1	0.090	0.130	2.29	3.30
A_2	0.020	—.	0.51	—
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.985	0.995	25.02	25.27
D_1	0.950	0.958	24.13	24.33
D_2	0.890	0.930	22.61	23.62
D_3	0.800 typ.		20.32 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Note: The control dimension is the inch column

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8 APPENDIX F

8255A Datasheet Reprint

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μPD8255A
PROGRAMMABLE PERIPHERAL INTERFACE

Description

The μPD8255A-2 and μPD8255A-5 are general purpose programmable input/output devices designed for use with the 8080A/8085A microprocessors. Twenty-four I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the basic mode, (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to input or output. In the strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The bidirectional bus mode, (MODE 2), uses the 8 lines of port A for a bi-directional bus, and five lines from port C for bus control signals.

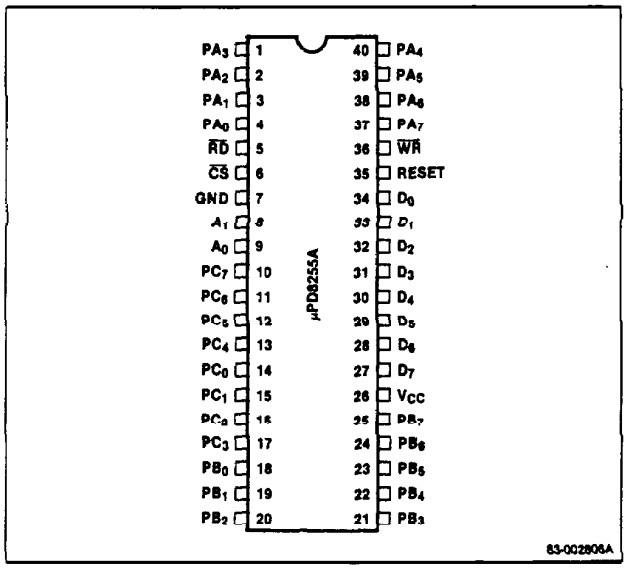
Features

- ☐ Fully compatible with the 8080A/8085 microprocessor families
- ☐ All inputs and outputs TTL compatible
- ☐ 24 programmable I/O pins
- ☐ Direct bit set/reset eases control application interfaces
- ☐ Eight Darlington drive outputs for printers and displays
- ☐ LSI drastically reduces system package count

Ordering Information

Part Number	Package Type	Max System Clock Frequency
μPD8255AC-2	40-pin plastic DIP	5 MHz
μPD8255AC-5	40-pin plastic DIP	4 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1-4, 37-40	PA_7-PA_0	Port A (I/O)
5	$\overline{RD}$	Read input
6	$\overline{CS}$	Chip select input
7	GND	Ground
8,9	A_1,A_0	Port address inputs
10-17	PC_7-PC_0	Port C (I/O)
18-25	PB_7-PB_0	Port B (I/O)
26	V_{CC}	+5 V power supply
27-34	D_7-D_0	Bidirectional data bus
35	RESET	Reset input
36	$\overline{WR}$	Write input

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Pin Functions

D_7-D_0 (Data Bus Buffer)

These pins form a three-state, bidirectional data bus buffer that is controlled by input and output instructions executed by the processor. Control words and status information are also transmitted via D_7-D_0.

$\overline{CS}$ (Chip Select)

A low input to this pin enables the μPD8255A for communication with the 8080A/8085A.

$\overline{RD}$ (Read)

A low input to this pin enables the μPD8255A for communication with the 8080A/8085A.

$\overline{WR}$ (Write)

A low input to this pin enables the data bus buffer to receive data or control words from the processor.

A_1, A_0 (Port Address)

These inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of the three ports on the control word register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor address bus.

RESET (Reset)

A high level input to this pin clears the control register and places ports A, B, and C in input mode. The input latches in ports A, B, and C are not cleared.

PA_7-PA_0, PB_7-PB_0, PC_7-PC_0 (Ports A, B, and C)

These three 8-bit I/O ports can be configured to meet a variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255A are further enhanced by special features unique to each of the ports, as follows:

- Port A has an 8-bit data output latch/buffer, data input latch/buffer, and data input latch.
- Port B has an 8-bit data I/O latch/buffer and an 8-bit data input buffer.
- Port C has an 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with ports A and B.

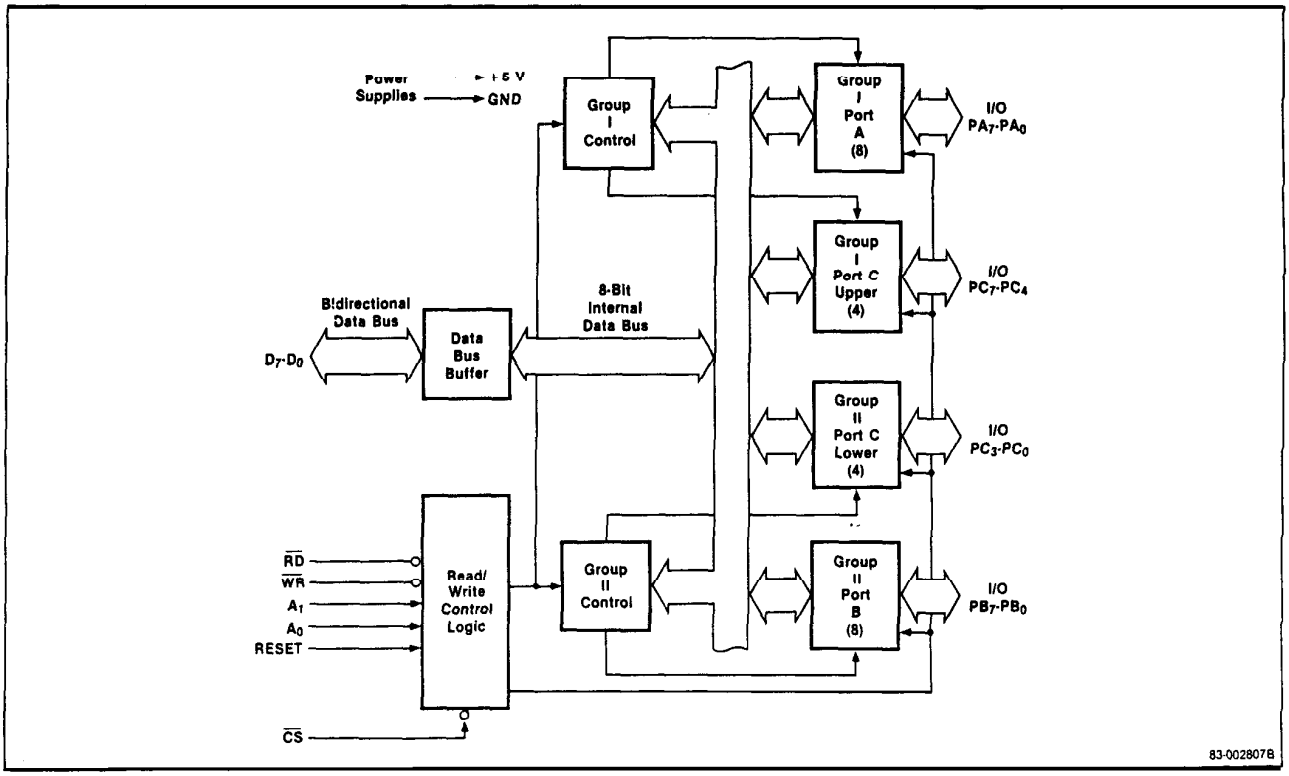
V_{CC}

+5 V power supply.

GND (Ground)

Connection to ground.

Block Diagram



Functional Description

The read/write and control logic manages all internal and external transfers of data, control, and status. It is through this block that the processor address and control buses control the peripheral interfaces.

Through an OUT instruction in system software from the processor, a control word is transmitted to the μPD8255A. Information such as the mode, bit set, and bit reset is used to initialize the functional configuration of each I/O port.

Both group I and group II accept commands from the read/write control logic and control words from the internal data bus and in turn controls its associated I/O ports, as follows:

- Group I: port A and upper port C (PC_7-PC_4)
- Group II: port B and lower port C (PC_3-PC_0)

While the control word register can be written to, the contents cannot be read back to the processor.

Absolute Maximum Ratings

T_A = 25°C

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin with respect to V_{SS}	−0.5 to +7 V

Comment: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ±10%; V_{SS} = 0 V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input low voltage	V_{IL}	−0.5	0.8	V	
Input high voltage	V_{IH}	2	V_{CC}	V	
Output low voltage	V_{OL}		0.45	V	(2)
Output high voltage	V_{OH}	2.4		V	(3)
Darlington drive current	I_{OH} (1)	−1	−4	mA	V_{EXT} = 1.5 V R_{EXT} = 750Ω
Power supply current	I_{CC}		120	mA	V_{CC} = +5 V, output open
Input leakage current	I_{LIH}		10	μA	V_{IN} = V = V_{CC}
Input leakage current	I_{LIL}		−10	μA	V_{IN} = 0.4 V
Output leakage current	I_{LOH}		±10	μA	V_{OUT} = V_{CC}; CS = 2.0 V
Output leakage current	I_{LOL}		−10	μA	V_{OUT} = 0.4 V; CS = 2.0 V

Note:

(1) Any set of eight outputs from either port A, B, C can source 4 mA into 1.5 V.

(2) I_{OL} = 2.5 mA for DB port; 1.7 mA for peripheral ports.

(3) I_{OH} = −400μA for DB port; −200 μA for peripheral ports.

Capacitance

T_A = 25°C; V_{CC} = 0V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input capacitance	C_I		10	pF	f_c = 1 MHz
I/O capacitance	C_{IO}		20	pF	Unmeasured pins returned to V_{SS}

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AC Characteristics

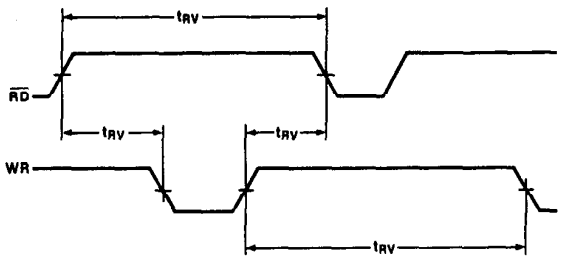
T_A = 0°C to +70°C; V_{CC} = +5 V ±5%; V_{SS} = 0 V

Parameter	Symbol	8255A-2 Limits Min	8255A-2 Limits Max	8255A-5 Limits Min	8255A-5 Limits Max	Unit	Test Conditions
Address stable before $\overline{READ}$	t_{AR}	0		0		ns	
Address stable after $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ pulse width	t_{RR}	200		250		ns	
Data valid from $\overline{READ}$	t_{RD}		140		170	ns	C_L = 150 pF
Data float after $\overline{READ}$	t_{DF}		100		100	ns	C_L = 100 pF
		10		10		ns	C_L = 15 pF
Time between $\overline{READ}$s and /$\overline{WRITE}$s	t_{RV}	200		850		ns	(Note 2)
Write							
Address stable before $\overline{WRITE}$	t_{AW}	0		0		ns	
Address stable after $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ pulse width	t_{WW}	200		250		ns	
Data valid to $\overline{WRITE}$ (T.E.)	t_{DW}	100		100		ns	
Data valid after $\overline{WRITE}$	t_{WD}	0		0		ns	
Other Timing							
$\overline{WR}$ = 0 to output	t_{WB}		350		350	ns	C_L = 150 pF
Peripheral data before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral data after $\overline{RD}$	t_{HR}	0		0		ns	
$\overline{ACK}$ pulse width	t_{AK}	300		300		ns	
$\overline{STB}$ pulse width	t_{ST}	350		350		ns	
Per. data before T.E. of $\overline{STB}$	t_{PS}	0		0		ns	
Per. data after T.E. of $\overline{STB}$	t_{PH}	150		150		ns	
$\overline{ACK}$ = 0 to output	t_{AD}		300		300	ns	C_L = 150 pF
$\overline{ACK}$ = 0 to output float	t_{KD}		250		250	ns	C_L = 50 pF
		20		20			C_L = 15 pF
$\overline{WR}$ = 1 to OBF = 0	t_{WOB}		300		650	ns	
$\overline{ACK}$ = 0 to OBF = 1	t_{AOB}		350		350	ns	
$\overline{STB}$ = 0 to IBF = 1	t_{SIB}		300		300	ns	
$\overline{RD}$ = 1 to IBF = 0	t_{RIB}		300		300	ns	
$\overline{RD}$ = 0 to INTR = 0	t_{RIT}		400		400	ns	
$\overline{STB}$ = 1 to INTR = 1	t_{SIT}		300		300	ns	C_L = 150 pF
$\overline{ACK}$ = 1 to INTR = 1	t_{AIT}		350		350	ns	
$\overline{WR}$ = 0 to INTR = 0	t_{WIT}		450		850	ns	C_L = 150 pF (Note 3)

Note:

(1) Period of reset pulse must be at least 50 μs during or after power on. Subsequent reset pulse can be 500 ns min.

(2)



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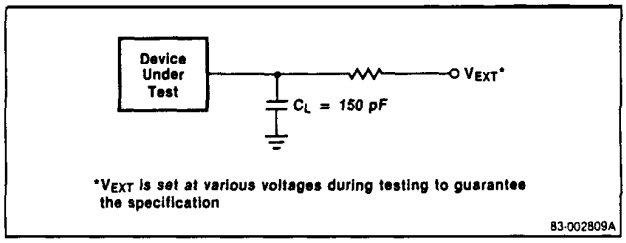
(3) INTR↑ may occur as early as $\overline{WR}$↓.

AC Testing Load Circuit



*V_{EXT} is set at various voltages during testing to guarantee the specification

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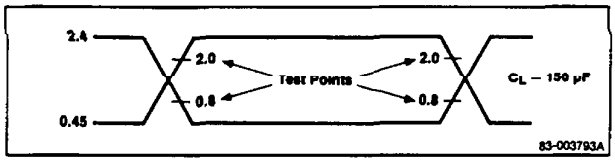
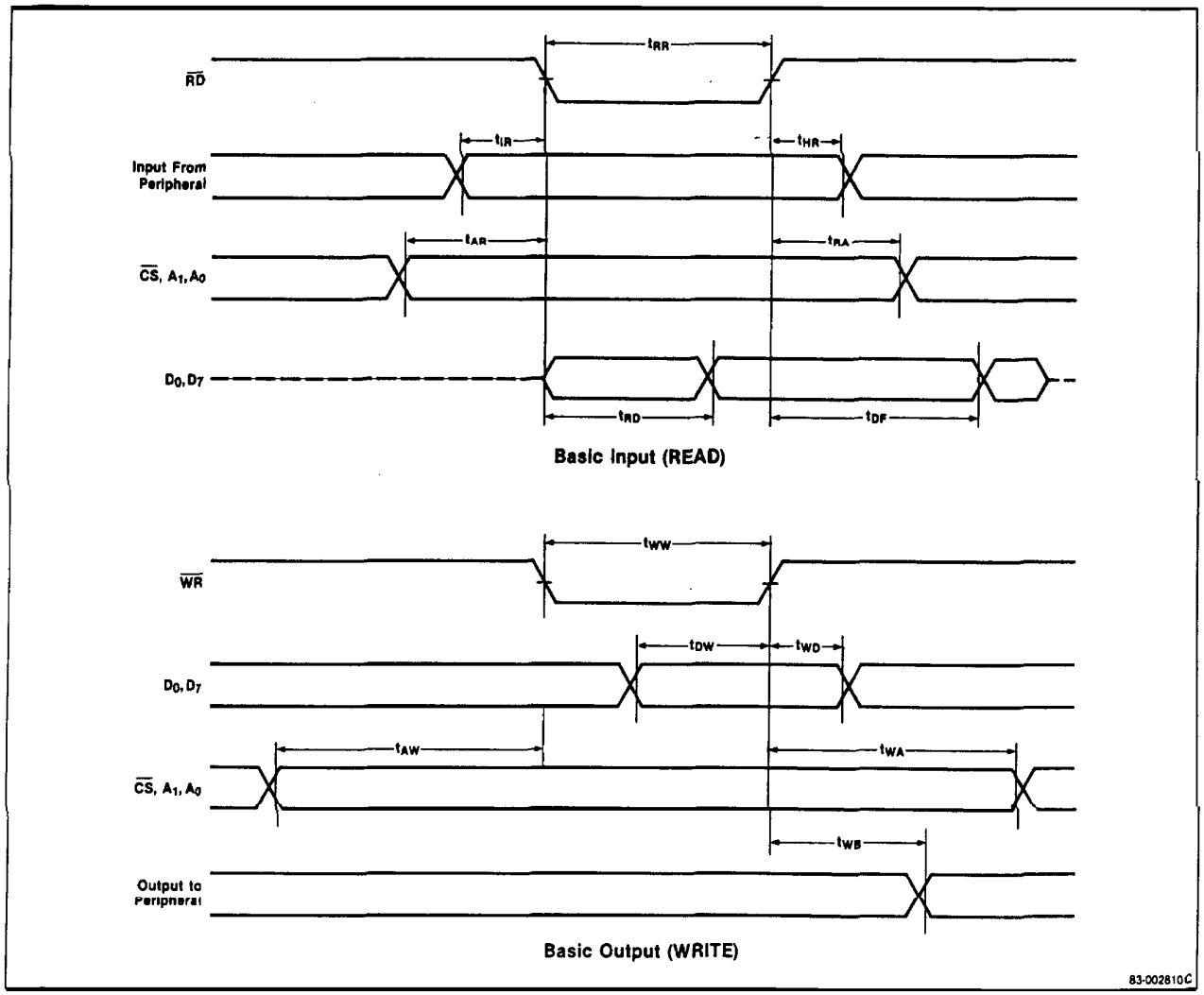
Timing Waveforms

AC Testing Input, Output Waveform



Mode 0



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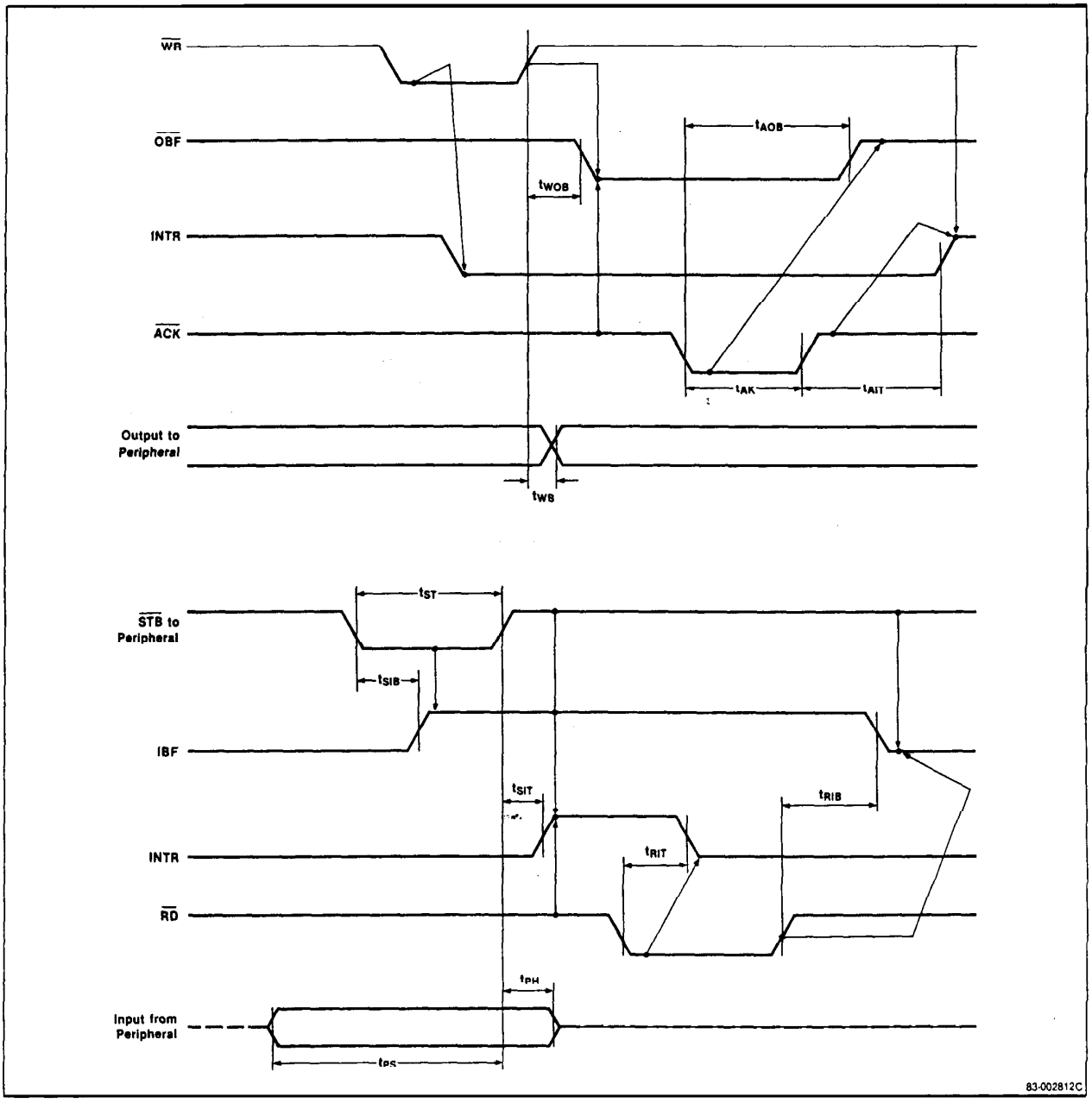
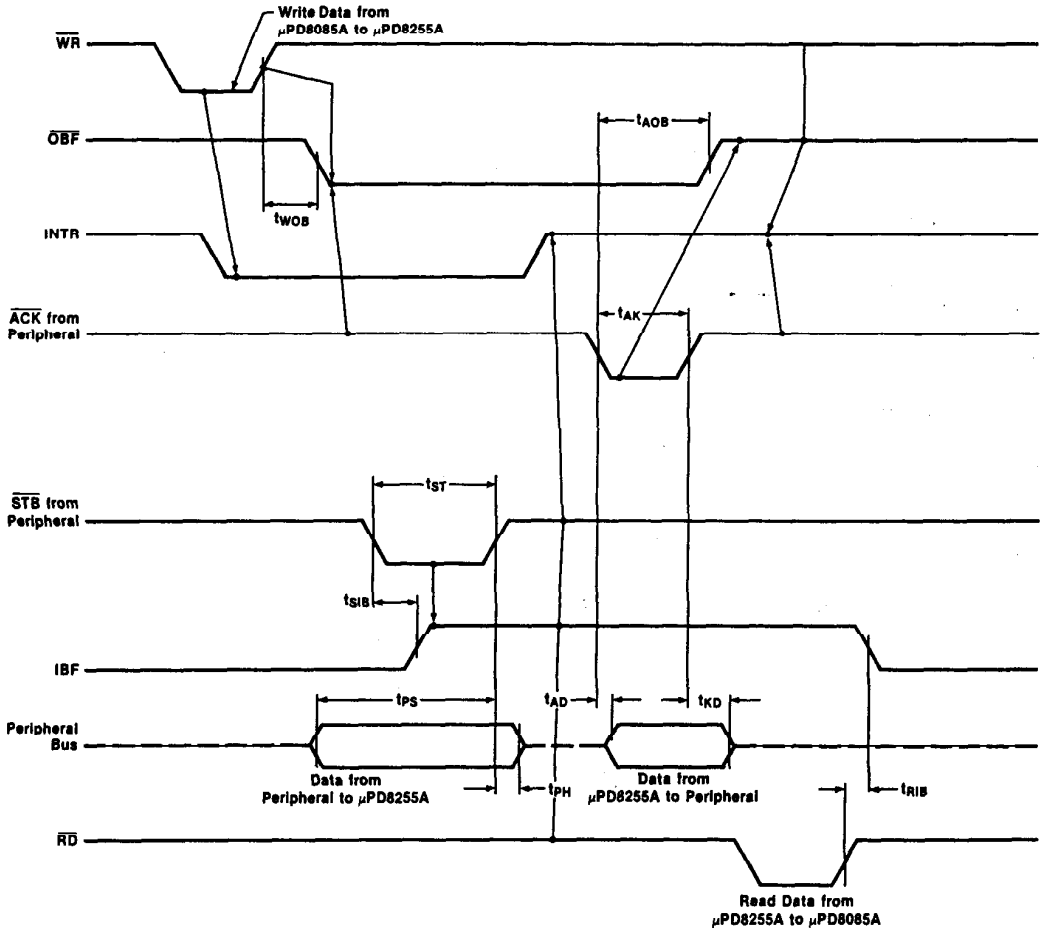
Timing Waveforms (cont)

Mode 1



Timing Waveforms (cont)

Mode 2



Note:

(1) Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$).

(2) When the μPD8255A is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

83-002813C

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Modes

The μPD8255A can be operated in modes 0, 1 or 2 which are selected by appropriate control words and are detailed below.

Mode 0

Mode 0 provides basic input and output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

- 16 different configurations in mode 0
- Two 8-bit ports and two 4-bit ports
- Inputs are not latched
- Outputs are latched

Mode 1

Mode 1 provides for strobed input and output operations with data transferred through port A or B and handshaking through port C.

- Two I/O groups (I and II)
- Both groups contain an 8-bit data port and a 4-bit control/data port
- Both 8-bit data ports can be either latched input or latched output

Mode 2

Mode 2 provides for strobed bidirectional operation using PA_0PA_7 as the bidirectional latched data bus. PC_3PC_7 is used for interrupts and "handshaking" bus flow control similar to mode 1. Note that PB_0PB_7 and PC_0PC_2 may be defined as mode 0 or 1, input or output in conjunction with port A in mode 2.

- An 8-bit latched bidirectional bus port (PA_0-PA_7) and a 5-bit control port (PC_3PC_7)
- Both inputs and outputs are latched
- An additional 8-bit input or output port with a 3-bit control port.

Basic Operation

Input Operation (Read)

A_1	A_0	RD	WR	CS	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

Output Operation (Write)

A_1	A_0	RD	WR	CS	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

Disable Function

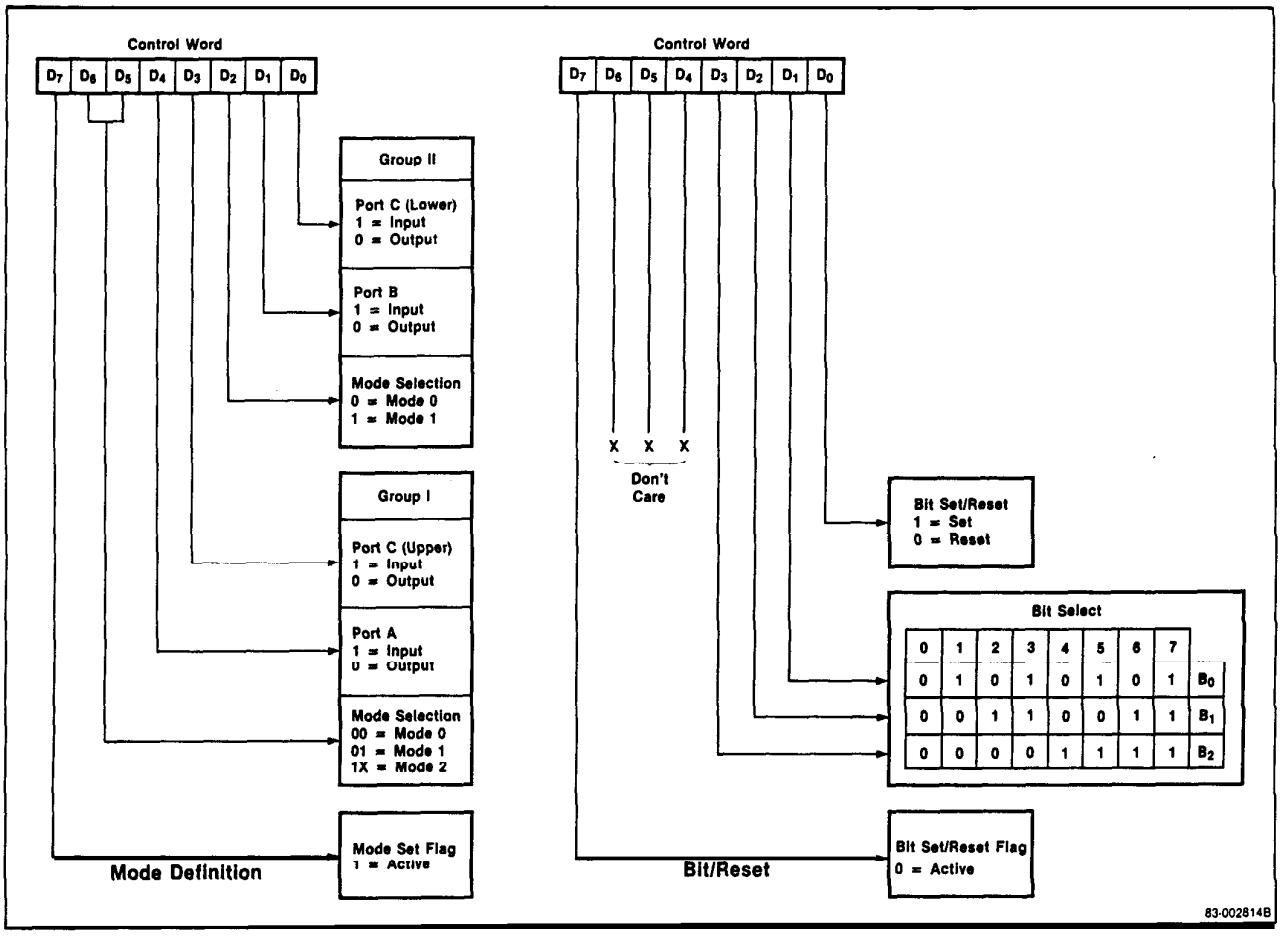
A_1	A_0	RD	WR	CS	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

Note:

(1) X means "DO NOT CARE"
(2) All conditions not listed are illegal and should be avoided.

Formats

Mode Definition, Bit/Rest Format



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9 APPENDIX G

DS1202 Datasheet Reprint

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DALLAS SEMICONDUCTOR

DS1202, DS1202S
Serial Timekeeping Chip

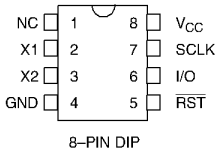
FEATURES

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100
- 24 x 8 RAM for scratchpad data storage
- Serial I/O for minimum pin count
- 2.0–5.5 volt full operation
- Uses less than 300 nA at 2 volts
- Single–byte or multiple–byte (burst mode) data transfer for read or write of clock or RAM data
- 8–pin DIP or optional 16–pin SOIC for surface mount
- Simple 3–wire interface
- TTL–compatible (V_{CC} = 5V)
- Optional industrial temperature range –40°C to +85°C (IND)

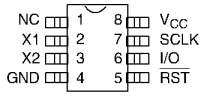
ORDERING INFORMATION

DS1202	8–pin DIP
DS1202S	16–pin SOIC
DS1202S–8	8–pin SOIC
DS1202N	8–pin DIP (IND)
DS1202SN	16–pin SOIC (IND)
DS1202SN–8	8–pin SOIC (IND)

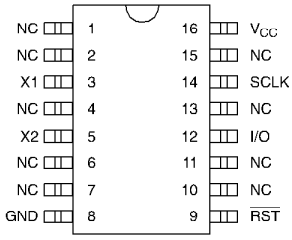
PIN ASSIGNMENT



8–PIN DIP



8–PIN SOIC (208 mil)



16–PIN SOIC

PIN DESCRIPTION

NC	–	No Connection
X1, X2	–	32.768 KHz Crystal Input
GND	–	Ground
$\overline{RST}$	–	Reset
I/O	–	Data Input/Output
SCLK	–	Serial Clock
V_{CC}	–	Power Supply Pin

DESCRIPTION

The DS1202 Serial Timekeeping Chip contains a real time clock/calendar and 24 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24–hour or 12–hour format with an AM/PM indicator. Interfacing the DS1202 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: (1) $\overline{RST}$ (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock/RAM one byte at a time or in a burst of up to 24 bytes. The DS1202 is designed to operate on very low power and retain data and clock information on less than 1 microwatt.

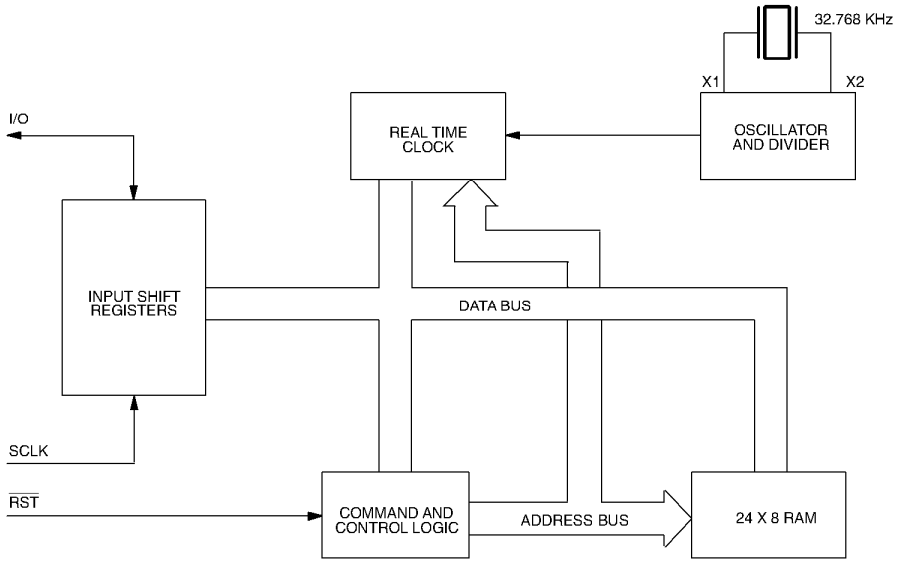
OPERATION

The main elements of the Serial Timekeeper are shown in Figure 1: shift register, control logic, oscillator, real time clock, and RAM. To initiate any transfer of data, $\overline{RST}$ is taken high and eight bits are loaded into the shift register providing both address and command information. Data is serially input on the rising edge of the SCLK. The first eight bits specify which of 32 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur. After the first eight clock cycles have occurred which load the command word into the shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equals eight plus eight for byte mode or eight plus up to 192 for burst mode.

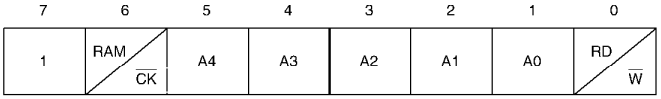
COMMAND BYTE

The command byte is shown in Figure 2. Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logic 1. If it is zero, further action will be terminated. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits one through five specify the designated registers to be input or output, and the LSB (Bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

DS1202 BLOCK DIAGRAM Figure 1



ADDRESS/COMMAND BYTE Figure 2



RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves two functions. First, $\overline{RST}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{RST}$ signal provides a method of terminating either single byte or multiple byte data transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on t he falling edge of clock. All data transfer terminates if the $\overline{RST}$ input is low and the I/O pin goes to a high impedance state. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0. Due to the inherent nature of the logic state machine, writing times containing an absolute value of "59" seconds should be avoided.

DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as $\overline{RST}$ remains high. This operation permits continuous burst mode read capability. Data is output starting with bit 0.

BURST MODE

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits one through five = logical one). As before, bit six specified clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 8 through 31 in the Clock/Calendar Registers or locations 24 through 31 in the RAM registers. When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred.

However, when writing to RAM in burst mode it is not necessary to write all 24 bytes for the data to transfer. Each byte that is written to will be transferred to RAM regardless of whether all 24 bytes are written or not.

CLOCK/CALENDAR

The clock/calendar is contained in eight write/read registers as shown in Figure 4. Data contained in the clock/calendar registers is in binary coded decimal format (BCD).

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is stopped and the DS1202 is placed into a low–power standby mode with a current drain of not more than 100 nanoamps. When this bit is written to logic 0, the clock will start.

AM–PM/12–24 MODE

Bit 7 of the hours register is defined as the 12– or 24–hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24–hour mode, bit 5 is the second 10 hour bit (20–23 hours).

WRITE PROTECT BIT

Bit 7 of the control register is the write protect bit. The first seven bits (bits 0–6) are forced to zero and will always read a zero when read. Before any write operation to the clock or RAM, bit 7 must be zero. When high, the write protect bit prevents a write operation to any other register.

CLOCK/CALENDAR BURST MODE

The clock/calendar command byte specifies burst mode operation. In this mode the eight clock/calendar registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

RAM

The static RAM is 24 x 8 bytes addressed consecutively in the RAM address space.

RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 24 RAM registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

REGISTER SUMMARY

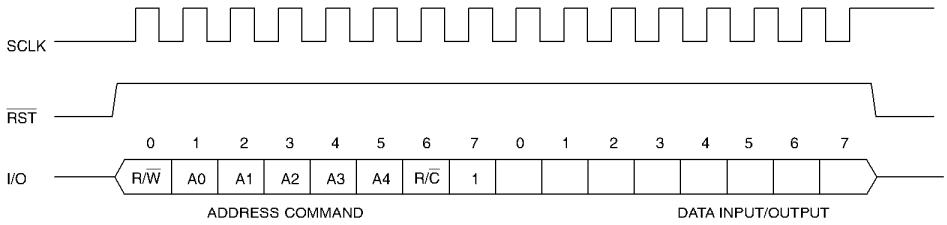
A register data format summary is shown in Figure 4.

CRYSTAL SELECTION

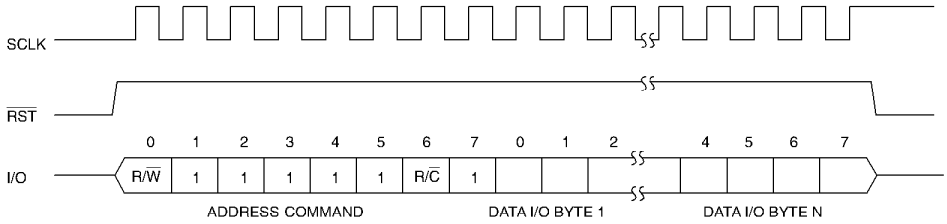
A 32.768 KHz crystal, can be directly connected to the DS1202 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (CL) of 6 pF. The crystal is connected directly to the X1 and X2 pins. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real Time Clocks”.

DATA TRANSFER SUMMARY Figure 3

SINGLE BYTE TRANSFER

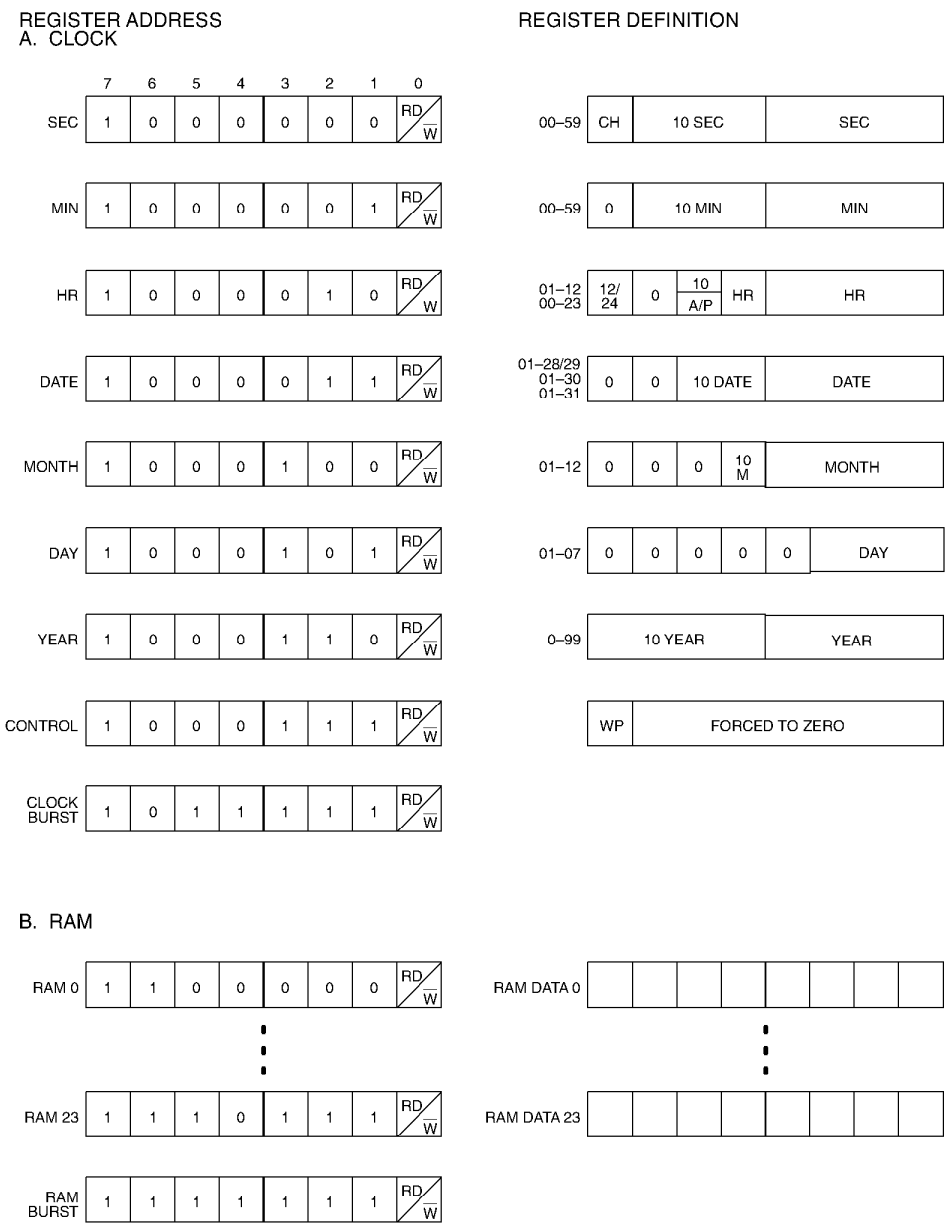


BURST MODE TRANSFER



FUNCTION	BYTE N	SCLK n
CLOCK	8	72
RAM	24	200

REGISTER ADDRESS/DEFINITION Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		2.0		5.5	V	1
Logic 1 Input	V_{IH}		2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	V_{CC}=2.0V	–0.3		+0.3	V	1
		V_{CC}=5V	–0.3		+0.8		

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 2.0 to 5.5V*)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}				+500	µA	6
I/O Leakage	I_{LO}				+500	µA	6
Logic 1 Output	V_{OH}	V_{CC}=2V	1.6			V	2
		V_{CC}=5V	2.4				
Logic 0 Output	V_{OL}	V_{CC}=2V			0.4	V	3
		V_{CC}=5V			0.4		
Active Supply Current	I_{CC}	V_{CC}=2V			0.4	mA	5
		V_{CC}=5V			1.2		
Timekeeping Current	I_{CC1}	V_{CC}=2V			0.3	µA	4
		V_{CC}=5V			1		
Leakage Current	I_{CC2}	V_{CC}=2V			100	nA	10
		V_{CC}=5V			100		

*Unless otherwise noted.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance	C_X		6		pF	

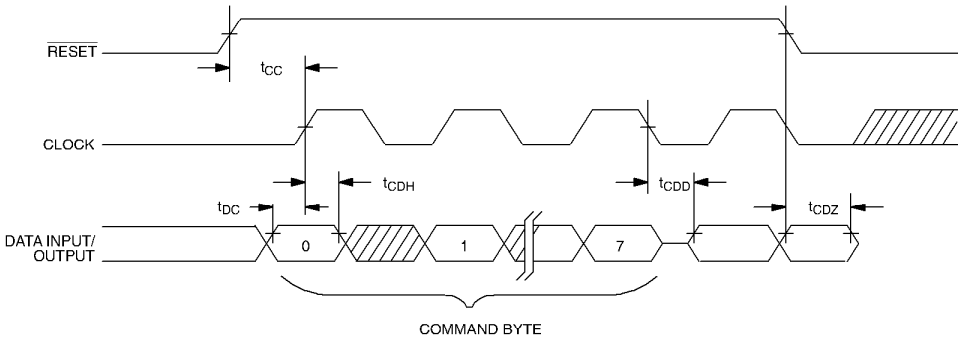
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 2.0 to 5.5V*)

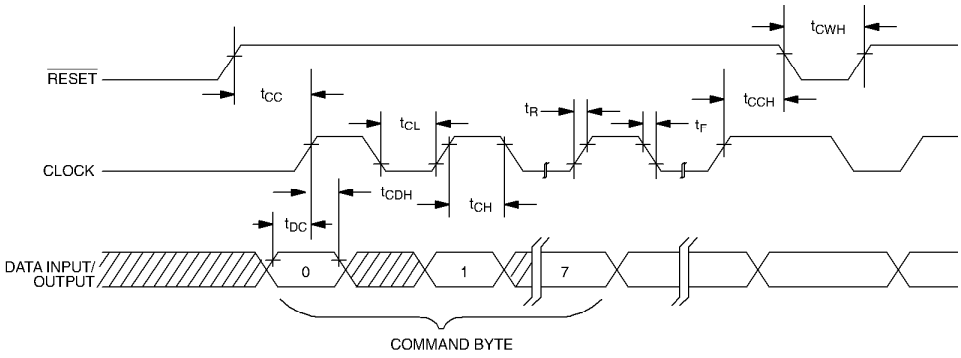
PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	V_{CC}=2V	200			ns	7
		V_{CC}=5V	50				
CLK to Data Hold	t_{CDH}	V_{CC}=2V	280			ns	7
		V_{CC}=5V	70				
CLK to Data Delay	t_{CDD}	V_{CC}=2V			800	ns	7, 8, 9
		V_{CC}=5V			200		
CLK Low Time	t_{CL}	V_{CC}=2V	1000			ns	7
		V_{CC}=5V	250				
CLK High Time	t_{CH}	V_{CC}=2V	1000			ns	7, 12
		V_{CC}=5V	250				
CLK Frequency	f_{CLK}	V_{CC}=2V			0.5	MHz	7, 12
		V_{CC}=5V	DC		2.0		
CLK Rise and Fall	t_R, t_F	V_{CC}=2V			2000	ns	
		V_{CC}=5V			500		
$\overline{RST}$ to CLK Setup	t_{CC}	V_{CC}=2V	4			µs	7
		V_{CC}=5V	1				
CLK to $\overline{RST}$ Hold	t_{CCH}	V_{CC}=2V	1000			ns	7
		V_{CC}=5V	250				
$\overline{RST}$ Inactive Time	t_{CWH}	V_{CC}=2V	4			µs	7
		V_{CC}=5V	1				
$\overline{RST}$ to I/O High Z	t_{CDZ}	V_{CC}=2V			280	ns	7
		V_{CC}=5V			70		

*Unless otherwise noted.

TIMING DIAGRAM: READ DATA TRANSFER Figure 5



TIMING DIAGRAM: WRITE DATA TRANSFER Figure 6



NOTES:

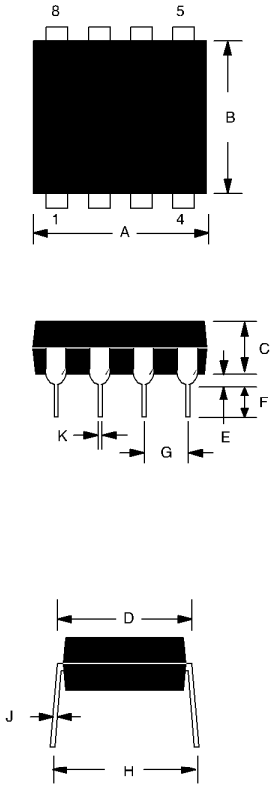
1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA at V_{CC}=5V and 0.4 mA at V_{CC}=2V, V_{OH}=V_{CC} for capacitive loads.
3. Logic zero voltages are specified at a sink current of 4 mA at V_{CC}=5V and 1.5 mA at V_{CC}=2V.
4. I_{CC1} is specified with I/O open, $\overline{RST}$ set to a logic 0, and clock halt flag=0 (oscillator enabled).
5. I_{CC} is specified with the I/O pin open, $\overline{RST}$ high, SCLK=2 MHz at V_{CC}=5V; SCLK=500 KHz, V_{CC}=2V and clock halt flag=0 (oscillator enabled).
6. $\overline{RST}$, SCLK, and I/O all have 40KΩ pull–down resistors to ground.
7. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10 ms maximum rise and fall time.
8. Measured at V_{OH}=2.4V or V_{OL}=0.4V.
9. Load capacitance = 50 pF.

10. I_{CC2} is specified with $\overline{RST}$, I/O, and SCLK open. The clock halt flag must be set to logic one (oscillator disabled).

11. At power–up, $\overline{RST}$ must be at a logic 0 until $V_{CC} \geqq 2$ volts. Also, SCLK must be at a logic 0 when $\overline{RST}$ is driven to a logic one state.

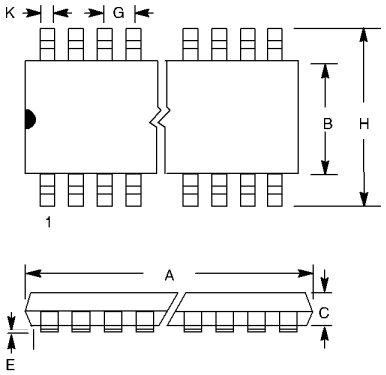
12. If t_{CH} exceeds 100 ms with $\overline{RST}$ in a logic one state, then I_{CC} may briefly exceed I_{CC} specification.

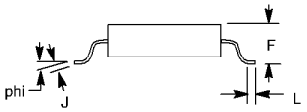
DS1202 SERIAL TIMEKEEPER 8–PIN DIP



PKG	8–PIN	
DIM	MIN	MAX
A IN. MM	0.360	0.400
B IN. MM	0.240	0.260
C IN. MM	0.120	0.140
D IN. MM	0.300	0.325
E IN. MM	0.015	0.040
F IN. MM	0.110	0.140
G IN. MM	0.090	0.110
H IN. MM	0.320	0.370
J IN. MM	0.008	0.012
K IN. MM	0.015	0.021

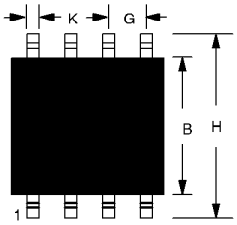
DS1202S SERIAL TIMEKEEPER 16–PIN SOIC

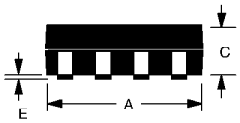




PKG	16–PIN	
DIM	MIN	MAX
A IN. MM	0.500 12.70	0.511 12.99
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN MM	0.016 0.406	0.040 1.20
phi	0°	8°

DS1202S8 8–PIN SOIC 200 MIL





PKG	8–PIN	
DIM	MIN	MAX
A IN. MM	0.203 5.16	0.213 5.41
B IN. MM	0.203 5.16	0.213 5.41
C IN. MM	0.070 1.78	0.074 1.88
E IN. MM	0.004 0.102	0.010 0.390
F IN. MM	0.074 1.88	0.84 2.13
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.302 7.67	0.318 8.07
J IN. MM	0.006 0.152	0.010 0.254
K IN. MM	0.013 0.33	0.020 0.508
L IN. MM	0.19 4.83	0.030 0.762

10 APPENDIX H

MAX186 Datasheet Reprint

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19-0123; Rev. 4; 8/96

EVALUATION KIT AVAILABLE

Low-Power, 8-Channel, Serial 12-Bit ADCs

General Description

The MAX186/MAX188 are 12-bit data-acquisition systems that combine an 8-channel multiplexer, high-bandwidth track/hold, and serial interface together with high conversion speed and ultra-low power consumption. The devices operate with a single +5V supply or dual ±5V supplies. The analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™ and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320 family digital signal processors. The MAX186/MAX188 use either the internal clock or an external serial-interface clock to perform successive-approximation A/D conversions. The serial interface can operate beyond 4MHz when the internal clock is used.

The MAX186 has an internal 4.096V reference while the MAX188 requires an external reference. Both parts have a reference-buffer amplifier that simplifies gain trim .

The MAX186/MAX188 provide a hard-wired $\overline{SHDN}$ pin and two software-selectable power-down modes. Accessing the serial interface automatically powers up the devices, and the quick turn-on time allows the MAX186/MAX188 to be shut down between every conversion. Using this technique of powering down between conversions, supply current can be cut to under 10µA at reduced sampling rates.

The MAX186/MAX188 are available in 20-pin DIP and SO packages, and in a shrink small-outline package (SSOP), that occupies 30% less area than an 8-pin DIP. For applications that call for a parallel interface, see the MAX180/MAX181 data sheet. For anti-aliasing filters, consult the MAX274/MAX275 data sheet.

Applications

Portable Data Logging

Data-Acquisition

High-Accuracy Process Control

Automatic Testing

Robotics

Battery-Powered Instruments

Medical Instruments

SPI and QSPI are registered trademarks of Motorola.
Microwire is a registered trademark of National Semiconductor.

Features

- ♦ **8-Channel Single-Ended or 4-Channel Differential Inputs**
- ♦ **Single +5V or ±5V Operation**
- ♦ **Low Power: 1.5mA (operating mode)**
  2µA (power-down mode)
- ♦ **Internal Track/Hold, 133kHz Sampling Rate**
- ♦ **Internal 4.096V Reference (MAX186)**
- ♦ **SPI-, QSPI-, Microwire-, TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar or Bipolar Inputs**
- ♦ **20-Pin DIP, SO, SSOP Packages**
- ♦ **Evaluation Kit Available**

Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX186_CPP	0°C to +70°C	20 Plastic DIP
MAX186_CWP	0°C to +70°C	20 SO
MAX186_CAP	0°C to +70°C	20 SSOP
MAX186DC/D	0°C to +70°C	Dice*
MAX186_EPP	-40°C to +85°C	20 Plastic DIP
MAX186_EWP	-40°C to +85°C	20 SO
MAX186_EAP	-40°C to +85°C	20 SSOP
MAX186_MJP	-55°C to +125°C	20 CERDIP**

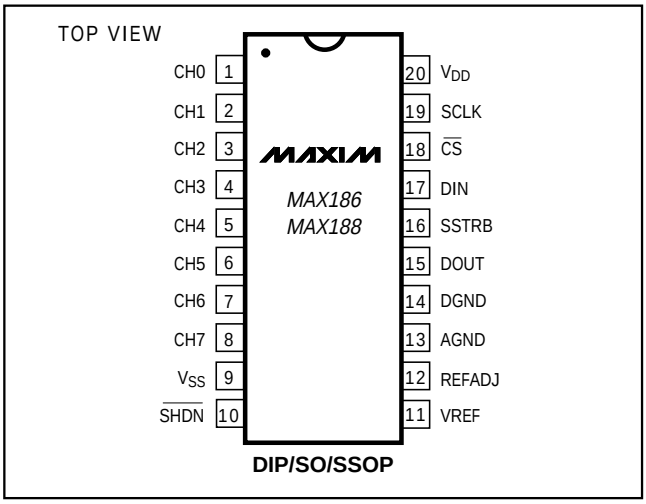
Ordering Information continued on last page.

† NOTE: Parts are offered in grades A, B, C and D (grades defined in Electrical Characteristics). When ordering, please specify grade. Contact factory for availability of A-grade in SSOP package.

** Dice are specified at +25°C, DC parameters only.*

*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



Low-Power, 8-Channel, Serial 12-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +6V
V_{SS} to AGND .....+0.3V to -6V
V_{DD} to V_{SS} .....-0.3V to +12V
AGND to DGND .....-0.3V to +0.3V
CH0–CH7 to AGND, DGND .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
CH0–CH7 Total Input Current .....±20mA
VREF to AGND .....-0.3V to (V_{DD} + 0.3V)
REFADJ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX186_C/MAX188_C .....0°C to +70°C
MAX186_E/MAX188_E .....-40°C to +85°C
MAX186_M/MAX188_M .....-55°C to +125°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				12			Bits
Relative Accuracy (Note 2)		MAX186A/MAX188A				±0.5	LSB
		MAX186B/MAX188B				±0.5	
		MAX186C				±1.0	
		MAX188C				±0.75	
		MAX186D/MAX188D				±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature				±1	LSB
Offset Error		MAX186A/MAX188A				±2.0	LSB
		MAX186B/MAX188B				±3.0	
		MAX186C/MAX188C				±3.0	
		MAX186D/MAX188D				±3.0	
Gain Error (Note 3)		MAX186 (all grades)				±3.0	LSB
		External reference 4.096V (MAX188)	MAX188A			±1.5	
			MAX188B			±2.0	
			MAX188C			±2.0	
			MAX188D			±3.0	
Gain Temperature Coefficient		External reference, 4.096V			±0.8		ppm/°C
Channel-to-Channel Offset Matching					±0.1		LSB
DYNAMIC SPECIFICATIONS (10kHz sine wave input, 4.096V_{P-P}, 133ksps, 2.0MHz external clock, bipolar input mode)							
Signal-to-Noise + Distortion Ratio	SINAD			70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD					-80	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		65kHz, V_{IN} = 4.096V_{P-P} (Note 4)			-85		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal Bandwidth		-3dB rolloff			4.5		MHz
Full-Power Bandwidth					800		kHz
CONVERSION RATE							
Conversion Time (Note 5)	t_{CONV}	Internal clock		5.5		10	µs
		External clock, 2MHz, 12 clocks/conversion		6			
Track/Hold Acquisition Time	t_{AZ}					1.5	µs
Aperture Delay					10		ns
Aperture Jitter					<50		ps
Internal Clock Frequency					1.7		MHz
External Clock Frequency Range		External compensation, 4.7µF		0.1		2.0	MHz
		Internal compensation (Note 6)		0.1		0.4	
		Used for data transfer only			10		
ANALOG INPUT							
Input Voltage Range, Single-Ended and Differential (Note 9)		Unipolar, V_{SS} = 0V				0 to VREF	V
		Bipolar, V_{SS} = -5V				±VREF/2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = ±5V			±0.01	±1	µA
Input Capacitance		(Note 6)			16		pF
INTERNAL REFERENCE (MAX186 only, reference buffer enabled)							
VREF Output Voltage		T_A = +25°C		4.076	4.096	4.116	V
VREF Short-Circuit Current						30	mA
VREF Tempco		MAX186A, MAX186B, MAX186C	MAX186_C		±30	±50	ppm/°C
			MAX186_E		±30	±60	
			MAX186_M		±30	±80	
		MAX186D			±30		
Load Regulation (Note 7)		0mA to 0.5mA output load			2.5		mV
Capacitive Bypass at VREF		Internal compensation		0			µF
		External compensation		4.7			
Capacitive Bypass at REFADJ		Internal compensation		0.01			µF
		External compensation		0.01			
REFADJ Adjustment Range					±1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled, VREF = 4.096V)							
Input Voltage Range				2.50		V_{DD} + 50mV	V
Input Current					200	350	µA
Input Resistance				12	20		kΩ
Shutdown VREF Input Current					1.5	10	µA
Buffer Disable Threshold REFADJ				V_{DD} - 50mV			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference-Buffer Gain		MAX186		1.678		V/V
		MAX188		1.638		
REFADJ Input Current		MAX186			±50	µA
		MAX188			±5	
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}		2.4			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.15		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}				0.5	V
$\overline{SHDN}$ Input Current, High	I_{INH}	$\overline{SHDN}$ = V_{DD}			4.0	µA
$\overline{SHDN}$ Input Current, Low	I_{INL}	$\overline{SHDN}$ = 0V	-4.0			µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}		1.5		V_{DD} -1.5	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		2.75		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$\overline{SHDN}$ = open	-100		100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	4			V
Three-State Leakage Current	I_L	$\overline{CS}$ = 5V			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = 5V (Note 6)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}			5 ±5%		V
Negative Supply Voltage	V_{SS}			0 or -5 ±5%		V
Positive Supply Current	I_{DD}	Operating mode		1.5	2.5	mA
		Fast power-down		30	70	µA
		Full power-down		2	10	
Negative Supply Current	I_{SS}	Operating mode and fast power-down			50	µA
		Full power-down			10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186—4.7µF capacitor at VREF pin; MAX188—external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Rejection (Note 8)	PSR	V_{DD} = 5V ±5%; external reference, 4.096V; full-scale input		±0.06	±0.5	mV
Negative Supply Rejection (Note 8)	PSR	V_{SS} = -5V ±5%; external reference, 4.096V; full-scale input		±0.01	±0.5	mV

Note 1: Tested at V_{DD} = 5.0V; V_{SS} = 0V; unipolar input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX186 – internal reference, offset nulled; MAX188 – external reference (VREF = +4.096V), offset nulled.
Note 4: Ground on-channel; sine wave applied to all off channels.
Note 5: Conversion time defined as the number of clock cycles times the clock period; clock has 50% duty cycle.
Note 6: Guaranteed by design. Not subject to production testing.
Note 7: External load should not change during conversion for specified accuracy.
Note 8: Measured at V_{SUPPLY} +5% and V_{SUPPLY} -5% only.
Note 9: The common-mode range for the analog inputs is from V_{SS} to V_{DD}.

TIMING CHARACTERISTICS

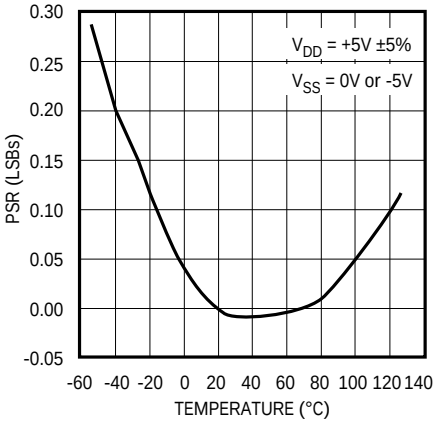
(V_{DD} = 5V ±5%; V_{SS} =0V or -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{AZ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	MAX18_ _C/E	20		150	ns
			MAX18_ _M	20		200	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF				200	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 6)	t_{SDV}	External clock mode only, C_{LOAD} = 100pF				200	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 6)	t_{STR}	External clock mode only, C_{LOAD} = 100pF				200	ns
SSTRB Rise to SCLK Rise (Note 6)	t_{SCK}	Internal clock mode only		0			ns

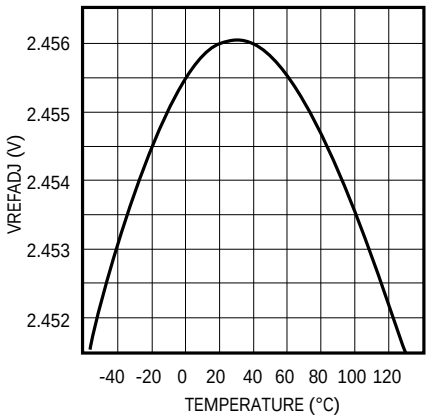
Low-Power, 8-Channel, Serial 12-Bit ADCs

Typical Operating Characteristics

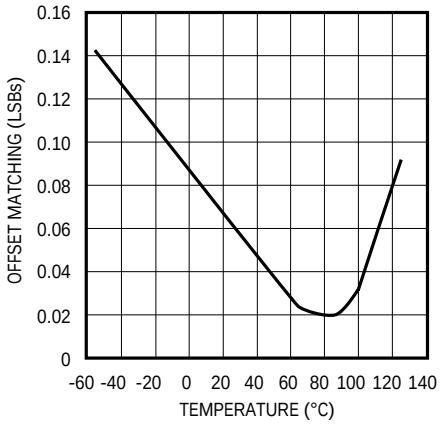
POWER-SUPPLY REJECTION vs. TEMPERATURE



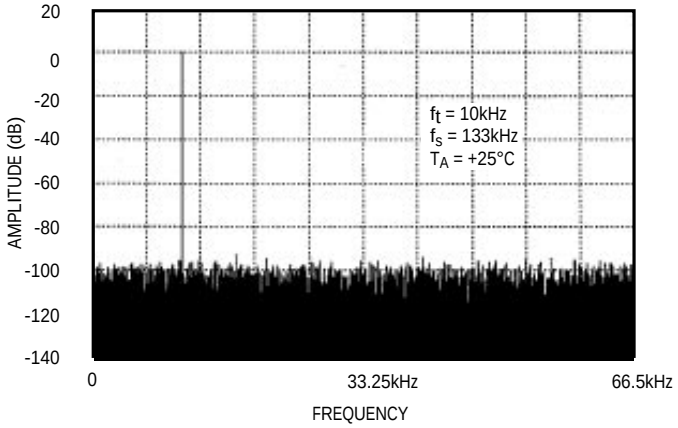
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



MAX186/MAX188 FFT PLOT – 133kHz



Pin Description

PIN	NAME	FUNCTION
1-8	CH0-CH7	Sampling Analog Inputs
9	V_{SS}	Negative Supply Voltage. Tie to -5V ±5% or AGND
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX186/MAX188 down to 10µA (max) supply current, otherwise the MAX186/MAX188 are fully operational. Pulling $\overline{SHDN}$ high puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
11	VREF	Reference Voltage for analog-to-digital conversion. Also, Output of the Reference Buffer Amplifier (4.096V in the MAX186, 1.638 x REFADJ in the MAX188). Add a 4.7µF capacitor to ground when using external compensation mode. Also functions as an input when used with a precision external reference.

Pin Description (continued)

PIN	NAME	FUNCTION
12	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD}.
13	AGND	Analog Ground. Also IN- Input for single-ended conversions.
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX186/MAX188 begin the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external mode).
17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK.
18	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60% in external clock mode.)
20	V_{DD}	Positive Supply Voltage, +5V ±5%

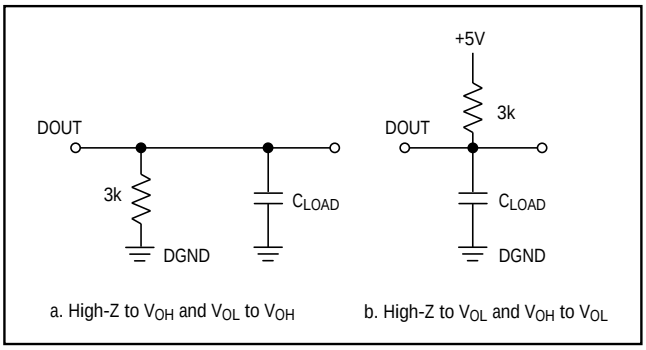


Figure 1. Load Circuits for Enable Time

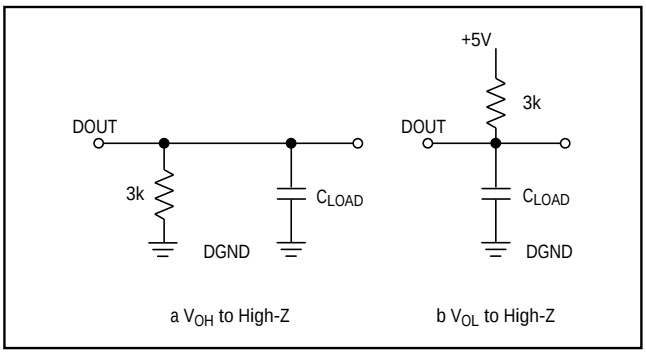


Figure 2. Load Circuits for Disabled Time

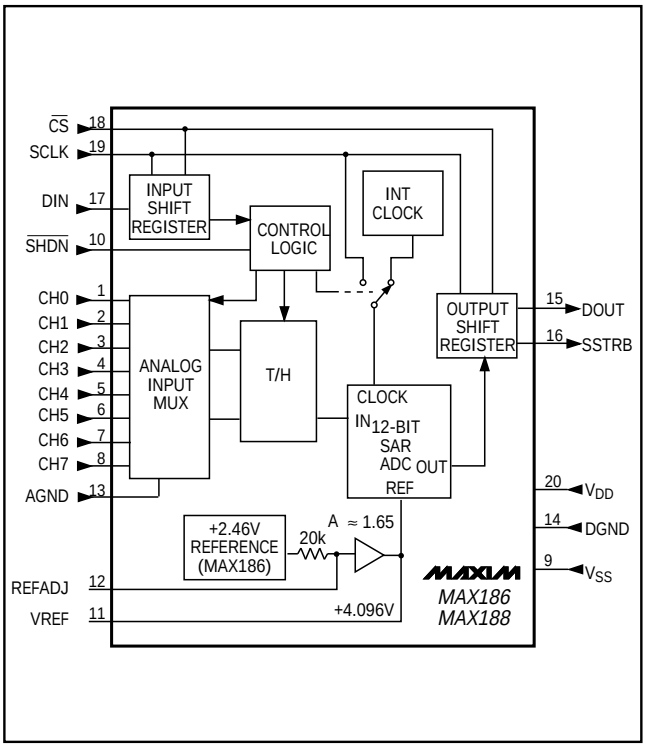


Figure 3. Block Diagram

Low-Power, 8-Channel, Serial 12-Bit ADCs

Detailed Description

The MAX186/MAX188 use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors. No external hold capacitors are required. Figure 3 shows the block diagram for the MAX186/MAX188.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the Equivalent Input Circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0-CH7 and IN- is switched to AGND. In differential mode, IN+ and IN- are selected from pairs of CH0/CH1, CH2/CH3, CH4/CH5 and CH6/CH7. Configure the channels with Table 3 and Table 4.

In differential mode, IN- and IN+ are internally switched to either one of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. Accomplish this by connecting a 0.1µF capacitor from AIN- (the selected analog input, respectively) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply AGND. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge of 16pF x $[(V_{IN}+) - (V_{IN}-)]$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. The T/H enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to AGND, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

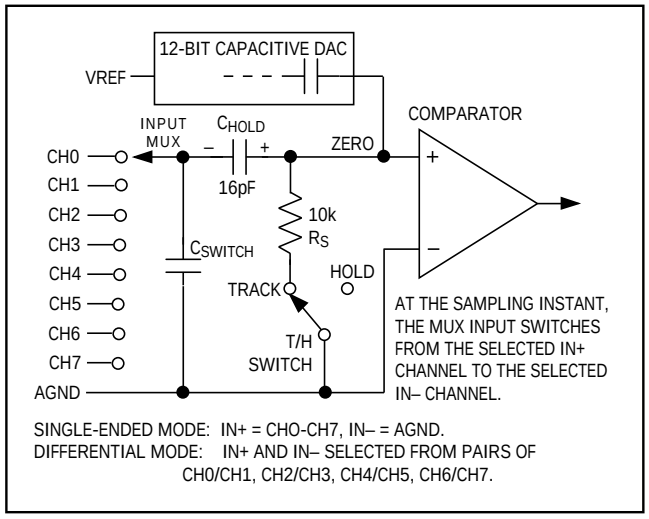


Figure 4. Equivalent Input Circuit

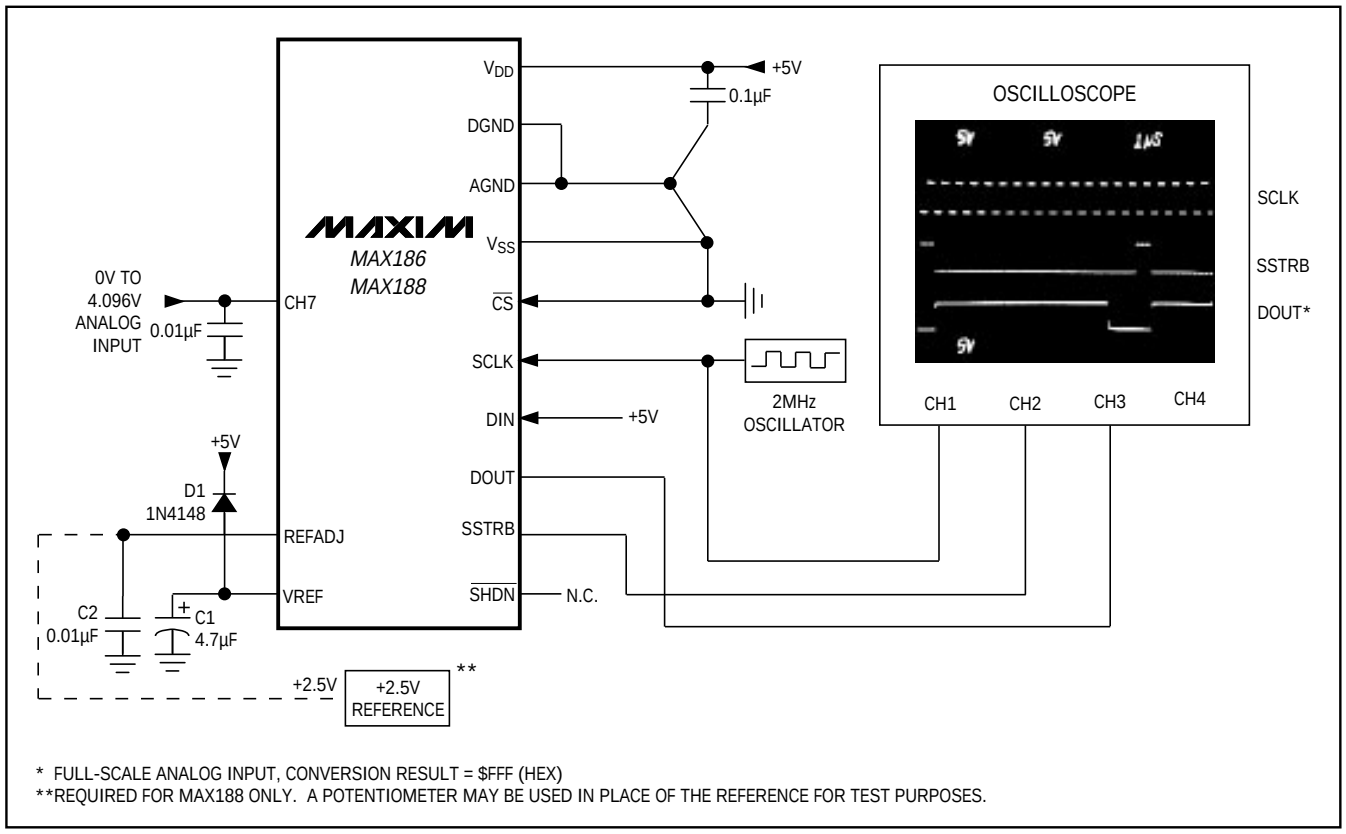
The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{AZ} = 9 \times (R_S + R_{IN}) \times 16pF,$$

where R_{IN} = 5kΩ, R_S = the source impedance of the input signal, and t_{AZ} is never less than 1.5µs. Note that source impedances below 5kΩ do not significantly affect the AC performance of the ADC. Higher source impedances can be used if an input capacitor is connected to the analog inputs, as shown in Figure 5. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 4.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.



* FULL-SCALE ANALOG INPUT, CONVERSION RESULT = $FFF (HEX)
**REQUIRED FOR MAX188 ONLY. A POTENTIOMETER MAY BE USED IN PLACE OF THE REFERENCE FOR TEST PURPOSES.

Figure 5. Quick-Look Circuit

Analog Input Range and Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and V_{SS}, allow the channel input pins to swing from V_{SS} - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV, or be lower than V_{SS} by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off-channels over two milliamperes, as excessive current will degrade the conversion accuracy of the on-channel.

The full-scale input voltage depends on the voltage at VREF. See Tables 1a and 1b.

Quick Look

To evaluate the analog performance of the MAX186/MAX188 quickly, use the circuit of Figure 5. The MAX186/MAX188 require a control byte to be written to DIN before each conversion. Tying DIN to +5V feeds in control bytes of $FF (HEX), which trigger

Table 1a. Unipolar Full Scale and Zero Scale

Reference	Zero Scale	Full Scale
Internal Reference (MAX186 only)	0V	+4.096V
External Reference at REFADJ	0V	V_{REFADJ} x A*
at VREF	0V	VREF

** A = 1.678 for the MAX186, 1.638 for the MAX188*

Table 1b. Bipolar Full Scale, Zero Scale, and Negative Full Scale

Reference	Negative Full Scale	Zero Scale	Full Scale
Internal Reference (MAX186 only)	-4.096V/2	0V	+4.096V/2
External Reference at REFADJ	-1/2V_{REFADJ} x A*	0V	+1/2V_{REFADJ} x A*
at VREF	-1/2 VREF	0V	+1/2 VREF

** A = 1.678 for the MAX186, 1.638 for the MAX188*

single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the 12-bit conversion result comes out of DOUT. Varying the analog input to CH7 should alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

How to Start a Conversion

A conversion is started on the MAX186/MAX188 by clocking a control byte into DIN. Each rising edge on SCLK, with $\overline{CS}$ low, clocks a bit from DIN into the MAX186/MAX188's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the MSB of the control byte. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 2 shows the control-byte format.

The MAX186/MAX188 are fully compatible with Microwire and SPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire and SPI both transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result).

Example: Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode, call it TB1. TB1 should be of the format: 1XXXXX11 Binary, where the Xs denote the particular channel and conversion-mode selected.

Table 2. Control-Byte Format

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

Bit	Name	Description
7(MSB)	START	The first logic "**1**" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion. See Tables 3 and 4.
3	UNI/$\overline{BIP}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.
2	SGL/$\overline{DIF}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to AGND. In differential mode, the voltage difference between two channels is measured. See Tables 3 and 4.
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode **0** **0** Full power-down (I_Q = 2µA) **0** **1** Fast power-down (I_Q = 30µA) **1** **0** Internal clock mode **1** **1** External clock mode

Table 3. Channel Selection in Single-Ended Mode (SGL/$\overline{DIFF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	AGND
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 4. Channel Selection in Differential Mode (SGL/$\overline{DIFF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ on the MAX186/MAX188 low.
3) Transmit TB1 and simultaneously receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 HEX) and simultaneously receive byte RB2.
5) Transmit a byte of all zeros ($00 HEX) and simultaneously receive byte RB3.
6) Pull $\overline{CS}$ on the MAX186/MAX188 high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of dead time between 8-bit transfers. Make sure that the total conversion time does not exceed 120µs, to avoid excessive T/H droop.

Digital Output

In unipolar input mode, the output is straight binary (see Figure 15). For bipolar inputs, the output is twos-complement (see Figure 16). Data is clocked out at the falling edge of SCLK in MSB-first format.

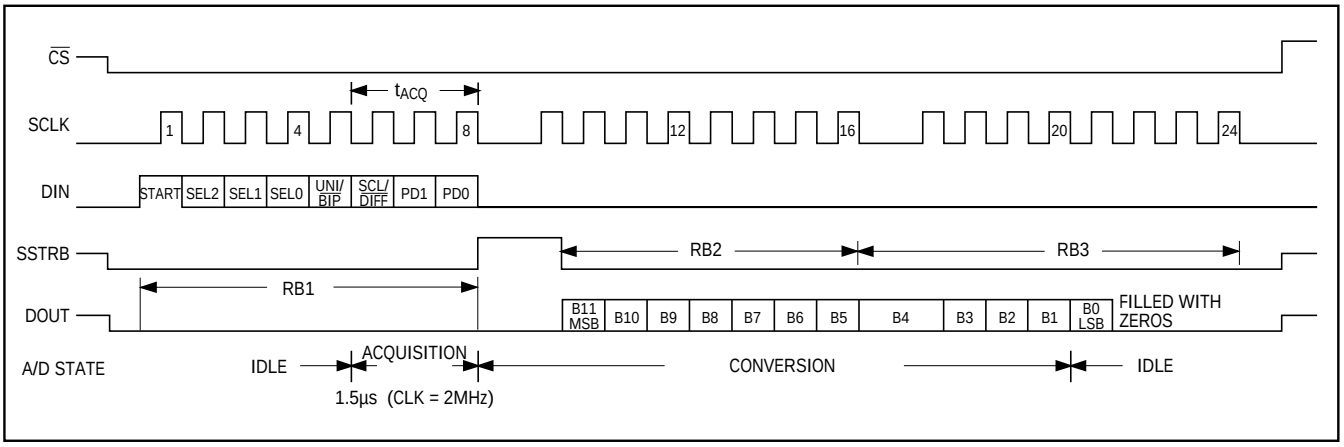


Figure 6. 24-Bit External Clock Mode Conversion Timing (SPI, QSPI and Microwire Compatible)

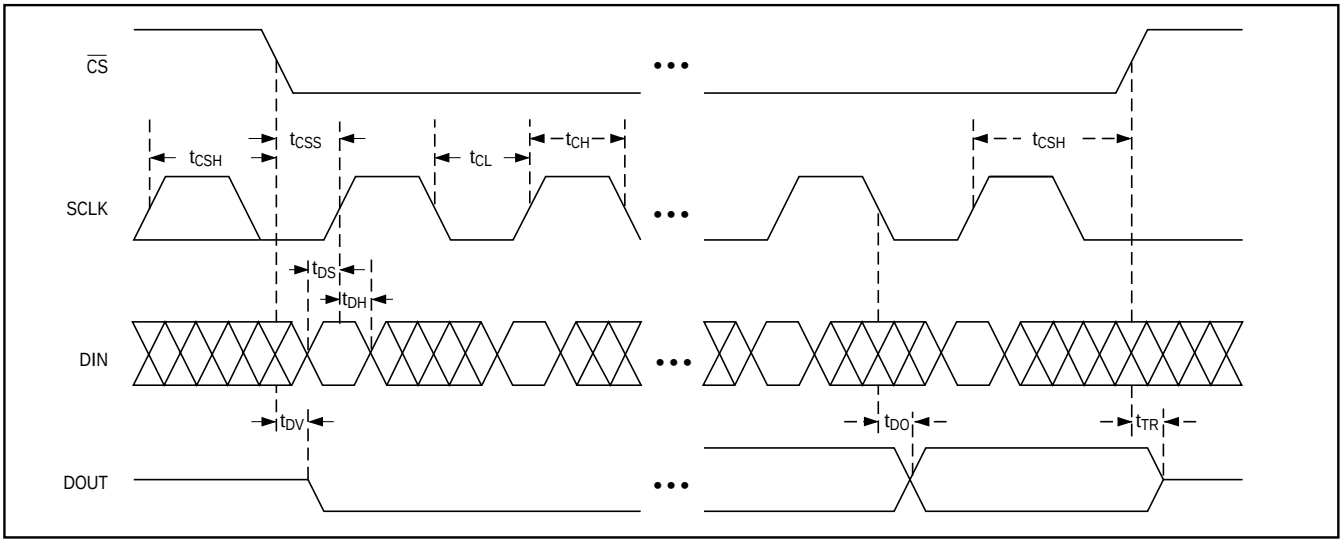


Figure 7. Detailed Serial-Interface Timing

Internal and External Clock Modes

The MAX186/MAX188 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX186/MAX188. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7 through 10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (see Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or else droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the clock period exceeds 10µs, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

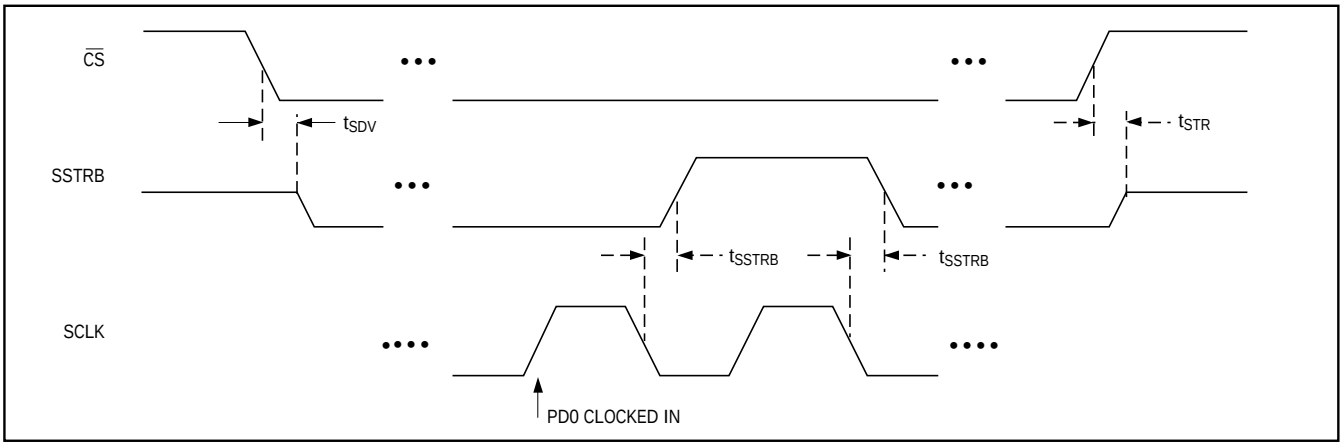


Figure 8. External Clock Mode SSTRB Detailed Timing

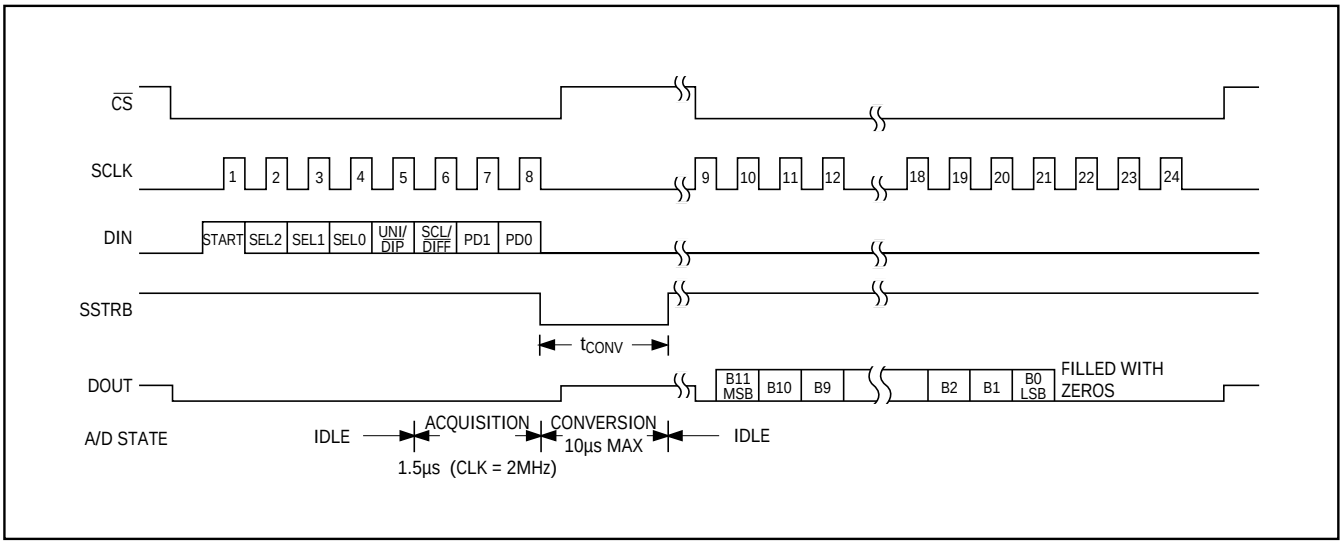


Figure 9. Internal Clock Mode Timing

Internal Clock

In internal clock mode, the MAX186/MAX188 generate their own conversion clock internally. This frees the microprocessor from the burden of running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to typically 10MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 10µs, during which time SCLK should remain low for best noise performance. An internal register stores data when the conversion is in progress. SCLK clocks the data out at this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge will produce the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (see Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX186/MAX188 and three-states DOUT, but it does not adversely effect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In internal clock mode, data can be shifted in and out of the MAX186/MAX188 at clock rates exceeding 4.0MHz, provided that the minimum acquisition time, t_{AZ}, is kept above 1.5µs.

Low-Power, 8-Channel, Serial 12-Bit ADCs

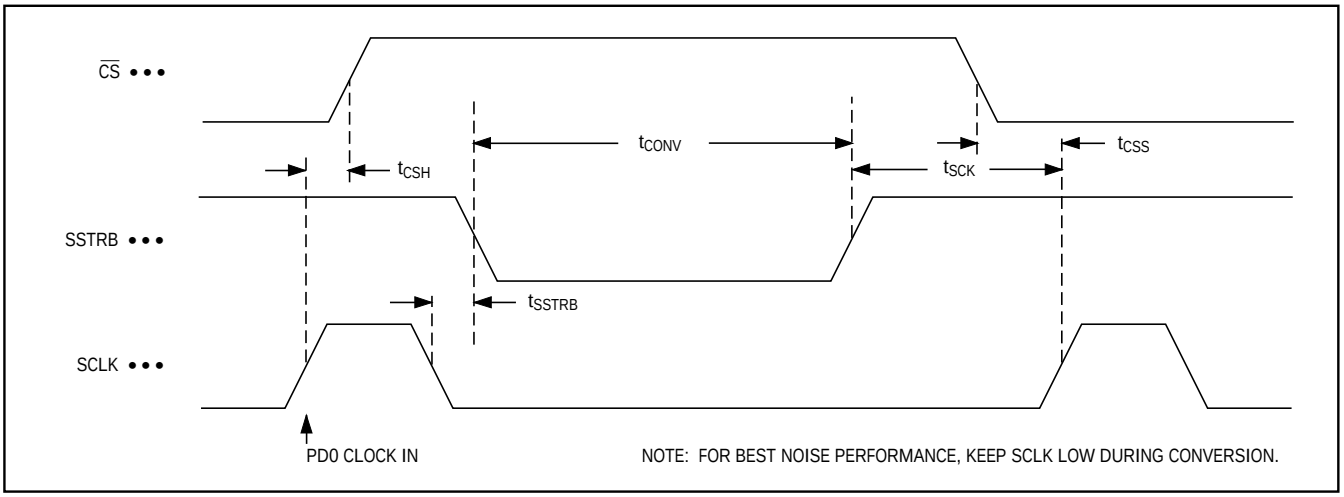


Figure 10. Internal Clock Mode SSTRB Detailed Timing

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX186/MAX188. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle, e.g. after V_{CC} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If a falling edge on $\overline{CS}$ forces a start bit before bit 5 (B5) becomes available, then the current conversion will be terminated and a new one started. Thus, the fastest the MAX186/MAX188 can run is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX186/MAX188. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry will activate the MAX186/MAX188 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have been stabilized, the internal reset time is 100µs and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT will shift out zeros.

Reference-Buffer Compensation

In addition to its shutdown function, the $\overline{SHDN}$ pin also selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. Compensated or not, the minimum clock rate is 100kHz due to droop on the sample-and-hold.

To select external compensation, float $\overline{SHDN}$. See the *Typical Operating Circuit*, which uses a 4.7µF capacitor at VREF. A value of 4.7µF or greater ensures stability and allows operation of the converter at the full clock speed of 2MHz. External compensation increases power-up time (see the *Choosing Power-Down Mode* section, and Table 5).

Internal compensation requires no external capacitor at VREF, and is selected by pulling $\overline{SHDN}$ high. Internal compensation allows for shortest power-up times, but is only available using an external clock and reduces the maximum clock rate to 400kHz.

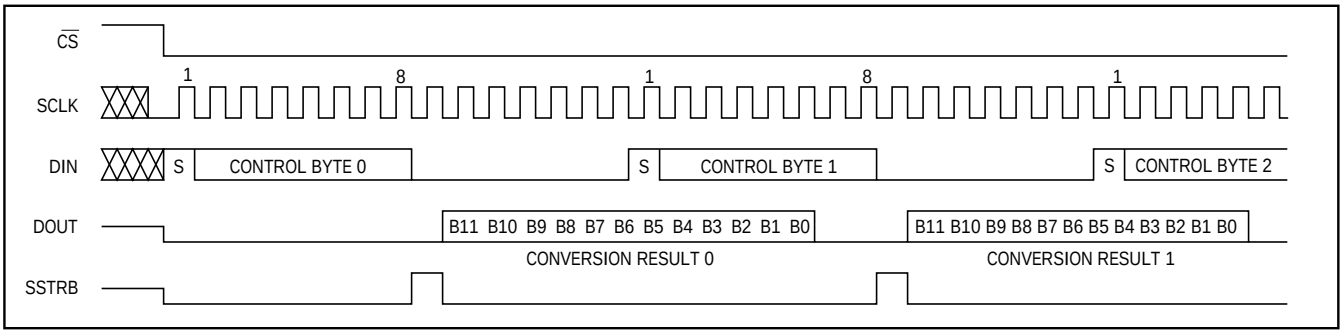


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

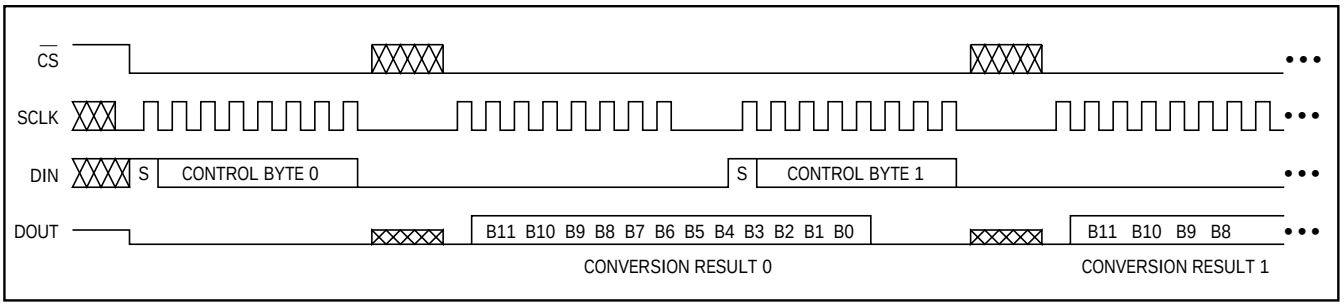


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

Power-Down

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 7 and 8 of the DIN control byte with $\overline{SHDN}$ high or floating (see Tables 2 and 6). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 7 and 8 of DIN word (see Table 7).

Full power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} and I_{SS} typically to 2µA.

Fast power-down mode turns off all circuitry except the bandgap reference. With the fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

In both software shutdown modes, the serial interface remains operational, however, the ADC will not convert. Table 5 illustrates how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate.

In external compensation mode, the power-up time is 20ms with a 4.7µF compensation capacitor (200ms with a 33µF capacitor) when the capacitor is fully discharged. In fast power-down, you can eliminate start-up time by using low-leakage capacitors that will not discharge more than 1/2LSB while shut down. In shutdown, the capacitor has to supply the current into the reference (1.5µA typ) and the transient currents at power-up.

Figures 12a and 12b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC will continue to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out while the MAX186/MAX188 have already entered a software power-down.

The first logical 1 on DIN will be interpreted as a start bit, and powers up the MAX186/MAX188. Following the start bit, the data input word or control byte also determines clock and power-down modes. For example, if the DIN word contains PD1 = 1, then the chip will remain powered up. If PD1 = 0, a power-down will resume after one conversion.

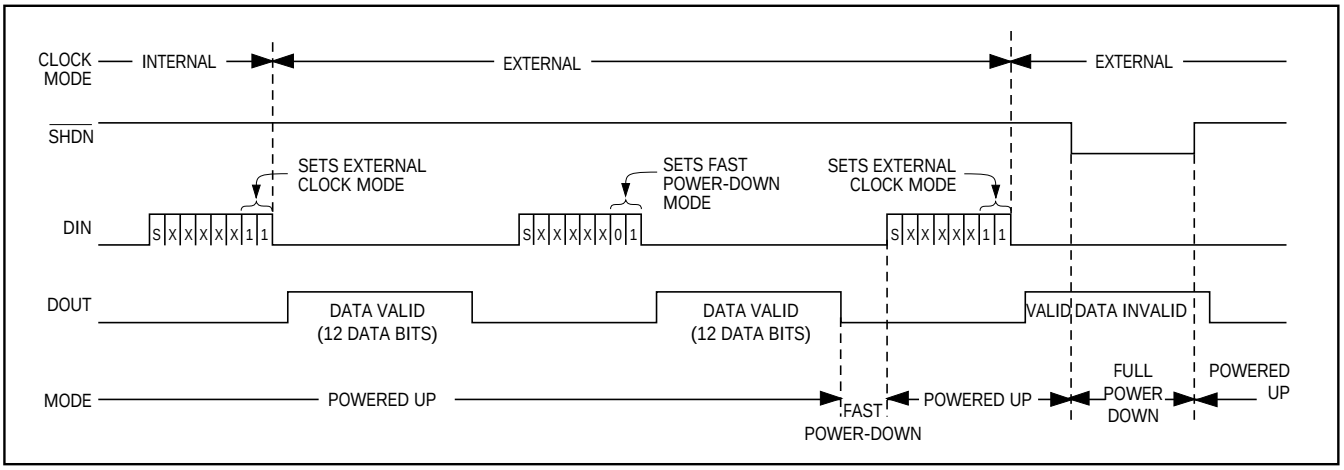


Figure 12a. Timing Diagram Power-Down Modes, External Clock

Table 5. Typical Power-Up Delay Times

Reference Buffer	Reference-Buffer Compensation Mode	VREF Capacitor (µF)	Power-Down Mode	Power-Up Delay (sec)	Maximum Sampling Rate (ksps)
Enabled	Internal		Fast	5µ	26
Enabled	Internal		Full	300µ	26
Enabled	External	4.7	Fast	See Figure 14c	133
Enabled	External	4.7	Full	See Figure 14c	133
Disabled			Fast	2µ	133
Disabled			Full	2µ	133

Table 6. Software Shutdown and Clock Mode

PD1	PD0	Device Mode
1	1	External Clock Mode
1	0	Internal Clock Mode
0	1	Fast Power-Down Mode
0	0	Full Power-Down Mode

Table 7. Hard-Wired Shutdown and Compensation Mode

$\overline{SHDN}$ State	Device Mode	Reference-Buffer Compensation
1	Enabled	Internal Compensation
Floating	Enabled	External Compensation
0	Full Power-Down	N/A

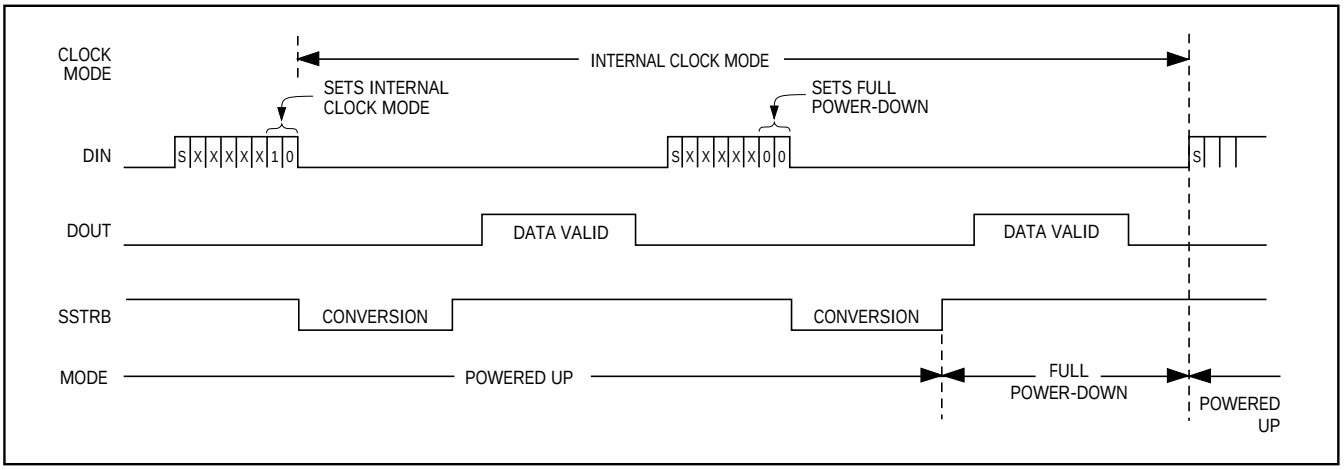


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Hardware Power-Down

The $\overline{SHDN}$ pin places the converter into the full power-down mode. Unlike with the software shut-down modes, conversion is not completed. It stops coincidentally with $\overline{SHDN}$ being brought low. There is no power-up delay if an external reference is used and is not shut down. The $\overline{SHDN}$ pin also selects internal or external reference compensation (see Table 7).

Power-Down Sequencing

The MAX186/MAX188 auto power-down modes can save considerable power when operating at less than maximum sample rates. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples illustrate two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 14a depicts the MAX186 power consumption for one or eight channel conversions utilizing full power-down mode and internal reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.2ms time constant. To achieve full 12-bit accuracy, 10 time constants or 2ms are required after power-up. Waiting 2ms in FASTPD mode instead of full power-up will reduce the power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 13.

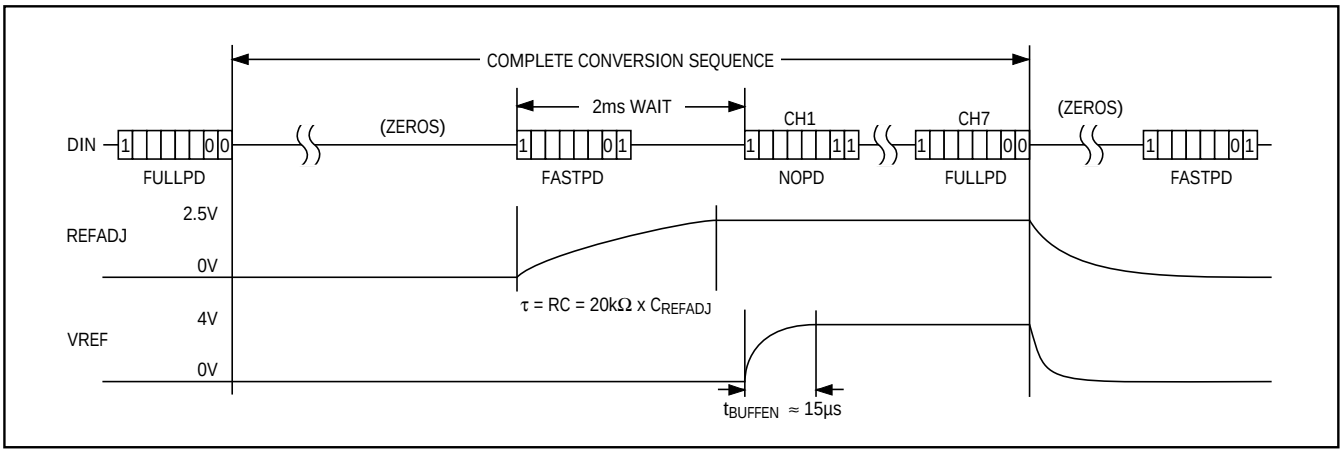


Figure 13. MAX186 FULLPD/FASTPD Power-Up Sequence

Low-Power, 8-Channel, Serial 12-Bit ADCs

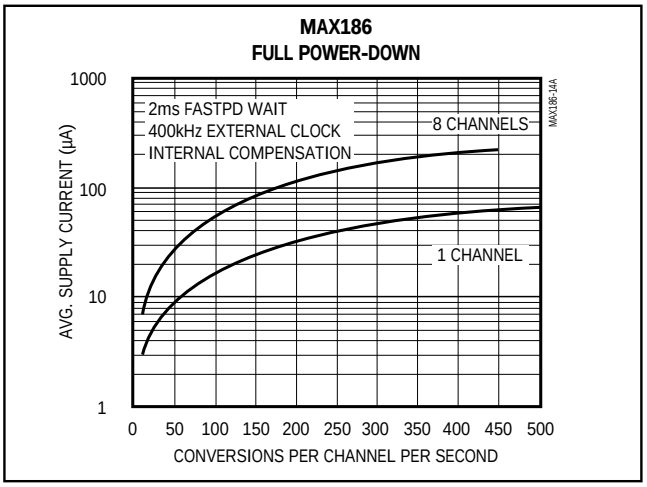


Figure 14a. MAX186 Supply Current vs. Sample Rate/Second, FULLPD, 400kHz Clock

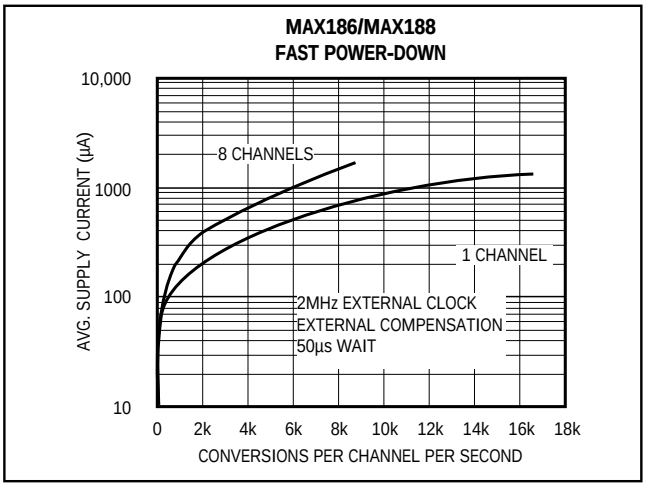


Figure 14b. MAX186/MAX188 Supply Current vs. Sample Rate/Second, FASTPD, 2MHz Clock

Lowest Power at Higher Throughputs

Figure 14b shows the power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7µF compensation requires a 50µs wait after power-up, accomplished by 75 idle clocks after a dummy conversion. This circuit combines fast multi-channel conversion with lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX186/MAX188 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

External and Internal References

The MAX186 can be used with an internal or external reference, whereas an external reference is required for the MAX188. Diode D1 shown in the *Typical Operating Circuit* ensures correct start-up. Any standard signal diode can be used. For both parts, an external reference can either be connected directly at the VREF terminal or at the REFADJ pin.

An internal buffer is designed to provide 4.096V at VREF for both the MAX186 and MAX188. The MAX186's internally trimmed 2.46V reference is buffered with a gain of 1.678. The MAX188's buffer is trimmed with a buffer gain of 1.638 to scale an external 2.5V reference at REFADJ to 4.096V at VREF.

MAX186 Internal Reference

The full-scale range of the MAX186 with internal reference is 4.096V with unipolar inputs, and ±2.048V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the Reference-Adjust Circuit of Figure 17.

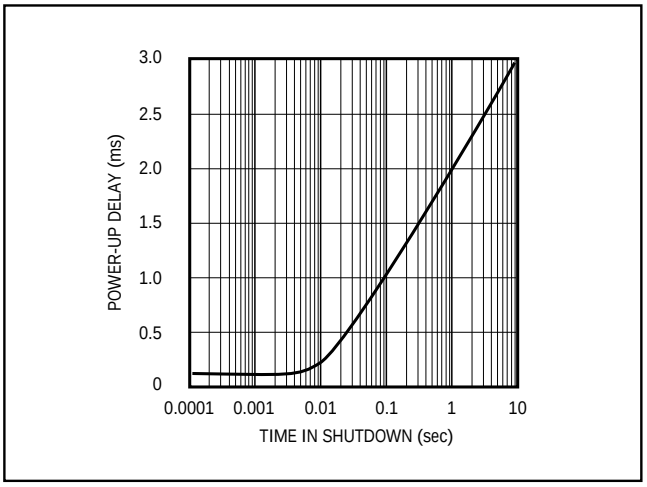


Figure 14c. Typical Power-Up Delay vs. Time in Shutdown

External Reference

With both the MAX186 and MAX188, an external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX186 and higher than 100kΩ for the MAX188, where the internal reference is omitted. At VREF, the input impedance is a minimum of 12kΩ for DC currents. During conversion, an external reference at VREF must be able to deliver up to 350µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7µF capacitor.

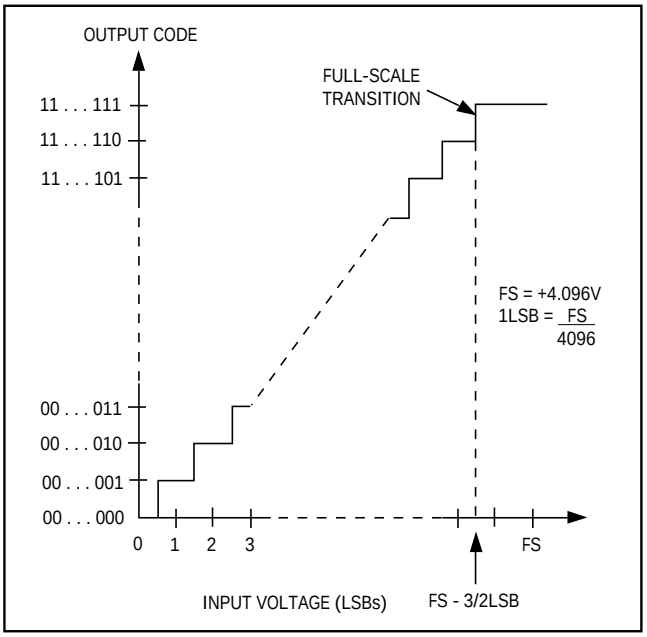


Figure 15. MAX186/MAX188 Unipolar Transfer Function, 4.096V = Full Scale

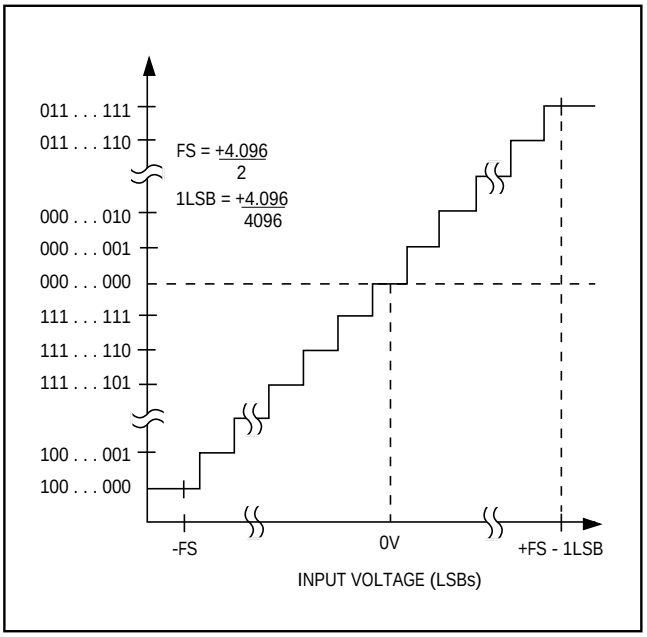


Figure 16. MAX186/MAX188 Bipolar Transfer Function, ±4.096V/2 = Full Scale

Using the buffered REFADJ input avoids external buffering of the reference. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{DD}.

Transfer Function and Gain Adjust

Figure 15 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 16 shows the bipolar input/output transfer function. Code transitions occur halfway between successive integer LSB values. Output coding is binary with 1 LSB = 1.00mV (4.096V/4096) for unipolar operation and 1 LSB = 1.00mV ((4.096V/2 - -4.096V/2)/4096) for bipolar operation.

Figure 17, the MAX186 Reference-Adjust Circuit, shows how to adjust the ADC gain in applications that use the internal reference. The circuit provides ±1.5% (±65LSBs) of gain adjustment range.

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. All other analog grounds

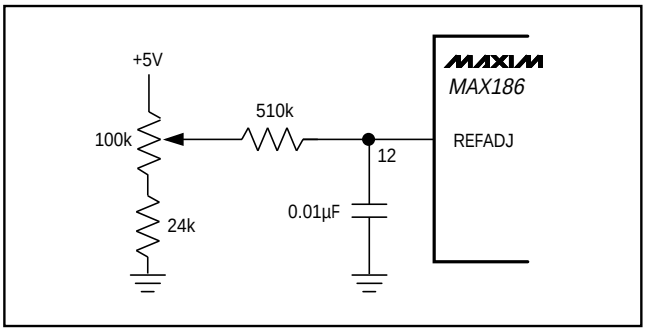


Figure 17. MAX186 Reference-Adjust Circuit

and DGND should be connected to this ground. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors close to the MAX186/MAX188. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a low-pass filter, as shown in Figure 18.

Low-Power, 8-Channel, Serial 12-Bit ADCs

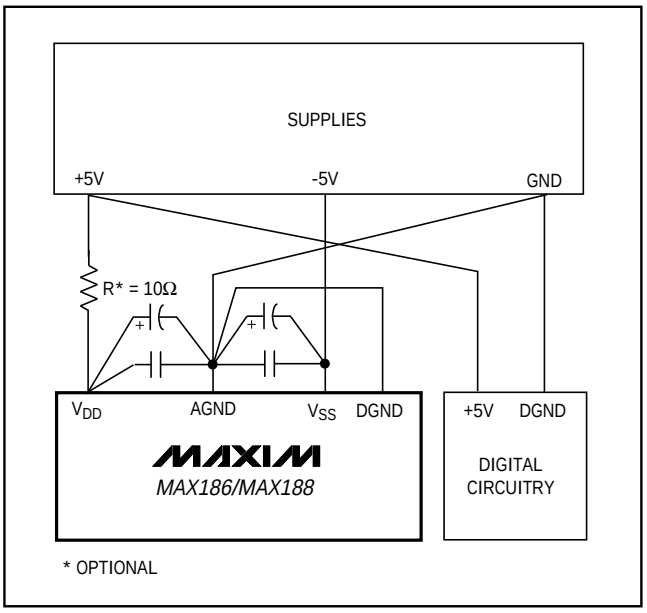


Figure 18. Power-Supply Grounding Connection

High-Speed Digital Interfacing with QSPI

The MAX186/MAX188 can interface with QSPI at high throughput rates using the circuit in Figure 19. This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU since QSPI incorporates its own micro-sequencer. Figure 19 depicts the MAX186, but the same circuit could be used with the MAX188 by adding an external reference to VREF and connecting REFADJ to V_{DD}.

Figure 20 details the code that sets up QSPI for autonomous operation. In external clock mode, the MAX186/MAX188 perform a single-ended, unipolar conversion on each of their eight analog input channels. Figure 21, QSPI Assembly-Code Timing, shows the timing associated with the assembly code of Figure 20. The first byte clocked into the MAX186/MAX188 is the control byte, which triggers the first conversion on CH0. The last two bytes clocked into the MAX186/MAX188 are all zero and clock out the results of the CH7 conversion.

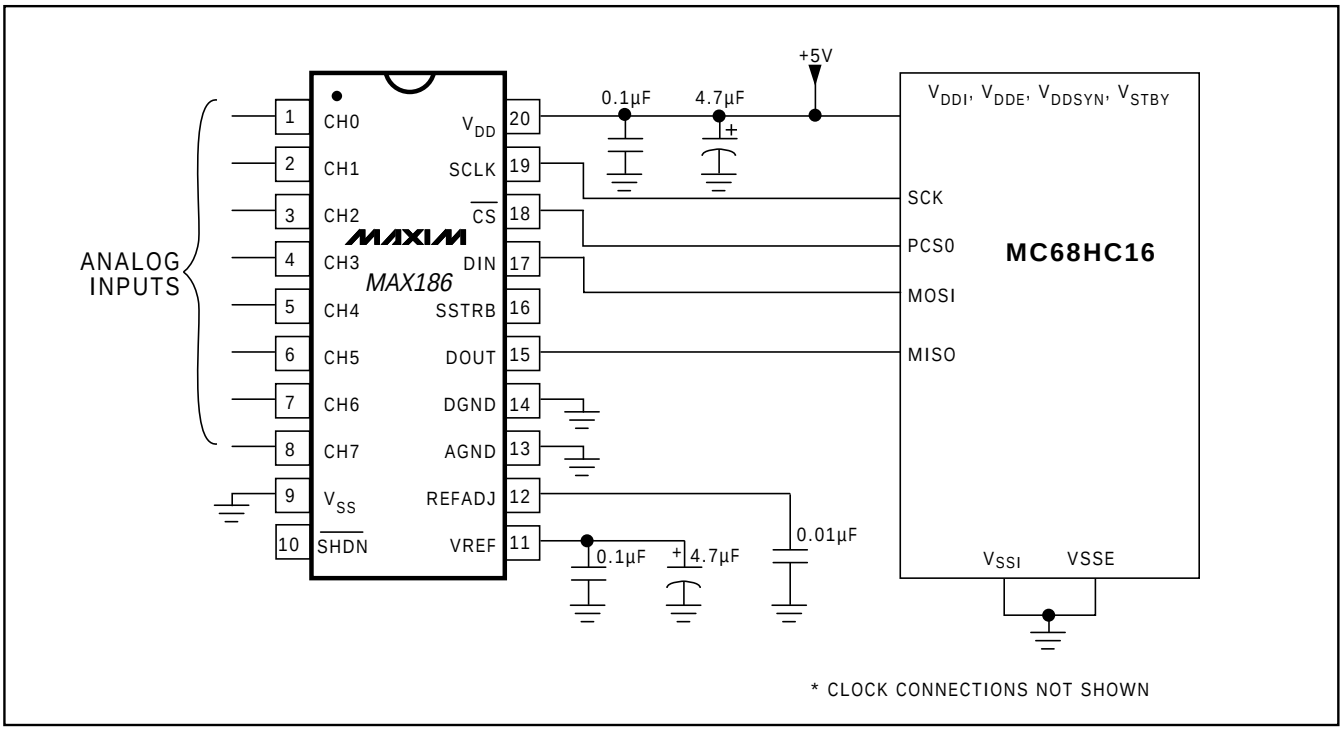


Figure 19. MAX186 QSPI Connection

```
*Title : MAX186.ASM
* Description :
*             This is a shell program for using a stand-alone 68HC16 without any external memory. The internal 1K RAM
*             is put into bank $0F to maintain 68HC11 code compatibility. This program was written with software
*             provided in the Motorola 68HC16 Evaluation Kit.
*
*  Roger J.A. Chen, Applications Engineer
*  MAXIM Integrated Products
*  November 20, 1992
*
*****************************************************************************************************************************************************************
      INCLUDE      'EQUATES.ASM'   ;Equates for common reg addrs
      INCLUDE      'ORG00000.ASM'  ;initialize reset vector
      INCLUDE      'ORG00008.ASM'  ;initialize interrupt vectors
      ORG    $0200                 ;start program after interrupt vectors
      INCLUDE  'INITSYS.ASM'       ;set EK=F,XK=0,YK=0,ZK=0
                                   ;set sys clock at 16.78 MHz, COP off
      INCLUDE  'INITRAM.ASM'       ;turn on internal SRAM at $10000
                                   ;set stack (SK=1, SP=03FE)
MAIN:
      JSR    INITQSPI
MAINLOOP:
      JSR    READ186
WAIT:
      LDAA   SPSR
      ANDA   #$80
      BEQ    WAIT                  ;wait for QSPI to finish
      BRA MAINLOOP
ENDPROGRAM:

INITQSPI:

;This routine sets up the QSPI microsequencer to operate on its own.
;The sequencer will read all eight channels of a MAX186/MAX188 each time
;it is triggered. The A/D converter results will be left in the
;receive data RAM. Each 16 bit receive data RAM location will
;have a leading zero, 12 bits of conversion result and three zeros.
;
;Receive RAM Bits 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
;A/D Result           0   MSB                                LSB 0   0   0
*****  Initialize the QSPI Registers   ******
      PSHA
      PSHB
      LDAA   #%01111000
      STAA   QPDR              ;idle state for PCS0-3 = high
      LDAA   #%01111011
      STAA   QPAR              ;assign port D to be QSPI
      LDAA   #%01111110
      STAA   QDDR              ;only MISO is an input
      LDD    #$8008
      STD    SPCR0             ;master mode,16 bits/transfer,
                               ;CPOL=CPHA=0,1MHz Ser Clock
      LDD    #$0000
      STD    SPCR1             ;set delay between PCS0 and SCK,
```

Figure 20. MAX186/MAX188 Assembly-Code Listing

```
                                ;set delay between transfers
      LDD    #$0800
      STD    SPCR2              ;set ENDQP to $8 for 9 transfers
*****  Initialize QSPI Command RAM  *****

      LDAA   #$80          ;CONT=1,BITSE=0,DT=0,DSCK=0,PCS0=ACTIVE
      STAA   $FD40          ;store first byte in COMMAND RAM
      LDAA   #$C0          ;CONT=1,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
      STAA   $FD41
      STAA   $FD42
      STAA   $FD43
      STAA   $FD44
      STAA   $FD45
      STAA   $FD46
      STAA   $FD47
      LDAA   #$40          ;CONT=0,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
      STAA   $FD48
*****  Initialize QSPI Transmit RAM *****

      LDD    #$008F
                                STD    $FD20
      LDD    #$00CF
                                STD    $FD22
      LDD    #$009F
                                STD    $FD24
      LDD    #$00DF
                                STD    $FD26
      LDD    #$00AF
                                STD    $FD28
      LDD    #$00EF
                                STD    $FD2A
      LDD    #$00BF
                                STD    $FD2C
      LDD    #$00FF
                                STD    $FD2E
      LDD    #$0000
                                STD    $FD30
      PULB
      PULA
      RTS

READ186:
;This routine triggers the QSPI microsequencer to autonomously
;trigger conversions on all 8 channels of the MAX186. Each
;conversion result is stored in the receive data RAM.
      PSHA
      LDAA   #$80
      ORAA   SPCR1
      STAA   SPCR1          ;just set SPE
      PULA
      RTS

*****  Interrupts/Exceptions  *****

BDM: BGND               ;exception vectors point here
```

Figure 20. MAX186/MAX188 Assembly-Code Listing (continued)

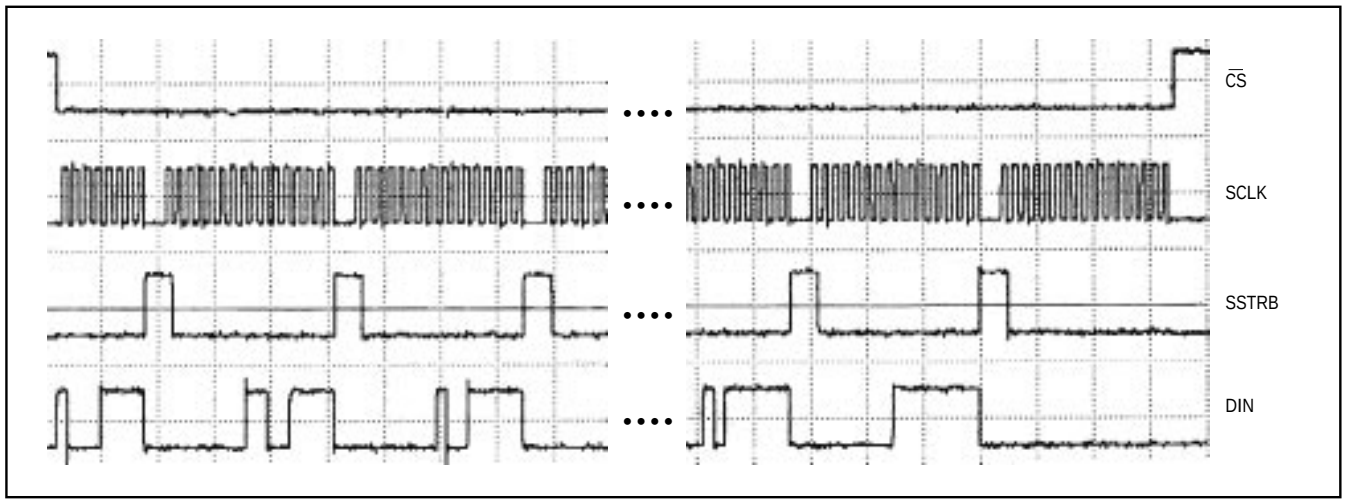


Figure 21. QSPI Assembly-Code Timing

TMS320C3x to MAX186 Interface

Figure 22 shows an application circuit to interface the MAX186/MAX188 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 23.

Use the following steps to initiate a conversion in the MAX186/MAX188 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR of the TMS320 are tied together with the SCLK input of the MAX186/MAX188.
2) The MAX186/MAX188 $\overline{CS}$ is driven low by the XF_ I/O port of the TMS320 to enable data to be clocked into DIN of the MAX186/MAX188.
3) An 8-bit word (1XXXXX11) should be written to the MAX186/MAX188 to initiate a conversion and place the device into external clock mode. Refer to Table 2 to select the proper XXXXX bit values for your specific application.
4) The SSTRB output of the MAX186/MAX188 is monitored via the FSR input of the TMS320. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX186/MAX188.

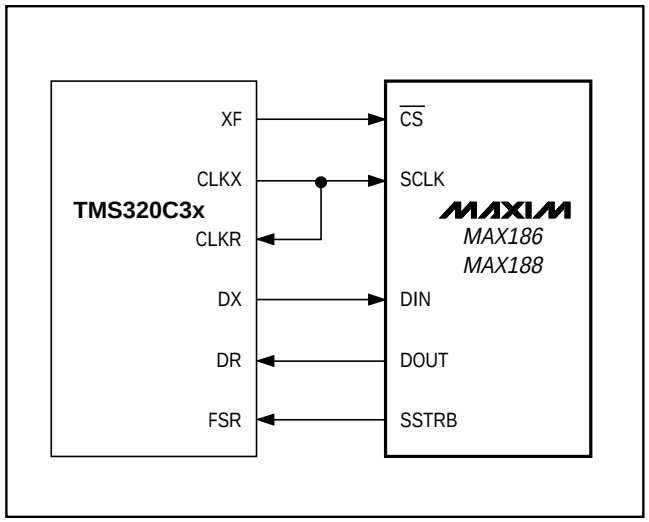


Figure 22. MAX186/MAX188 to TMS320 Serial Interface

5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX186/MAX188 until the next conversion is initiated.

Low-Power, 8-Channel, Serial 12-Bit ADCs

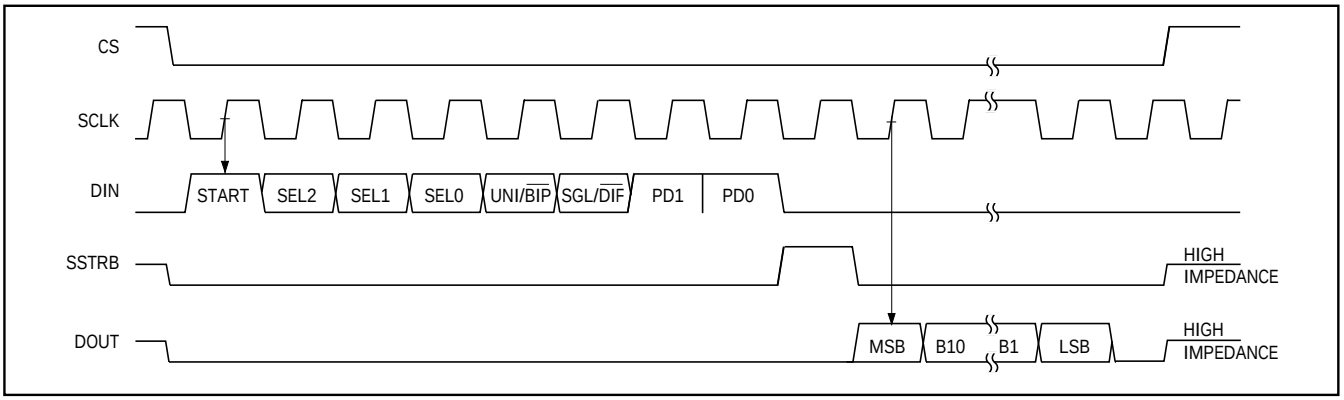
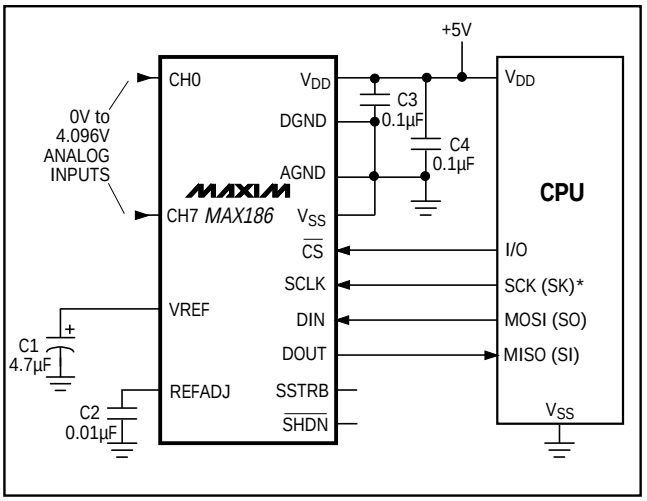
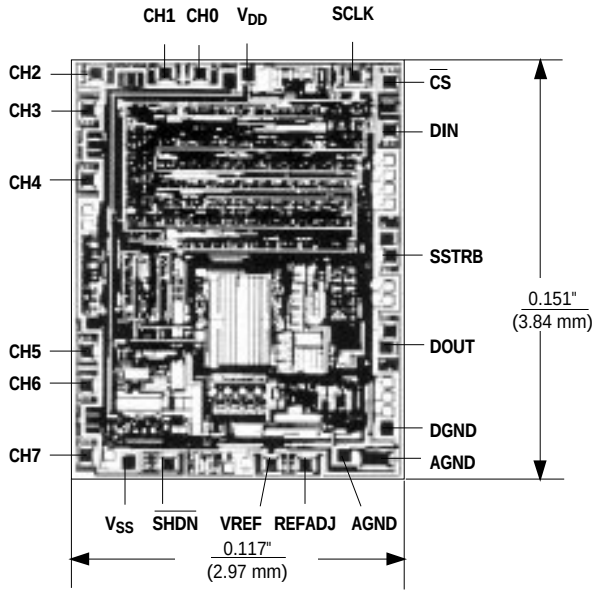


Figure 23. TMS320 Serial Interface Timing Diagram

Typical Operating Circuit



Chip Topography



MAX186/MAX188

TRANSISTOR COUNT: 2278;
SUBSTRATE CONNECTED TO V_{DD}

Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE
MAX188_CPP	0°C to +70°C	20 Plastic DIP
MAX188_CWP	0°C to +70°C	20 SO
MAX188_CAP	0°C to +70°C	20 SSOP
MAX188DC/D	0°C to +70°C	Dice*
MAX188_EPP	-40°C to +85°C	Plastic DIP
MAX188_EWP	-40°C to +85°C	20 SO
MAX188_EAP	-40°C to +85°C	20 SSOP
MAX188_MJP	-55°C to +125°C	20 CERDIP**

PART	TEMP. RANGE	BOARD TYPE
MAX186EVKIT-DIP	0°C to +70°C	Through-Hole

† NOTE: Parts are offered in grades A, B, C and D (grades defined in Electrical Characteristics). When ordering, please specify grade.
** Dice are specified at +25°C, DC parameters only.*
*** Contact factory for availability and processing to MIL-STD-883.*

11 APPENDIX I

SAT-V41 Mechanical Drawing

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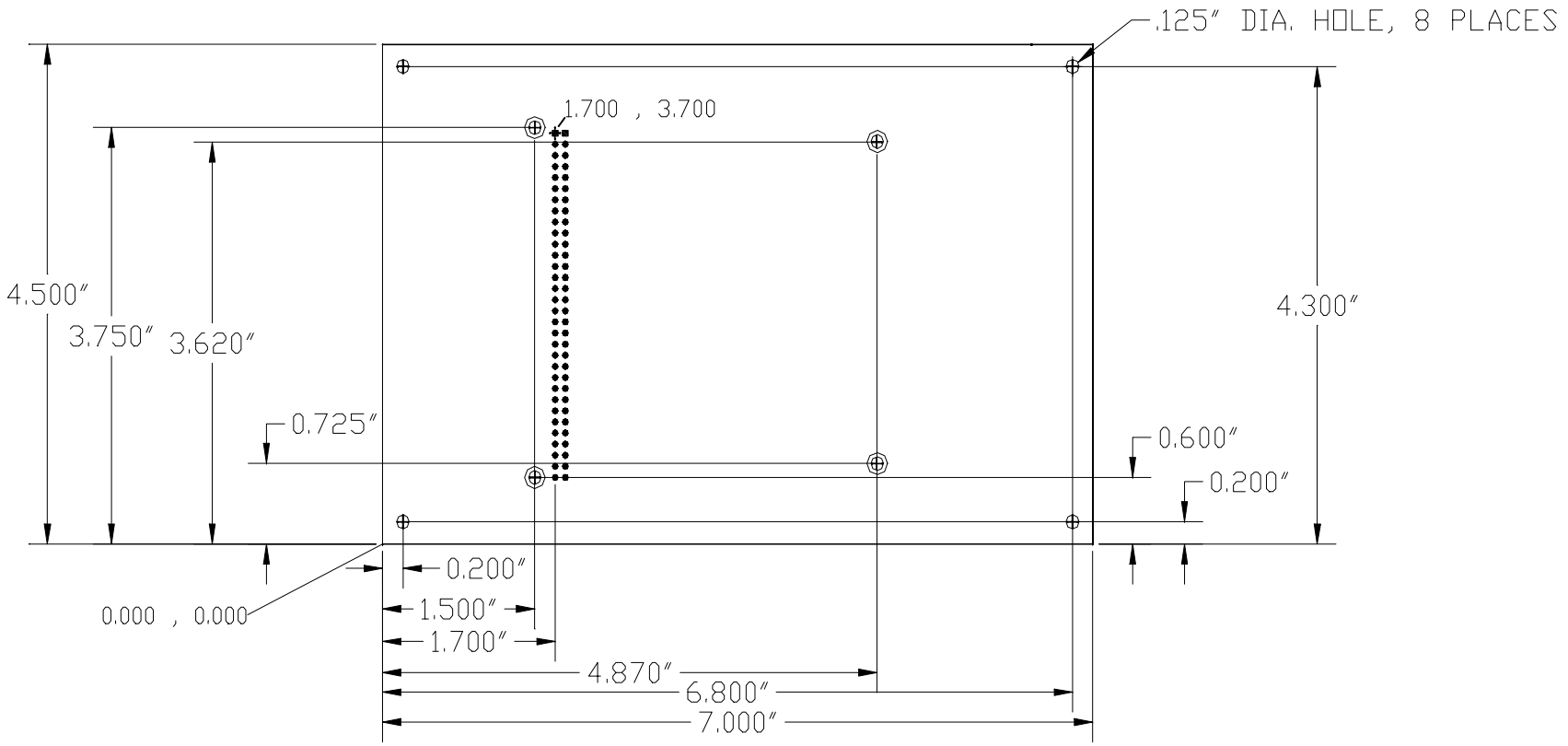
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A			



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE FRACTIONS ANGLES +/- 1/2" DECIMALS: .XX ± .03 .XXX ± .005	DRAFT/DESIGN M.BROWNING	DATE 4/24/95	*WinSystems, Inc.* "THE EMBEDDED SYSTEMS AUTHORITY"
	CHECKER	DATE	SAT-V40/V41 MOUNTING HOLES
MACHINE FINISH: √	APPROVAL	DATE	SIZE B / CAGE CODE 1AU87 / DWG NO. / REV A
	CUSTOMER APPROVAL	DATE	SCALE / CAD ID: SATV40.DWG / SHEET

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12 APPENDIX J

SAT-V41 Schematic Diagrams

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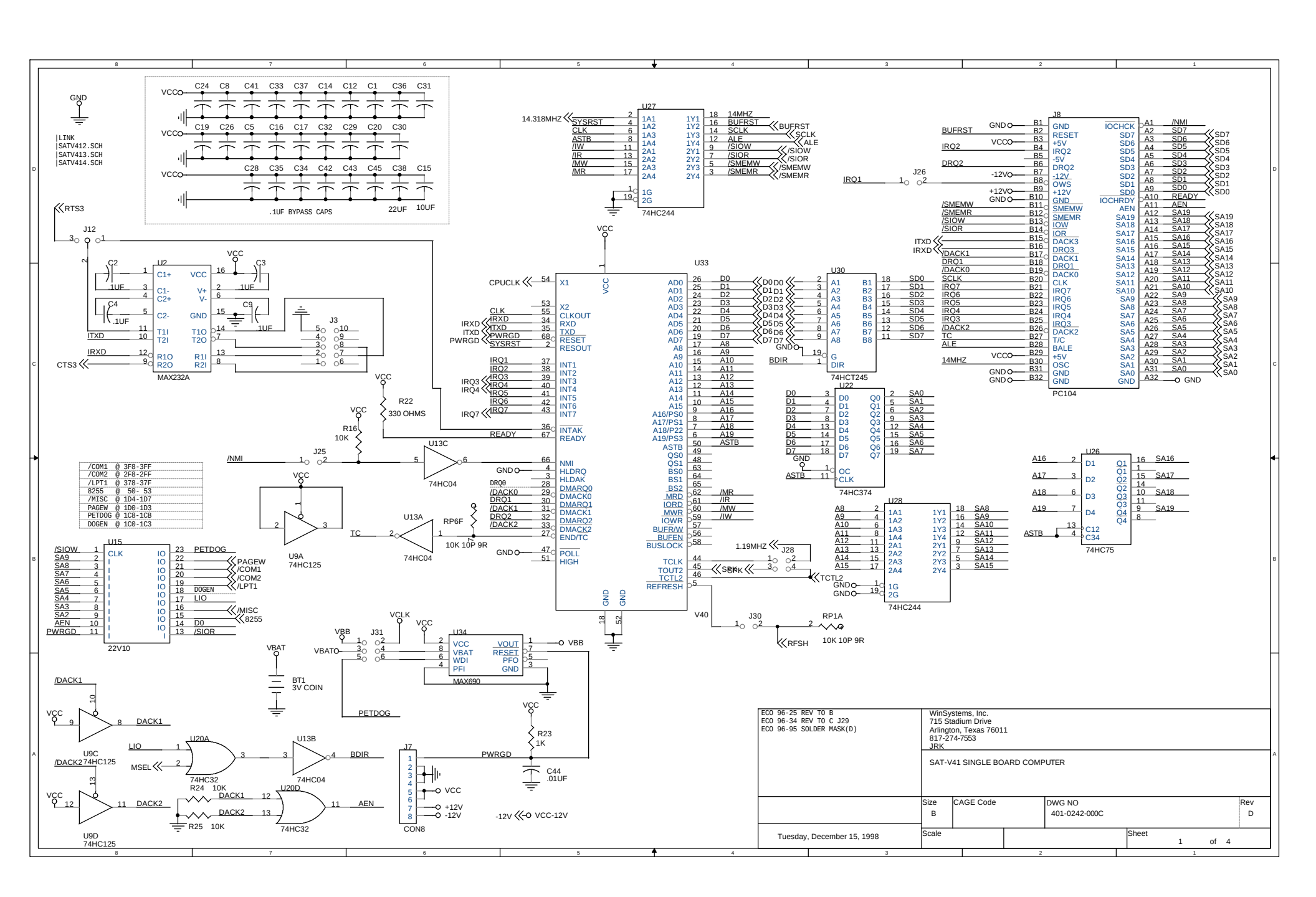
|LINK
|SATV412.SCH
|SATV413.SCH
|SATV414.SCH
.1UF BYPASS CAPS
22UF
10UF
MAX232A
74HC244
74HCT245
74HC374
74HC04
74HC125
74HC32
74HC75
PC104
22V10
MAX690
74HC00
CON8
10K 10P 9R
330 OHMS
1.19MHZ
14.318MHZ
3V COIN
ECO 96-25 REV TO B
ECO 96-34 REV TO C J29
ECO 96-95 SOLDER MASK(D)
WinSystems, Inc.
715 Stadium Drive
Arlington, Texas 76011
817-274-7553
JRK
SAT-V41 SINGLE BOARD COMPUTER
Size B
CAGE Code
DWG NO 401-0242-000C
Rev D
Tuesday, December 15, 1998
Scale
Sheet 1 of 4

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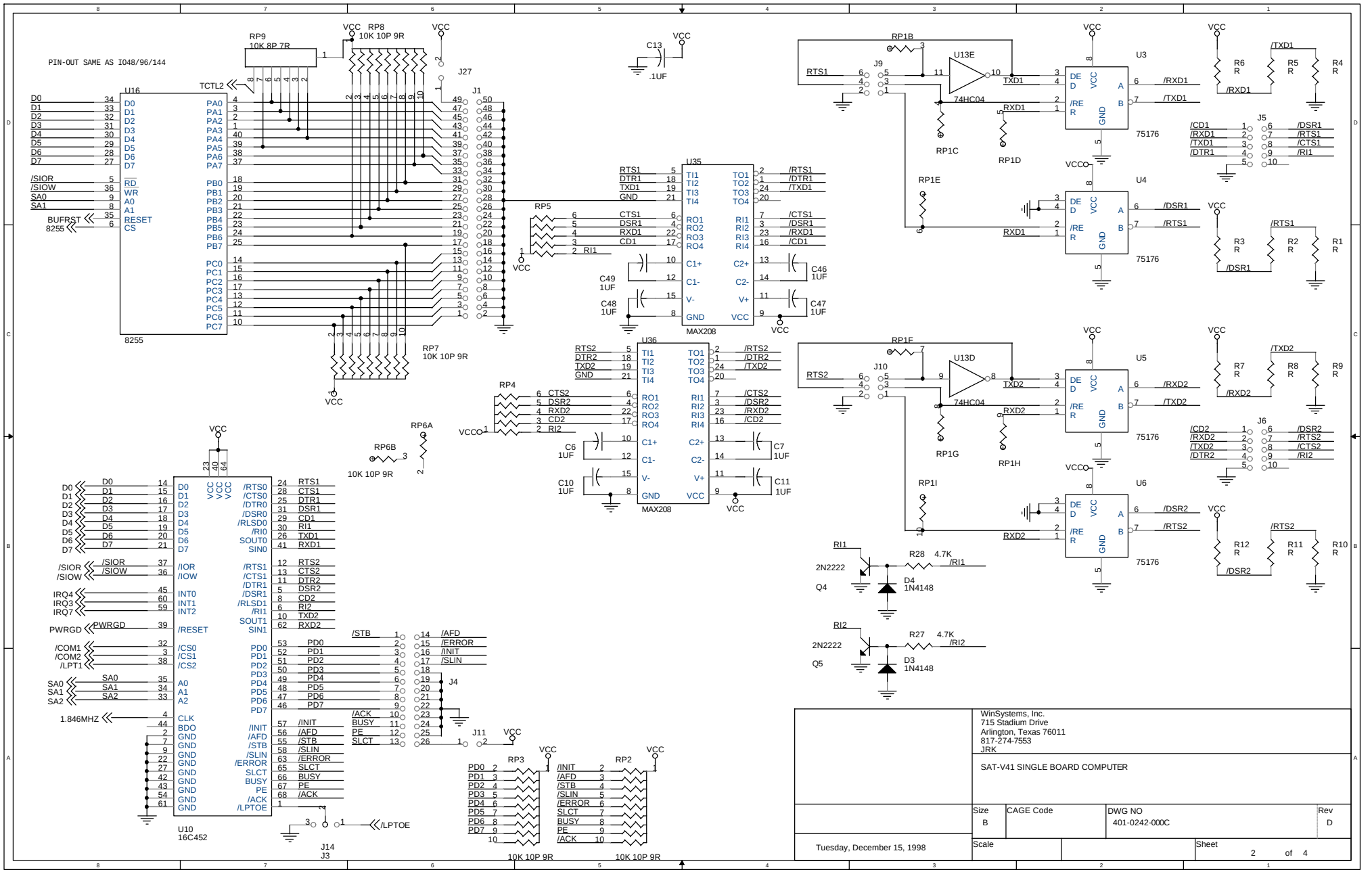
PIN-OUT SAME AS IO48/96/144
RP9
10K 8P 7R
RP8
10K 10P 9R
VCC
C13
.1UF
J27
TCTL2
U16
8255
BUFRST
8255
J1
RP7
10K 10P 9R
RP5
RP4
RP6A
RP6B
10K 10P 9R
U35
MAX208
C46 1UF
C47 1UF
C48 1UF
C49 1UF
U36
MAX208
C6 1UF
C7 1UF
C10 1UF
C11 1UF
RP1B
RP1C
RP1D
RP1E
RP1F
RP1G
RP1H
RP1I
U13E
U13D
74HC04
J9
J10
U3
U4
U5
U6
75176
R6 R
R5 R
R4 R
R3 R
R2 R
R1 R
R7 R
R8 R
R9 R
R12 R
R11 R
R10 R
/TXD1
/RXD1
/DSR1
/RTS1
/TXD2
/RXD2
/DSR2
/RTS2
J5
J6
/CD1
/RXD1
/TXD1
/DTR1
/DSR1
/RTS1
/CTS1
/RI1
/CD2
/RXD2
/TXD2
/DTR2
/DSR2
/RTS2
/CTS2
/RI2
RI1
RI2
2N2222
Q4
Q5
R28 4.7K
R27 4.7K
D4 1N4148
D3 1N4148
U10
16C452
J4
J11
J14
J3
/LPTOE
RP3
RP2
10K 10P 9R
10K 10P 9R
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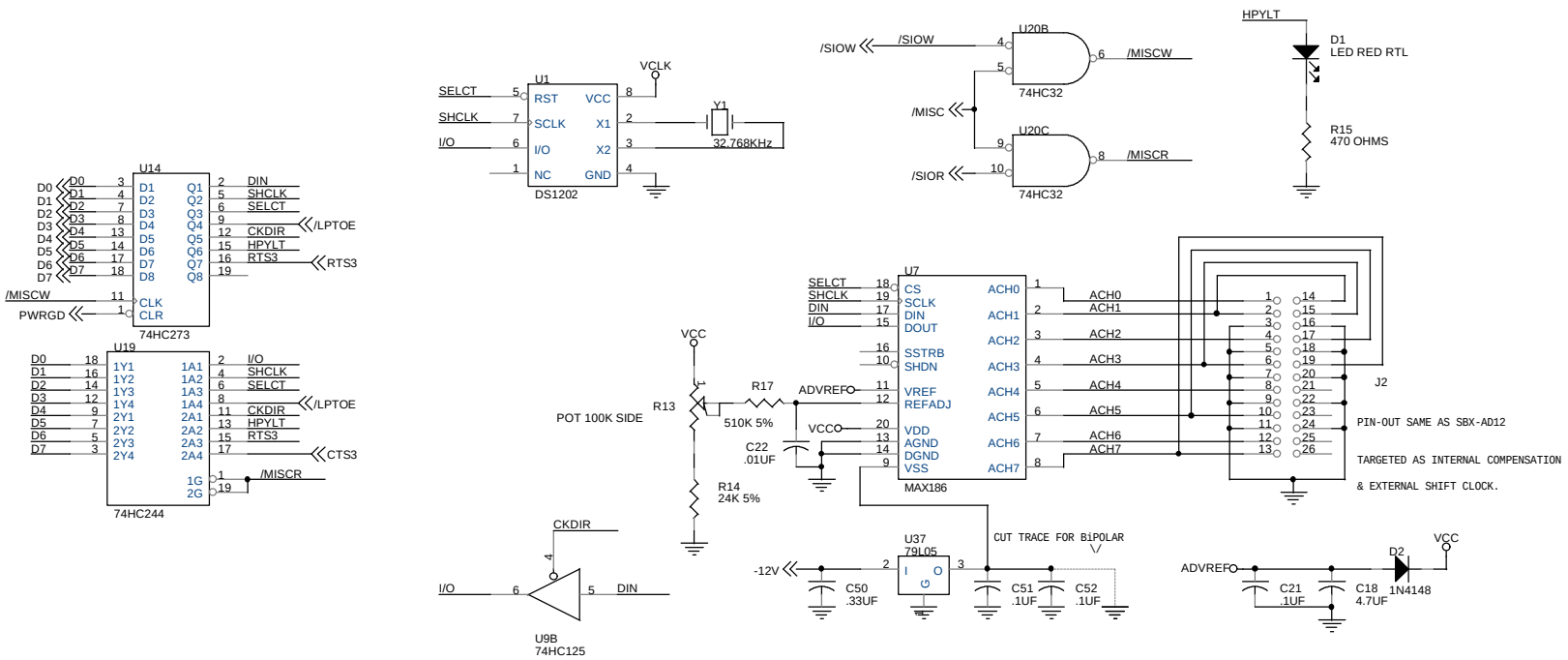

	WinSystems, Inc. 715 Stadium Drive Arlington, Texas 76011 817-274-7553 JRK		
	SAT-V41 SINGLE BOARD COMPUTER		
	Size: B	CAGE Code:	DWG NO: 401-0242-000C
Tuesday, December 15, 1998	Scale:		Sheet: 3 of 4

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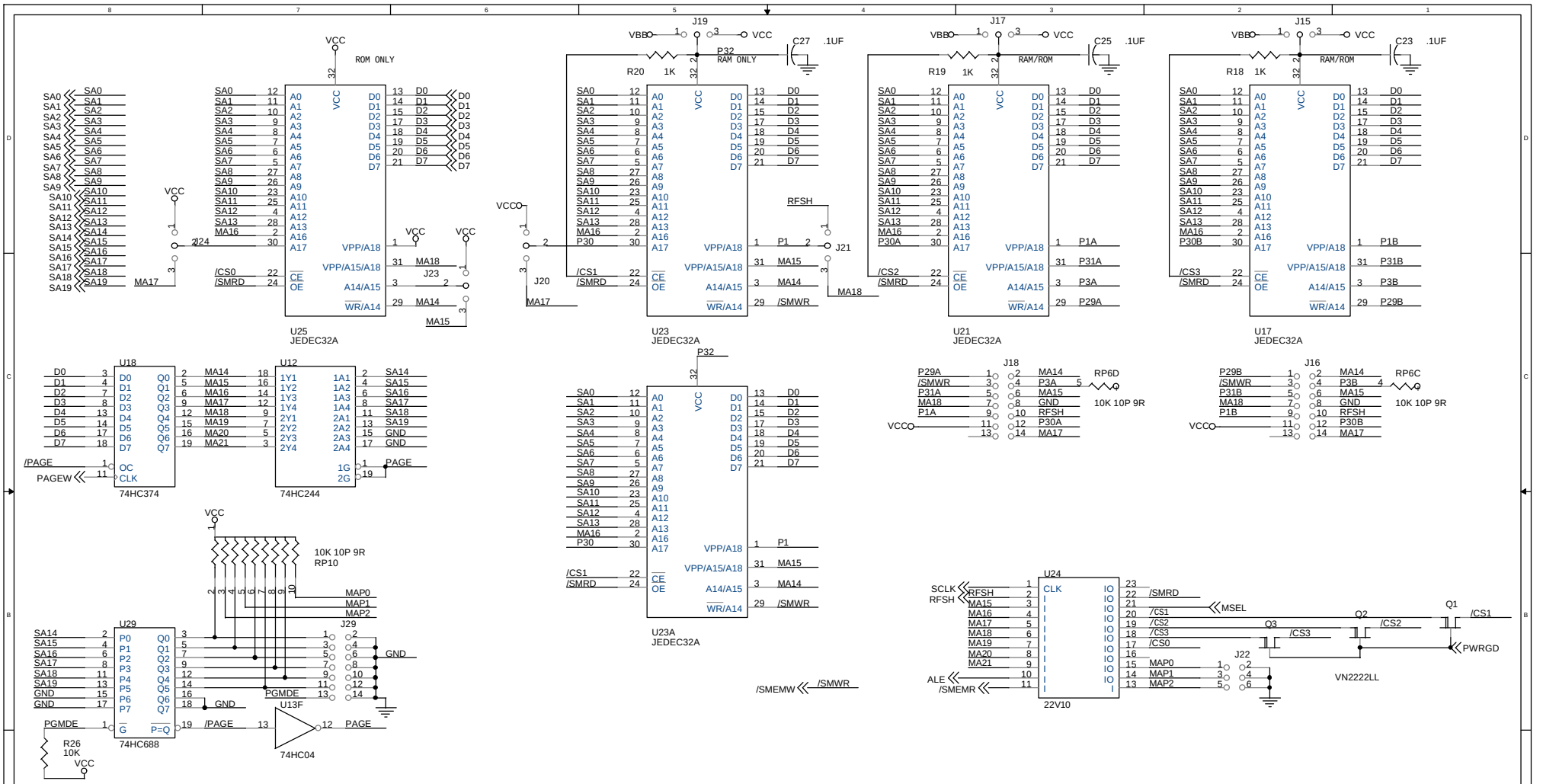

	ROM ONLY	RAM ONLY	RAM/ROM	
32K EPROM	*		*	
64K EPROM	*		*	
128K EPROM	*		*	
256K EPROM	*		*	
512K EPROM	*		*	
32K EEPROM			*	
128K EEPROM			*	
256K EEPROM			*	<--<< DIAGONAL JUMPER
512K EEPROM			*	
32K SRAM		*	*	
128K SRAM		*	*	
256K SRAM		*	*	
512K SRAM		*	*	
128K PSRAM		*	*	
512K PSRAM		*	*	

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SAT-V41 SINGLE BOARD COMPUTER

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Sheet 4 of 4

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