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ATR0630, ATR0635
ANTARIS 4 GPS Single Chips

Data Sheet

PRELIMINARY

Features

- Integrated solution including RF + IF filter + baseband requiring minimum footprint
- ATR0635: SuperSense® Indoor GPS: down to –157 dBm
- 16 channel ANTARIS 4 positioning engine
- Ultra-low power consumption: 62 mW
- Assisted GPS and Autonomous GPS operation, AssistNow™ ready
- Minimum bill of material
- 4 Hz position update rate
- 1 USB and 2 UART ports
- Supports DGPS, WAAS, EGNOS and MSAS
- RoHS Compliant (lead-free)

your position is our focus

Data Sheet

Title	ATR0630, ATR0635
Subtitle	ANTARIS 4 GPS Single Chips
Doc Type	Data Sheet Preliminary
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Revision Index	Date	Name	Status / Comments
P1	02. June 2006	GzB	Basis: ATR0630: 01/06, ATR0635: 02/06
P2	25. July 2006	GzB	Basis: ATR0630: 06/06, ATR0635: 06/06 Modified Table 5.1 (P9, P13, P16, P19, P22, P31), Table 5.2 (AGCOUT, SDI), Section 6, Table 8.4 (No. 1.16, 1.27…1.33), Section 8.5, Section 9

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Data Sheet Revisions	Identification of applicable hardware	Comments
P1, P2	ATR0630N-7KQY, ATR0635-7KQY	Firmware 5.0 in ROM

	Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).
	This is an Electrostatic Sensitive Device (ESD). Observe precautions for handling.

Semiconductor technology provided by ATMEL.

Contents

1 Description

1.1 Overview

The ATR0630 and ATR0635 are low-power, single-chip GPS receivers, especially designed to meet the requirements of mobile applications. They are based on the ultra low power ANTARIS 4 technology and integrate an RF front-end, filtering, and a baseband processor in a single, tiny 7 mm x 10 mm 96 pin BGA package. The baseband processor includes a 16-channel GPS correlator and the ARM7TDMI core, a 32-bit RISC architecture. Following interfaces are provided USB device port, two USARTs and the SPI interface (for optional serial EEPROM).

Both ATR0630 and ATR0635 include a complete ANTARIS 4 GPS firmware running directly from on-chip ROM. The ATR0635 features SuperSense® which provides exceptionally high sensitivity. The firmware performs acquisition, tracking, navigation and position data output. The NMEA protocol, the binary UBX protocol and RTCM for differential GPS are supported. The firmware provides full support of SBAS satellites (WAAS, EGNOS and MSAS) and assisted GPS (A-GPS). For normal PVT (Position / Velocity / Time) applications, there is no need for external Flash- or ROM-memory. The firmware supports the possibility to store the configuration settings in an optional external EEPROM or on-chip battery backed SRAM.

Due to the fully integrated design, just an RF SAW filter, a GPS XTAL (ATR0630) or TCXO (ATR0635) and blocking capacitors are required to realize a stand-alone GPS functionality. The ATR0630 and ATR0635 operate in a complete autonomous mode, utilizing on Automatic Gain Control (AGC) in closed loop operation. For maximum performance, we recommend to use these single chip GPS receivers together with a low noise amplifier (e.g. ATR0610).

1.2 Features

- Integrated solution including RF + IF filter + baseband requiring minimum footprint
- ATR0635: SuperSense® Indoor GPS: down to -157 dBm
- 16 channel ANTARIS 4 positioning engine
- Ultra-low power consumption: 62 mW
- Assisted GPS and Autonomous GPS operation, AssistNow™ ready
- Minimum bill of material
- 4 Hz position update rate
- 1 USB and 2 UART ports
- Supports DGPS, WAAS, EGNOS and MSAS
- Power saving modes
- 5 µA backup current
- SPI Master & Slave (suitable for optional serial EEPROMs)
- Real Time Clock (RTC)
- Supports passive and active antennas
- Antenna short and open circuit detection and protection
- Operating temperature range: –40 to 85°C
- RoHS compliant (lead-free)
- Semiconductor technology provided by ATMEL

1.3 Block Diagram

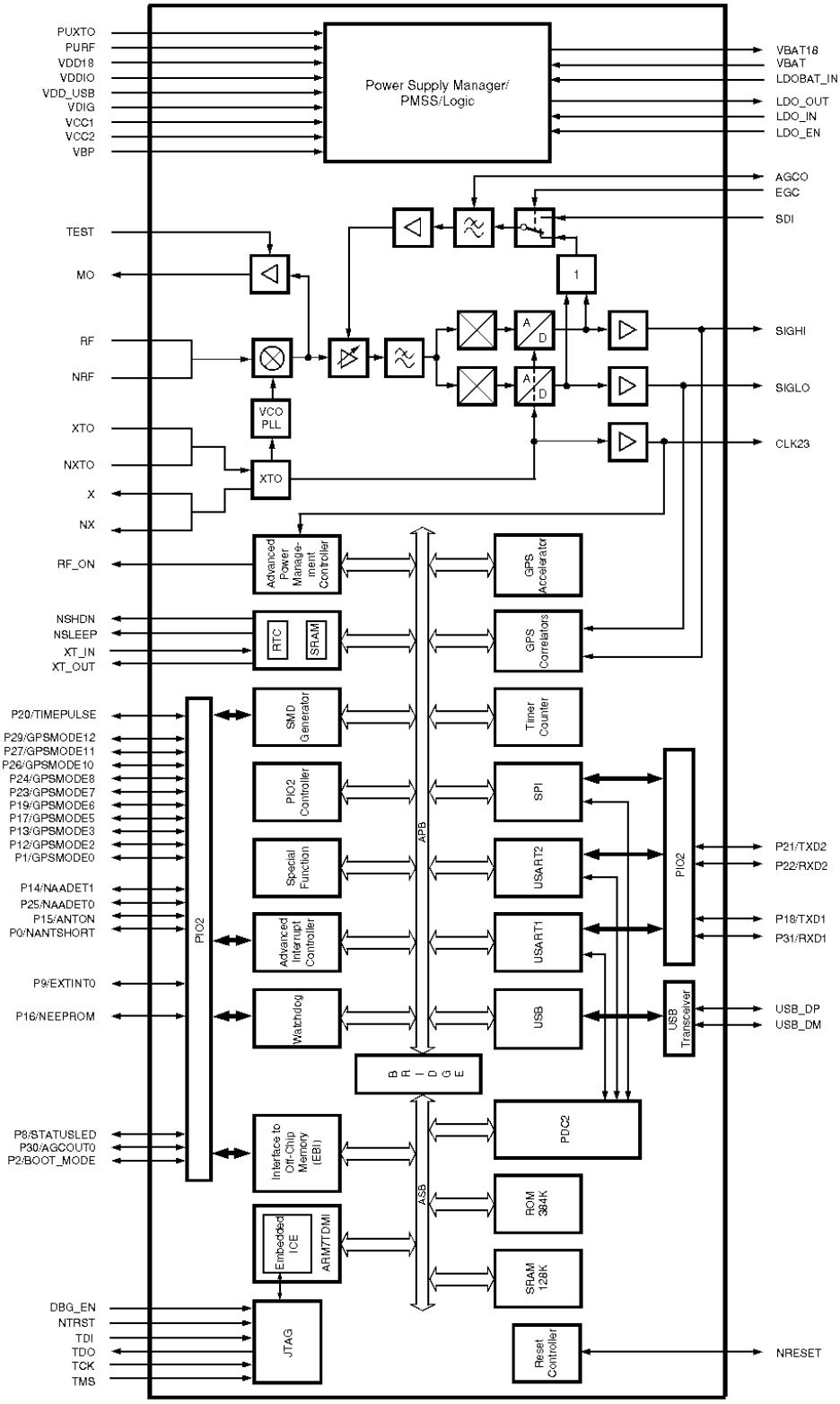


Figure 1-1: Block Diagram

1.4 Operating Modes

The ANTARIS 4 GPS Technology supports following Operating Modes:

Operating Modes	Description
Continuous Tracking Mode (CTM)	In this mode, the Autonomous Power Management (APM) automatically optimizes power consumption. It powers off parts of the receiver when they are not used. Also, the CPU speed is reduced when the CPU workload is low.
Power Saving Modes	A configurable power saving mode is available where the GPS is put into sleep mode and activated up on a selectable time interval or upon external request (signal activity on serial port or EXTINT input). This mode is ideally suited in applications with stringent power budget requirements in mobile and battery operated end products.

Table 1-1: Operating Modes

For more information see the *ANTARIS 4 Receiver Description* [1].

1.5 Protocols

The LEA-4A supports different serial protocols.

Protocol	Type	Runs on
NMEA	Input/output, ASCII, 0183, 2.3 (compatible to 3.0)	All serial ports and USB
UBX	Input/output, binary, u-blox proprietary	All serial ports and USB
RTCM	Input, message 1,2,3,9	All serial ports and USB

Table 1-2: Available Protocols

For specification of the various protocols see the *Protocol Specification* [2].

1.6 Assisted GPS (A-GPS)

The ANTARIS 4 GPS engine supports both MS assisted (output of raw tracking information for position computation by the service provider) and MS based (accelerated acquisition and position computation in the GPS receiver) A-GPS. Supply of aiding information like ephemeris, almanac, rough last position and time and satellite status and an optional time synchronization signal will reduce time to first fix significantly.

2 Architectural Overview

Feature	Description	
RF	Sampling	1.5 Bit
IF-Filter		Built-In
Processor	ARM7TDMI	High performance 32-bit RISC architecture
On-chip memory	ROM	384. Kbytes
	RAM	128 Kbytes
	Backup RAM	4 Kbytes
Serial I/O	USB	USB V1.2 (V2.0 compatible)
	USARTs	2
	SPI (Master + Slave)	4 SPI Chip selects
Digital I/O	GPIO	24
	Interrupt capable:	2 (EXTINT0, EXTINT1)
Power supply system	LDO Regulators	LDO18 (generates internal 1.8 V)
		LDOBAT (regulates backup voltage)
	Pads	User-definable I/O voltages for several GPIOs with 5V tolerance
Other features	6 channel peripheral data controller (PDC)	
	8-level priority, individually maskable, vectored interrupt controller	
	Programmable watchdog timer	
	Advanced power management controller (APMC)	
	Real-time clock (RTC)	

Table 2-1: Features

2.1 Description

The ATR0630 and ATR0635 have been designed especially for mobile terminal applications. They provide high isolation between GPS and cellular bands, as well as very low power consumption.

The ANTARIS4 chipset has a very low power consumption and comes with a very low BoM for the passive components. Especially, due to its fast search engine and GPS accelerator, the ATR0630 only needs a GPS crystal (XTAL) as a resonator for the integrated crystal oscillator of the ATR0630. This saves the considerable higher cost of a TCXO which is required for competitor's systems. For the ATR0635, a TCXO is required.

The L input signal (f_{RF}) is a Direct Sequence Spread Spectrum (DSSS) signal with a center frequency of 1575.42 MHz. The digital modulation scheme is Bi-Phase-Shift-Keying (BPSK) with a chip rate of 1.023 Mbps.

2.2 PMSS Logic

The power management, startup and shutdown (PMSS) logic ensures reliable operation within the recommended operating conditions. The external power control signals PUrf and PUxto are passed through Schmitt trigger inputs to eliminate voltage ripple and prevent undesired behavior during start-up and shut-down. Digital and analog supply voltages are analyzed by a monitoring circuit, enabling the startup of the IC only when it is within a safe operating range.

2.3 XTO

The XTO is designed for minimum phase noise and frequency perturbations. The balanced topology gives maximum isolation from external and ground coupled noise. The built-in jump-start circuitry ensures reliable start-up behavior of any specified crystal. For use with an external TCXO, the XTO circuitry can be used as a single-ended or balanced input buffer.

The recommended reference frequency is: f_{XTO} = 23.104 MHz.

2.4 VCO/PLL

The frequency synthesizer features a balanced VCO and a fully integrated loop filter, thus no external components are required. The VCO combines very good phase noise behavior and excellent spurious suppression. The relation between the reference frequency (f_{XTO}) and the VCO center frequency (f_{VCO}) is given by: $f_{VCO} = f_{XTO} \times 64 = 23.104\ MHz \times 64 = 1478.656\ MHz$.

2.5 RF-Mixer Image-Filter

Combined with the antenna an external LNA provides a first band-pass filtering of the signal. For the LNA, the ATR0610 is recommended, due to it's low noise figure, high linearity and low power consumption. The output of the LNA drives an SAW filter, which provides image rejection for the mixer and the required isolation of all GSM bands. The output of the SAW filter is fed into a highly linear mixer with high conversion gain and excellent noise performance.

2.6 VGA/AGC

The on-chip automatic gain control (AGC) stage sets the gain of the VGA in order to optimally load the input of the following analog-to-digital converter. The AGC control loop can be selected for on-chip closed-loop operation or for baseband controlled gain mode.

2.7 Analog-to-digital Converter

The analog-to-digital converter stage has a total resolution of 1.5 bits. It comprises balanced comparators and a sub-sampling unit, clocked by the reference frequency (f_{XTO}). The frequency spectrum of the digital output signal (f_{OUT}), present at the data outputs SIGLO0 and SIGHI0, is 4.348 MHz.

2.8 Baseband

The GPS baseband core includes a 16-channel correlator is based on an ARM7TDMI ARM processor core with very low power consumption. It has a high-performance 32 bit RISC architecture and uses a high-density 16-bit instruction set. The ARM standard In-Circuit Emulation debug interface is supported via the JTAG/ICE port. The ARM7TDMI processor operates in little-endian mode.

The baseband architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories. The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA™ Bridge provides an interface between the ASB and the APB.

An on-chip Peripheral Data Controller (PDC2) transfers data between the on-chip USARTs/SPI and the on-chip and off-chip memories without processor intervention. Most importantly, the PDC2 removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64K contiguous bytes without reprogramming the starting address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

The baseband peripherals are designed to be easily programmable with a minimum number of instructions. Each peripheral has a 16 Kbyte address space allocated in the upper 3 Mbyte of the 4 Gbyte address space. (Except for the interrupt controller, which has 4 Kbyte address space.) The peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status, and interrupt registers.

All of the external signals of the on-chip peripherals are under the control of the Parallel I/O (PIO2) Controller. The PIO2 Controller can be programmed to insert an input filter on each pin or generate an interrupt on a signal change. After reset, the user must carefully program the PIO2 Controller in order to define which peripheral signals are connected with off-chip logic.

An Advanced Power Management Controller (APMC) allows for the peripherals to be deactivated individually. Automatic master clock gearing reduces power consumption. A Sleep Mode is available with disabled 23.104 MHz master clock, as well as a Backup Mode operating 32.768 kHz master clock.

A 32.768 kHz Real Time Clock (RTC), together with a built-in battery back-up SRAM, allows for storage of Almanac, Ephemeris, software configurations to make quick hot- and warm starts.

The functionality of the ROM-based firmware is described in the *ANTARIS 4 Receiver Description* [1].

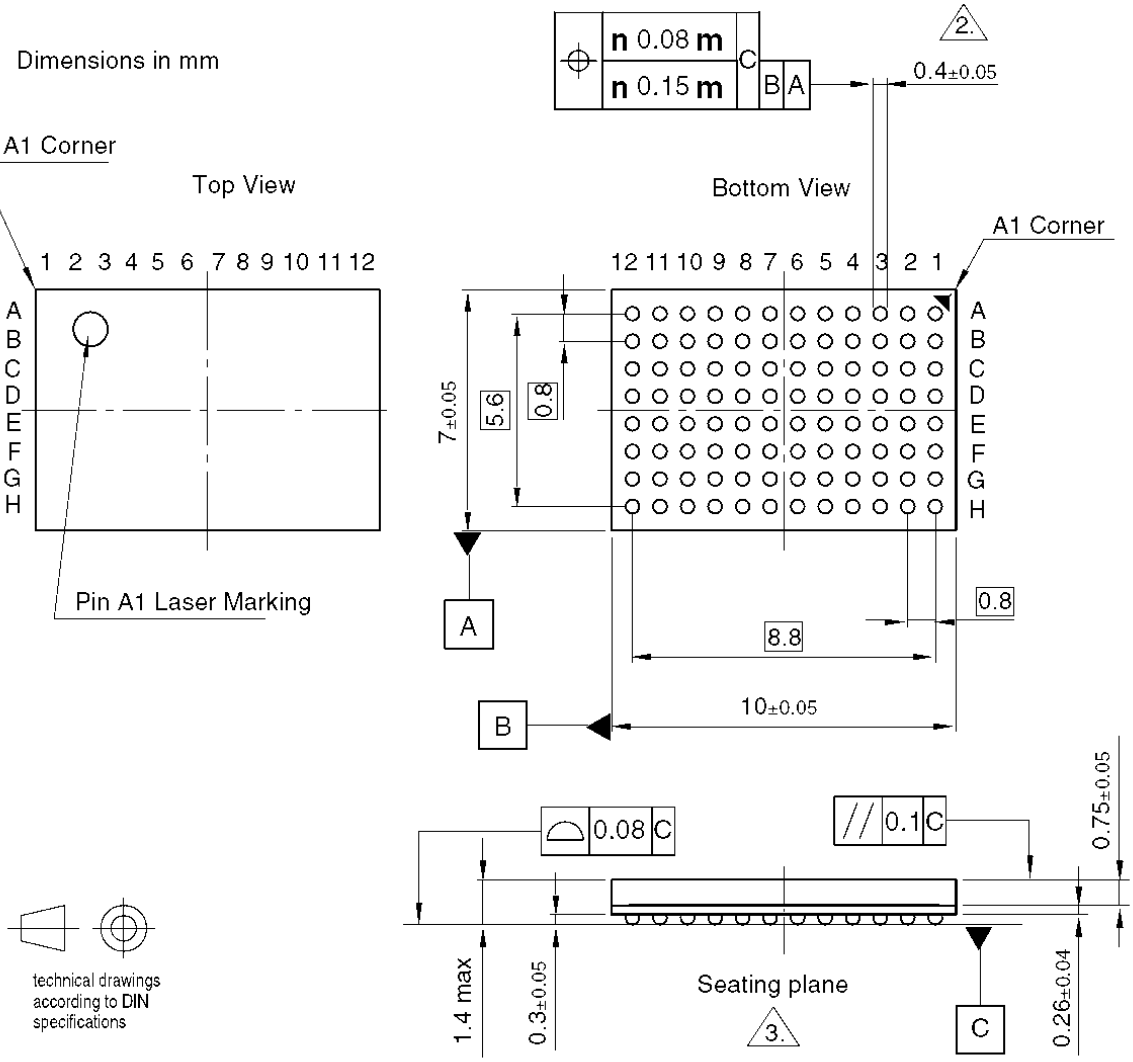
3 Performance Specification

Parameter	Specification				
Receiver Type		L1 frequency, C/A Code, 16-Channels 8192 time / frequency search windows			
Max Navigation Update Rate		4 Hz			
Accuracy	Position	2.5 m CEP[2]	5.0 m SEP[3]		
	Position DGPS / SBAS[1]	2.0 m CEP	3.0 m SEP		
Acquisition[4, 5]	GPS Mode (UBX-CFG Msg):	Fast Acquisition Mode	Normal Mode	High Sensitivity Mode	Auto Mode
	Cold Start	34 s	36 s	41 s	34 s
	Warm Start	33 s			
	Hot Start	<3.5 s			
	Aided Start[6]	5 s			
	Reacquisition	<1 s			
Sensitivity[7] (ATR0630)		Fast Acquisition Mode	Normal Mode	High Sensitivity Mode	Auto Mode
	Acquisition	-133 dBm	-137 dBm	-139 dBm	See [8]
	Tracking	-142 dBm	-145 dBm	-149 dBm	-149 dBm
Sensitivity[9] (ATR0635 with SuperSense)	Tracking	-157 dBm			
	Acquisition & Reacquisition	-147 dBm			
	Cold Starts	-141dBm			
Accuracy of Timepulse Signal	RMS	50 ns			
	99%	<100 ns			
	Granularity	43 ns			
Dynamics	Strong signals	≤ 4 g			
Operational Limits (COCOM)	Altitude	18,000 m			
	Velocity	515 m/s			
	One of the limits may be exceeded but not both.				

Table 3-1: Performance Specification

[1] Depends on accuracy of correction data of DGPS or SBAS service
[2] CEP = Circular Error Probability: The radius of a horizontal circle, centered at the antenna's true position, containing 50% of the fixes.
[3] SEP = Spherical Error Probability. The radius of the sphere, centered at the true position, contains 50% of the fixes.
[4] The different start-up modes like cold, warm and hot start are described in the *ANTARIS 4 Receiver Description* [1].
[5] Measured with good visibility and -125 dBm signal strength
[6] Time synch. signal from aiding source must be supplied to **EXTINT0** or **EXTINT1** pin, having accuracy of better than 200 µs
[7] Demonstrated with a good active antenna
[8] Sensitivity for finding first satellite: -133 dBm. Sensitivity increases up to –149 dBm for searching additional satellites.
[9] Demonstrated with a good active antenna

4 Mechanical Specification



Note:

1. All dimensions and tolerance conform to ASME Y 14.5M-1994
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C
3. Primary datum C and seating plane are defined by the spherical crowns of the solder balls
4. The surface finish of the package shall be EDM CHARMILLE #24 - #27
5. Unless otherwise specified tolerance: Decimal ±0.05, Angular ±2°
5. Raw ball diameter: 0.4 mm ref.

Figure 4-1: Package Information

5 Pin Configuration

5.1 Pinout

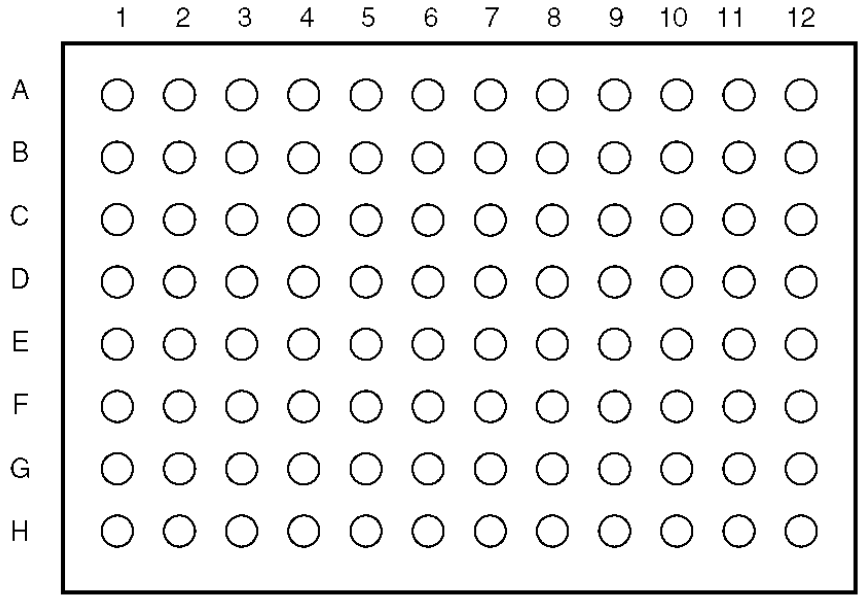


Figure 5-1: Pinout QFN96 (Top View)

Pin Name	QFN 96	Pin Type	Pull Resistor (Reset Value) [1]	Firmware Label	PIO Bank A		PIO Bank B	
AGCO	A4	Analog I/O						
CLK23	A8	Digital OUT						
DBG_EN	E8	Digital IN	PD					
EGC	D4	Digital IN						
GDIG	C5	Supply						
GND	A6	Supply						
GND	A9	Supply						
GND	B11	Supply						
GND	F5	Supply						
GND	H8	Supply						
GND	H12	Supply						
GNDA	A3	Supply						
GNDA	B1	Supply						
GNDA	B4	Supply						
GNDA	D2	Supply						
GNDA	E1	Supply						
GNDA	E2	Supply						
GNDA	E3	Supply						
GNDA	F1	Supply						
GNDA	F2	Supply						
GNDA	F3	Supply						
GNDA	G1	Supply						
GNDA	H1	Supply						
LDOBAT_IN	D11	Supply						
LDO_EN	C11	Digital IN						

Pin Name	QFN 96	Pin Type	Pull Resistor (Reset Value) [1]	Firmware Label	PIO Bank A		PIO Bank B	
LDO_IN	E11	Supply						
LDO_OUT	E12	Supply						
MO	C3	Analog OUT						
NRESET	A7	Digital I/O	Open Drain PU					
NRF	C1	Analog IN						
NSHDN	E9	Digital OUT						
NSLEEP	E10	Digital OUT						
NTRST	H11	Digital IN	PD					
NX	B2	Analog OUT						
NXTO	B3	Analog IN						
P0	C8	Digital I/O	PD	NANTSHORT				
P1	D8	Digital I/O	Configurable (PD)	GPSMODE0		AGCOUT1		
P2	C6	Digital I/O	Configurable (PD)	BOOT_-MODE		"0"		
P8	D7	Digital I/O	Configurable (PD)	STATUSLED		"0"		
P9	A11	Digital I/O	PU to VBAT18	EXTINT0	EXTINT0			
P12	D6	Digital I/O	Configurable (PU)	GPSMODE2		NPCS2		
P13	B10	Digital I/O	PU to VBAT18	GPSMODE3	EXTINT1			
P14	G6	Digital I/O	Configurable (PD)	NAADET1		"0"		
P15	F11	Digital I/O	PD	ANTON				
P16	G8	Digital I/O	Configurable (PU)	NEEPROM				NWD_OVF
P17	H6	Digital I/O	Configurable (PD)	GPSMODE5	SCK1	SCK1		
P18	C7	Digital I/O	Configurable (PU)	TXD1		TXD1		"0"
P19	F6	Digital I/O	Configurable (PU)	GPSMODE6				"0"
P20	G7	Digital I/O	Configurable (PD)	TIMEPULSE	SCK2	SCK2		TIMEPULSE
P21	E6	Digital I/O	Configurable (PU)	TXD2		TXD2		"0"
P22	D10	Digital I/O	PU to VBAT18	RXD2	RXD2			
P23	F8	Digital I/O	Configurable (PU)	GPSMODE7	SCK	SCK		MCLK_OUT
P24	H7	Digital I/O	Configurable (PU)	GPSMODE8	MOSI	MOSI		"0"
P25	G5	Digital I/O	Configurable (PD)	NAADET0	MISO	MISO		"0"
P26	B6	Digital I/O	Configurable (PU)	GPSMODE10	NSS	NPCS0		"0"
P27	F7	Digital I/O	Configurable (PU)	GPSMODE11		NPCS1		
P28	E7	Digital I/O	OH					
P29	D5	Digital I/O	Configurable (PU)	GPSMODE12		NPCS3		
P30	G12	Digital I/O	PD	AGCOUT0		AGCOUT0		"0"
P31	C10	Digital I/O	PU to VBAT18	RXD1	RXD1			
PURF	G4	Digital IN						

Pin Name	QFN 96	Pin Type	Pull Resistor (Reset Value) [1]	Firmware Label	PIO Bank A		PIO Bank B	
PURF	H4	Digital IN						
PUXTO	F4	Digital IN						
RF	D1	Analog IN	PD					
RF_ON	F10	Digital OUT	PD					
SDI	C4	Digital IN						
SIGHI0	B8	Digital OUT						
SIGLO0	B7	Digital OUT						
TCK	G9	Digital IN	PU					
TDI	H10	Digital IN	PU					
TDO	F9	Digital OUT						
TEST	D3	Analog IN						
TMS	G10	Digital IN	PU					
USB_DM	D9	Digital I/O						
USB_DP	C9	Digital I/O						
VBAT	D12	Supply						
VBAT18 [2]	C12	Supply						
VBP	G2	Supply						
VBP	G3	Supply						
VBP	H2	Supply						
VBP	H3	Supply						
VCC1	C2	Supply						
VCC2	E4	Supply						
VDD_USB [3]	A10	Supply						
VDD18	H9	Supply						
VDD18	G11	Supply						
VDD18	F12	Supply						
VDD18	B9	Supply						
VDD18	E5	Supply						
VDDIO [4]	B5	Supply						
VDDIO	H5	Supply						
VDIG	A5	Supply						
X	A2	Analog OUT						
XT_IN	A12	Analog IN						
XT_OUT	B12	Analog OUT						
XTO	A1	Analog IN						

Notes:

[1] PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset

[2] VBAT18 represent the internal power supply of the backup power domain, see section 6, "Power Supply"

[3] VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP, see section 6, "Power Supply". For operation of the USB interface, supply of 3.0 to 3.6 V is required.

[4] VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29, see section 6, "Power Supply"

Table 5-1: Pin Description

5.2 Signal Description

Pin Number	Pin Name	Type	Active Level	Pin Description / Comment
RF Section				
D1	RF	Analog IN	-	Input from SAW Filter
C1	NRF	Analog IN	-	Inverted input from SAW filter
GPS XTAL Section				
A1	XTO	Analog IN	-	XTO input (23.104 MHz) / optional TCXO input
B3	NXTO	Analog IN	-	Inverted XTO input (23.104 MHz) / optional TCXO input
A2	X	Analog OUT	-	XTO interface (capacitor)
B2	NX	Analog OUT	-	Inverted XTO interface (capacitor)
RTC Section				
A12	XT_IN	Analog IN	-	Oscillator input (32.768 KHz)
B12	XT_OUT	Analog OUT	-	Oscillator output (32.768 KHz)
Automatic Gain Control, bandwidth setting				
A4	AGCO	Analog I/O	-	Automatic gain control analog voltage, connect shunt capacitor to GND
D4	EGC	Digital IN	-	Enable external gain control (high = software gain control, low = automatic gain control)
G12	AGCOUT	Digital OUT	-	Software gain control
C4	SDI	Digital IN	-	Software gain control
Boot Section				
C6	BOOT_-MODE	Digital IN	-	Leave open, internal pull down
Reset				
A7	NRESET	Digital I/O	Low	Reset input; open drain with internal pull-up resistor
APMC / Power Management				
E9	NSHDN	Digital OUT	Low	Shutdown output, connect to LDO_EN (C11)
C11	LDO_EN	Digital IN	-	Enable LDO18
E10	NSLEEP	Digital OUT	Low	Power-up output for GPS XTAL, connect to PUXTO (F4)
F4	PUXTO	Digital IN	-	Power-up input for GPS XTAL
G4, H4	PURF	Digital IN	-	Power-up input for GPS radio
F10	RF_ON	Digital OUT	-	Power-up output for GPS radio, connect to PURF (G4, H4)
Advanced Interrupt Controller (AIC)				
A11, B10	EXTINT0, 1	Digital IN	High / Low / Edge	External interrupt request
USART				
C10, D10	RXD1 / RXD2	Digital OUT	-	USART receive data output
C7, E6	TXD1 / TXD2	Digital IN	-	USART transmit data input
H6, G7	SCK1 / SCK2	Digital I/O	-	External synchronous serial clock
USB				
C9	USB_DP	Digital I/O	-	USB Data (D+)
D9	USB_DM	Digital I/O	-	USB Data (D-)
SPI Interface				
F8	SCK	Digital I/O	-	SPI clock
H7	MOSI	Digital I/O	-	Master out slave in
G5	MISO	Digital I/O	-	Master in slave out
B6	NSS / NPCS0	Digital I/O	Low	Slave Select
F7, D6, D5	NPCS1…3	Digital OUT	Low	Slave Select
PIO				
A11,B6, B10, C6…8, C10, D5…8, D10, E6…7, F6…8, G5…8,H6…7	P0…31	Digital I/O	-	Programmable I/O Ports

Pin Number	Pin Name	Type	Active Level	Pin Description / Comment
Configuration				
B6, B10, D5, D6, D8, F6…8, H6…7	GPSMODE 0…12	Digital IN	-	GPS mode pins
G8	NEEPROM	Digital IN	Low	Enable EEPROM support
GPS				
D7	STATUSLED	Digital OUT	-	Status LED
G7	TIMEPULSE	Digital OUT	-	GPS synchronized time pulse
Active Antenna Supervision				
C8	NANTSHORT	Digital IN	Low	Active antenna short detection Input
G5, G6	NAADET0 / NAADET1	Digital IN	Low	Active antenna detection Input
F11	ANTON	Digital OUT	-	Active antenna power-on Output
JTAG Interface				
E8	DBG_EN	Digital IN	-	Debug enable
F9	TDO	Digital OUT	-	Test data out
G9	TCK	Digital IN	-	Test clock
G10	TMS	Digital IN	-	Test mode select
H10	TDI	Digital IN	-	Test data in
H11	NTRST	Digital IN	Low	Test reset input
Debug / Test				
C3	MO	Analog OUT	-	IF output buffer
D3	TEST	Analog IN	-	Enable IF output buffer
B7	SIGLO0	Digital OUT	-	Digital IF (data output "Low")
B8	SIGHI0	Digital OUT	-	Digital IF (data output "High")
A8	CLK23	Digital OUT		Digital IF (sample clock)
Power Analog Part				
C2	VCC1	Supply	-	Analog supply 3V
E4	VCC2	Supply	-	Analog supply 3V
G2, G3, H2, H3	VBP	Supply	-	Analog supply 3V
A3, B1, B4, D2, E1…3, F1…3, G1, H1	GNDA	Supply	-	Analog Ground
Power Digital Part				
A5	VDIG	Supply	-	Digital supply (radio) 1.8 V
B9, E5, F12, G11, H9	VDD18	Supply	-	Core voltage 1.8 V
A10	VDD_USB	Supply	-	USB transceiver supply voltage (3.0V to 3.6V (USB enabled) or 0 to 2.0V (USB disabled))
B5, H5	VDDIO	Supply	-	Variable I/O voltage 1.65 to 3.6 V
C5	GDIG	Supply	-	Digital ground (radio)
A6, A9, B11, F5, H8, H12	GND	Supply	-	Digital ground
LDO18				
E11	LDO_IN	Supply	-	2.3V to 3.6 V
E12	LDO_OUT	Supply	-	1.8V LDO18 output, max. 80 mA
LDOBAT				
D11	LDOBAT_IN	Supply	-	2.3V to 3.6 V
D12	VBAT	Supply	-	1.5V to 3.6 V
C12	VBAT18	Supply	-	1.8V LDOBAT Output

Table 5-2: Signal Description

5.3 Boot-Time GPSMODE Configuration

The start-up configuration of a ROM-based system without external non-volatile memory is defined by the status of the GPSMODE pins after system reset. Alternatively, the system can be configured through message commands passed through the serial interface after start-up. This configuration can be stored in an external non-volatile memory like EEPROM. Default designates settings used by ROM firmware if GPSMODE configuration is disabled (GPSMODE0 = 0).

Module	Name
GPSMODE0 (P1)	Enable configuration with GPSMODE pins
GPSMODE1 (P9)	This pin (EXTINT0) is used for FixNow™ functionality and not used for GPSMODE configuration
GPSMODE2 (P12)	GPS sensitivity settings
GPSMODE3 (P13)	
GPSMODE4 (P14)	This pin (NAADET1) is used as active antenna supervisor input and not used for GPSMODE configuration. This is the default selection if GPSMODE configuration is disabled
GPSMODE5 (P17)	Serial I/O configuration
GPSMODE6 (P19)	
GPSMODE7 (P23)	USB power mode
GPSMODE8 (P24)	General I/O configuration
GPSMODE9 (P25)	This pin (NAADET0) is used as active antenna supervisor input and not used for GPSMODe configuration
GPSMODE10 (P26)	General I/O configuration
GPSMODE11 (P27)	
GPSMODE12 (P29)	Serial I/O configuration

Table 5-3: GPSMODE Functions

In the case tat GPSMODE pins with internal pull-up or pull-down resistors are connected to GND/VDD18, additional current is drawn over these resistors. Especially GPSMODE3 can impact the backup current. For more information see the *ANTARIS 4 Receiver Description* [1].

5.4 Active Antenna Supervisor

The two pins P0/NANTSHORT and P15/ANTON plus one pin of P25/NAADET0/MISO or P14/NAADET1 are always initialized as general purpose I/Os and used as follows:

- P15/ANTON is an output which can be used to switch on and off antenna power supply.
- Input P0/NANTSHORT will indicate an antenna short circuit, i.e. zero DC voltage at the antenna, to the firmware. If the antenna is switched off by output P15/ANTON, it is assumed that also input P0/NANTSHORT will signal zero DC voltage, i.e. switch to its active low state.
- Input P25/NAADET0/MISO or P14/NAADET1 will indicate a DC current into the antenna. In case of short circuit, both P0 and P25/P14 will be active, i.e. at low level. If the antenna is switched off by output P15/ANTON, it is assumed that also input P25/NAADET0/MISO will signal zero DC current, i.e. switch to its active low state. Which pin is used as NAADET (P14 or P25) depends on the settings of GPSMODE11 and GPSMODE10.

Pin	Usage	Meaning
P0 / NANTSHORT	NANTSHORT	Active antenna short circuit detection input High = No antenna DC short circuit present Low = Antenna DC short circuit present
P25 / NAADET0 / MISO or P14 / NAADET1	NAADET	Active antenna detection input High = No active antenna present Low = Active antenna is present
P15 / ANTON	ANTON	Active antenna power on output High = Power supply to active antenna is switched on Low = Power supply to active antenna is switched off

Table 5-4: GPS Sensitivity Settings

6 Power Supply

The RF part is supplied with following supply voltages:

- **VCC1, VCC2, VBP**, the power supply for RF part, 2.7 – 3.3 V
- **VDIG18**, the 1.8V supply of the digital pins of the RF part (SIGHI0, SIGLO0 and CLK23). VDIG should be connected to VDD18.

The baseband part is supplied with four distinct supply voltages:

- **VDD18**, the nominal 1.8V supply voltage for the core, the RF-I/O pins, the memory interface and the test pins and all GPIO-pins not mentioned in next item.
- **VDDIO**, the variable supply voltage within 1.8V to 3.6V for following GPIO-pins: P1, P2, P8, P12, P14, P16, P17…P21, P23…P27 and P29. In input mode, these pins are 5V input tolerant.
- **VDD_USB**, the power supply of the USB pins: USB_DM and USB_DP. The USB Transceiver is disabled if VDD_USB < 2.0V. In this case the pins USB_DM and USB_DP are connected to GND (internal pull-down resistors). The USB Transceiver is enabled if VDD_USB within 3.0V and 3.6V.
- **VBAT18** to supply the backup domain: RTC, backup SRAM and the pins NSLEEP, NSHDN, LDO_EN, VBAT18, P9/EXTINO, P13/EXTINT1, P22/RXD2 and P31/RXD1 and the 32kHz oscillator. In input mode, the four GPIO-pins are 5V input tolerant.

In addition, the ATR0630 / ATR0635 features two low dropout linear regulators (LDO's):

- **LDO18** converts supply voltages between 2.3 and 3.6V to 1.8V for the core and, if necessary, external Flash EPROM. The LDO18 can be deactivated if a1.8V supply is available.
- **LDOBAT** provides supply voltage for RTC and backup SRAM from battery backup supply input VBAT between 1.5V and 3.6V.

For the core, the following power supply configurations are supported:

- 1.8V is available to supply the core directly
- A higher supply voltage (2.3V…3.6V) is available and must be converted to 1.8V using the LDO18
- The supply is drawn from the USB port. In this case, an external LDO converting to 3.3V is needed.

Only after VDD18 has been supplied to baseband IC the RTC section will be initialized properly. If only VBAT is applied first, the current consumption of the RTC and backup SRAM is undetermined.

For more information see the *ANTARIS 4 Receiver Description* [1].

7 Oscillators

7.1 GPS Oscillator

For the ATR0630, the choice of 23.104 MHz crystal or TCXO is available. For the ATR0635, a 23.104 MHz TCXO is required.

7.2 RTC Oscillator

Following RTC configurations are supported:

- Use of 32.768 KHz RTC crystal
- Use of an external 32.768 signal (shared with other semiconductor chips)
- No RTC (GPS must do cold starts at power-up)

8 Electrical Specifications

8.1 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pin	Symbol	Min.	Max.	Unit
Operating temperature range		T_{op}	-40	+85	°C
Storage temperature		T_{stg}	-55	+125	°C
Analog supply voltage	VCC1, VCC2, VBP	V_{CC}	-0.3	+3.7	V
Digital supply voltage RF	VDIG	V_{DIG}	-0.3	+3.7	V
Digital supply voltage core	VDD18	VDD18	-0.3	+1.95	V
DC supply voltage VDDIO domain	VDDIO	VDDIO	-0.3	+3.6	V
DC supply voltage USB	VDD_USB	VDD_USB	-0.3	+3.6	V
DC supply voltage LDO18	LDO_IN	LDO_IN	-0.3	+3.6	V
DC supply voltage LDOBAT	LDOBAT_IN	LDOBAT_IN	-0.3	+3.6	V
DC supply voltage VBAT	VBAT	VBAT	-0.3	+3.6	V
DC input voltage	P0, P15, P30, XT_IN, TMS, TCK, TDI, NTRST, DBG_EN, DLO_EN, NRESET		-0.3	+1.95	V
DC input voltage USB	USB_DM, USB_DP		-0.3	+3.6	V
DC input voltage VDDIO domain	P1, P2, P8, P9, P12…P14, P16…P27, P29, P31		-0.3	+5.0	V

Note: Minimum/maximum limits are at +25°C ambient temperature, unless otherwise specified

Table 8-1: Absolute Maximum Ratings

8.2 Operating Conditions – RF Section

Parameters	Pin	Symbol	Min.	Typ	Max.	Unit
Analog supply voltage	VCC1, VCC2, VBP	V_{CC}	2.70		3.30	V
Digital supply voltage RF	VDIG	V_{DIG}	1.65	1.8	1.95	V
Supply voltage difference ($V_{\Delta} = V_{CC} - V_{DIG}$)		V_{Δ}		≥ 0.80		V
Input frequency		f_{RF}		1575.42		MHz
Reference frequency GPS XTAL		f_{XTO}		23.104		MHz
Temperature range		Temp	-40		+85	°C

Table 8-2: Operating Range

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
1	**RF Front-end**							
1.1	Output frequency	f_{XTO} = 23.104 MHz	MO	f_{IF}		96.764		MHz
1.2	Input impedance (balanced)	f_{RF}= 1575.42 MHz	RF, NRF	Z_{11}		10-j80		Ω
1.3	Mixer conversion gain		MO	G_{MIX}		10		dB
1.4	Mixer noise figure (SSB)		MO	NF_{MIX}		6		dB
1.5	Maximum total gain	V_{AGCO} = 2.2 V		$G_{max,tot}$		90		dB
1.6	Total noise figure (SSB)			NF_{tot}			6.8	dB
2	**VGA / AGC**							
2.1	Minimum gain	V_{AGCO} = 1.0 V		$G_{VGA,min}$		0		dB
2.2	Maximum gain	V_{AGCO} = 2.2 V		$G_{VGA,max}$		70		dB
3.3	Control-voltage sensitivity	V_{AGCO} = 2.2 V		$N_{VGA,min}$		6.6		dB/V
		V_{AGCO} = 1.0 V		$N_{VGA,max}$		150		dB/V
2.4	AGC cut-off frequency	C_{ext} = open	AGCO	F_{3dB_AGC}		250		KHz
2.5	AGC cut-off frequency	C_{ext} = 100 pF	AGCO	F_{3dB_AGC}		33		KHz
2.6	Gain-control output voltage		AGCO	V_{AGCO}	0.9		2.3	V
3	**Reference Oscillator**							
3.1	XTO phase noise at 100 Hz	with specified crystal	CLK23	Pn_{100}		-80		dBc/Hz
3.2	XTO phase noise at 1 KHz	with specified crystal	CLK23	Pn_{1K}		-100		dBc/Hz
4	**PMSS**							
4.1	Voltage level power-on		PUXTO, PURF	$V_{PU,on}$	1.3			V
4.2	Voltage level power-off		PUXTO, PURF	$V_{PU,off}$			0.5	V

Table 8-3: Operating Conditions – RF Section

8.3 Operating Conditions – Baseband Section

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
1.1	DC supply voltage core		VDD18	VDD18	1.65	1.8	1.95	V
1.2	DC supply voltage VDDIO domain [1]		VDDIO	VDDIO	1.65	1.8 / 3.3	3.6	V
1.3	DC supply voltage USB [2]		VDD_USB	VDD_USB	3.0	3.3	3.6	V
1.4	DC supply voltage backup domain [3]		VBAT18	VBAT18	1.65	1.8	1.95	V
1.5	DC output voltage VDD18			$V_{O,18}$	0		VDD18	V
1.6	DC output voltage VDDIO			$V_{O,IO}$	0		VDDIO	V
1.7	Low-level input voltage VDD18 domain	VDD18 = 1.65…1.95V		$V_{IL,18}$	-0.3		0.3 x VDD18	V
1.8	High-level input voltage VDD18 domain	VDD18 = 1.65…1.95V		$V_{IH,18}$	0.7 x VDD18		VDD18 + 0.3	V
1.9	Schmitt Trigger threshold rising	VDD18 = 1.65…1.95V	NRESET	$V_{th+,NRESET}$	0.8		1.3	V
1.10	Schmitt Trigger threshold falling	VDD18 = 1.65…1.95V	NRESET	$V_{th-,NRESET}$	0.46		0.77	V
1.11	Low-level input voltage VDDIO domain	VDDIO = 1.65…3.6V		$V_{IL,IO}$	-0.3		+0.41	V
1.12	High-level input voltage VDDIO domain	VDDIO = 1.65…3.6V		$V_{IH,IO}$	1.46		5.0	V

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
1.13	Low-level input voltage VBAT domain	VBAT18 = 1.65…1.95V	P9, P13, P22, P31	$V_{IL,BAT}$	-0.3		+0.41	V
1.14	High-level input voltage VBAT domain	VBAT18 = 1.65…1.95V	P9, P13, P22, P31	$V_{IH,BAT}$	1.46		5.0	V
1.15	Low-level input voltage USB	VDD_USB = 3.0…3.6V	DP, DM	$V_{IL,USB}$	-0.3		+0.8	V
1.16	High-level input voltage USB	VDD_USB = 3.0…3.6V 39 Ω source resistance 27 Ω ext. series resistor	DP, DM	$V_{IH,USB}$	2.0		4.6	V
1.17	Low-level output voltage VDD18 domain	I_{OL} = 1.5 mA, VDD18=1.65V		$V_{OL,18}$			0.4	V
1.18	High-level output voltage VDD18 domain	I_{OH} = -1.5 mA, VDD18=1.65V		$V_{OH,18}$	VDD18 -0.45			V
1.19	Low-level output voltage VDDIO domain	I_{OL} = 1.5 mA, VDDIO=3.0V		$V_{OL,IO}$			0.4	V
1.20	High-level output voltage VDDIO domain	I_{OH} = -1.5 mA, VDDIO=3.0V		$V_{OH,IO}$	VDDIO -0.5			V
1.21	Low-level output voltage VBAT18 domain	I_{OL} = 1 mA	P9, P13, P22, P31	$V_{OL,BAT}$			0.4	V
1.22	High-level output voltage VBAT18 domain	I_{OH} = -1 mA	P9, P13, P22, P31	$V_{OH,BAT}$	1.2			V
1.23	Low-level output voltage USB	I_{OL} = 2.2 mA, VDD_USB = 3.0...3.6V 27Ω ext. series resistor	DP, DM	$V_{OL,USB}$			0.3	V
1.24	High-level output voltage USB	I_{OL} = -0.2 mA, VDD_USB = 3.0...3.6V 27Ω ext. series resistor	DP, DM	$V_{OH,USB}$	2.8			V
1.25	Input leakage current (standard inputs and I/Os)	VDD18 = 1.95V V_{IL} = 0V		I_{LEAK}	-1		1	µA
1.26	Input capacitance			I_{CAP}			10	pF
1.27	Input pull-up resistor	-40°C to +85°C	NRESET	R_{PU}	0.7		1.8	KΩ
1.28	Input pull-up resistor	-40°C to +85°C	TCK, TDI, TMS	R_{PU}	7		18	KΩ
1.29	Input pull-up resistor	-40°C to +85°C	P9, P13, P22, P31	R_{PU}	100		235	KΩ
1.30	Input pull-down resistor	-40°C to +85°C	DBG_EN, NTRST	R_{PD}	7		18	KΩ
1.31	Input pull-down resistor	-40°C to +85°C	RF_ON, P0, P15, P30	R_{PD}	100		235	KΩ
1.32	Configurable input pull-up resistor	-40°C to +85°C	P1, P2, P8, P12, P14, P16…P21, P23…P27, P29	R_{CPU}	50		160	KΩ
1.33	Configurable input pull-down resistor	-40°C to +85°C		R_{CPD}	40		160	KΩ
1.34	Configurable input pull-up resistor (idle state)	-40°C to +85°C	USB_DP	R_{CPU}	0.9		1.575	KΩ
1.35	Configurable input pull-up resistor (operation state)	-40°C to +85°C	USB_DP	R_{CPU}	1.425		3.09	KΩ
1.36	Input pull-down resistor	-40°C to +85°C	USB_DP, USB_DM	R_{PD}	10		500	KΩ

Notes:
[1] VDDIO is the supply voltage for the following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
[2] Values defined for operating the USB interface. Otherwise VDD_USB may be connected to ground
[3] Supply voltage VBAT18 for backup domain is generated internally by the LDOBAT

Table 8-4: Operating Conditions – Baseband Section

8.4 Power Consumption

Mode	Conditions	Typ.	Unit
Sleep	At 1.8V, no CLK23	0.065 [1]	mA
Shutdown	RTC, backup SRAM and LDOBAT	0.007 [1]	mA
Normal	Satellite acquisition	40	mA
	Normal tracking on 6 channels with 1 fix/s; each additional active tracking channel adds 0.5 mA	29	mA
	All channels disabled	26	mA

Note: [1] Specified value only

Table 8-5: Power Consumption

8.5 LDO18

The LDO18 is a built-in low dropout voltage regulator which can be used if the host system does not provide the core voltage VDD18.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (LDO_IN)		2.3		3.6	V
Output voltage (LDO_OUT)		1.65	1.8	1.95	V
Output current (LDO_OUT)				80	mA
Current consumption	After start-up, no load, at room temperature			80	µA
Current consumption	Standby mode (LDO_EN = 0), at room temperature		1	5	µA

Table 8-6: Electrical Characteristics of LDO18

For well-defined start-up of LDO18, LDO_IN needs to be connected to LDOBAT_IN.

8.6 LDOBAT and Backup Domain

The LDOBAT is a built-in low dropout voltage regulator which provides the supply voltage for VBAT18 for the RTC, backup SRAM, P9, P13, P22, P31, NSLEEP and NSHDN. The LDOBAT voltage regulator switches in battery mode if LDOBAT_IN falls below 1.5 V

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply voltage LDOBAT_IN		2.3		3.6	V
Supply voltage VBAT		1.5		3.6	V
Output voltage (VBAT18)	If switch connects to LDOBAT_N	1.65	1.8	1.95	V
Output current (VBAT18)	No external load allowed			1.5	mA
Current consumption LDOBAT_IN [1]	After start-up (sleep/backup mode), at room temperature			15	µA
Current consumption VBAT_IN [1]	After start-up (backup mode and LDOBAT_IN = 0V), at room temperature			10	µA
Current consumption	After start-up (normal mode), at room temperature			1.5	mA

Note: [1] If no current is caused by outputs (pad output current as well as current across internal pull-up resistors)

Table 8-7: Electrical Characteristics of LDOBAT

9 Ordering Information

Ordering No.	Product
ATR0630N-7KQY	ATR0630 ANTARIS 4 GPS Single Chip, ROM-Based Firmware V 5.00 Delivery Packing: Taped and reeled, MPQ 3000
ATR0635-7KQY	ATR0635 ANTARIS 4 GPS Single Chip, ROM-Based Firmware V 5.00 with SuperSense Delivery Packing: Taped and reeled, MPQ 3000

Table 9-1: Ordering Information

Parts of this product are patent protected.

Related Documents

[1] ANTARIS 4 GPS Chipset: ANTARIS 4 Receiver Description, Docu No. GPS.G5-DK-06004

[2] ANTARIS 4 Protocol Specification, Docu. No GPS.G3-X-03002

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