Leach Amp Clone

Construction manual and builders guide

DELTA AUDIO

Jens Rasmussen

1 Introduction

I always liked the original amp designed by Mr. Leach, but thought that all the wiring to the output transistors was a bit of a bad solution, because it is easy to make a wiring mistake and maybe destroy expensive transistors in the process. This is the reason that I made my own PCB layout to fit my need for a powerful and good sounding amplifier. I like the flat pack transistors, so I decided to use these types in my design.

There has been a lot of discussion on www.diyaudio.com regarding the safe operating area and power derating for these types compared to the original TO-3 types. This is the reason that I choose 5 and 3 parallel transistors instead of the original two. The higher transistor count enables me to run the amplifier with +-68V rails and above depending on the type and amount output devises, and also into a lower speaker resistance without the need for a protection circuit to protect the devises under normal working conditions. I recommend using the protection circuit to make sure that no transistors are damaged if a short circuit of the output should occur.

During my work with this amplifier project, I needed to compare and evaluate some different types of output transistors, to be able to pick a reliable part and do various other calculations during the project. This work can be transferred to other projects also, why I have chosen to include all of the transistor data in this document.

I use Mathcad version 12 at work, so all graphs and equations are written in this program. Please don't ask me for excel files, I don't have any, and I'm not going to make any.

I have tried to make a comparison between some of the most used ONSEMI power output devises. All you need to do is read through these pages and evaluate the data presented yourself.

I will give my conclusions and try to explain the choices I have made in my Extended Leach Amps.

Please take extreme care when working with voltages above +-36V DC and mains connected equipment. Voltages can be lethal to touch, if you don't feel that your skills are good enough to safely work with these voltages; I suggest you improve your skills before starting a project of this type.

Happy reading and/or building.

Contents

2 Overview

3 The revised schematics

4 Output section

4.1 Summery of the devises

The output section is where my layout differs mostly from the original design. I have designed a PCB that incorporates all output devises as well as a Zobel network. To make a convenient layout I wanted to use devises in the TO-264 package, as these are great for an "onboard" solution.

Creating a short list of main characteristics for interesting output devises is in order to better compare the different devises.

	MJ15024 (NPN) MJ15025 (PNP)	MJ15003 (NPN) MJ15004 (PNP)	MJ21194 (NPN) MJ21193 (PNP)	MJL21194 (NPN) MJL21193 (PNP)	MJ21196 (NPN) MJ21195 (PNP)	MJL21196 (NPN) MJL21195 (PNP)	MJL3281A (NPN) MJL302A (PNP)	MJL4281A (NPN) MJL4302A (PNP)
Package	TO-3	TO-3	TO-3	TO-264	TO-3	TO-264	TO-264	TO-264
V_{CEO} [V]	250	140	250	250	250	250	230	**350**
P_D @25 °C [W]	**250**	**250**	**250**	200	**250**	200	200	230
T_J [°C]	**200**	**200**	**200**	150	**200**	150	150	150
Derating Δ [W/°C]	**1.43**	**1.43**	**1.43**	**1.43**	**1.43**	**1.43**	**1.43**	1.84
F_T [MHz]	4	2	4	4	4	4	30	**35**
I_C max [A]	16	**20**	16	16	16	16	15	15
Rth_{JC} [°C/W]	0.7	0.7	0.7	0.7	0.7	0.7	0.625	**0.54**
SOA [A@V/1s]	2A@80V	5A@50V	2.5A@80V	2.25A@80V	**3A@80V**	2.5A@80V	1A@100V	1A@100V

Table 4-1 Highlights of some data from standard output transistors

4.1.1 Safe operating area - SOA

Generally the safe operating area (SOA) is defined by a graph rather than the single point mentioned on the first page of a datasheet. This means that the SOA needs to be examined closer and in connection with e.g. the $R_{\Theta JC}$ and the power derating number (P_D).

Luckily most datasheets provide a really nice graph that shows the SOA curve(s). I prefer to use is the curve that gives information on the V_{CE} and I_C during one second.

One major problem with the curves is that they are made data from the maximum junction temperature (T_J) of the devises; this temperature is different from the TO-3 to the TO-264 devises. The curves are however made at the maximum junction temperature for all the devises, so in a way it's ok to compare the graphs directly from the datasheet.

Below I have drawn all the SOA for the different devises in the same double logarithmic graph. This gives a little overview, but is also a bit difficult to conclude anything from.

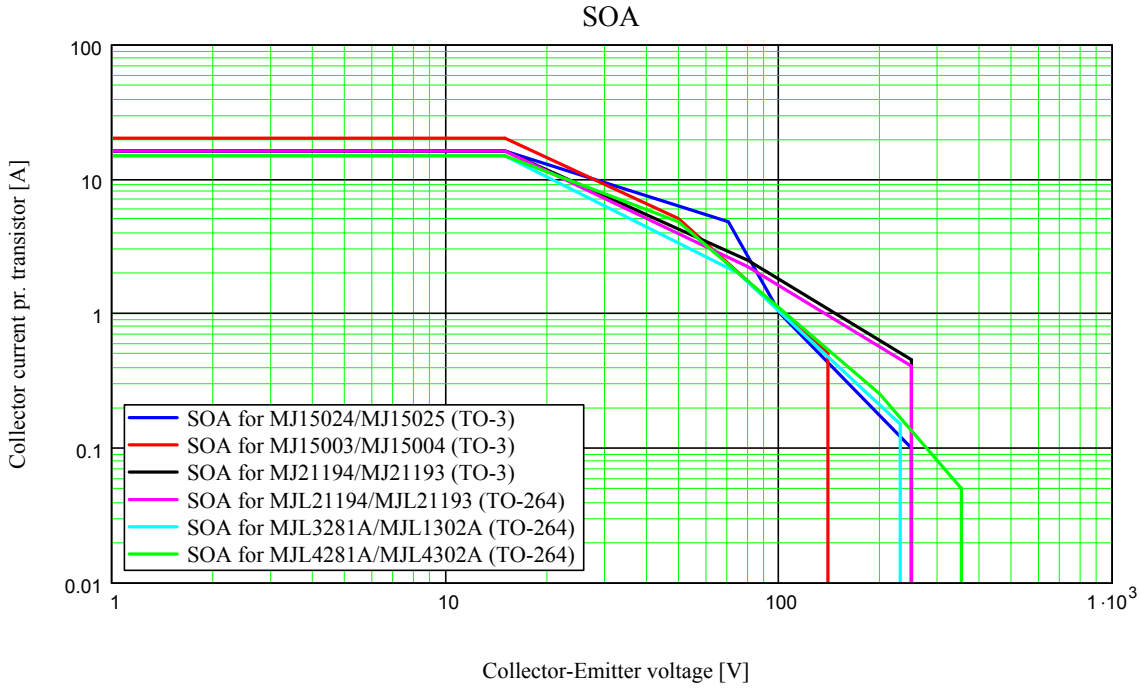


Figure 4-1 1 second SOA curves for the standard output transistors

Looking at the curves there is, in my opinion, no correlation between SOA and package type. This leads me to conclude that the choice of output devise must be based on a deeper evaluation.

The curve is the one second curve that I use for examining the output stage working conditions, and to find out if a protection circuit is needed. More explanation follows in section 4.1.3.

4.1.2 Load line

Try imaging the voltage across the CE of the output transistor in a class AB output stage with a negligible standing current. Now try thinking about the output current through the transistor and into the load. In Figure 4-2 is an example of load lines in 4 and 8 ohms.

On the Y-axis (The current axis) calculate two points (I + II)

$$Yaxis_1 = \frac{V_{CC}}{RL_1 \cdot N} \qquad RL_1 = 8\Omega \qquad N = \text{number of transistors}$$

$$Yaxis_2 = \frac{V_{CC}}{RL_2 \cdot N} \qquad RL_1 = 4\Omega$$

I High-Power Audio Amplifier Construction Manual, ISBN 0-07-134119-6 , G.Randy Slone, p 247-252
II Audio Power Amplifier Design Handbook, ISBN 0-7506-5636-0, Douglas Self, p 375-377

On the X-axis place a point at VCC. Then draw a line from the two points on the Y-axis to the VCC point on X-axis. These two lines enclose all the different voltages/currents the output transistors can be subjected to. The worst case is when the current and voltage is out of phase. This occurs when the load is 100% reactive (unlikely yes, but it is a good start). The result is that the point on the X-axis should be moved to 2 x VCC.

Consult Figure 4-2 that show the load line for the 10 transistor version if in doubt.

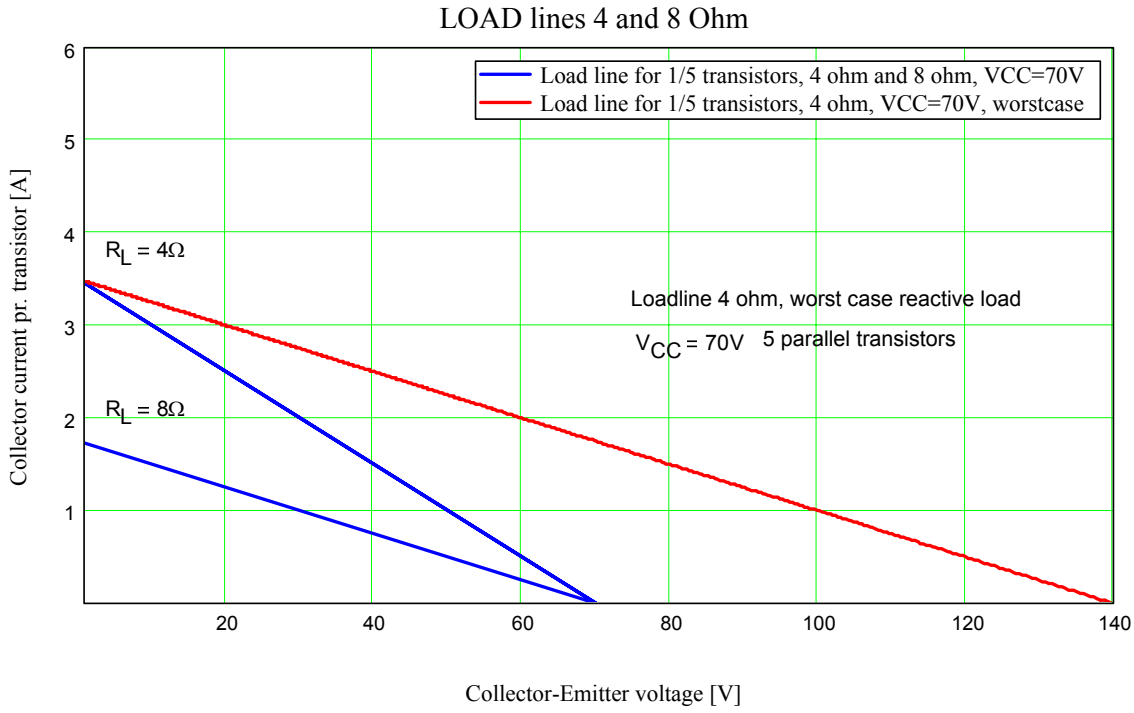


Figure 4-2 Load lines

Finally the worst-case line can be drawn in a double logarithmic graph.

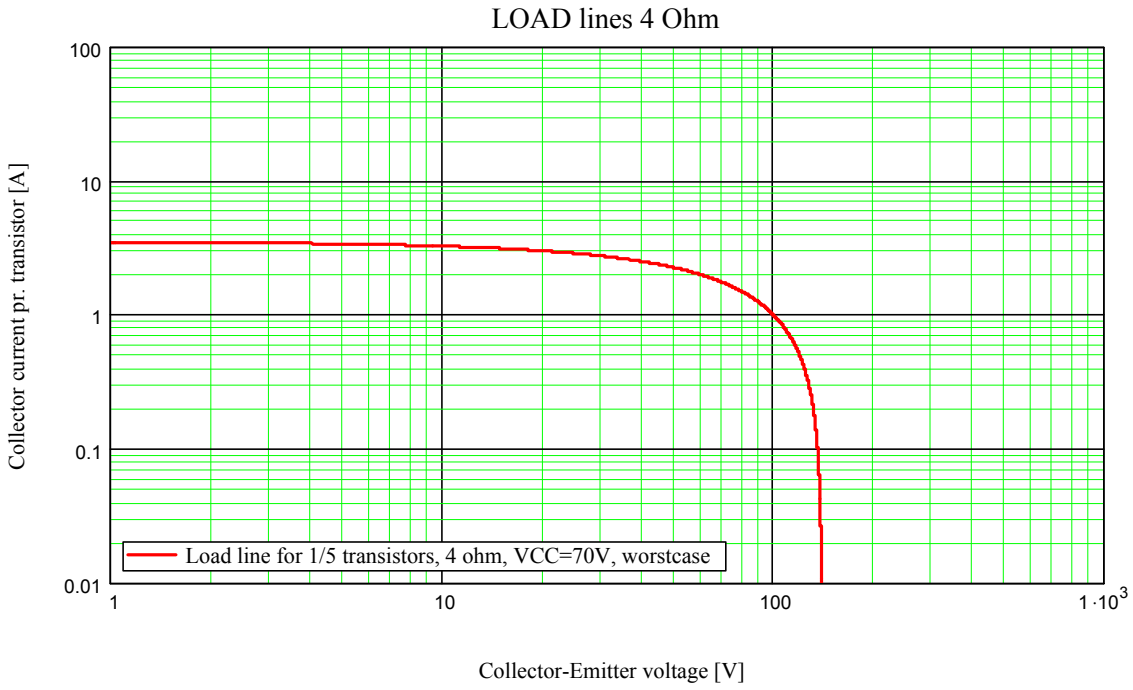


Figure 4-3 Worst-case 4 ohm load line for 1 of 5 parallel transistors double logarithmic

The relevance of worst-case line can of cause be discussed, I choose to use it, and accept a smaller safety margin when looking at the SOA and load line in the same graph.
While evaluating the graphs one must also remember that the rail voltage will be subject to a degree of load dependent regulation that will influence the working conditions for the output devise. This means that the long-term conditions for the power transistors need to be tested with the power supply that is going to be used in the specific amplifier.

Things like the amount of capacitance and V/A rating of the transformer are important parameters in the PSU that will have a direct impact on the operating area of the output transistors.

4.1.3 Temperature derating the SOA

Temperature derating is the process where the designer must make sure that the output stage will survive the load while working at a give temperature. Most amps have a maximum ambient working temperature provided in their datasheet e.g. 50 ^{o}C. This temperature is closely related to the working conditions and SOA of the output stage, and other temperature dependent components in the amplifier.

The output transistors typically have a power rating curve like the one in Figure 4-4. It shows that the maximum allowed power dissipation at a case temperature of 87.5 degrees C is roughly 115W or half of the power rating at a case temperature of 25 degrees C.

With the knowledge of the curve the designer must decide what case temperature the output stage is going to be allowed to have, and find the corresponding maximum power level. The decisions made will influence the size of heatsinks needed, but I will return to the subject of heatsinks later on.

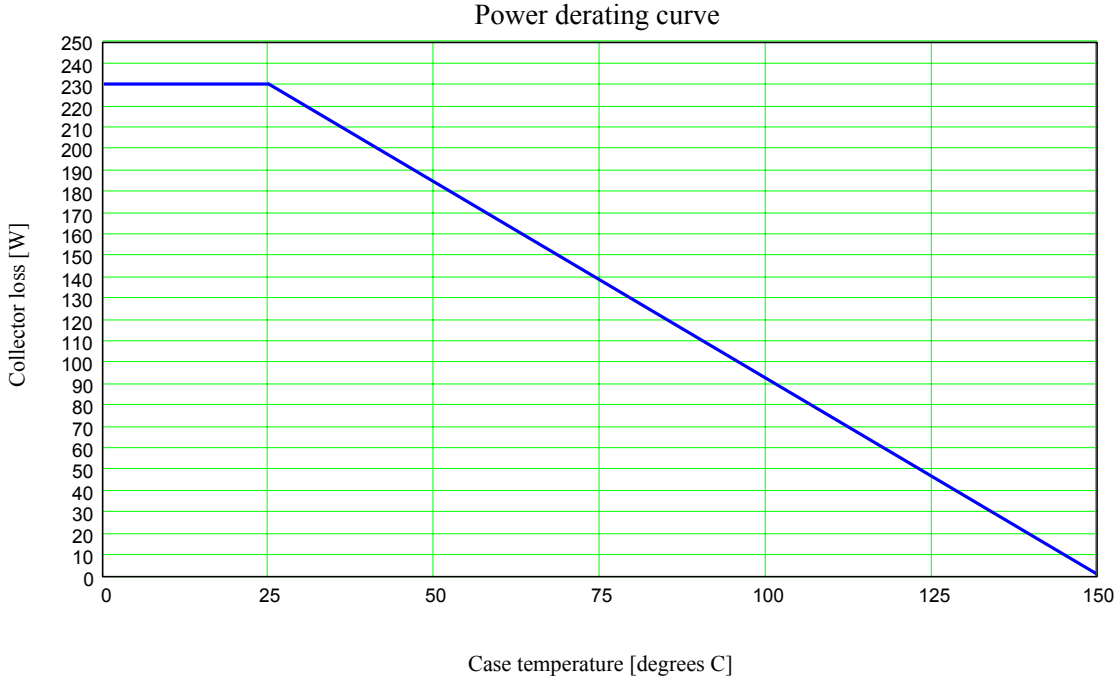


Figure 4-4 Power derating for the MJL4281A/MJL4302A pair

In Figure 4-5 the normalized power dissipation is shown, to use the graph, simply multiply the SOA current with the number on the Y-axis that corresponds to a given case temperature.

I choose to have a maximum case temperature of about 90 degrees C, and therefore I can allow a maximum dissipation of 90W. This is 0.45 times the power allowed at 25 degrees C, so if the SOA current is divided by two (multiplied by 0.4 from Figure 4-5) the temperature compensated SOA curve can be used to evaluate the operating area for the output stage with different loads.

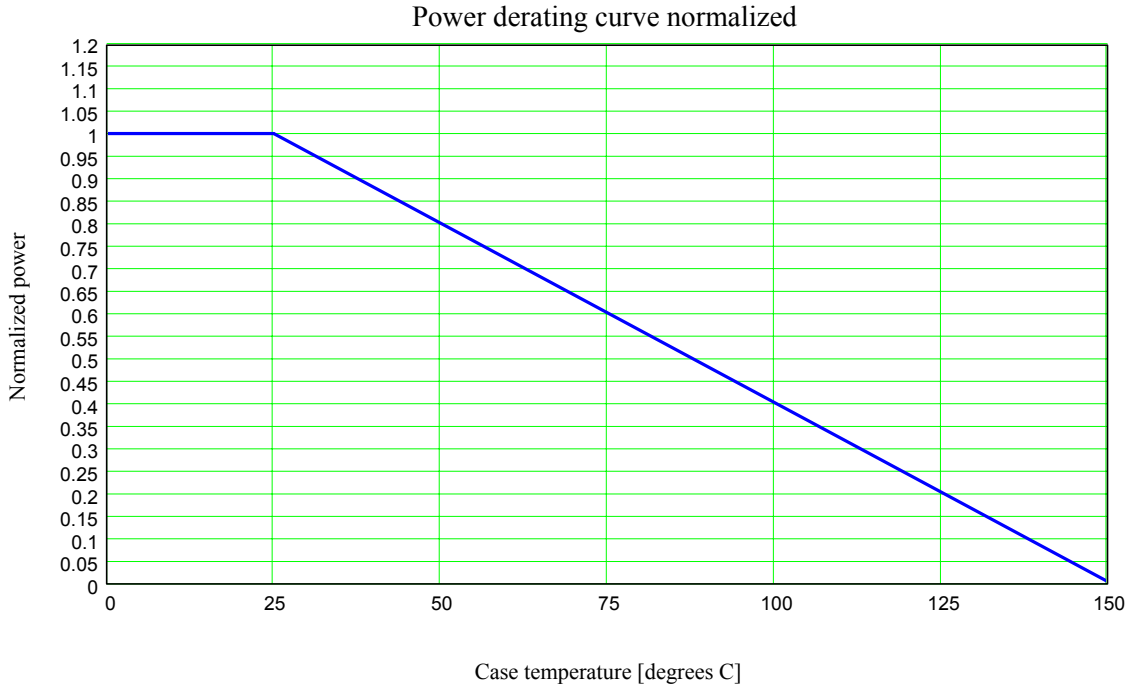


Figure 4-5: Normalized power dissipation vs. junction temperature, MJL4281A/MJL4302A pair

4.2 Returning to the SOA curves

The SOA is depending on the temperature of the case temperature of the devise, but in the datasheets only a few graphs are shown, and it is (almost) always necessary to use the derating guideline described in section 4.1.3.

Figure 4-6 shows two of three provided curves from the MJL4281A/MJL4302A datasheet. The red is a 10 ms curve, and the blue is the 1 s curve.

Since music is varying in level and rarely a pure DC voltage, it can be allowed to use the 10 ms SOA curve as reference when plotting the load line. It is however necessary to perform some temperature derating.

In Figure 4-7 the red line is the 10 ms SOA curve that has been derated for a case temperature of 100 degrees (More than the 90 degrees needed). Comparing with the blue 1 s SOA curve, it is obvious that the blue line is the more conservative one in the area where the load line has the most chance of intercepting the SOA curve. This is the reason that I will use the 1 second SOA curves in the following comparison between the different output transistors.

I'm sure other conclusions can be drawn from the derating exercise, but this is the reasoning that I have used successfully until now, if I ever encounter problems I will have to revaluate the situation.

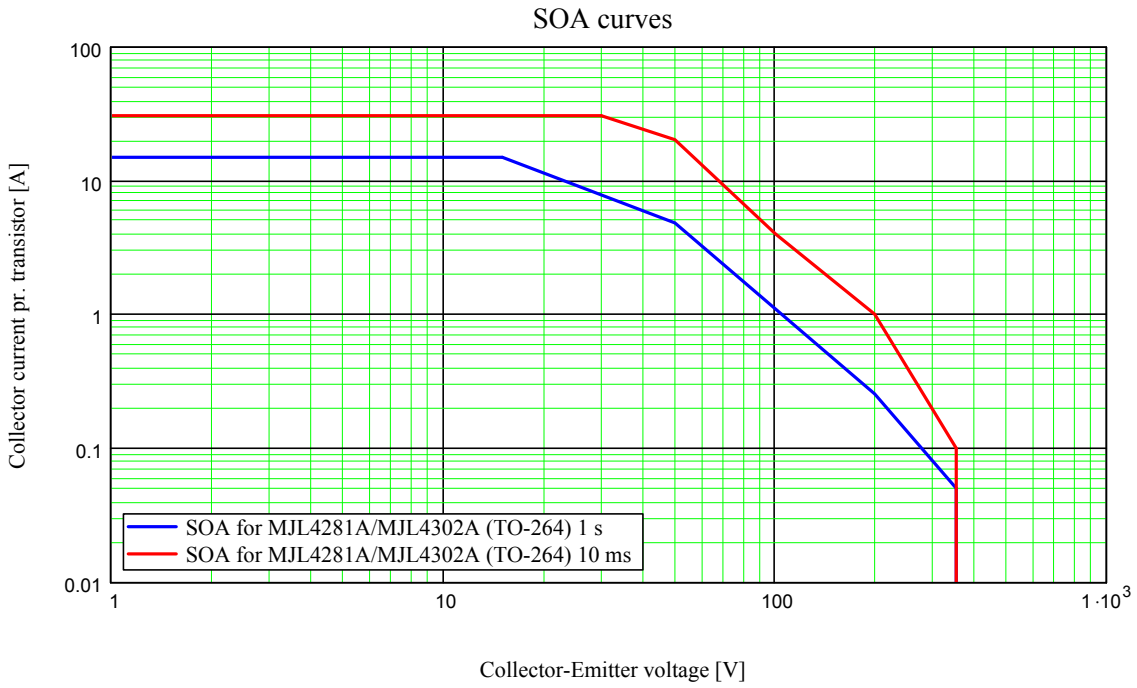


Figure 4-6 SOA curves for the MJL4281A/MJL4302A pair case temperature = 25 degrees C

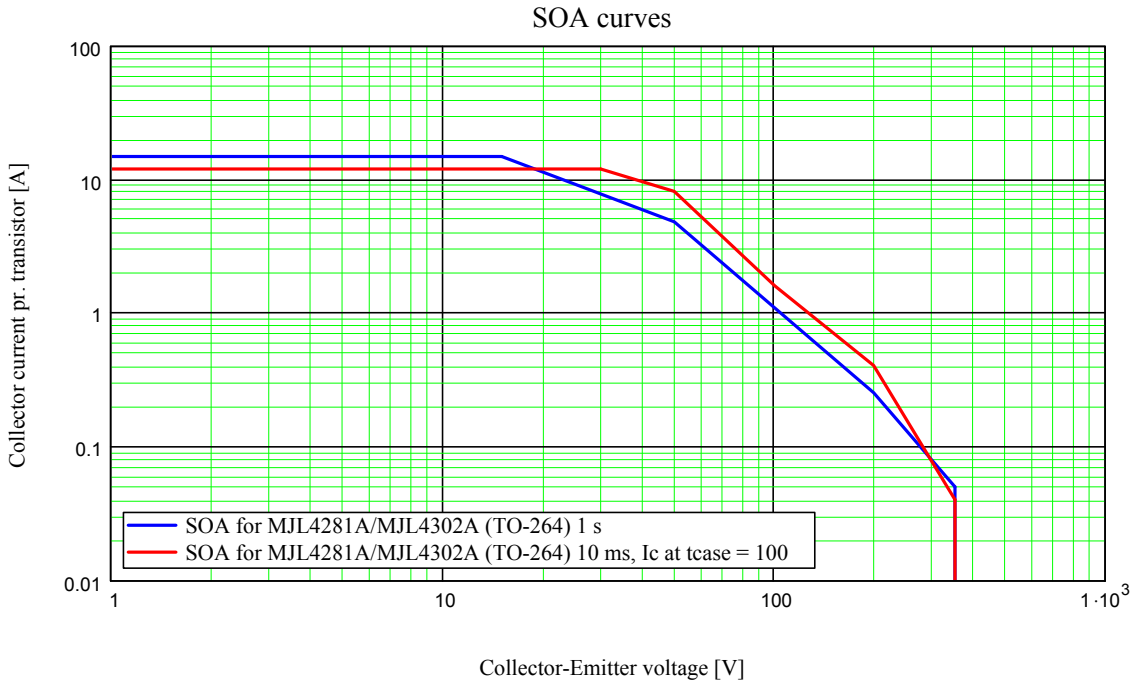


Figure 4-7 SOA curves showing the temperature derated 10 ms curve and the 1 s curve

4.3 Calculating the power loss in the output stage

When does the output stage get hottest, and how much power is then dissipated? In order to find out it is necessary understand how the power is dissipated.

In section 4.1.2 it was assumed that the load could be 100% reactive. This is of course not the case as any loudspeaker will have both a resistive and reactive part. The resistive part is

constant with varying frequency (and neglecting temperature affects to the cobber), but the reactive part will change from inductive to capacitive depending on the type of speaker, and the frequency. In the following I will look at three cases of load

- The purely resistive load
- 45 degree lacking (inductive) load
- 45 degree leading (capacitive) load

4.3.1 The Purely resistive load

To make things easy to start with, let's assume that the amplifier sees a purely resistive load and examine how much power is lost when the output voltage is a sine wave.

$$P = V_{CE} \cdot I_C = \left(V_{CC} - V_{out}\right) \cdot \frac{V_{out}}{R_L \cdot N}$$

$$V_{out}(t) = A \cdot \sin(2\pi \cdot F \cdot t)$$

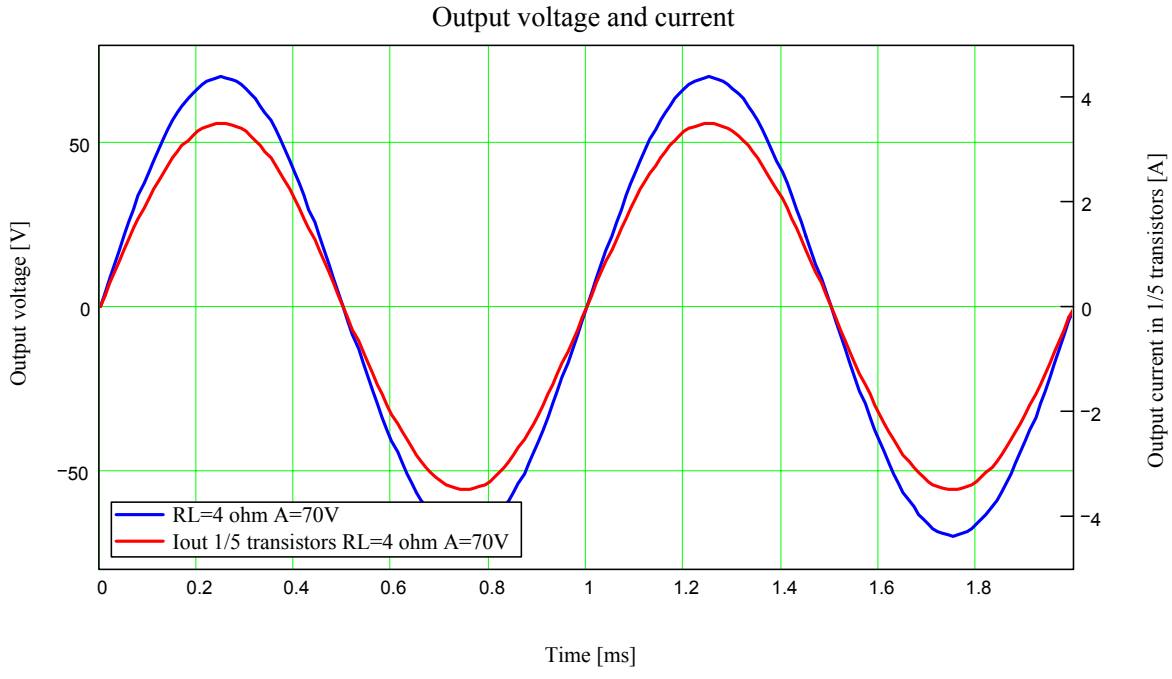
$$I(t) = \frac{V_{out}(t)}{R_L \cdot N}$$

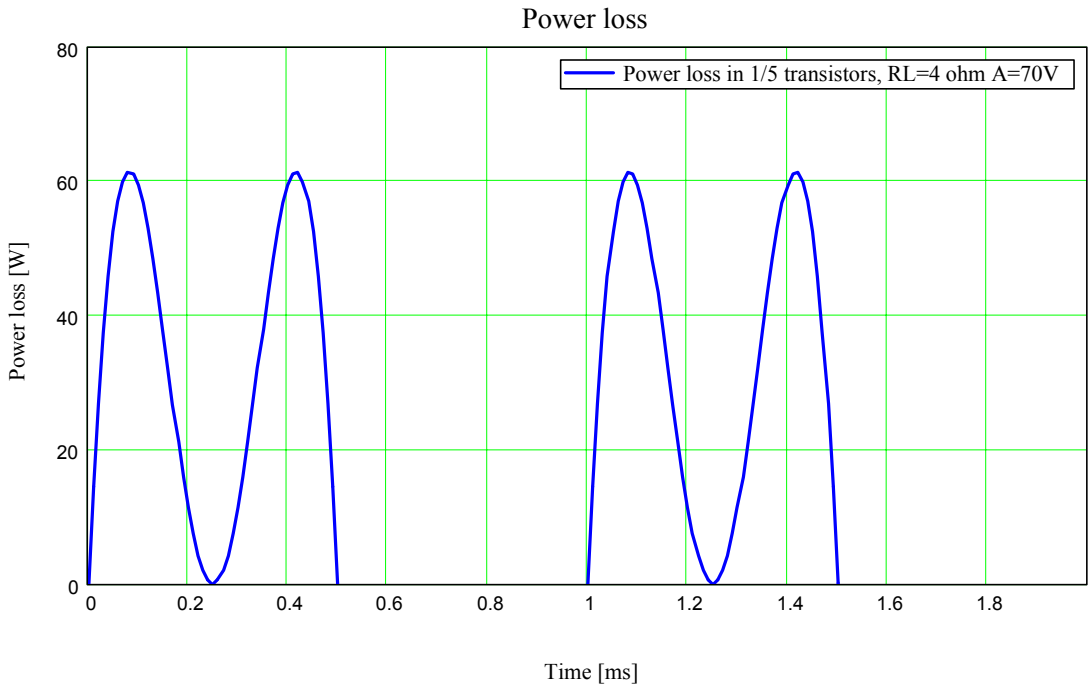
$$P(t) = \left(V_{CC} - V_{out}(t)\right) \cdot I(t)$$

The period of the sine wave is T and F is 1000 [hz]

$$T = \frac{1}{F}$$

I have assumed that there is no emitter resistor in on the output transistors (And therefore no voltage drop across this resistor), and that the output level in fact can reach the rail voltage V_{CC}. This is not the case for the Leach output stage topology, but other designs may offer this feature. The output amplitude A can be anywhere from 0 to V_{CC}.





The average power loss during 1 cycle in one transistor is (assuming no idle current):

$$P_{avg} = \frac{1}{T}\cdot\int_0^{\frac{T}{2}} P(t)\,dt = \frac{1}{T}\cdot\int_0^{\frac{T}{2}} \left(V_{CC} - A\cdot\sin\left(2\cdot\pi\cdot\frac{1}{T}\cdot t\right)\right)\cdot\frac{A\cdot\sin\left(2\cdot\pi\cdot\frac{1}{T}\cdot t\right)}{R_L\cdot N}\,dt$$

This simplifies to:

$$P_{avg} = \frac{A\cdot\left(4\cdot V_{CC} - A\cdot\pi\right)}{4\cdot\pi\cdot R_L\cdot N}$$

To find the output level where the power loss is the greatest, the expression is differentiated with respect to “A” and the result is set to equal 0 in order to find the maximum.

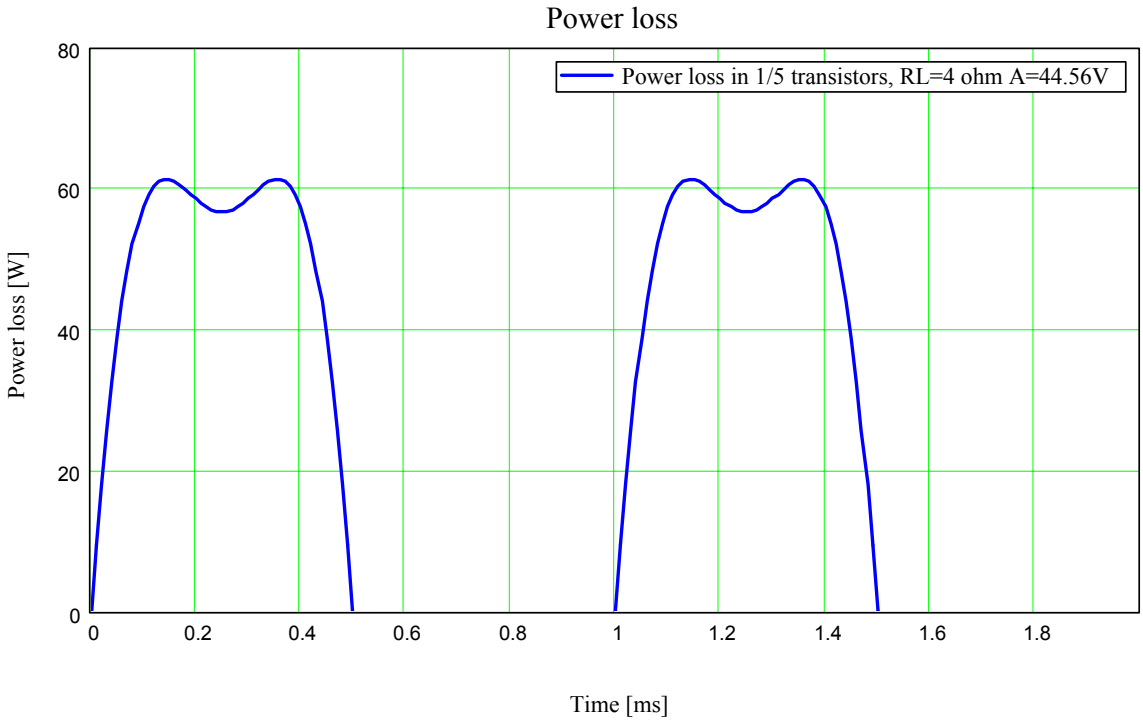
$$\frac{1}{4}\cdot\frac{4\cdot V_{CC} - A\cdot\pi}{\pi\cdot R_L\cdot N} - \frac{1}{4}\cdot\frac{A}{R_L\cdot N} = 0$$

This solves to:

$$A = \frac{2}{\pi}\cdot V_{CC} = 0.637\cdot V_{CC}$$

So at $A=0.637*V_{CC}$ the average power loss is maximum.

Next drawing is a new power graph with $A=0.637*V_{CC}= 44.56V$



The maximum average power is:

$$P_{avg} = \frac{A\cdot\left(4\cdot V_{CC} - A\cdot\pi\right)}{4\cdot\pi\cdot R_L\cdot N} = \frac{44.56\cdot(4\cdot 70 - 44.56\cdot\pi)}{4\cdot\pi\cdot 4\cdot 5} = 24.824 \quad [W]$$

Equation 4-1

This is the power in one transistor, but since there are 2 x 5 in parallel (5 NPN and 5 PNP) the total heating power is:

$$P_{total} = 2\cdot N\cdot P_{avg} = 2\cdot N\cdot\frac{A\cdot\left(4\cdot V_{CC} - A\cdot\pi\right)}{4\cdot\pi\cdot R_L\cdot N} = \frac{A\cdot\left(4\cdot V_{CC} - A\cdot\pi\right)}{2\cdot\pi\cdot R_L} = 248.2 \quad [W]$$

Equation 4-2 Total heating power

This power can be used to calculate the temperature of the transistor junction, case and heatsink temperature.

4.3.2 Finding the junction, case and heatsink temperature

Before proceeding with temperature calculations it's important to select a heatsink that will work well in a high power application such as this one. Because I have chosen to use flat pack transistors, I need an extrusion that has a large flat rear plate. I have selected the KL-271 extrusion from seifert-electronic in Germany in 150 mm length.

From Figure 4-9 the thermal resistance from heatsink to ambient (Rth_{ha}) can be found to be 0.11 [^{o}C/W]. Next the thermal resistance between the case and heatsink is needed.

According to (III) the thermal resistance between transistor-case and heatsink (Rth_{ch}) is about 0.5 [°C/W] if silicone insulators are used. I favour these over any other means of insulation because they are completely un-messy, and provide a most excellent thermal coupling.

Finally we need the thermal resistance between transistor junction and case (Rth_{jc}) this is found in the transistor datasheet. I will use the data for the MJL4281A/4302A pair of 0.54 [°C/W].

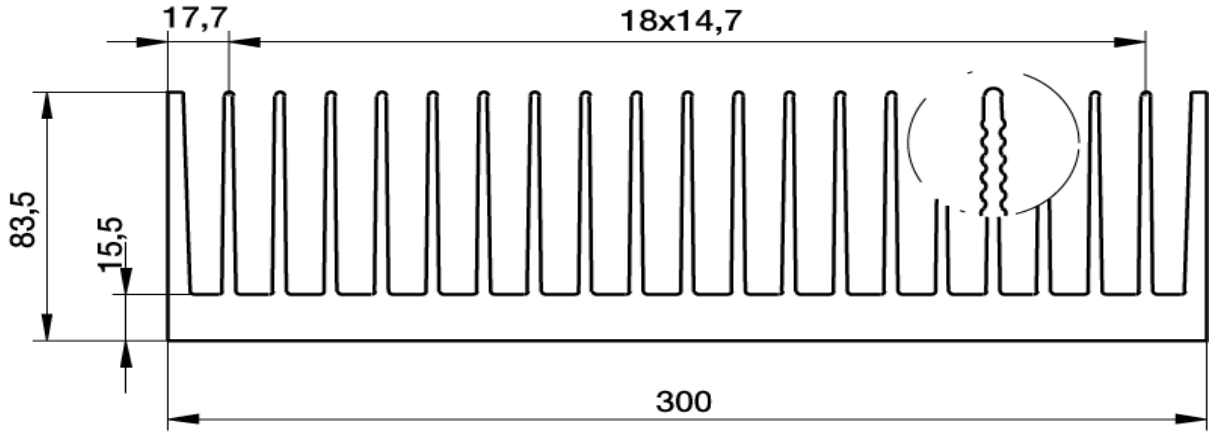


Figure 4-8 Heatsink drawing of the KL-271 extrusion

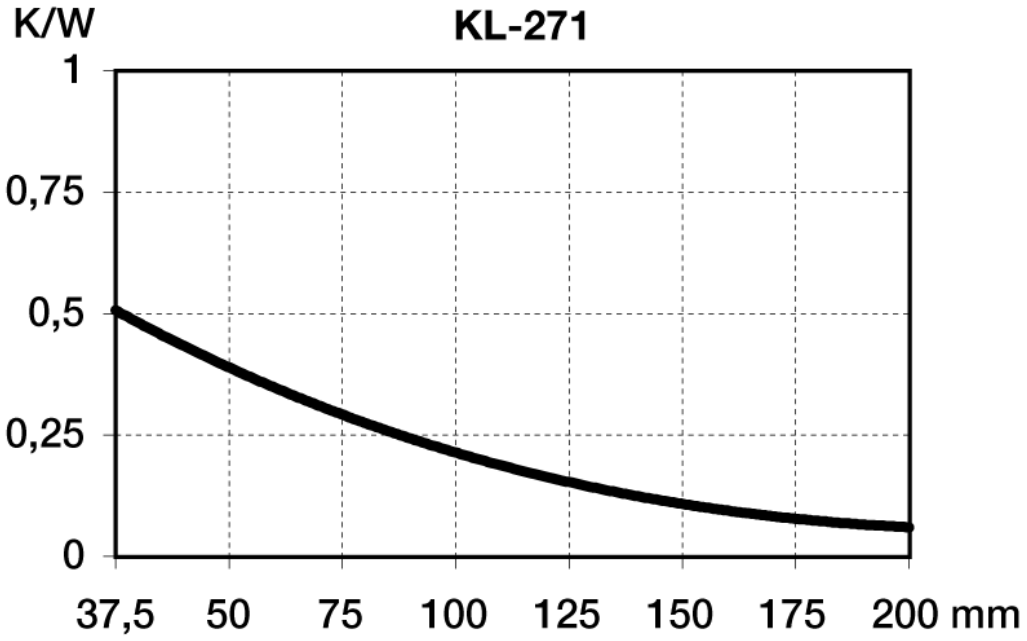


Figure 4-9 Thermal resistance vs. Extrusion length

Let's take a look at the thermal system of the 10 transistor version to understand the behaviour of temperatures inside an amplifier. Figure 4-10 shows the thermal model of the 10 transistor amplifier, which can be used to derive thermal equations that can aid in the creation of expressions for calculating junction, case and heatsink temperature.

III High-Power Audio Amplifier Construction Manual, ISBN 0-07-134119-6 , G.Randy Slone, p 361

Starting from the left there is a number of power sources that heat the transistors and thus the heatsink. Each power source is the loss in an output transistor, since there are 10 transistors the power sources are numbered from 1 to 10. In Equation 4-2 the total heating power was calculated as the sum of the dissipated power in all of the output devises, e.g. $P_1+P_2….P_{10}$. In the thermal model the power is represented as a current that flows through the thermal resistors creating a temperature (voltage) drop over each thermal resistor.

By means of the current law, it is easy to se that all thermal current runs through the thermal resistance from heatsink to ambient (Called Rth_{ha})

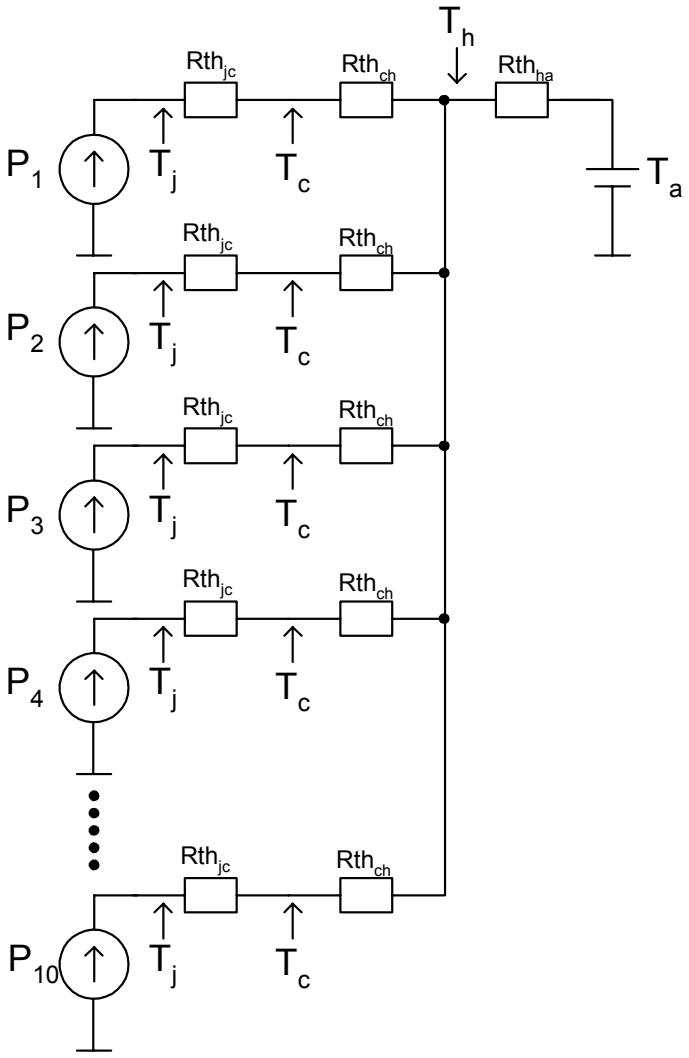


Figure 4-10 Thermal model of the 10 transistor amplifier´

This leads to the first of the thermal equations where the heatsink temperature (T_h) is calculated.

$$T_h = P_{total} \cdot Rth_{ha} + T_a$$

Next, the case temperature (T_c) can be found

$$T_c = T_h + P_{avg} \cdot Rth_{ch}$$

And finally the junction temperature (t_j) is found

$$T_j = T_c + P_{avg} \cdot Rth_{jc}$$

Now for some numbers:

$$T_h = P_{total} \cdot Rth_{ha} + T_a = 248.37 \cdot 0.11 + 25 = 52.3 \quad [^oC]$$

$$T_c = T_h + P_{avg} \cdot Rth_{ch} = 52.3 + 24.8 \cdot 0.5 = 64.7 \quad [^oC]$$

$$T_j = T_c + P_{avg} \cdot Rth_{jc} = 64.7 + 24.8 \cdot 0.54 = 78.1 \quad [^oC]$$

So the worst case temperature on the heatsink is about 53 [°C] at an ambient temperature of 25 [°C]. In summer conditions in Denmark the ambient temperature might climb as high as 35 [°C], this means that the case temperature is 75 [°C] maximum during worst case conditions.

According to (IV) it is ok to assume that music only will make ½ of the worst case dissipation in the output stage, so only about 125 [W] total will be dissipated when playing music. This will result in a heatsink temperature of about 48 [°C] at 35 [°C] ambient, while the case temperature on the transistors will be about 54[°C]. The allowed power dissipation in one transistor at 54 [°C] case temperature is about 175 [W] so it seems that there is plenty of margin.

4.3.3 45 degree lacking (inductive) load

4.3.4 45 degree leading (capacitive) load

IV http://www.sound.westhost.com/soa.htm

4.4 The 10 transistor version

4.4.1 Load line

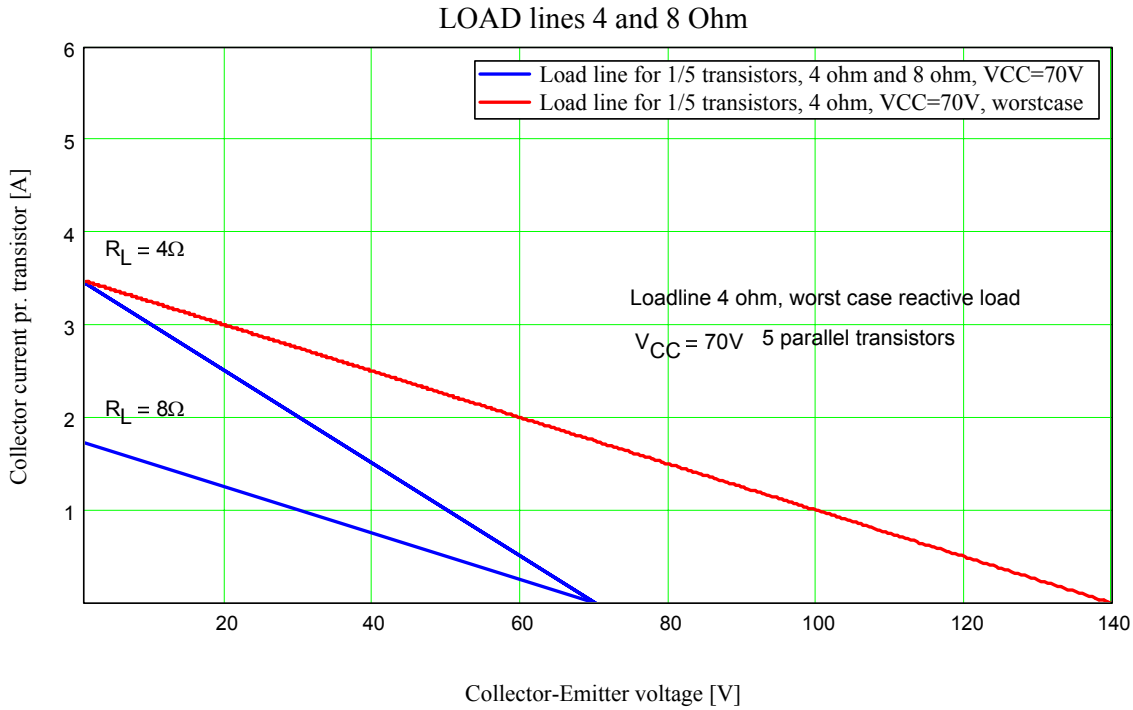


Figure 4-11

4.4.2 The MJ15024 (NPN) and MJ15025 (PNP) devises

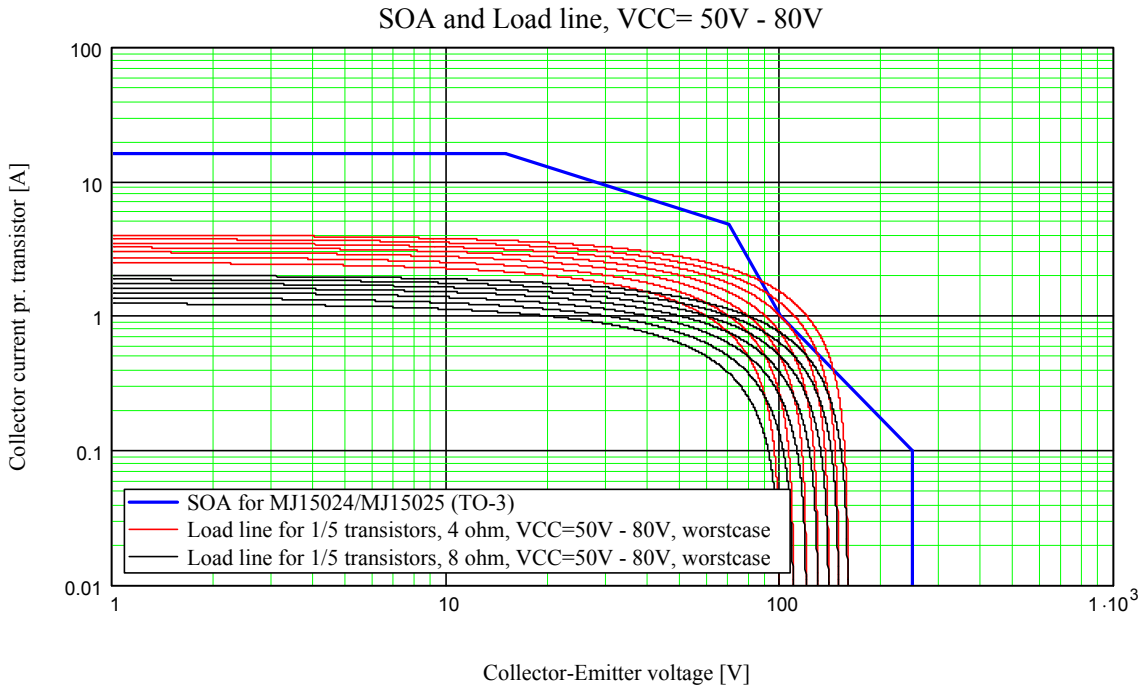


Figure 4-12

Five transistors in parallel of the MJ15025 / MJ15025 pair would work ok at +- 65V rails into 4 ohms and +-80V rails into 8 ohms. The transistors are relatively slow with an F_T of 4 MHz, so it is not my first choice of output devise.

4.4.3 The MJ15003 (NPN) and MJ15004 (PNP) devises

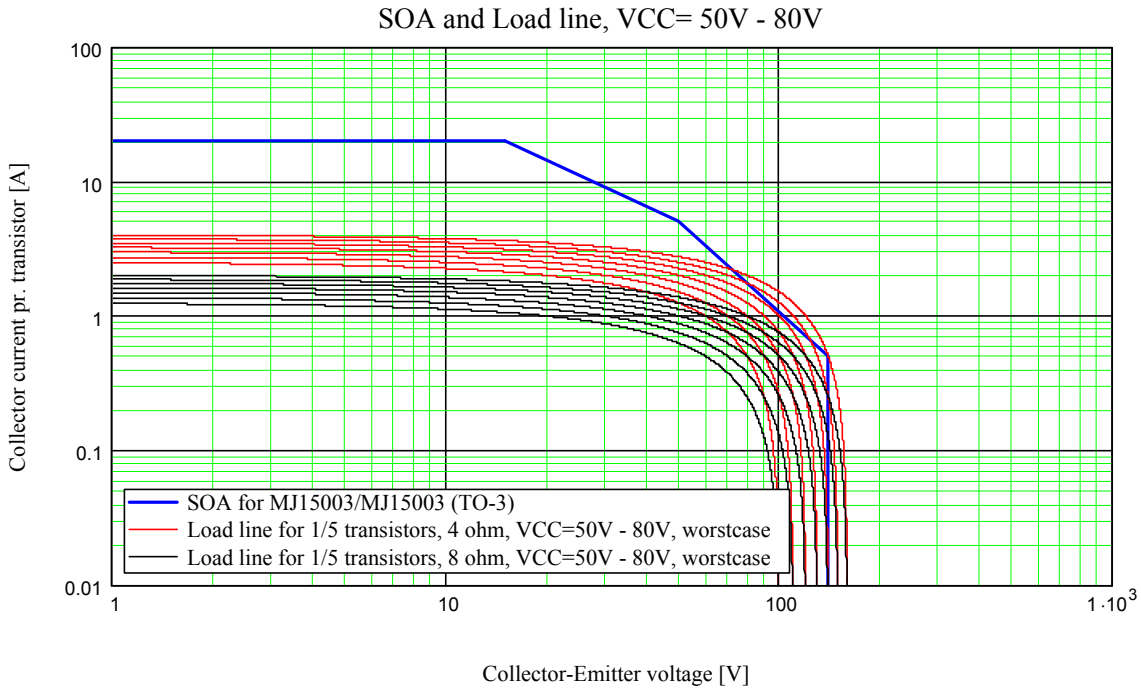


Figure 4-13

Five transistors in parallel of the MJ15003 / MJ15004 pair would work ok at +- 60V rails into 4 ohms and +-65V rails into 8 ohms. The transistors with an F_T of 2 MHz are even slower than the MJ15025 / MJ15025 pair so I would not use these devises at all as new parts are quicker and more rugged.'

The transistor have a low maximum CE voltage, that really means that the devise is unsuited for really high power output amplifiers that use the emitter follower output topology.

4.4.4 The MJ21194 (NPN) and MJ21193 (PNP) devises

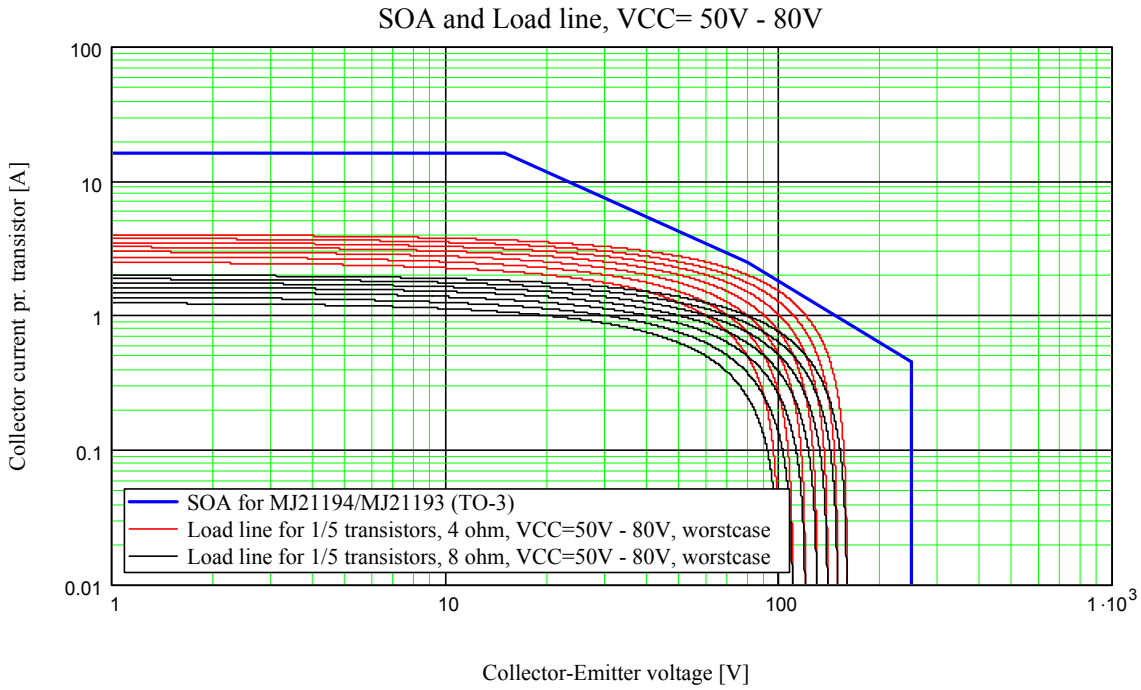


Figure 4-14

Five transistors in parallel of the MJ21194 / MJ21193 pair would work ok at +- 80V rails into 4 and 8 ohms if. The transistors with an F_T of 4 MHz are as slow as the MJ15025 / MJ15025 pair so I would not use these devises though they are very rugged.

4.4.5 The MJL21194 (NPN) and MJL21193 (PNP) devises

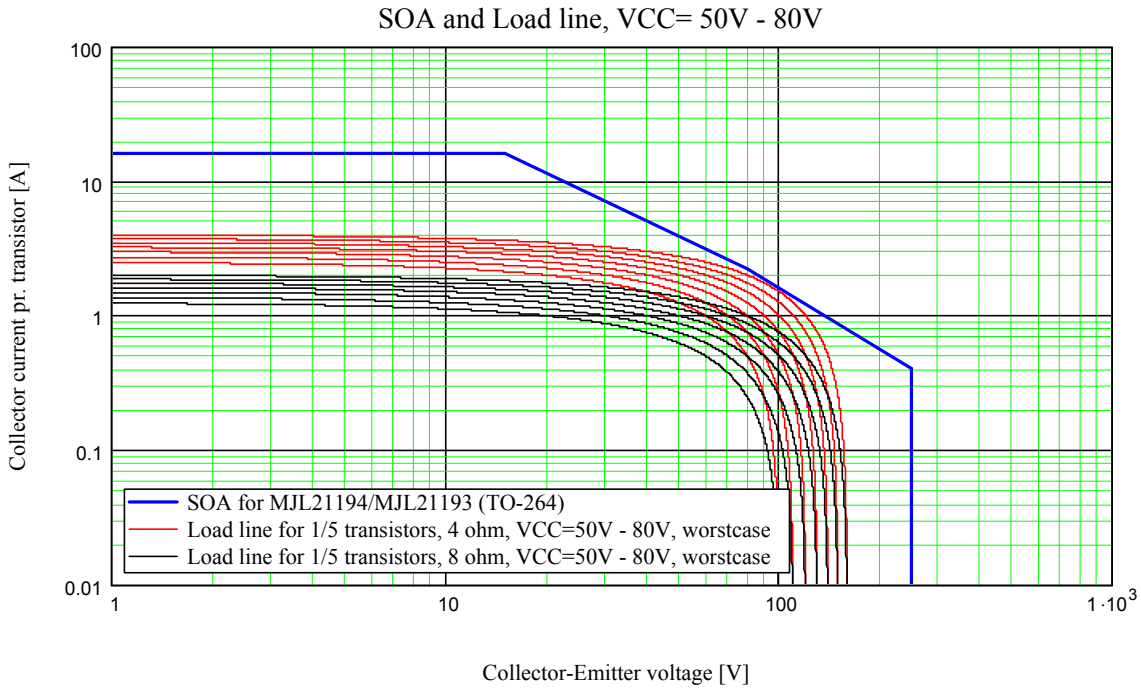


Figure 4-15

Five transistors in parallel of the MJL21194 / MJL21193 pair would work ok at +- 75V rails into 4 ohms and +-80V rails into 8 ohms. The transistors with an F_T of 4 MHz are as slow as the MJ21194 / MJ21193 pair, but because they are flat pack types I would consider using them for subwoofers and other applications where long-term power is needed.

I suggest this transistor for high power amplifiers (power between 200W-550W into 4 Ohm or up to 350W into 8 Ohm, but for subwoofers only, and remember only with 5 parallel sets)

4.4.6 The MJL3281A (NPN) and MJL1302A (PNP) devises

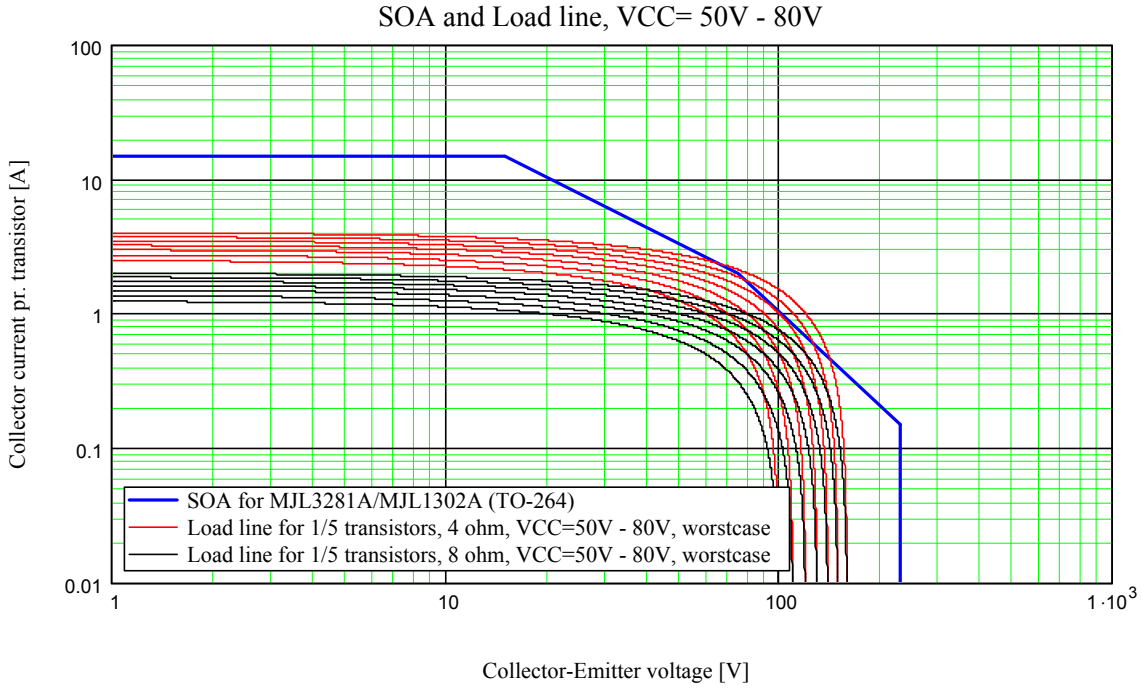


Figure 4-16

Five transistors in parallel of the MJL3281A / MJL1302A pair would work ok at +- 65V rails into 4 ohms and +-80V rails into 8 ohms. The transistors with an F_T of 30 MHz are much faster than any of the TO-3 types examined in this document. I would consider using them for full range amplifiers, but I would not use the devise for a subwoofer or other applications where high long-term power is needed.

I suggest this transistor for medium power full range amplifiers (power between 200W-450W into 4 Ohm or below 350W into 8 Ohm with 5 parallel sets)

4.4.7 The MJL4281A (NPN) and MJL4302A (PNP) devises

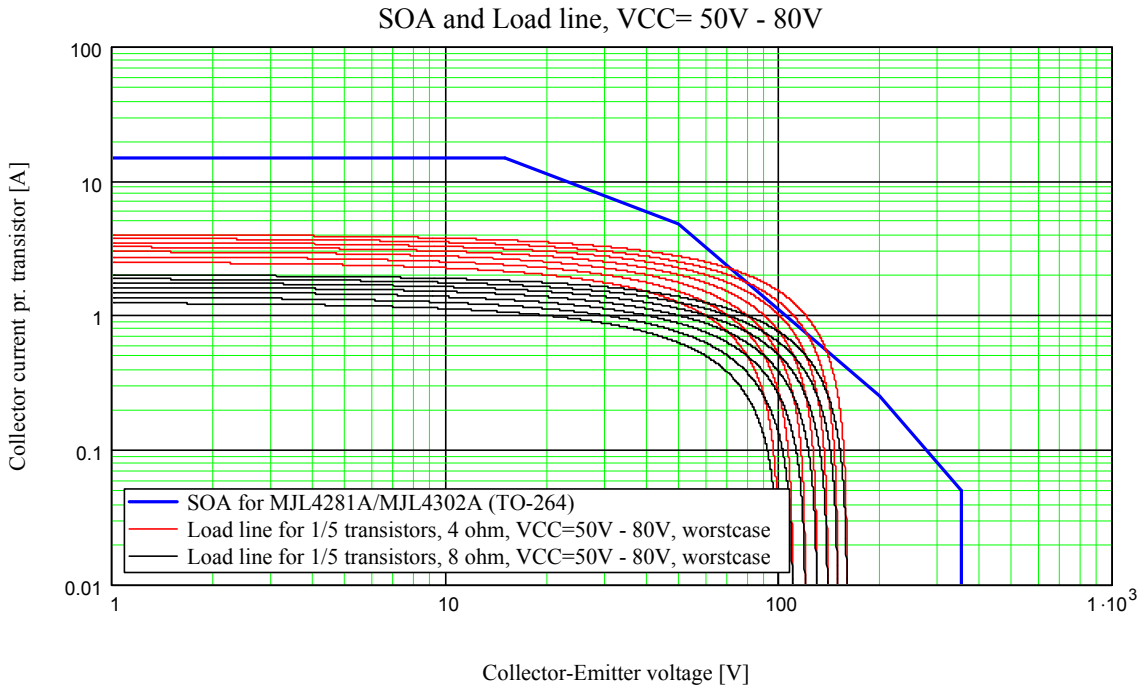


Figure 4-17

Five transistors in parallel of the MJL4281A / MJL4302A pair would work ok at +- 70 V rails into 4 ohms and +-80V rails into 8 ohms. The transistors with an F_T of 35 MHz are faster than any of the transistor types examined in this document. I would consider using them for full range amplifiers, but I would not use the devise for a subwoofer or other applications where high long-term power is needed.

I suggest this transistor for medium power full range amplifiers (power between 200W-450W into 4 Ohm or below 350W into 8 Ohm with 5 parallel sets)

4.5 The 6 transistor version

4.5.1 Load line

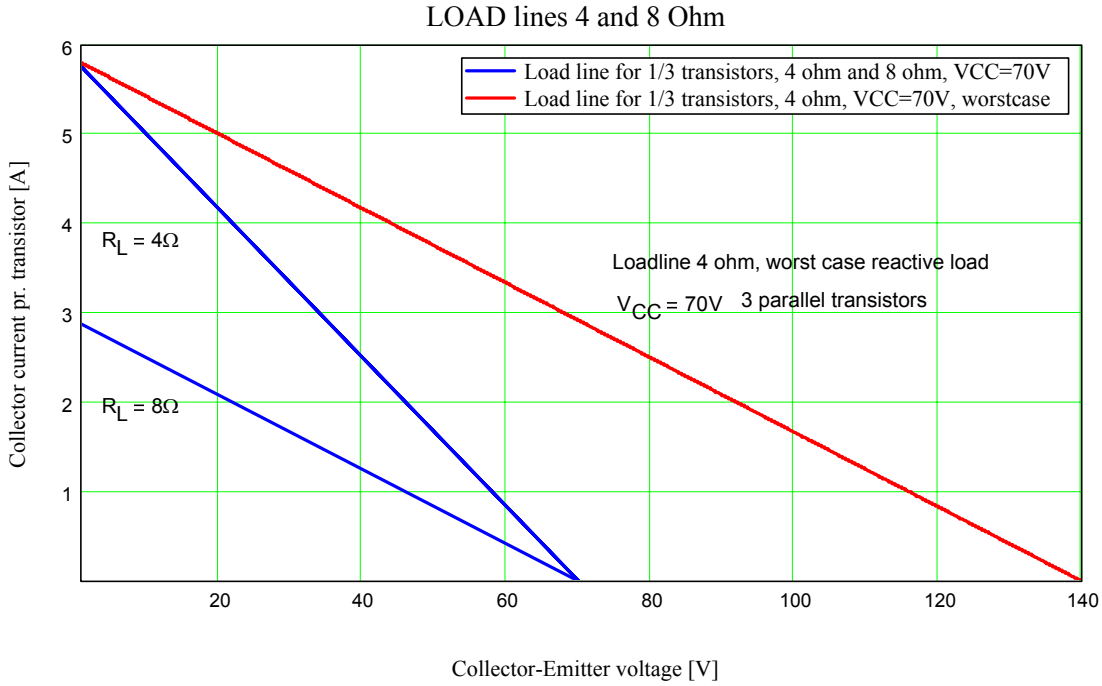


Figure 4-18 Load lines

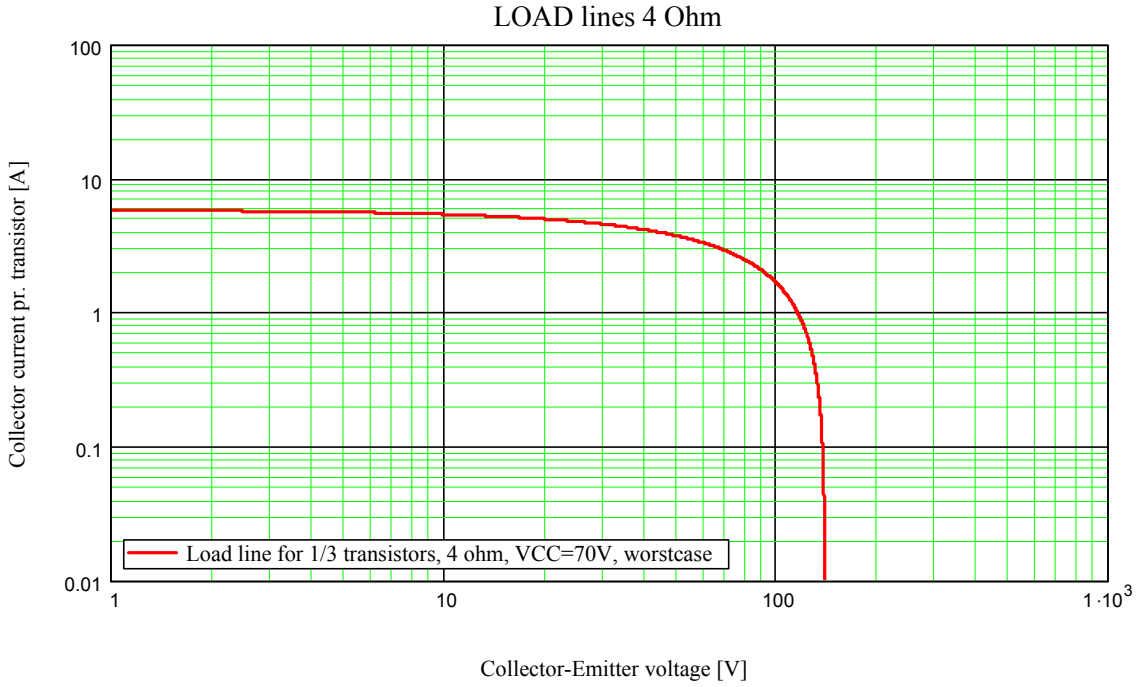


Figure 4-19 Worst-case load line for 1 of 3 parallel transistors

4.5.2 The MJ15024 (NPN) and MJ15025 (PNP) devises

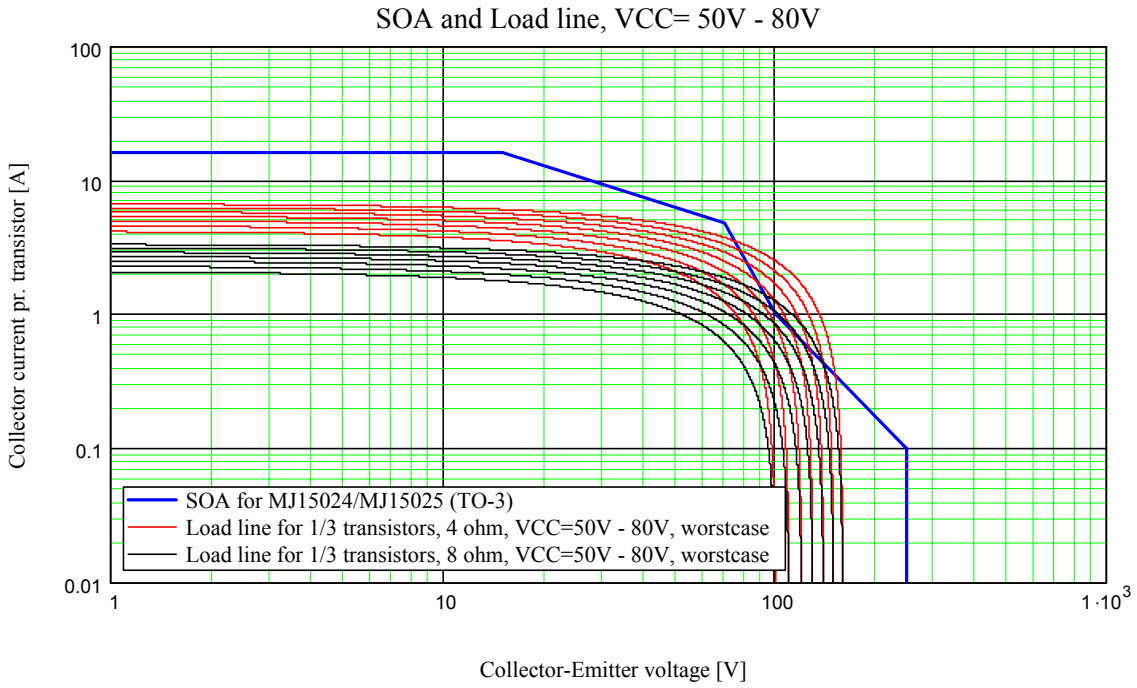


Figure 4-20

Three transistors in parallel of the MJ15025 / MJ15025 pair would work ok at +- 60V rails into 4 ohms and +-70V rails into 8 ohms.

4.5.3 The MJ15003 (NPN) and MJ15004 (PNP) devises

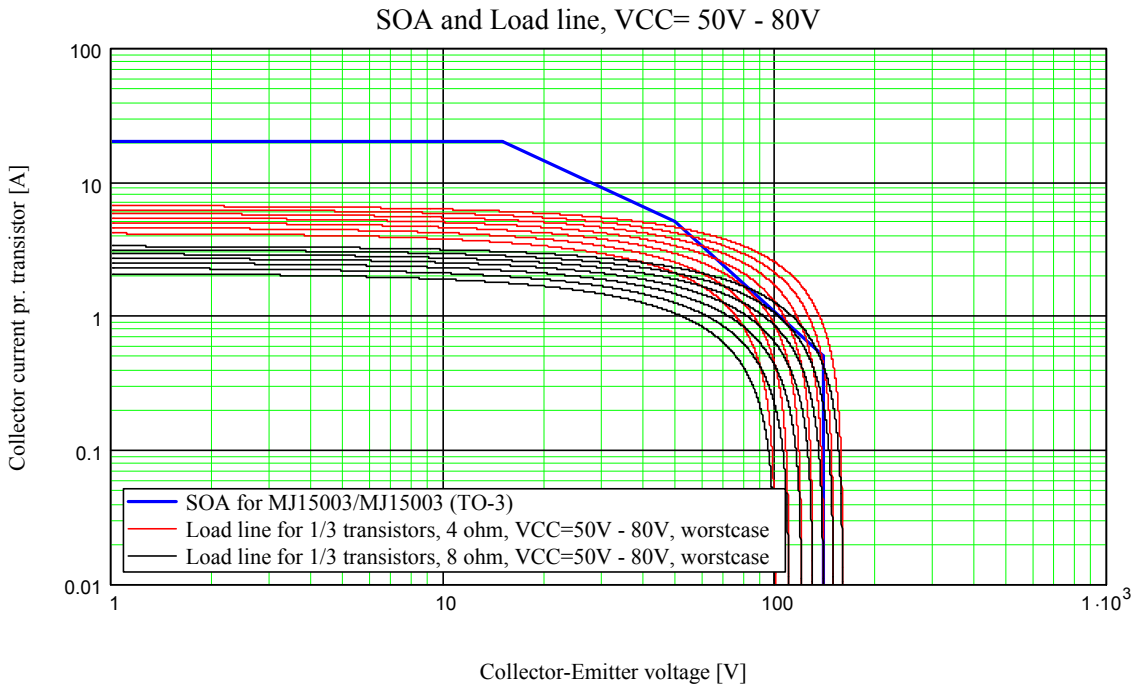


Figure 4-21

Three transistors in parallel of the MJ15003 / MJ15004 pair would work ok at +- 60V rails into 4 ohms and +-65V rails into 8 ohms.

4.5.4 The MJ21194 (NPN) and MJ21193 (PNP) devises

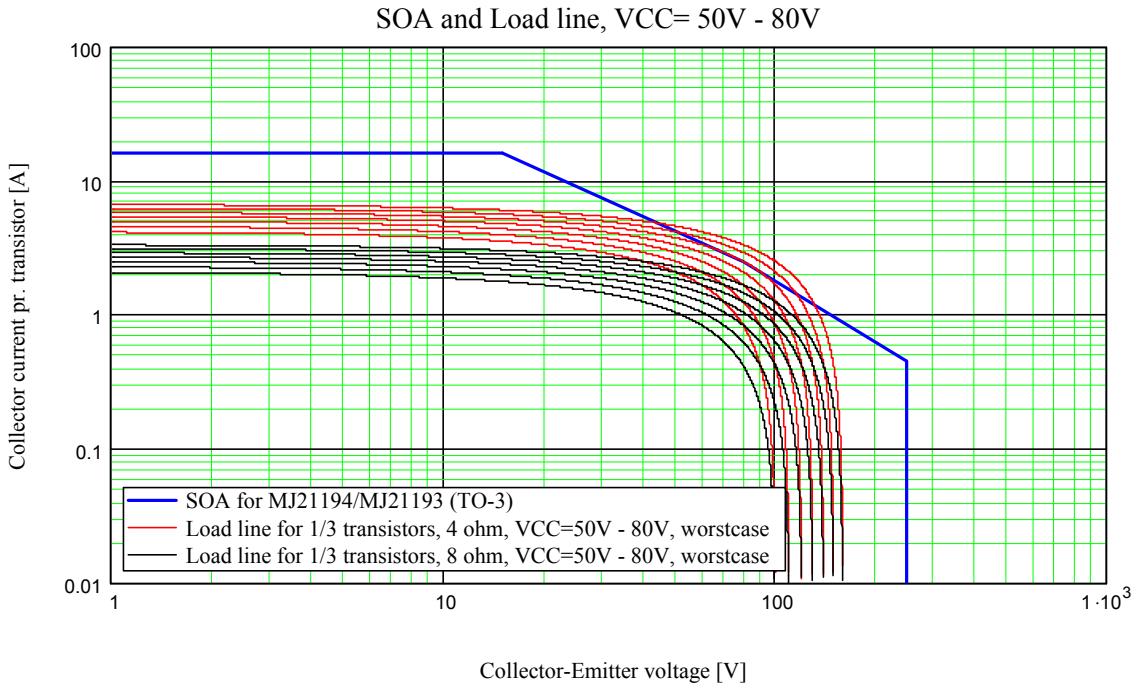


Figure 4-22

Three transistors in parallel of the MJ21194 / MJ21193 pair would work ok at +- 65V rails into 4 and +- 80V into 8 ohms.

4.5.5 The MJL21194 (NPN) and MJL21193 (PNP) devises

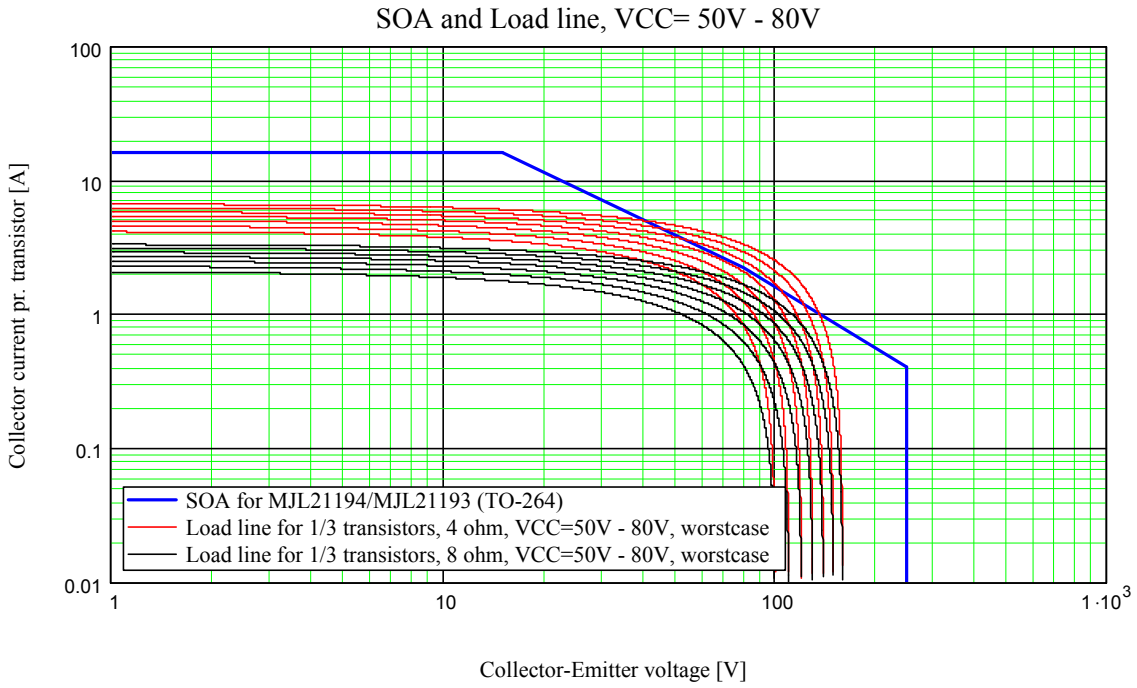


Figure 4-23

Three transistors in parallel of the MJL21194 / MJL21193 pair would work ok at +- 60V rails into 4 ohms and +-80V rails into 8 ohms.

4.5.6 The MJL3281A (NPN) and MJL1302A (PNP) devises

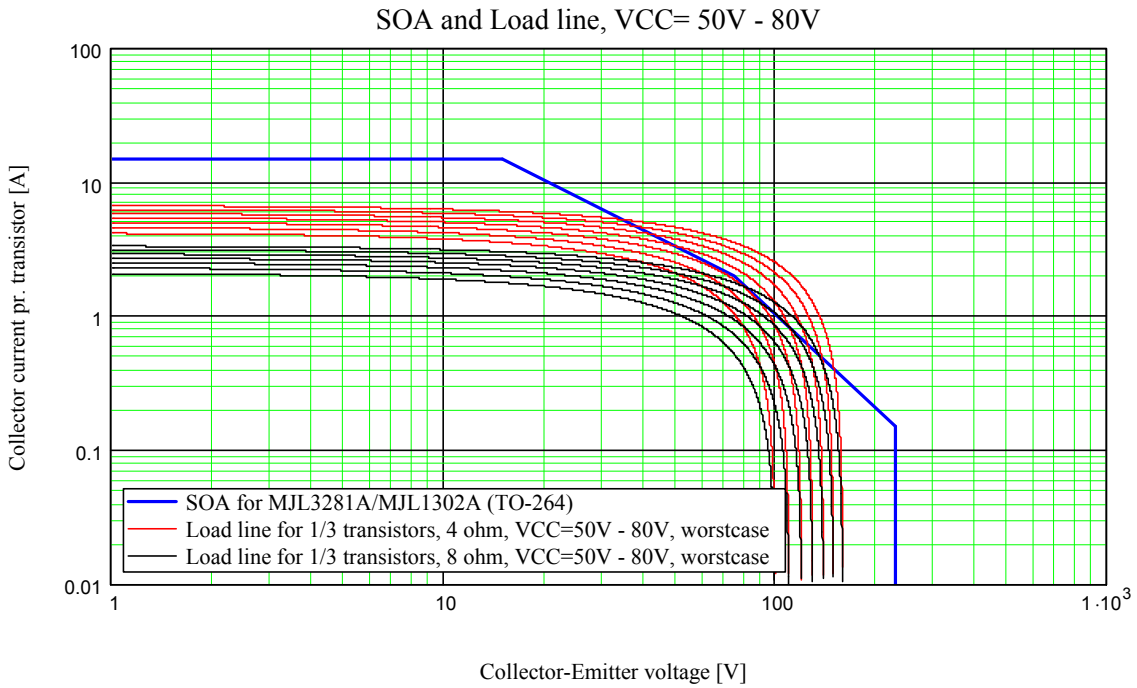


Figure 4-24

Three transistors in parallel of the MJL3281A / MJL1302A pair would work ok at +- 60V rails into 4 ohms and +-70V rails into 8 ohms.

4.5.7 The MJL4281A (NPN) and MJL4302A (PNP) devises

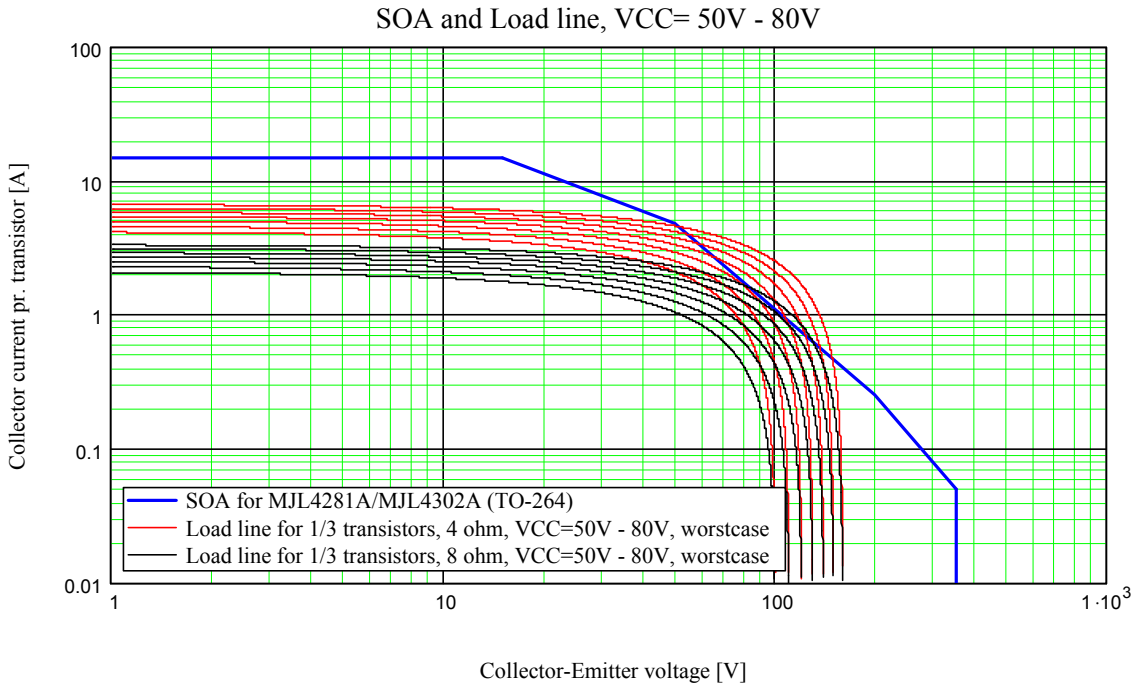


Figure 4-25

Three transistors in parallel of the MJL4281A / MJL4302A pair would work ok at +- 60 V rails into 4 ohms and +-70V rails into 8 ohms if 5 pairs are used in parallel.

4.6 Output stage summary

	MJ15024 (NPN) MJ15025 (PNP)	MJ15003 (NPN) MJ15004 (PNP)	MJ21194 (NPN) MJ21193 (PNP)	MJL21194 (NPN) MJL21193 (PNP)	MJ21196 (NPN) MJ21195 (PNP)	MJL21196 (NPN) MJL21195 (PNP)	MJL3281A (NPN) MJL302A (PNP)	MJL4281A (NPN) MJL4302A (PNP)
Package	TO-3	TO-3	TO-3	TO-264	TO-3	TO-264	TO-264	TO-264
5 parallel 4 ohm rails	+-65V	+-60V	+-80V	+-75V			+-65V	+-70V
5 parallel 8 ohm rails	+-80V	+-65V	+-80V	+-80V			+-80V	+-80V
3 parallel 4 ohm rails	+-60V	+-60V	+-65V	+-60V			+-60V	+-60V
3 parallel 8 ohm rails	+-70V	+-65V	+-80V	+-80V			+-70V	+-70V

5 Assembly guide

Get your tools and soldering iron out and get ready to build an amp.

From the left there is a cutter, and two different component pliers. The funny looking thing in the top of the picture is use to remove solder if a component needs replacement.