Revision Guide for AMD Family 10h Processors

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Advanced Micro Devices

Revision History

Date	Revision	Description
June 2009	3.50	Added HY-D0, Fr6 package and Six-Core AMD Opteron™ Processor information in Overview, Tables 3, 6, 8 and 12-15; Added DA-C2, and AMD Athlon™ II X2 Processor information in Overview, Tables 5 and 10-15; Updated Tables 4 and 11; Updated erratum #372 in Table 14; Updated Suggested Workaround in erratum #389; Added errata #373, #374, #384-#386, #388 and #395.
April 2009	3.46	Updated Programming and Displaying the Processor Name String; Updated Table 11; Added Fr5 (1207) package processors to Tables 2, 8-9 and 15; Updated Table 14 for errata #344 and #354 due to Fr5 (1207) processors; Updated erratum #337; Clarified erratum #382; Added errata #387, #389, #391 and #393.
February 2009	3.40	Added AMD Phenom™ II X3 Processor brand information in Overview, Tables 5, 10 and 14; Updated Table 10; Corrected Table 15; Added AM3 package information to Tables 5, 10 and 11; Corrected Description in erratum #244 without change to application of Suggested Workaround; Added errata #344, #354, #372, #378-#379, #382.
January 2009	3.38	Added AMD Phenom™ II X4 Processor brand information in Overview, Tables 4, 10, 11 and 14.
November 2008	3.34	Split Table 1 into Tables 1-2 for clarity; Corrected Table 1; Added AMD Athlon™ brand information in Overview, Tables 2, 10, 11 and 14; Added RB-C2 information to Tables 1, 6, 12 and 13; Updated Mixed Silicon Support; Clarify use of package terms in Tables 8-11 and add note to Table 8; Clarified revision information in Table 12; Corrected Table 14; Clarified workaround requirements for erratum #263 and #293; Updated Suggested Workaround for erratum #351; Added errata #327, #343, #346, #348, #350, #359-#362, and #370.
September 2008	3.28	Added Conventions and updated MSR register usage and CPUID functions throughout; Added DR-B3 to Table 1, Table 6 and Table 13; Updated brand information in Overview, Table 1, Table 8, Table 9, Table 10, Table 11 and Table 14; Simplified MSRC001_0140 OS Visible Work-around MSR0 (OSVW_ID_Length) and removed Table 8: OSVW_ID_Length Per Processor Revision; Added Table 12: Cross Reference of Product Revision to OSVW ID; Renumbered tables appropriately; Added #322, #326, #328, #336-#339, #342, #351-#353, #355; Updated Description and Suggested Workaround in erratum #263 and #293; Updated Fix Planned in erratum #312 and updated Table 13 for erratum #312; Corrected Description, Potential Effect on System and Suggested Workaround in erratum #319; Updated Documentation Support section.

Date	Revision	Description
February 2008	3.16	Added AMD Phenom™ brand information in Table 1 and Table 14; Added Mixed Silicon Support section; Added Table 6; Supported Mixed Silicon Revision Configurations and Deleted Table 9: Cross Reference of Product Revision to OSVW_ID and renumbered tables accordingly; Added AM2r2 String Tables 10 and 11; Updated MSRC001_0140 OS Visible Work-around MSR0 (OSVW_ID_Length) and MSRC001_0141 OS Visible Work-around MSR1 (OSVW_Status) sections for OsvwId0; Added errata #293, #295, #297-#298, #295, #300-#302, #308-#309, #312, #315, and #319; Editorial update to Suggested Workaround in erratum #254; Updated Fix Planned in erratum #263 and updated entry in Table 13; Updated Documentation Support section.
September 2007	3.00	Initial public release.

Revision Guide for AMD Family 10h Processors

Overview

The purpose of the *Revision Guide for AMD Family 10h Processors* is to communicate updated product information to designers of computer systems and software developers. This revision guide includes information on the following products:

- AMD Athlon™ Dual-Core Processor
- AMD Athlon II X2 Processor
- Quad-Core AMD Opteron™ Processor
- Six-Core AMD Opteron Processor
- Embedded AMD Opteron Processor
- AMD Phenom™ Triple-Core Processor
- AMD Phenom Quad-Core Processor
- AMD Phenom II X2 Processor
- AMD Phenom II X3 Processor
- AMD Phenom II X4 Processor

This guide consists of three major sections:

- **Processor Identification:** This section, starting on page 9, shows how to determine the processor revision, program and display the processor name string, and construct the processor name string.
- **Product Errata:** This section, starting on page 21, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification, and as such may cause the behavior of the processor to deviate from the published specifications.
- **Documentation Support:** This section, starting on page 97, provides a listing of available technical support resources.

Revision Guide Policy

Occasionally, AMD identifies product errata that cause the processor to deviate from published specifications. Descriptions of identified product errata are designed to assist system and software designers in using the processors described in this revision guide. This revision guide may be updated periodically.

Conventions

Numbering

- **Binary numbers.** Binary numbers are indicated by appending a “b” at the end, e.g., 0110b.
- **Decimal numbers.** Unless specified otherwise, all numbers are decimal. This rule does not apply to the register mnemonics.
- **Hexadecimal numbers.** Hexadecimal numbers are indicated by appending an “h” to the end, e.g., 45F8h.
- **Underscores in numbers.** Underscores are used to break up numbers to make them more readable. They do not imply any operation. e.g., 0110_1100b.
- **Undefined digit.** An undefined digit, in any radix, is notated as a lower case “x”.

Register References and Mnemonics

In order to define errata workarounds it is sometimes necessary to reference processor registers. References to registers in this document use a mnemonic notation consistent with that defined in the *BIOS and Kernel Developer’s Guide (BKDG) for AMD Family 10h Processors*, order# 31116. Each mnemonic is a concatenation of the register-space indicator and the offset of the register. The mnemonics for the various register spaces are as follows:

- IOXXX: x86-defined input and output address space registers; XXX specifies the byte address of the I/O register in hex (this may be 2 or 3 digits). This space includes the I/O-Space Configuration Address Register (IOCF8) and the I/O-Space Configuration Data Port (IOCFC) to access configuration registers.
- FYxXXX: PCI-defined configuration space; XXX specifies the byte address of the configuration register (this may be 2 or 3 digits) in hex; Y specifies the function number. For example, F3x40 specifies the register at function 3, address 40h. Each processor node includes five functions, 0 through 4.
- FYxXXX_xZZZZZ: Port access through the PCI-defined configuration space; XXX specifies the byte address of the data port configuration register (this may be 2 or 3 digits) in hex; Y specifies the function number; ZZZZZ specifies the port address (this may be 2 to 7 digits) in hex. For example, F2x9C_x1C specifies the port 1Ch register accessed using the data port register at function 2, address 9Ch. Refer to the *BIOS and Kernel Developer’s Guide (BKDG) for AMD Family 10h Processors*, order# 31116 for access properties.

- APICXXX: APIC memory-mapped registers; XXX is the byte address offset from the base address in hex (this may be 2 or 3 digits). The base address for this space is specified by the APIC Base Address Register (APIC_BAR) at MSR1B.
- CPUID FnXXXX_XXXX_RRR: processor capabilities information returned by the CPUID instruction where the CPUID function is XXXX_XXXX (in hex). When a register is specified by RRR, the reference is to the data returned in that register. For example, CPUID Fn8000_0001_EAX refers to the data in the EAX register after executing CPUID instruction function 8000_0001h.
- MSRXXXX_XXXX: model specific registers; XXXX_XXXX is the MSR number in hex. This space is accessed through x86-defined RDMSR and WRMSR instructions.

Many register references use the notation "[]" to identify a range of registers. For example, F2x[1,0][4C:40] is a shorthand notation for F2x40, F2x44, F2x48, F2x4C, F2x140, F2x144, F2x148, and F2x14C.

Processor Identification

This section shows how to determine the processor revision, program and display the processor name string, and construct the processor name string.

Revision Determination

Figure 1 shows the format of the value from CPUID Fn0000_0001_EAX.

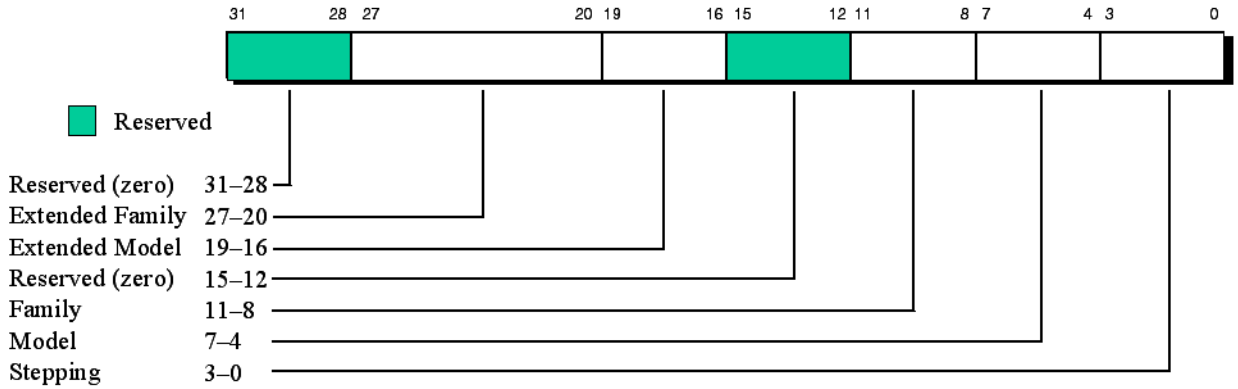

Figure 1. Format of CPUID Fn0000_0001_EAX

Tables 1 through 4 cross-references the identification number from CPUID Fn0000_0001_EAX for each revision of the processor to each processor segment. “X” signifies that the revision has been used in the processor segment. “N/A” signifies that the revision has not been used in the processor segment.

Table 1. CPUID Values for AMD Family 10h Fr2 (1207) Processor Revisions

CPUID Fn0000_0001_EAX (Mnemonic)	Quad-Core AMD Opteron™ Processor	Embedded AMD Opteron™ Processor
00100F2Ah (DR-BA)	X	N/A
00100F22h (DR-B2)	X	X
00100F23h (DR-B3)	X	X
00100F42h (RB-C2)	X	N/A

Table 2. CPUID Values for AMD Family 10h Fr5 (1207) Processor Revisions

CPUID Fn0000_0001_EAX (Mnemonic)	Quad-Core AMD Opteron™ Processor
00100F42h (RB-C2)	X

Table 3. CPUID Values for AMD Family 10h Fr6 (1207) Processor Revisions

CPUID Fn0000_0001_EAX (Mnemonic)	Six-Core AMD Opteron™ Processor
00100F60h (HY-D0)	X

Table 4. CPUID Values for AMD Family 10h AM2r2 Processor Revisions

CPUID Fn0000_0001_EAX (Mnemonic)	Quad-Core AMD Opteron™ Processor	AMD Phenom™ Triple-Core Processor	AMD Phenom™ Quad-Core Processor	AMD Athlon™ Dual-Core Processor	AMD Phenom™ II X3 Processor	AMD Phenom™ II X4 Processor
00100F22h (DR-B2)	X	X	X	N/A	N/A	N/A
00100F23h (DR-B3)	X	X	X	X	N/A	N/A
00100F42h (RB-C2)	N/A	N/A	N/A	N/A	X	X

Table 5. CPUID Values for AMD Family 10h AM3 Processor Revisions

CPUID Fn0000_0001_EAX (Mnemonic)	Quad-Core AMD Opteron™ Processor	AMD Athlon™ II X2 Processor	AMD Phenom™ II X2 Processor	AMD Phenom™ II X3 Processor	AMD Phenom™ II X4 Processor
00100F42h (RB-C2)	X	N/A	X	X	X
00100F62h (DA-C2)	N/A	X	N/A	N/A	N/A

Mixed Silicon Support

AMD Family 10h processors with different silicon revisions can be mixed in a multiprocessor system. Mixed silicon revision support includes the AMD Opteron™ processor configurations as shown in Table 6. Processors of different package types can not be mixed in a multiprocessor system.

Table 6. Supported Mixed Silicon Revision Configurations

Silicon Revision	DR-BA	DR-B2	DR-B3	RB-C2	HY-D0
DR-BA	YES	YES	YES	NO	NO
DR-B2	YES	YES	YES	NO	NO
DR-B3	YES	YES	YES	NO	NO
RB-C2	NO	NO	NO	YES	NO
HY-D0	NO	NO	NO	NO	YES

Refer to Table 1 through 3 for the CPUID Fn0000_0001_EAX values for these revisions. Errata workarounds must be applied according to revision as described in the Product Errata section starting on page 21 unless otherwise noted in the workraound of an erratum.

Programming and Displaying the Processor Name String

This section, intended for BIOS programmers, describes how to program and display the 48-character processor name string that is returned by CPUID Fn8000_000[4:2]. The hardware or cold reset value of the processor name string is 48 ASCII NUL characters, so the BIOS must program the processor name string before any general purpose application or operating system software uses the extended functions that read the name string. It is common practice for the BIOS to display the processor name string and model number whenever it displays processor information during boot up.

Note: *Motherboards that do not program the proper processor name string and model number will not pass AMD validation and will not be posted on the AMD Recommended Motherboard Web site.*

The name string must be ASCII NUL terminated and the 48-character maximum includes that NUL character.

The processor name string is programmed by MSR writes to the six MSR addresses covered by the range MSRC001_00[35:30]h. Refer to the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116, for the format of how the 48-character processor name string maps to the 48 bytes contained in the six 64-bit registers of MSRC001_00[35:30].

The processor name string is read by CPUID reads to a range of CPUID functions covered by CPUID Fn8000_000[4:2]. Refer to CPUID Fn8000_000[4:2] in the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116, for the 48-character processor name string mapping to the 48 bytes contained in the twelve 32-bit registers of CPUID Fn8000_000[4:2].

Constructing the Processor Name String

This section describes how to construct the processor name string. BIOS uses the following fields to create the name string:

- BrandId[15:0] is from CPUID Fn8000_0001_EBX[15:0].
  - **String1[3:0]** is defined to be BrandID[14:11]. This field is an index to a string value used to create the processor name string. The definitions of the String1 values are provided in Tables 8, and 10.
  - **String2[3:0]** is defined to be BrandID[3:0]. This field is an index to a string value used to create the processor name string. The definitions of the String2 values are provided in Tables 9, and 11.
  - **PartialModel[6:0]** is defined to be BrandID[10:4]. This field is normally used to create some or all of the model number in the name string. This field represents a number which should be converted to ASCII for display. This field may be decremented by one before use.
  - **Pg[0]** is defined to be BrandID[15]. This field is used to index the appropriate page for the tables.

- PkgType[3:0] is from CPUID Fn8000_0001_EBX[31:28]. This field specifies the package type as defined in the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116, and is used to index the appropriate string tables from Table 7.
- NC[7:0] is from CPUID Fn8000_0008_ECX[7:0]. This field identifies how many physical cores are present as defined in the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116, and is used to index the appropriate strings from Tables 8 through 11.

The name string is formed as follows:

1. Decrement PartialModel[6:0] by one if PkgType[3:0] is greater than or equal to 2h.
2. Translate PartialModel[6:0] into an ASCII value (*PartialModelAscii*). This number will range from 00-99 and should include a leading zero if less than 10, e.g., 09.
3. Select the appropriate string tables based on PkgType[3:0] from Table 7.
4. Index into the referenced tables using Pg[0], String1[3:0], String2[3:0], and NC[7:0] to obtain the *String1* and *String2* values.
5. If *String1* is an undefined value skip all remaining steps and program the name string as follows:

   Name String = AMD Processor Model Unknown
6. Else concatenate the strings with the two character ASCII translation of PartialModel[3:0] from step 2 to obtain the name string as follows:

   If *String2* is undefined, *Name string = String1, PartialModelAscii*

   Else, *Name string = String1, PartialModelAscii, String2*

Table 7. String Table Reference Per Package Type

PkgType [3:0]	String1 Table	String2 Table
0h	Table 8	Table 9
1h	Table 10	Table 11
2h-Fh	Reserved	Reserved

Table 8. String1 Values for Fr2, Fr5 and Fr6 (1207) Processors

Pg[0]	NC [7:0]	String1 [3:0]	Value	Note	Description
0b	03h	0h	`Quad-Core AMD Opteron(tm) Processor 83`	-	MP Server
		1h	`Quad-Core AMD Opteron(tm) Processor 23`	-	DP Server
	05h	0h	`Six-Core AMD Opteron(tm) Processor 84`	-	MP Server
		1h	`Six-Core AMD Opteron(tm) Processor 24`	-	DP Server
1b	03h	1h	`Embedded AMD Opteron(tm) Processor`	1	Embedded
All other values			`AMD Processor Model Unknown`	-	

Notes:

1. *The string includes a space as the trailing character.*

Table 9. String2 Values for Fr2, Fr5 and Fr6 (1207) Processors

Pg[0]	NC [7:0]	String2 [3:0]	Value	Note	Description
0b	03h	Ah	SE	1	
		Bh	HE	1	
	xxh	Fh		2	
1b	03h	1h	GF HE	-	
		2h	HF HE	-	
All other values			Reserved	-	

Notes:

1. *The string includes a space as the leading character.*
2. *The String2 index 0Fh is defined as an empty string, i.e., no suffix.*

Table 10. String1 Values for AM2r2 and AM3 Processors

Pg[0]	NC [7:0]	String1 [3:0]	Value	Note	Description
0b	01h	1h	AMD Athlon(tm)	1	Client
		3h	AMD Athlon(tm) II X2 2		Client
		7h	AMD Phenom(tm) II X2 5		Client
	02h	0h	AMD Phenom(tm)	1	Client
		8h	AMD Phenom(tm) II X3 7		Client
	03h	0h	Quad-Core AMD Opteron(tm) Processor 13	-	UP Server
		2h	AMD Phenom(tm)	1	Client
		3h	AMD Phenom(tm) II X4 9		Client
		4h	AMD Phenom(tm) II X4 8		Client
All other values			AMD Processor Model Unknown	-	

Notes:

1. *The string includes a space as the trailing character.*

Table 11. String2 Values for AM2r2 and AM3 Processors

Pg[0]	NC [7:0]	String2 [3:0]	Value	Note	Description
0b	01h	3h	50 Dual-Core Processor	-	
		6h	Processor	1	
		7h	e Processor	-	
		9h	0 Processor	-	
		Ah	0e Processor	-	
	02h	0h	00 Triple-Core Processor	-	
		1h	00e Triple-Core Processor	-	
		2h	00B Triple-Core Processor	-	
		3h	50 Triple-Core Processor	-	
		4h	50e Triple-Core Processor	-	
		5h	50B Triple-Core Processor	-	
		6h	Processor	1	
		7h	e Processor	-	
		9h	0e Processor	-	
		Ah	0 Processor	-	
	03h	0h	00 Quad-Core Processor	-	
		1h	00e Quad-Core Processor	-	
		2h	00B Quad-Core Processor	-	
		3h	50 Quad-Core Processor	-	
		4h	50e Quad-Core Processor	-	
		5h	50B Quad-Core Processor	-	
		6h	Processor	1	
		7h	e Processor	-	
		9h	0e Processor	-	
		Eh	0 Processor	-	
	xxh	Fh		2	
All other values			Reserved	-	

Notes:

1. *The string includes a space as the leading character.*
2. *The String2 index 0Fh is defined as an empty string, i.e., no suffix.*

F4x164 Fixed Errata Register

Communicating the status of an erratum requiring a workaround within a stepping of a processor family is necessary in certain circumstances. F4x164 is used to communicate the status of such an erratum fix so that BIOS or system software can determine the necessity of applying the workaround. Under these circumstances, the erratum workaround references the specified bit to enable software to test for the presence of the erratum. The revisions of a processor, prior to the definition of a bit may not be affected by the erratum. Therefore, software should use the stepping as the first criteria to identify the applicability of an erratum. Once defined, the definition of the status bit will persist within the family of processors.

Bits	Description
31:0	0000_0000h. Reserved.

MSRC001_0140 OS Visible Work-around MSR0 (OSVW_ID_Length)

This register, as defined in *AMD64 Architecture Programmer's Manual Volume 2: System Programming*, order# 24593, is used to specify the number of valid status bits within the OS Visible Work-around status registers.

The reset default value of this register is 0000_0000_0000_0000h.

BIOS shall program the OSVW_ID_Length to 0001h prior to hand-off to the OS.

Bits	Description
63:16	Reserved.
15:0	**OSVW_ID_Length: OS visible work-around ID length**. Read-write

MSRC001_0141 OS Visible Work-around MSR1 (OSVW_Status)

This register, as defined in *AMD64 Architecture Programmer's Manual Volume 2: System Programming*, order# 24593, provides the status of the known OS visible errata. Known errata are assigned an OSVW_ID corresponding to the bit position within the valid status field.

Operating system software should use MSRC001_0140 to determine the valid length of the bit status field. For all valid status bits: 1=Hardware contains the erratum, and an OS software work-around is required or may be applied instead of a BIOS workaround. 0=Hardware has corrected the erratum, so an OS software work-around is not necessary.

The reset default value of this register is 0000_0000_0000_0000h.

Bits	Description
63:1	**OsvwStatusBits:** Reserved. OS visible work-around status bits. Read-write.
0	**OsvwId0:** 1= Hardware contains erratum #298, an OS workaround may be applied if available. 0= Hardware has corrected erratum #298. In a multiprocessor platform, OsvwId0 should be set to 1 for all processors regardless of silicon revision when an affected processor is present. Read-write.

BIOS shall program the state of the valid status bits as shown in Table 12 prior to hand-off to the OS.

Table 12. Cross Reference of Product Revision to OSVW ID

CPUID Fn0000_0001_EAX (Mnemonic)	MSRC001_1041 Bits
00100F2Ah (DR-BA)	0000_0000_0000_0001h
00100F22h (DR-B2)	0000_0000_0000_0001h
00100F23h (DR-B3)	0000_0000_0000_0000h or 0000_0000_0000_0001h if mixed with DR-BA or DR-B2 processors in a multiprocessor platform
00100F42h (RB-C2)	0000_0000_0000_0000h
00100F62h (DA-C2)	0000_0000_0000_0000h
00100F80h (HY-D0)	0000_0000_0000_0000h

Product Errata

This section documents product errata for the processors. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 13 cross-references the revisions of the part to each erratum. An "X" indicates that the erratum applies to the revision. The absence of an "X" indicates that the erratum does not apply to the revision. An "*" indicates advance information that the erratum has been fixed but not yet verified. "No fix planned" indicates that no fix is planned for current or future revisions of the processor.

Note: *There may be missing errata numbers. Errata that have been resolved from early revisions of the processor have been deleted, and errata that have been reconsidered may have been deleted or renumbered.*

Table 13. Cross-Reference of Product Revision to Errata

No.	Errata Description	Revision Number					
		DR-BA	DR-B2	DR-B3	RB-C2	DA-C2	HY-D0
57	Some Data Cache Tag Eviction Errors Are Reported As Snoop Errors	No fix planned					
60	Single Machine Check Error May Report Overflow	No fix planned					
77	Long Mode CALLF or JMPF May Fail To Signal GP When Callgate Descriptor is Beyond GDT/LDT Limit	No fix planned					
178	Default RdPtrInit Value Does Not Provide Sufficient Timing Margin	X	X	X			
244	A DIV Instruction Followed Closely By Other Divide Instructions May Yield Incorrect Results	X	X	X			
246	Breakpoint Due to An Instruction That Has an Interrupt Shadow May Be Delivered to the Hypervisor	X	X	X			
248	INVLPGA of A Guest Page May Not Invalidate Splintered Pages	X					
254	Internal Resource Livelock Involving Cached TLB Reload	X	X				
260	REP MOVS Instruction May Corrupt Source Address	X	X	X			
261	Processor May Stall Entering Stop-Grant Due to Pending Data Cache Scrub	No fix planned					
263	Incompatibility With Some DIMMs Due to DQS Duty Cycle Distortion	No fix planned					
264	Incorrect DRAM Data Masks Asserted When DRAM Controller Data Interleaving Is Enabled	X	X	X			
269	ITT Specification Exceeded During Power-Up Sequencing	No fix planned					
273	Lane Select Function Is Not Available for Link BIST on 8-Bit HyperTransport™ Links In Ganged Mode	X	X	X			
274	IDDIO Specification Exceeded During Power-Up Sequencing	X					
278	Incorrect Memory Controller Operation In Ganged Mode	X					
279	HyperTransport™ Link RTT and RON Specification Violations	X					
280	Time Stamp Counter May Yield An Incorrect Value	X	X	X			
293	Memory Instability After PWROK Assertion	X	X				
295	DRAM Phy Configuration Access Failures		X	X			

Table 13. Cross-Reference of Product Revision to Errata (Continued)

No.	Errata Description	Revision Number					
		DR-BA	DR-B2	DR-B3	RB-C2	DA-C2	HY-D0
297	Single Machine Check Error May Report Overflow	No fix planned					
298	L2 Eviction May Occur During Processor Operation To Set Accessed or Dirty Bit	X	X				
300	Hardware Memory Clear Is Not Supported After Software DRAM Initialization	X	X	X			
301	Performance Counters Do Not Accurately Count MFENCE or SFENCE Instructions	X	X	X			
302	MWAIT Power Savings May Not Be Realized when Two or More Cores Monitor the Same Address	X	X	X			
308	Processor Stall in C1 Low Power State	X	X	X			
309	Processor Core May Execute Incorrect Instructions on Concurrent L2 and Northbridge Response	X	X				
312	CVTSD2SS and CVTPD2PS Instructions May Not Round to Zero	X	X	X			
315	FST and FSTP Instructions May Calculate Operand Address in Incorrect Mode	X	X	X			
319	Inaccurate Temperature Measurement	X	X	X			
322	Address and Command Fine Delay Values May Be Incorrect	No fix planned					
326	Misaligned Load Operation May Cause Processor Core Hang	X	X	X			
327	HyperTransport™ Link RTT Specification Violation				X	X	X
328	BIST May Report Failures on Initial Powerup	X	X	X			
336	Instruction Based Sampling May Be Inaccurate	X	X	X			
337	CPU Instruction Based Sampling Fields May Be Inaccurate	X	X	X			
338	Northbridge Instruction Based Sampling Fields May Be Inaccurate	X	X	X			
339	APIC Timer Rollover May Be Delayed	No fix planned					
342	SMIs That Are Not Intercepted May Disable Interrupts	X	X	X	X		
343	Eviction May Occur When Using L2 Cache as General Storage During Boot				X	X	X
344	Intermittent HyperTransport™ Link Training Failures				X	X	X
346	System May Hang if Core Frequency is Even Divisor of Northbridge Clock				X	X	
348	Processor On-die Termination Resistance is Higher than Specification				X		
350	DRAM May Fail Training on Cold Reset				X	X	X
351	HyperTransport™ Technology LS2 Low-Power Mode May Not Function Correctly	X	X	X	X		*
352	SYSCALL Instruction May Execute Incorrectly Due to Breakpoint	X	X	X	X	X	
353	SYSRET Instruction May Execute Incorrectly Due to Breakpoint	X	X	X	X	X	
354	HyperTransport™ Link Training Failure				X	X	
355	DRAM Read Errors May Occur at Memory Speeds Higher than DDR2-800	X	X	X			
359	MEMCLK is Not Provided for Minimum Specified Time Before CKE Assertion	X	X	X	X	X	
360	DRAM CKE and Address Drive Strength Values May Be Incorrect	No fix planned					
361	Breakpoint Due to an Instruction That Has an Interrupt Shadow May Be Lost				X	X	X
362	Illegal Packet on HyperTransport™ Link May Prevent Warm Reset	X	X	X	X	X	
370	DRAM Read Errors May Occur at DDR2-800 Memory Speeds With Higher Read DQS Delays	X	X	X			

Table 13. Cross-Reference of Product Revision to Errata (Continued)

No.	Errata Description	Revision Number					
		DR-BA	DR-B2	DR-B3	RB-C2	DA-C2	HY-D0
372	Processor Read That Matches The Address of an Earlier Uncompleted Write May Be Incorrect				X	X	X
373	Processor Write to APIC Task Priority Register May Cause Error Status Bit to Set	No fix planned					
374	Processor Read From L3 Cache May Return Stale Data						X
378	Processor May Operate at Reduced Frequency				X	X	
379	DDR3-1333 Configurations with Two DIMMs per Channel May Experience Unreliable Operation				X	X	
382	L3 Cache Index Disable Cannot Be Modified After L3 Cache is Enabled				X		
384	DRAM Prefetch May Cause System Hang When Probe Filter is Enabled						X
385	Processor May Report Incorrect Address For an L3 Cache Error Machine Check						X
386	HyperTransport™ Link in Retry Mode That Receives Repeated Invalid Packets May Cause MCA Exception						X
387	Performance Counters Do Not Accurately Count L3 Cache Evictions	No fix planned					
388	L3 Cache Scrubbing Does Not Bypass Disabled L3 Cache Locations				X		X
389	HyperTransport™ Link in Retry Mode May Consume Link Packet Buffer Incorrectly				X		X
391	HyperTransport™ Link RTT and RON Specification Violations				X	X	X
393	Performance Monitor May Count Fastpath Double Operation Instructions Incorrectly	No fix planned					
395	Incorrect Data Masking in Ganged DRAM Mode					X	

Table 14 cross-references the errata to each processor segment. An empty cell signifies that the erratum does not apply to the processor segment. “X” signifies that the erratum applies to the processor segment. “N/A” signifies that the erratum does not apply to the processor segment due to the silicon revision.

Table 14. Cross-Reference of Errata to Processor Segments

Errata Number	Quad-Core AMD Opteron™ Processor	Six-Core AMD Opteron™ Processor	Embedded AMD Opteron™ Processor	AMD Phenom™ Triple-Core and Quad-Core Processor	AMD Athlon™ Dual-Core Processor	AMD Phenom™ II X2, X3 and X4 Processor	AMD Athlon™ II X2 Processor
57	X	X	X	X	X	X	X
60	X	X	X	X	X	X	X
77	X	X	X	X	X	X	X
178	X	N/A	X	X	X	N/A	N/A
244	X	N/A	X	X	X	N/A	N/A
246	X	N/A	X	X	X	N/A	N/A
248	X	N/A	N/A	N/A	N/A	N/A	N/A
254	X	N/A	X	X	N/A	N/A	N/A
260	X	N/A	X	X	X	N/A	N/A
261	X	X	X	X	X	X	X
263	X	X	X	X	X	X	X
264	X	N/A	X	X	X	N/A	N/A
269	X	X	X	X	X	X	X
273	X	N/A	X	X	X	N/A	N/A
274	X	N/A	N/A	N/A	N/A	N/A	N/A
278	X	N/A	N/A	N/A	N/A	N/A	N/A
279	X	N/A	N/A	N/A	N/A	N/A	N/A
280	X	N/A	X	X	X	N/A	N/A
293	X	N/A	X	X	N/A	N/A	N/A
295	X	N/A	X	X	X	N/A	N/A
297	X	X	X	X	X	X	X
298	X	N/A	X	X	N/A	N/A	N/A
300	X	N/A	X	X	X	N/A	N/A
301	X	N/A	X	X	X	N/A	N/A
302	X	N/A	X	X	X	N/A	N/A
308	X	N/A	X	X	X	N/A	N/A
309	X	N/A	X	X	N/A	N/A	N/A
312	X	N/A	X	X	X	N/A	N/A
315	X	N/A	X	X	X	N/A	N/A
319	X	N/A	X	X	X	N/A	N/A
322	X	X	X	X	X	X	X
326	X	N/A	X				
327	X	X	N/A	N/A	N/A	X	X

Table 14. Cross-Reference of Errata to Processor Segments (Continued)

Errata Number	Quad-Core AMD Opteron™ Processor	Six-Core AMD Opteron™ Processor	Embedded AMD Opteron™ Processor	AMD Phenom™ Triple-Core and Quad-Core Processor	AMD Athlon™ Dual-Core Processor	AMD Phenom™ II X2, X3 and X4 Processor	AMD Athlon™ II X2 Processor
328	X	N/A	X	X	X	N/A	N/A
336	X	N/A	X	X	X	N/A	N/A
337	X	N/A	X	X	X	N/A	N/A
338	X	N/A	X	X	X	N/A	N/A
339	X	X	X	X	X	X	X
342	X	N/A	X	X	X	X	X
343	X	X	N/A	N/A	N/A	X	X
344	X	X	N/A	N/A	N/A	X	X
346	X	N/A	N/A	N/A	N/A	X	X
348	X	N/A	N/A	N/A	N/A	X	X
350	X	X	N/A	N/A	N/A	X	X
351	X	N/A	X	X	X	X	N/A
352	X	N/A	X	X	X	X	X
353	X	N/A	X	X	X	X	X
354	X	N/A	N/A	N/A	N/A	X	X
355				X	X	N/A	N/A
359	X	N/A	X	X	X	X	X
360	X	X	X	X	X	X	X
361	X	X	N/A	N/A	N/A	X	X
362	X	N/A	X	X	X	X	X
370	X	N/A	X	X	X	N/A	N/A
372	X					X	X
373							X
374	N/A	X	N/A	N/A	N/A	N/A	N/A
378	X					X	X
379	X					X	X
382	X	N/A	N/A	N/A	N/A	X	N/A
384	N/A	X	N/A	N/A	N/A	N/A	N/A
385	N/A	X	N/A	N/A	N/A	N/A	N/A
386	N/A	X	N/A	N/A	N/A	N/A	N/A
387	X	X	X	X	X	X	N/A
388	X	X	N/A	N/A	N/A	X	N/A
389	X	X	N/A				
391	X	X	N/A	N/A	N/A	X	X
393	X	X	X	X	X	X	X
395	N/A	N/A	N/A	N/A	N/A	N/A	X

Table 15 cross-references the errata to each package type. An empty cell signifies that the erratum does not apply to the package type. “X” signifies that the erratum applies to the package type. “N/A” signifies that the erratum does not apply to the package type due to the silicon revision.

Table 15. Cross-Reference of Errata to Package Type

Errata Number	Fr2 (1207)	Fr5 (1207)	Fr6 (1207)	AM2r2	AM3
57	X	X	X	X	X
60	X	X	X	X	X
77	X	X	X	X	X
178	X	N/A	N/A	X	N/A
244	X	N/A	N/A	X	N/A
246	X	N/A	N/A	X	N/A
248	X	N/A	N/A	N/A	N/A
254	X	N/A	N/A	X	N/A
260	X	N/A	N/A	X	N/A
261	X	X	X	X	X
263	X	X	X	X	X
264	X	N/A	N/A	X	N/A
269	X	X	X	X	X
273	X	N/A	N/A	X	N/A
274	X	N/A	N/A	N/A	N/A
278	X	N/A	N/A	N/A	N/A
279	X	N/A	N/A	N/A	N/A
280	X	N/A	N/A	X	N/A
293	X	N/A	N/A	X	N/A
295	X	N/A	N/A	X	N/A
297	X	X	X	X	X
298	X	N/A	N/A	X	N/A
300	X	N/A	N/A	X	N/A
301	X	N/A	N/A	X	N/A
302	X	N/A	N/A	X	N/A
308	X	N/A	N/A	X	N/A
309	X	N/A	N/A	X	N/A
312	X	N/A	N/A	X	N/A
315	X	N/A	N/A	X	N/A
319	X	N/A	N/A	X	N/A
322	X	X	X	X	X
326	X	N/A	N/A	X	N/A
327	X	X	X	X	X
328	X	N/A	N/A	X	N/A
336	X	N/A	N/A	X	N/A
337	X	N/A	N/A	X	N/A

Table 15. Cross-Reference of Errata to Package Type (Continued)

Errata Number	Fr2 (1207)	Fr5 (1207)	Fr6 (1207)	AM2r2	AM3
338	X	N/A	N/A	X	N/A
339	X	X	X	X	X
342	X	X	N/A	X	X
343	X	X	X	X	X
344		X	X	X	X
346	X	X	N/A	X	X
348	X	X	N/A	X	X
350	X	X	X	X	X
351	X	X	N/A	X	X
352	X	X	N/A	X	X
353	X	X	N/A	X	X
354		X	N/A	X	X
355				X	N/A
359	X	X	N/A	X	X
360	X	X	X	X	X
361	X	X	X	X	X
362	X	X	N/A	X	X
370	X	N/A	N/A	X	N/A
372					X
373					X
374	N/A	N/A	X	N/A	N/A
378					X
379					X
382	X	X	X	X	X
384	N/A	N/A	X	N/A	N/A
385	N/A	N/A	X	N/A	N/A
386	N/A	N/A	X	N/A	N/A
387	X	X	X	X	X
388	X	X	X	X	X
389		X	X		
391	X	X	X	X	X
393	X	X	X	X	X
395	N/A	N/A	N/A	N/A	X

57 Some Data Cache Tag Eviction Errors Are Reported As Snoop Errors

Description

In some cases, the machine check error code on a data cache (DC) tag array parity error erroneously classifies an eviction error as a snoop error.

The common cases of cache line replacements and external probes are classified correctly (as eviction and snoop respectively). The erroneous cases occur when a tag error is detected during a DC eviction that was generated by a hardware prefetch, a cache line state change operation, or a number of other internal microarchitectural events. In such cases, the error code logged in the DC Machine Check Status register (MC0_STATUS, MSR401) erroneously indicates a snoop error.

Potential Effect on System

Internally detected DC tag errors may be reported to software as having been detected by snoops. Depending upon machine check software architecture, the system response to such errors may be broader than necessary.

Suggested Workaround

None required.

Fix Planned

No

60 Single Machine Check Error May Report Overflow

Description

A single parity error encountered in the data cache tag array may incorrectly report the detection of multiple errors, as indicated by the overflow bit of the DC Machine Check Status register (bit 62 of MSR401).

Potential Effect on System

System software may be informed of a machine check overflow when only a single error was actually encountered.

Suggested Workaround

Do not rely on the state of the OVER bit in the DC Machine Check Status register.

Fix Planned

No

77 Long Mode CALLF or JMPF May Fail To Signal GP When Callgate Descriptor is Beyond GDT/LDT Limit

Description

If the target selector of a far call or far jump (CALLF or JMPF) instruction references a 16-byte long mode system descriptor where any of the last 8 bytes are beyond the GDT or LDT limit, the processor fails to report a General Protection fault.

Potential Effect on System

None expected, since the operating system typically aligns the GDT/LDT limit such that all descriptors are legal. However, in the case of erroneous operating system code, the above described GP fault will not be signaled, resulting in unpredictable system failure.

Suggested Workaround

None required, it is anticipated that long mode operating system code will ensure the GDT and LDT limits are set high enough to cover the larger (16-byte) long mode system descriptors.

Fix Planned

No

178 Default RdPtrInit Value Does Not Provide Sufficient Timing Margin

Description

Insufficient separation of the read pointer and write pointer in the synchronization FIFO can lead to setup violations in the transmit FIFO.

Potential Effect on System

The setup violations may lead to data corruption.

Suggested Workaround

BIOS should program F2x[1, 0]78[3:0] (RdPtrInit) to 5h.

Fix Planned

Yes

244 A DIV Instruction Followed Closely By Other Divide Instructions May Yield Incorrect Results

Description

A DIV instruction with a dividend less than 64 that is followed in close proximity by a DIV, IDIV, or AAM instruction may produce incorrect results.

Potential Effect on System

Possible data corruption.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

246 Breakpoint Due to An Instruction That Has an Interrupt Shadow May Be Delivered to the Hypervisor

Description

A #DB exception occurring in guest mode may be delivered in the host context under the following conditions:

- A trap-type #DB exception is generated in guest mode during execution of an instruction with an interrupt shadow, and
- The instruction that generated the exception is immediately followed by an instruction resulting in #VMEXIT.

Potential Effect on System

Unpredictable results due to an unexpected #DB exception.

Suggested Workaround

The hypervisor should have a valid interrupt gate in the IDT of the #DB handler entry and the handler must be able to determine that this event has occurred. If the event is detected, the handler should execute an IRET back to the hypervisor; one method that could be used to evaluate for this condition is to compare the RIP pushed on the stack to the RIP of the instruction following VMRUN, if they are equivalent then this event has occurred.

Fix Planned

Yes

248 INVLPGA of A Guest Page May Not Invalidate Splintered Pages

Description

When an address mapped by a guest uses a larger page size than the host, the TLB entry created uses the size of the smaller page; this is referred to as page splintering. TLB entries that are the result of page splintering may not be invalidated when the large page is invalidated in the guest using INVLPGA.

Potential Effect on System

Unpredictable system behavior may result due to inconsistent entries in the TLB.

Suggested Workaround

The hypervisor should always intercept INVLPGA instructions. On returning to the guest from the INVLPGA intercept the hypervisor should set TLB_Control = 1 in the VMCB to ensure correctness.

Fix Planned

Yes

254 Internal Resource Livelock Involving Cached TLB Reload

Description

Under a highly specific and detailed set of conditions, an internal resource livelock may occur between a TLB reload and other cached operations.

Potential Effect on System

The system may hang.

Suggested Workaround

BIOS should set MSRC001_1023[21] to 1b.

Fix Planned

Yes

260 REP MOVS Instruction May Corrupt Source Address

Description

The processor may corrupt the source address for REP MOVS instructions using 16- or 32-bit addressing when a fault occurs on the first iteration and ECX is greater than 255 and EDI equals 0.

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

261 Processor May Stall Entering Stop-Grant Due to Pending Data Cache Scrub

Description

The processor may stall if a correctable error is identified by the data cache scrubber within a small window of time before the processor enters a stop-grant state when another scrub is pending.

Potential Effect on System

The system may hang.

Suggested Workaround

BIOS should set MSRC001_1022[24].

Fix Planned

No

263 Incompatibility With Some DIMMs Due to DQS Duty Cycle Distortion

Description

Some DIMMs exhibit a duty cycle distortion on the first DQS pulse of an incoming read request which may cause the processor's DRAM interface to miss a beat of data in a read burst.

Potential Effect on System

Undefined system behavior due to incorrect read data.

Suggested Workaround

If the memory is DDR2-533 or DDR2-667 write 00000800h to F2x[1, 0]9C_xD040F30, else write 00000000h to F2x[1, 0]9C_xD040F30.

The write of 00000000h to F2x[1, 0]9C_xD040F30 is not necessary if BIOS can not change the memory clock speed without a cold reset or if BIOS does not support the above mentioned memory configurations.

When exiting from the S4 or S5 state, apply this workaround prior to setting DRAM Configuration Low Register[InitDram] (F2x[1,0]90[0]). In addition, for the above mentioned memory configurations, BIOS should set the DRAM read DQS timing control loop range to 32 during DQS position training.

When exiting from the S3 state, apply this workaround prior to setting DRAM Configuration Low Register[ExitSelfRef] (F2x[1,0]90[1]).

Fix Planned

No

264 Incorrect DRAM Data Masks Asserted When DRAM Controller Data Interleaving Is Enabled

Description

The processor may incorrectly assert the DRAM data masks for writes less than a cache line when DRAM controller data interleaving is enabled.

Potential Effect on System

Data corruption.

Suggested Workaround

BIOS should set MSRC001_001F[36] (DisDatMsk) to 1b when F2x110[5] (DctDatIntLv) is set to 1b.

Fix Planned

Yes

269 ITT Specification Exceeded During Power-Up Sequencing

Description

Processor current consumption may exceed the ITT maximum specified for C0/S0 operation if the VTT voltage regulator is enabled before the VDDIO voltage regulator and the VDDIO regulator enables a low resistance path to VSS while VTT - VDDIO > 400 mV.

Potential Effect on System

The VTT voltage regulator may shut down if ITT exceeds the platform design limit.

Suggested Workaround

None required if either of the following are true:

- The VTT regulator is enabled at the same time or after the VDDIO regulator.
- The VDDIO regulator does not enable a low resistance path to VSS while VTT - VDDIO > 400 mV.

For affected systems, the VTT voltage regulator should be enabled at the same time or after the VDDIO voltage regulator during power-up power sequencing. Existing specifications limiting the VDDIO to VTT relationship must be maintained.

Fix Planned

No

273 Lane Select Function Is Not Available for Link BIST on 8-Bit HyperTransport™ Links In Ganged Mode

Description

The link BIST engine incorrectly initiates tests on sublink 1 rather than sublink 0 under the following conditions:

- The HyperTransport™ link is configured as an 8-bit link in ganged mode,
- LaneSel[1], F0x[18C:170][13], is set to 1b,
- BistEn, F0x[18C:170][10], is set to 1b, and
- BIST is initiated by assertion of warm reset or a LDTSTOP_L disconnect.

Potential Effect on System

No impact to normal operational mode; however, the lane select function is not available for testing asymmetric links or isolation of errors to the uplink or downlink on symmetric links.

Suggested Workaround

None.

Fix Planned

Yes

274 IDDIO Specification Exceeded During Power-Up Sequencing

Description

Processor current consumption may exceed the IDDIO maximum specified for C0/S0 operation during power-up sequencing.

Potential Effect on System

None expected if the VDDIO voltage regulator is sourced by a RUN (running) plane from the power supply during power-up sequencing. Otherwise, during power-up sequencing the VDDIO voltage regulator may shut down if IDDIO exceeds the platform budget or the power supply may shut down if the SUS (suspend) rail current capacity is exceeded.

Suggested Workaround

Three options exist to ensure the VDDIO voltage regulator is sourced with sufficient current during processor power-up sequencing:

1. Enable the VDDIO voltage regulator after POWER_GOOD is asserted from the high-current (RUN) source rail.
2. Provide a path for a high-current (RUN) rail to source current to the VDDIO voltage regulator prior to POWER_GOOD assertion from the high-current (RUN) rail. This solution assumes the high-current (RUN) rail is enabled early enough relative to enabling the VDDIO voltage regulator.
3. Choose a power supply with increased capacity for the rail sourcing the VDDIO voltage regulator during power-up sequencing. The capacity required is system specific and should allocate 7 A per processor in the power budget. The following is an example of a supply current capacity calculation assuming a 5 V suspend rail and 3 W rest of system power for a single-processor system. Other platform-specific factors such as power supply or regulator efficiencies should also be considered.
   - Rest of system (non-processor) power = 3 W
   - Processor power = 7 A/processor * 1 processor * 1.8 V = 12.6 W
   - Source rail capacity = (rest of system power + processor power) / source rail voltage; (3 W + 12.6 W) / 5 V = 3.12 A

Fix Planned

Yes

278 Incorrect Memory Controller Operation In Ganged Mode

Description

The DRAM controller 0 (DCT0) and DRAM controller 1 (DCT1) refresh counters may not be initialized to the same value using hardware controlled DRAM initialization when operating in ganged mode.

Potential Effect on System

Incorrect memory controller operation.

Suggested Workaround

BIOS should apply the following workaround prior to DRAM training when using hardware-controlled DRAM initialization and F2x110[4] (DctGangEn) is set to 1b.

1. Disable automatic refresh cycles by setting F2x8C[18] (DisAutoRefresh) to 1b.
2. Begin DRAM initialization by setting F2x90[0] to 1b.
3. Poll F2x90[0] until it reads 0b then wait at least 50 microseconds.
4. Enable automatic refresh cycles by clearing F2x8C[18] (DisAutoRefresh) to 0b.
5. Disable automatic refresh cycles by setting F2x8C[18] (DisAutoRefresh) to 1b.
6. Enable automatic refresh cycles by clearing F2x8C[18] (DisAutoRefresh) to 0b.
7. Begin DRAM training.

In addition, when resuming from S3, BIOS should apply the following workaround.

1. Disable automatic refresh cycles by setting F2x8C[18] (DisAutoRefresh) to 1b.
2. Initiate exit from self refresh by setting F2x90[1] to 1b.
3. Poll F2x90[1] until it reads 0b then wait at least 50 microseconds.
4. Enable automatic refresh cycles by clearing F2x8C[18] (DisAutoRefresh) to 0b.
5. Disable automatic refresh cycles by setting F2x8C[18] (DisAutoRefresh) to 1b.
6. Enable automatic refresh cycles by clearing F2x8C[18] (DisAutoRefresh) to 0b.

Fix Planned

Yes

279 HyperTransport™ Link R_{TT} and R_{ON} Specification Violations

Description

The R_{TT} and R_{ON} specifications for the HyperTransport™ link may be violated on some processor revisions.

Potential Effect on System

These violations do not result in any other HyperTransport™ link electrical specification violations. There are no known functional failures related to this problem.

Suggested Workaround

None required.

Fix Planned

Yes

280 Time Stamp Counter May Yield An Incorrect Value

Description

Reads of the time stamp counter may yield an inconsistent result.

Potential Effect on System

Undefined behavior for software that relies on a continuously increasing time stamp counter value.

Suggested Workaround

Contact your AMD representative for information on a BIOS upgrade.

Fix Planned

Yes

293 Memory Instability After PWROK Assertion

Description

The DRAM DQS DLL may not lock properly after PWROK is asserted.

Potential Effect on System

The system may have degraded memory margins leading to unreliable DRAM signaling. In some circumstances, this may cause BIOS to degrade the memory speed.

Suggested Workaround

During DRAM controller (DCT) initialization, system software should perform the following workaround to every enabled DCT in the system:

1. Perform a dummy DRAM read to any address on any DIMM attached to the DCT.
2. Write 0000_8000h to register F2x[1, 0]9C_xD080F0C.
3. Wait at least 300 nanoseconds.
4. Write 0000_0000h to register F2x[1, 0]9C_xD080F0C.
5. Wait at least 2 microseconds.

When exiting from the S4 or S5 state, apply the workaround immediately prior to the Receiver Enable Training. During resume from the S3 state, apply the workaround after F2x[1, 0]90[ExitSelfRef] has been cleared and prior to restoring the F2x[1, 0]9C registers.

Fix Planned

Yes

295 DRAM Phy Configuration Access Failures

Description

Under a highly specific set of asynchronous timing conditions established during cold boot (S5 to S0 transition) or resume (S4 or S3 to S0 transition), the skew between the DRAM controllers (DCTs) and DRAM phy may lead to unreliable communication for DRAM phy configuration accesses.

Potential Effect on System

The system may hang during DRAM configuration accesses when using DCT link ganged mode ([DRAM Controller Select Low Register] F2x110[DctGangEn] = 1b), or fail DRAM training in link ganged mode or in link unganged mode.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

297 Single Machine Check Error May Report Overflow

Description

A single tag snoop parity error encountered in the instruction cache tag array may incorrectly report the detection of multiple errors, as indicated by the overflow bit of the IC Machine Check Status register (MSR405[62]).

Potential Effect on System

System software may be informed of a machine check overflow when only a single error was actually encountered.

Suggested Workaround

None required.

Fix Planned

No

298 L2 Eviction May Occur During Processor Operation To Set Accessed or Dirty Bit

Description

The processor operation to change the accessed or dirty bits of a page translation table entry in the L2 from 0b to 1b may not be atomic. A small window of time exists where other cached operations may cause the stale page translation table entry to be installed in the L3 before the modified copy is returned to the L2.

In addition, if a probe for this cache line occurs during this window of time, the processor may not set the accessed or dirty bit and may corrupt data for an unrelated cached operation.

Potential Effect on System

One or more of the following events may occur:

- Machine check for an L3 protocol error. The MC4 status register (MSR410) will be equal to B2000000_000B0C0Fh or BA000000_000B0C0Fh. The MC4 address register (MSR412) will be equal to 26h.
- Loss of coherency on a cache line containing a page translation table entry.
- Data corruption.

Suggested Workaround

BIOS should set MSRC001_0015[3] (HWCR[TlbCacheDis]) to 1b and MSRC001_1023[1] to 1b.

In a multiprocessor platform, the workaround above should be applied to all processors regardless of silicon revision when an affected processor is present.

Fix Planned

Yes

300 Hardware Memory Clear Is Not Supported After Software DRAM Initialization

Description

When using software-controlled DRAM device initialization through EnDramInit (F2x[1, 0]7C DRAM Initialization Register[31]), hardware memory clear using MemClrInit (F2x110 DRAM Controller Select Low Register[3]) does not function.

Potential Effect on System

After BIOS sets MemClrInit (F2x110[3]), the hardware will not clear memory and will not set MemCleared (F2x110[10]). The BIOS will hang waiting for the operation to complete.

Suggested Workaround

BIOS should use hardware initialization of DRAM using InitDram (F2x[1, 0]90 DRAM Configuration Low Register[0]). If BIOS uses software initialization, alternative methods to initialize ECC must be used.

Fix Planned

Yes

301 Performance Counters Do Not Accurately Count MFENCE or SFENCE Instructions

Description

MFENCE and SFENCE instructions are not accurately counted by the performance monitor when MSRC001_000[3:0][7:0] (EventSelect) is 1D4h, or 1D5h.

Potential Effect on System

Performance monitoring software will not be able to count MFENCE and SFENCE instructions.

Suggested Workaround

None.

Fix Planned

Yes

302 MWAIT Power Savings May Not Be Realized when Two or More Cores Monitor the Same Address

Description

Execution of the MONITOR instruction may cause another core to exit the monitor event pending state.

Potential Effect on System

No functional impact; however, the power savings associated with the MWAIT instruction may not be realized.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

308 Processor Stall in C1 Low Power State

Description

Under a highly specific set of internal timing conditions, an L3 eviction may stall for a processor core that has entered the C1 (Halt) state. If the processor core has already entered the low power state and the CpuPrbEn bit in the C1 SMAF is 0b (F3x84[24]), the stall persists until the processor core comes out of the low power state.

Potential Effect on System

The system may hang.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

309 Processor Core May Execute Incorrect Instructions on Concurrent L2 and Northbridge Response

Description

Under a specific set of internal timing conditions, an instruction fetch may receive responses from the L2 and the Northbridge concurrently. When this occurs, the processor core may execute incorrect instructions.

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

BIOS should set MSRC001_1023[23].

Fix Planned

Yes

312 CVTSD2SS and CVTPD2PS Instructions May Not Round to Zero

Description

The Convert Scalar Double-Precision Floating Point to Scalar Single-Precision Floating Point (CVTSD2SS) and Convert Packed Double-Precision Floating Point to Packed Single-Precision Floating Point (CVTPD2PS) instructions do not round to zero when the Flush to Zero and Underflow Mask bits (MXCSR bits 15 and 11) are set to 1b and the double-precision operand is less than the smallest single-precision normal number.

Potential Effect on System

The conversion result will yield the smallest single-precision normalized number rather than zero. It is not expected that this will result in any anomalous software behavior since enabling flush to zero provides less precise results.

Suggested Workaround

None.

Fix Planned

Yes

315 FST and FSTP Instructions May Calculate Operand Address in Incorrect Mode

Description

A Floating-Point Store Stack Top (FST or FSTP) instruction in 64-bit mode that is followed shortly by an instruction that changes to compatibility mode may incorrectly calculate the operand address using compatibility mode. Also, an FST or FSTP instruction in compatibility mode that is followed shortly by an instruction that changes to 64-bit mode may incorrectly calculate the operand address using 64-bit mode.

The incorrect mode for address calculation is only used under highly specific internal timing conditions and when the Underflow Mask bit (FCW bit 4) is set and the data to be stored by the FST or FSTP instruction is a denormalized (tiny) number.

Potential Effect on System

The processor may store to an incorrect address. This may cause an unexpected page fault or unpredictable system behavior. This sequence has not been observed in any production software.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

319 Inaccurate Temperature Measurement

Description

The internal thermal sensor used for CurTmp (F3xA4[31:21]), hardware thermal control (HTC), software thermal control (STC) thermal zone, and the sideband temperature sensor interface (SB-TSI) may report inconsistent values.

Potential Effect on System

HTC, STC thermal zone, and SB-TSI do not provide reliable thermal protection. This does not affect THERMTRIP or the use of the STC-active state through StcPstateLimit or StcPstateEn (F3x68[30:28, 5]).

Suggested Workaround

None. Systems should be designed with conventional thermal control and throttling methods or utilize PROCHOT_L functionality based on temperature measurements from an analog thermal diode (THERMDA/THERMDC).

Systems should not rely on the HTC features, STC thermal zone features, or use SB-TSI.

Software should not modify HtcTmpLmt (F3x64[22:16]) or enable any of the STC thermal zone features by setting StcApcTmpLoEn, StcApcTmpHiEn, StcSbcTmpLoEn, or StcSpcTmpHiEn (F3x68[3:0]).

Fix Planned

Yes

322 Address and Command Fine Delay Values May Be Incorrect

Description

The DRAM phy uses the memory speed at the time of DRAM initialization or self-refresh exit to adjust the fine delay values based on internal DLL settings. Data written to fine delay registers prior to DRAM initialization or self-refresh exit may be adjusted incorrectly.

No effect is observed for all fine delays except those in the DRAM Address/Command Timing Control Register at F2x[1,0]9C_x04; these are written after DRAM initialization. However, F2x[1,0]9C_x04 may be written before DRAM initialization or self-refresh exit and may result in an incorrect adjustment.

This erratum only affects MEMCLK frequencies of 400 MHz and higher.

Potential Effect on System

The system may have degraded memory margins leading to unreliable DRAM signaling.

Suggested Workaround

The following workaround should be applied by BIOS prior to writing F2x[1,0]9C_x04 during DRAM controller (DCT) initialization and during the S3 resume sequence:

1. Write 00000000h to F2x[1,0]9C_xD08E000.
2. In unganged mode (DRAM Controller Select Low Register [DctGangEn] (F2x110[4]) = 0b), if DRAM Configuration Register[MemClkFreq] (F2x[1,0]94[2:0]) is greater than or equal to 011b, write 00000080h to F2x[1,0]9C_xD02E001, else write 00000090h to F2x[1,0]9C_xD02E001.
3. In ganged mode (DRAM Controller Select Low Register [DctGangEn] (F2x110[4]) = 1b), if DRAM Configuration Register[MemClkFreq] (F2x94[2:0]) is greater than or equal to 011b, write 00000080h to F2x9C_xD02E001 and F2x19C_xD02E001, else write 00000090h to F2x9C_xD02E001 and F2x19C_xD02E001.

The write of 00000090h to F2x[1,0]9C_xD02E001 is not necessary if BIOS can not change the memory clock speed without a cold reset.

Fix Planned

No

326 Misaligned Load Operation May Cause Processor Core Hang

Description

Under a highly specific set of internal timing conditions, load operations with a misaligned operand may hang.

Any instruction loading data from memory without a LOCK prefix where the first byte and the last byte are in separate octal words may cause the condition mentioned above.

Potential Effect on System

Processor core hang.

Suggested Workaround

BIOS should clear MSRC001_1022[43:42].

Fix Planned

Yes

327 HyperTransport™ Link R_{TT} Specification Violation

Description

The R_{TT} specification for the HyperTransport™ link may be violated on some processor revisions.

Potential Effect on System

These violations do not result in any other HyperTransport™ link electrical specification violations. There are no known functional failures related to this problem.

Suggested Workaround

BIOS should set the Link Phy Impedance Register[RttCtl] (F4x1[9C, 94, 8C, 84]_x[D0, C0][31:29]) to 010b and Link Phy Impedance Register[RttIndex] (F4x1[9C, 94, 8C, 84]_x[D0, C0][20:16]) to 00100b.

Fix Planned

Yes

328 BIST May Report Failures on Initial Powerup

Description

When BIST is run after initial powerup, a non-zero (i.e., failing) value may be erroneously reported in EAX.

Subsequent BIST runs (induced by warm resets) are not affected by this erratum, and accurately report pass/fail as determined by the presence or absence of detectable defects in the structures tested.

Potential Effect on System

The processor may incorrectly represent itself as being defective on initial powerup. The system response to this is system software dependent.

Suggested Workaround

On initial powerup, system software should disregard the BIST result in EAX.

Fix Planned

Yes

336 Instruction Based Sampling May Be Inaccurate

Description

The processor may experience sampling inaccuracies when instruction based sampling (IBS) is enabled in the following cases:

- The IBS may not tag an operation when the current counter in IBS Execution Control Register[IbsOpCurCnt] (MSRC001_1033[51:32]) reaches the value in IBS Fetch Control Register[IbsOpMaxCnt] (MSRC001_1030[15:0], resulting in a missed sample. When this occurs, the IBS counter rolls over without an interrupt.
- The selection of instructions for IBS may be significantly skewed due to effects of instruction cache misses and branch prediction. As a result, certain instructions may be tagged less frequently than other instructions even when executed in the same code block.

Potential Effect on System

Inaccuracies in performance monitoring software may be experienced. Despite this erratum, IBS can be used effectively for identifying performance issues associated with specific instructions. The sampling bias makes IBS less effective for measuring statistical distribution of operations and events across a large code sequence on affected silicon revisions.

Suggested Workaround

None.

Fix Planned

Yes

337 CPU Instruction Based Sampling Fields May Be Inaccurate

Description

The processor may experience sampling inaccuracies when instruction based sampling (IBS) is enabled in the following fields:

- IBS Op Data Register[IbsCompToRetCtr] (MSRC001_1035[15:0]) may be incorrect for floating point instructions, when IBS Op Data 3 Register[IbsStOp] (MSRC001_1037[1]) is set, or when IBS Op Data 3 Register[IbsLdOp] (MSRC001_1037[0]) is set.
- IBS Op Data 3 Register[IbsDcMissLat] (MSRC001_1037[47:32]) may be incorrect if the processor tags a load instruction for IBS and the data for a retired store operation is in the process of being written to the data cache. As a result, IbsDcMissLat may start counting early when the load instruction is tagged and may be non-zero on a data cache hit.
- IBS Op Data 3 Register[IbsDcStToLdFwd, IbsDcL2TlbHit2M, IbsDcL2TlbMiss] (MSR_C001_1037[11, 6, 3]) may be incorrect when IBS Op Data 3 Register[IbsDcStBnkCon] (bit 10) or IBS Op Data 3 Register[IbsDcLdBnkCon] (bit 9) are set.
- IBS Op Data 3 Register[IbsLdOp, IbsStOp] (MSRC001_1037[1:0]) may be set incorrectly for non load/store instructions that are tagged for IBS. Other fields in MSRC001_1037 may also be set based on an unrelated instruction. This occurs when a load/store instruction is tagged and then a branch misprediction causes it to be canceled. When a new instruction is tagged for IBS, it may trigger incorrect information if the same buffers are used for both instructions. This typically would not result in a statistically significant number of incorrect samples.
- IBS Op Logical Address Register (MSR C001_1034) may not point to the sampled instruction when highly specific conditions are met for the sampled and surrounding instructions. In these cases, the address reported may be 16 bytes past the sampled instruction and may not point to the beginning of an actual instruction.

Potential Effect on System

Inaccuracies in performance monitoring software may be experienced.

Suggested Workaround

None.

Fix Planned

Yes

338 Northbridge Instruction Based Sampling Fields May Be Inaccurate

Description

The IBS Op Data 2 Register[NbIbsReqDstProc] (MSRC001_1036[4]) may be incorrect when the Northbridge is performing back-to-back operations while an instruction tagged for instruction based sampling (IBS) is executed and IBS Op Data 2 Register[NbIbsReqSrc] (MSRC001_1036[2:0]) is 011b or 111b. This typically would not result in a statistically significant number of incorrect samples.

Potential Effect on System

Inaccuracies in performance monitoring software may be experienced.

Suggested Workaround

None.

Fix Planned

Yes

339 APIC Timer Rollover May Be Delayed

Description

The APIC timer does not immediately rollover when it transitions to zero and Timer Local Vector Table Entry[Mode] (APIC320[17]) is configured to run in periodic mode. In addition, when Timer Local Vector Table Entry[Mask] (APIC320[16]) is configured to generate an interrupt, the interrupt is also delayed whether configured for periodic or one-shot mode.

The per rollover error that may be observed is between 35 and 90 ns.

For systems that support C1E, the per rollover error may be as high as 640 ns if the roll over occurs while the processor is in the C1E state.

Potential Effect on System

None expected. The standard use of the APIC timer and the level of accuracy required does not make the error significant.

Suggested Workaround

None required.

Fix Planned

No

342 SMIs That Are Not Intercepted May Disable Interrupts

Description

During a resume from SMM that is due to an unintercepted SMI from a SVM guest context, the processor core does not restore the correct effective interrupt flag (IF) if the guest VMCB V_INTR_MASKING bit (offset 060h bit 24) is 1b. Under these circumstances, the effective interrupt flag may be zero.

SMIs are not intercepted if VMCB offset 00Ch bit 2 is 0b or HWCR[SmmLock] (MSRC001_0015[0]) is 1b.

Potential Effect on System

The guest context may run with interrupts disabled until the next guest intercept. The hypervisor may not be able to regain control and the system may hang.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

343 Eviction May Occur When Using L2 Cache as General Storage During Boot

Description

When system software is using the L2 cache as general storage before memory initialization, the processor may determine during speculative execution that data destined for the instruction cache is dirty. The processor will then evict these cache lines, resulting in lost data.

Potential Effect on System

System software using L2 cache as general storage before memory initialization may experience unpredictable system behavior.

Suggested Workaround

System software should set MSRC001_102A[35] to 1b prior to using L2 cache as general storage during boot. System software should clear MSRC001_102A[35] to 0b after the L2 cache is no longer used as general storage.

Fix Planned

No

344 Intermittent HyperTransport™ Link Training Failures

Description

The HyperTransport™ link training may fail at speeds greater than 2.0 GT/s.

Potential Effect on System

When exiting from S3, S4 or S5 state, the system may hang when a reset or LDTSTOP is applied and the link speed is greater than 2.0 GT/s. In addition, when F0x[18C:170][Ls2En] is set the system may hang exiting from LS2 link power state if the link speed is greater than 2.0 GT/s.

Suggested Workaround

System software should set bit 6 of F4x1[9C, 94, 8C, 84]_x[78:70, 68:60]. The bits should be set before the link frequency is changed from the cold reset value.

Fix Planned

No

346 System May Hang if Core Frequency is Even Divisor of Northbridge Clock

Description

When one processor core is operating at a clock frequency that is higher than the Northbridge clock frequency, and another processor core is operating at a clock frequency that is an even divisor of the Northbridge clock frequency, the Northbridge may fail to complete a cache probe.

Potential Effect on System

System hang.

Suggested Workaround

System software should set F3x188[22] to 1b.

Fix Planned

Yes

348 Processor On-die Termination Resistance is Higher than Specification

Description

The actual processor on-die termination resistance for DDR2 mode differs from the values specified for F2x[1, 0]9C_x00[29:28] (ProcOdt) in the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116 as shown in the table below:

ProcOdt	Specification in DDR2 mode	Silicon Implementation
00b	300 ohms +/- 20%	480 ohms +/- 20%
01b	150 ohms +/- 20%	240 ohms +/- 20%
10b	75 ohms +/- 20%	120 ohms +/- 20%
11b	Reserved	Reserved

Potential Effect on System

Increased ODT resistance may affect DDR2 memory margins.

Suggested Workaround

None.

Fix Planned

Yes

350 DRAM May Fail Training on Cold Reset

Description

The DRAM DQS DLL may not lock after PWROK is asserted, resulting in a DRAM training failure.

Potential Effect on System

The system may fail to boot.

Suggested Workaround

During DRAM controller (DCT) initialization, system software should perform the following workaround to every enabled DCT in the system:

1. Perform a dummy DRAM read to any address on any DIMM attached to the DCT.
2. Write 0000_8000h to register F2x[1, 0]9C_xD080F0C.
3. Wait at least 300 nanoseconds.
4. Write 0000_0000h to register F2x[1, 0]9C_xD080F0C.
5. Wait at least 2 microseconds.

When exiting from the S4 or S5 state, apply the workaround immediately prior to the Receiver Enable Training. During resume from the S3 state, apply the workaround after F2x[1, 0]90[ExitSelfRef] has been cleared and prior to restoring the F2x[1, 0]9C registers.

Fix Planned

Yes

351 HyperTransport™ Technology LS2 Low-Power Mode May Not Function Correctly

Description

The HyperTransport™ technology LS2 low-power state may not function correctly in all systems.

Potential Effect on System

System hang or video distortion due to excessive latency.

Suggested Workaround

System software should program the Link Extended Control Registers[LS2En] (F0x[18C:170][8]) to 0b for all links. This allows the LS1 low-power state to be used as an alternative to LS2. System software should also program Link Global Extended Control Register[ForceFullT0] (F0x16C[15:13]) to 000b.

Fix Planned

Yes

352 SYSCALL Instruction May Execute Incorrectly Due to Breakpoint

Description

A SYSCALL instruction will execute incorrectly and an incorrect debug exception will be taken when all of the following conditions are satisfied:

- An enabled instruction breakpoint address matches the RIP of the SYSCALL instruction.
- The processor is in 64-bit mode or compatibility mode.
- The instruction would not generate any other exception.
- SYSCALL Flag Mask Register[16] (MSRC000_0084[16]) is set to 1b.
- RFLAGS.RF is set to 1b.

Potential Effect on System

None expected during normal operation. Kernel debuggers may observe unpredictable system behavior.

Suggested Workaround

Operating system software should clear SYSCALL Flag Mask Register[16] (MSRC000_0084[16]) to 0b during initialization.

Fix Planned

Yes

353 SYSRET Instruction May Execute Incorrectly Due to Breakpoint

Description

A SYSRET instruction will execute incorrectly and an incorrect debug exception will be taken when all of the following conditions are satisfied:

- An enabled instruction breakpoint address matches the RIP of the SYSRET instruction.
- The processor is in 64-bit mode or compatibility mode.
- The instruction would not generate any other exception.
- R11[16] is cleared to 0b.
- RFLAGS.RF is set to 1b.

Potential Effect on System

None expected during normal operation. Kernel debuggers may observe unpredictable system behavior.

Suggested Workaround

Software should set R11[16] to 1b before executing the SYSRET instruction in 64-bit mode.

Fix Planned

Yes

354 HyperTransport™ Link Training Failure

Description

Some processors may fail HyperTransport™ link training at speeds greater than 2.0 GT/s. The link training failure may be intermittent.

Potential Effect on System

When exiting from S3, S4 or S5 state, the system may hang when a reset or LDTSTOP is applied and the link speed is greater than 2.0 GT/s. In addition, when F0x[18C:170][Ls2En] is set the system may hang exiting from LS2 link power state if the link speed is greater than 2.0 GT/s.

Suggested Workaround

System software should set bit 6 of F4x1[9C,94,8C,84]_x[58:50, 48:40] for all links. The bits should be set before the link frequency is changed from the cold reset value.

Fix Planned

Yes

355 DRAM Read Errors May Occur at Memory Speeds Higher than DDR2-800

Description

The processor DRAM interface may miss a beat of data under conditions of back-to-back read bursts to the same chip select using DDR2-1066 memory speed, resulting in incorrect data read by the DRAM interface until a processor reset occurs. This issue is sensitive to processor VDDIO and VTT voltage settings.

Potential Effect on System

Undefined system behavior that usually results in a system hang due to a triple fault.

Suggested Workaround

None.

Fix Planned

Yes

359 MEMCLK is Not Provided for Minimum Specified Time Before CKE Assertion

Description

During hardware DDR2 device initialization, the processor does not provide a running MEMCLK for the specified minimum time of 200 us before CKE is asserted.

Potential Effect on System

No adverse effects have been observed. The processor does not initiate a DRAM access for over 200 us from the start of MEMCLK and the assertion of CKE. If a DDR2 DIMM is sensitive to this issue, the system may fail to boot.

Suggested Workaround

None required.

Fix Planned

Yes

360 DRAM CKE and Address Drive Strength Values May Be Incorrect

Description

The processor does not correctly assign DRAM Output Driver Compensation Control Register[CkeDrvStren] (F2x[1,0]9C_x00[1:0]) and DRAM Output Driver Compensation Control Register[AddrCmdDrvStren] (F2x[1,0]9C_x00[9:8]) to the specified DRAM pins. Differences from the specified assignments are shown in the following table; other assignments are not affected:

Register Field	Extra Assigned DRAM Pins	Missing Assigned DRAM Pins
CkeDrvStren	DRAM address pins 1, 2 and 3	CKE
AddrCmdDrvStren	CKE	DRAM address pins 1, 2 and 3

This erratum applies only when programming two different settings to the CkeDrvStren and AddrCmdDrvStren register fields. Functionality is correct when the two register fields are programmed to identical values.

Potential Effect on System

Pin drive strengths that differ from those expected may affect memory margins.

Suggested Workaround

No workaround required for system designers using AMD recommended values in these fields. With the AMD recommended values, the erratum does not apply to any settings in 1T timing mode. A workaround is not necessary in 2T timing mode as the impact of this erratum to overall memory margins is minimal.

Fix Planned

No

361 Breakpoint Due to an Instruction That Has an Interrupt Shadow May Be Lost

Description

A #DB exception occurring in guest mode may be discarded under the following conditions:

- A trap-type #DB exception is generated in guest mode during execution of an instruction with an interrupt shadow, and
- The instruction that generated the exception is immediately followed by an instruction resulting in #VMEXIT.

Potential Effect on System

None expected under normal conditions. Programs running under a hypervisor may not receive an expected #DB exception.

Suggested Workaround

None.

Fix Planned

No

362 Illegal Packet on HyperTransport™ Link May Prevent Warm Reset

Description

The processor may fail to drive external pins to their reset pattern when warm reset is asserted, and may fail to restart after warm reset is subsequently deasserted, when both of the following conditions are satisfied:

- The processor has received an illegal packet from a non-coherent HyperTransport™ link with a specific encoding only used on coherent links. This packet may be detected near a warm reset as the processor may sample packets on the link for a brief time after warm reset is asserted. On some platforms, the conditions under which the processor may receive an illegal packet near a warm reset may not be observed. If link retry mode is enabled, this erratum applies only if the incoming illegal packet contains a valid CRC.
- One or more processor cores is in the C1 halt state with clocks ramped down. If C1 ACPI Power State Control Registers [CpuPrbEn] (F3x84[24]) = 1b, clocks are considered as ramped down for a processor core in the C1 halt state for any valid setting of F3x84[31:29] (ClkDivisor) other than 000b.

Potential Effect on System

System hang during a warm reset. This erratum does not impact cold reset or INIT.

Suggested Workaround

None required for platforms that do not observe this issue. For other platforms, platform BIOS should set a global SMI trap on any write to a port that could cause warm reset to assert, and then execute the write from within the SMI handler. This ensures that no cores have clocks ramped down when warm reset is asserted. This workaround is not effective for warm resets that are initiated without a software write to a port that can be trapped.

Fix Planned

Yes

370 DRAM Read Errors May Occur at DDR2-800 Memory Speeds With Higher Read DQS Delays

Description

The processor DRAM interface may miss a beat of data under conditions of back-to-back read bursts to the same chip select using DDR2-800 memory speeds, resulting in incorrect data read by the DRAM interface until a processor reset occurs. This issue is sensitive to higher levels of jitter on the read DQS inputs from DRAM in combination with higher settings of DRAM Read DQS Timing Control [High:Low] Registers[RdDqsTimeByte][7:0] at offsets F2x[1, 0]9C_x[3:0]0[6:5].

Potential Effect on System

For systems without ECC, undefined system behavior that usually results in a system hang due to a triple fault. Systems with ECC enabled may experience repeated multiple-bit ECC errors.

Suggested Workaround

If the system DRAM speed is DDR2-800, system software should constrain the settings of F2x[1, 0]9C_x[3:0]0[6:5][RdDqsTimeByte][7:0] obtained from DRAM training to values of 0Ch or less. Implementation of this workaround may have a nominal effect on DDR2-800 memory margins.

Fix Planned

Yes

372 Processor Read That Matches The Address of an Earlier Uncompleted Write May Be Incorrect

Description

Under highly specific and detailed internal timing conditions, processor data for a read may be corrupted when a read occurs that matches the address of an earlier uncompleted write or L3 eviction.

This erratum applies only when both of the following conditions are satisfied on any processor node:

- DRAM controllers are in DCT link unganged mode ([DRAM Controller Select Low Register] F2x110[DctGangEn] = 0b).
- The Northbridge current operating frequency (COF) is less than 3 times the memory clock frequency.

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

On systems supporting DDR3-1333 and using DCT link unganged mode, system software should set MSRC001_001F[52:51] to 11b.

Fix Planned

No

373 Processor Write to APIC Task Priority Register May Cause Error Status Bit to Set

Description

The processor may set Error Status Register[Send Accept Error] (APIC280[2]) after a write to a Task Priority Register (APIC080). This can occur only if a write to APIC080 follows a write to an Interrupt Command Register (APIC3[1, 0]0) that triggers an interprocessor interrupt (IPI).

This erratum does not apply if the IPI message type set on APIC3[1, 0]0[10:8] is 011b (remote read), or if an L3 cache is present.

Potential Effect on System

Software may observe and report a false APIC error.

Suggested Workaround

If an L3 cache is not present as indicated by CPUID Fn8000_0006_EDX[L3Size] (CPUID Fn8000_0006_EDX[31:18]) being equal to zero, system software should set MSRC001_001F[57] to 1b.

Fix Planned

No

374 Processor Read From L3 Cache May Return Stale Data

Description

Under highly specific and detailed internal timing conditions, a processor read from the L3 cache may return stale data.

Potential Effect on System

Unpredictable system behavior due to incorrect read data.

Suggested Workaround

System software should set F3x1B8[18] to 1b.

Fix Planned

Yes

378 Processor May Operate at Reduced Frequency

Description

When Product Information Register F3x1FC[31] is set, the reset values of the P-State Registers (MSRC001_00[68:64]) are not compliant with prior algorithms used to specify the P-state frequencies. Only one P-state register has bit 63 (PstateEn) set and the CPU frequency specified by this P-State register is below the maximum operating frequency for the processor.

Potential Effect on System

AM3 package processors may experience performance degradation when installed in an AM2r2 or AM3 platform.

Suggested Workaround

No workaround exists for AM2 platforms.

On AM2r2 and AM3 platforms, if F3x1FC[31] is set BIOS must follow the updated algorithm to write MSRC001_00[68:64] with corrected values, as documented in revision 3.23 or later versions of the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116.

Fix Planned

No

379 DDR3-1333 Configurations with Two DIMMs per Channel May Experience Unreliable Operation

Description

In systems with more than one DDR3-1333 unbuffered DIMM on a channel, the processor memory subsystem may exhibit unreliable operation over the allowable VDDIO voltage range.

This erratum does not apply to DDR3-1333 configurations when only one DIMM per channel is populated.

Potential Effect on System

Memory system failure leading to unpredictable system behavior.

Suggested Workaround

In a configuration where two unbuffered DDR3-1333 DIMMs are populated on one channel, BIOS should derate DDR3-1333 system memory to 533 MHz operation (DDR3-1066) by setting the DRAM Configuration High Register[MemClkFreq] (F2x[1, 0]94[2:0]) to 100b and adjusting memory subsystem timing parameters accordingly.

Fix Planned

Yes

382 L3 Cache Index Disable Cannot Be Modified After L3 Cache is Enabled

Description

The processor does not support the disabling of L3 locations through use of the L3 Cache Index Disable Registers (F3x[1C0, 1BC]) after the cache subsystem has been enabled through CR0.

Potential Effect on System

If software modifies F3x[1C0, 1BC] after the L3 cache has been enabled through CR0, unpredictable system behavior may result.

Suggested Workaround

None.

Fix Planned

Yes

384 DRAM Prefetch May Cause System Hang When Probe Filter is Enabled

Description

When the processor is accessing memory with the probe filter and DRAM prefetch enabled, a DRAM prefetch may not complete.

Potential Effect on System

System hang.

Suggested Workaround

If the probe filter is enabled, system software should program MSRC001_001F[20] to 1b.

Fix Planned

Yes

385 Processor May Report Incorrect Address For an L3 Cache Error Machine Check

Description

The processor may report an incorrect address at NB Machine Check Address Register MSR0000_0412 when executing a machine check for an L3 cache error. In addition, when disabling an L3 cache index by writing to L3 Cache Index Disable Registers F3x[1C0, 1BC] [Index], the processor may not disable the intended L3 cache index.

Potential Effect on System

Operating system software may take inappropriate action due to an incorrectly reported L3 cache error.

Suggested Workaround

System software should program F3x1B8[23] to 1b before enabling the L3 cache through CR0[30] (CD).

Fix Planned

No

386 HyperTransport™ Link in Retry Mode That Receives Repeated Invalid Packets May Cause MCA Exception

Description

Under highly specific and detailed internal timing conditions, a HyperTransport™ link in retry mode that receives repeated invalid packets in a specific sequence may cause the processor to generate a link data buffer overflow MCA exception.

This erratum applies only when a link is configured as 16-bit ganged and the Northbridge current operating frequency is less than the link clock frequency.

Potential Effect on System

System hang. A link data buffer overflow MCA exception will also be reported.

Suggested Workaround

System software should program the Link Base Channel Buffer Count Registers F0x[F0, D0, B0, 90][27:25] (FreeData) to 000b to disable all free list link data buffers. To maximize system performance when applying this workaround on NFCM coherent links, system software should modify the settings for F0x[F0, D0, B0, 90] as specified in the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116, per the following table:

Register/Field	NFCM Coherent Link Modified Setting
FreeData	0
FreeCmd	8
RspData	3
NpReqData	2
ProbeCmd	8
RspCmd	9
PReq	3
NpReqCmd	4

Fix Planned

Yes

387 Performance Counters Do Not Accurately Count L3 Cache Evictions

Description

The processor does not report the correct count of L3 cache evictions when Performance Event Select Register (PERF_CTL[3:0]) MSRC001_000[3:0][EventSelect] is 4E3h. This erratum applies to all unit mask settings for this event.

Potential Effect on System

Performance monitoring software will not be able to count L3 cache evictions with this event counter.

Suggested Workaround

Performance monitoring software can use EventSelect 0EAh, UnitMask 01h as an alternate method to count victim block writebacks.

Fix Planned

No

388 L3 Cache Scrubbing Does Not Bypass Disabled L3 Cache Locations

Description

The processor does not discontinue scrubbing L3 cache locations that are disabled through the L3 Cache Index Disable Registers F3x[1C0, 1BC].

Potential Effect on System

ECC errors that occur when scrubbing disabled L3 cache locations can generate unexpected machine check exceptions.

Suggested Workaround

System software should program Scrub Rate Control Register F3x58[28:24] (L3Scrub) to 00000b before disabling any L3 cache locations. This workaround should not be applied when all L3 cache locations are enabled.

Fix Planned

Yes

389 HyperTransport™ Link in Retry Mode May Consume Link Packet Buffer Incorrectly

Description

Under highly specific and detailed internal timing conditions, a coherent HyperTransport™ link in retry mode that receives an invalid per-packet CRC may cause the processor to incorrectly consume a link packet buffer during link retry. This erratum applies only when F0x150[11:9] (HtRetryCrcDatIns) is set to a value other than 000b.

Potential Effect on System

System hang.

Suggested Workaround

When CPUID Fn0000_0001_EAX[7:4] (Model) < 8, no workaround is required. For system developers that wish to provide a workaround for this event, system software may clear F0x150[11:9] (HtRetryCrcDatIns) to 000b.

System software should clear F0x150[11:9] (HtRetryCrcDatIns) to 000b for all other affected silicon revisions.

Fix Planned

Yes

391 HyperTransport™ Link R_{TT} and R_{ON} Specification Violations

Description

The R_{TT} and R_{ON} specifications of the HyperTransport™ link may be violated on some lanes.

Potential Effect on System

These violations do not result in any functional failures on HyperTransport™ links.

Suggested Workaround

None.

Fix Planned

No

393 Performance Monitor May Count Fastpath Double Operation Instructions Incorrectly

Description

The processor does not report the correct count for all fastpath double operation instructions when Performance Event Select Register (PERF_CTL[3:0]) MSRC001_000[3:0][EventSelect] is 0CCh. This erratum applies to all unit mask settings for this event.

Potential Effect on System

Performance monitoring software will not have an accurate count of fastpath double operation instructions.

Suggested Workaround

None.

Fix Planned

No

395 Incorrect Data Masking in Ganged DRAM Mode

Description

The DRAM controller may apply incorrect DRAM data masks when operating in ganged mode (DRAM Controller Select Low Register[DctGangEn] (F2x110[4]) is set to 1b).

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

The DRAM controllers should only be configured in the unganged mode. BIOS should not set DRAM Controller Select Low Register[DctGangEn] (F2x110[4]). When only a single DCT is in use, DctGangEn is always zero.

Fix Planned

Yes

Documentation Support

The following documents provide additional information regarding the operation of the processor:

- *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116
- *AMD64 Architecture Programmer's Manual Volume 1: Application Programming*, order# 24592
- *AMD64 Architecture Programmer's Manual Volume 2: System Programming*, order# 24593
- *AMD64 Architecture Programmer's Manual Volume 3: General-Purpose and System Instructions*, order# 24594
- *AMD64 Architecture Programmer's Manual Volume 4: 128-Bit Media Instructions*, order# 26568
- *AMD64 Architecture Programmer's Manual Volume 5: 64-Bit Media and x87 Floating-Point Instructions*, order# 26569
- *AMD CPUID Specification*, order# 25481
- *HyperTransport™ I/O Link Specification* (www.hypertransport.org)

See the AMD Web site at *www.amd.com* for the latest updates to documents.