SUN MICROELECTRONICS

STP2002QFP

August 2001

FEPS

DATA SHEET — Fast Ethernet, Parallel Port, SCSI

DESCRIPTION

The Fast Ethernet, Parallel Port, SCSI (FEPS) STP2002QFP provides an integrated high-performance fast and wide SCSI, 10/100Base-T Ethernet, and a Centronics-compatible parallel port.

FEATURES

- IEEE 1496 SBus Master interface with support for 64-bit mode access
- IEEE 1496 SBus Slave interface, 32-bit mode only
- 20-Mbps fast and wide single-ended SCSI using a QLogic FAS366 core
- 10-/100-Mbps Ethernet on the motherboard
- Media independent interface (MII) to support external transceivers
- DMA2-compatible Centronics parallel port with a maximum throughput of 4 Mbps
- Supports use on an SBus-card device
- Provides a path to an FCode PROM for use on SBus boards
- IEEE standard 1149.1 (JTAG) support for boundary- and internal-scan testing

FUNCTIONAL DESCRIPTION

Interface

The FEPS control and data path signal interfacing is shown in *Figure 1*.

A detailed listing for each pin is located on page 27 of this data sheet.

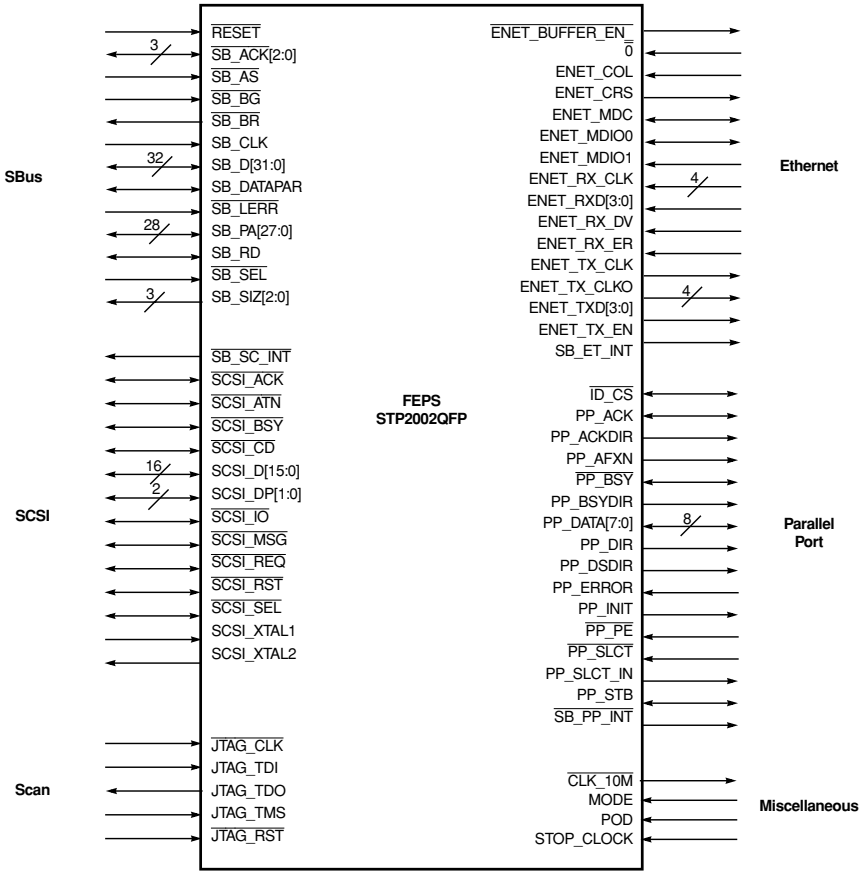


Figure 1. External Interfaces

Components

The FEPS internal block diagram is shown in *Figure 2*. The following is a description of each of the major components.

SBus Adapter (SBA)

This functional unit is the layer between the channel engine interface and the SBus. The SBA provides buffering and bus conversion between the SBus and channel engine interface. It includes one master port on the SBus side to funnel the SCSI, Ethernet, and parallel port engines onto the SBus, and one slave port to provide SBus access to those three engines. The SBA's primary function is data path and flow control between the SBus and the channel engine interface. The SBA supports only 32-bit programmed I/O on the SBus. There are two 64-byte DMA write buffers to allow buffered writes. A round-robin arbitration scheme is used between the three channel engines. Interrupts from the channel engines go directly to the SBus. The SBA contains no software-accessible registers.

The master accesses:

- are compliant with IEEE 1496.
- support 64-bit/32-bit transfer mode.
- support byte/half-word/word transfer size.
- support burst transfer size from 8 to 64 bytes.
- have parity generation/checking.
- do not issue atomic transactions.
- do not support bus sizing.

The slave accesses:

- support byte/half-word/word access, but not burst transfer
- support 32-bit transfer mode.
- have parity generation/checking.
- do not generate late error.
- do not generate Rerun Ack.
- Have a maximum latency of less than 22 SBus clocks.

Channel Engine Interface (CEI)

The CEI provides a common interface to the three channel engines, thus reducing verification time. This interface limits the amount of awareness that the SBA has concerning DMA transactions. The channel engine's DMA specifies a specific transaction size, and the SBA executes the exact transaction on the SBus. Signals in the CEI are either shared, going from the SBA to all of the engines, or dedicated, going from one channel engine to/from the SBA. Transactions include slave write, slave read, and DMA write (channel engine to memory).

Ethernet Channel Engine (ECE)

The two major functions of the ECE are to provide the media-access control (MAC) function for a 10-/100-Mbps CSMA/CD protocol-based network, and to provide a high-performance two-channel DVMA host interface between the BigMAC and the SBus. It is a high-performance, full-duplex device permitting simultaneous transfers of data to/from host memory to/from the "wire." The BigMAC portion of the ECE is compliant with the IEEE 802.3u (100Base-T) standard. It implements the management portion of the MII to an external transceiver, as defined in the IEEE 802.3 MII specification.

The Ethernet transmit functions provide the DMA engine for transferring frames from the host memory to the BigMAC. It contains a local buffer of 2K bytes for rate adaptation between the available bandwidth on SBus and on the network. The Ethernet receive functions supply the DMA engine for transferring frames from the BigMAC to the host memory. It also contains a local buffer of 2K bytes for rate adaptation. Other features include:

- Conformation to ISO / IEC 8802-3.
- Programmable network parameters for standard's extension and / or private applications.
- Flexible transceiver choice via the MII.
- Host packet management via descriptor rings.
- TCP checksum support in hardware.
- Transmit "gather" function.
- Programmable first by alignment on receive.
- Support for 32-bit or 64-bit SBus, maximum of 64-byte bursts.

SCSI Channel Engine

The SCSI channel consists of SCSI DVMA (also referred to as SCSI Channel Engine) and FAS366. FAS366 is a "fast and wide" SCSI controller core and is integrated as a hard macro into FEPS. The SCSI DVMA provides two 64-byte buffers used to transfer data to / from the FAS366. The FAS366 supplies a 16-bit SCSI data path and a throughput of 20 Mbps. All programmed I / O access to the FAS366 is driven by the SCSI DVMA.

Several programmable registers can be used by the SCSI device driver to direct the SCSI engine and FAS366 to move blocks of data to / from host memory or to / from devices on the SCSI bus. Once the transfer is complete, an interrupt is generated on the SBus to inform the driver that block movement is complete, freeing it to initiate further transfers.

Parallel Port Engine

This engine allows the CPU to send data to the standard Centronics printer in both programmed I / O and DMA modes. The parallel interface can support bidirectional transfers using Xerox (master read / write) and IBM (master write) schemes. A 64-byte buffer is used for data to and from the Channel Engine Interface and the parallel port in DMA mode, depending on the direction of the transfer. In synchrononus mode, the port can support a data transfer rate of up to 4 Mbps. The parallel port interface also provides the data path to read the FCode EPROM when the FEPS chip is used on an SBus-extended card. Two external 8-bit latches are needed for the most significant byte (MSB) and least significant byte (LSB) of the EPROM address.

JTAG

A JTAG Test Access Port and other testability features are built in to the FEPS chip. The JTAG macro, which implements the IEEE standard 1149.1-1990, provides access to the test structures on the chip.

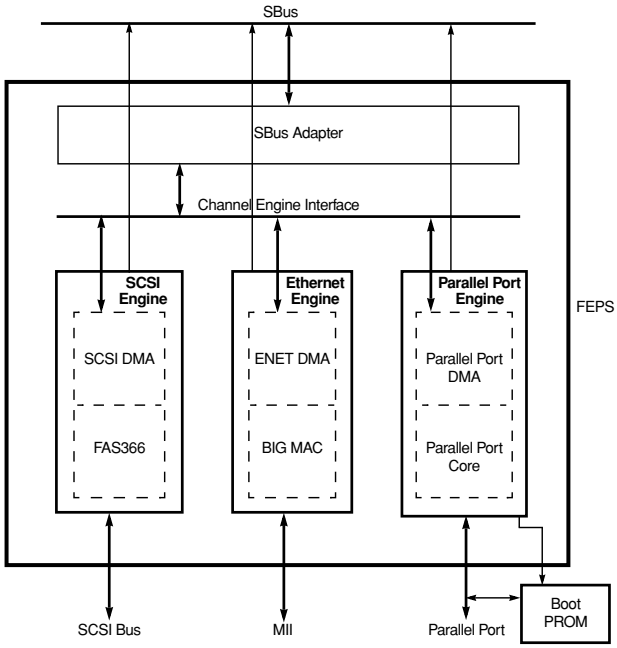


Figure 2. FEPS Functional Block Diagram

SIGNAL DESCRIPTIONS

SBus Interface Signals

Signal Name	I/O	Description
$\overline{\text{RESET}}$	I	Reset signal from the SBus controller; is used to reset all SBus devices at power-on or any other time necessary.
$\overline{\text{SB\_ACK}}$[2:0]	I/O	Slave acknowledge codes in response to master $\overline{\text{SB\_SEL}}$ signals. Decoded as follows: 210 000 = Idle/Wait 001 = Error acknowledgment 010 = Byte acknowledgment 011 = Rerun acknowledgment 100 = Word acknowledgment 101 = Double-word (64-bit) acknowledgment 110 = Half-word acknowledgment 111 = Reserved
$\overline{\text{SB\_AS}}$	I	SBus address strobe is asserted by the SBus controller when the physical address is valid and the appropriate slave $\overline{\text{SB\_SEL}}$ signal is set.
$\overline{\text{SB\_BG}}$	I	SBus bus grant, used in SBus arbitration; the SBus controller asserts this signal when the bus is available for the requesting master's use.
$\overline{\text{SB\_BR}}$	O	SBus bus request, used in SBus arbitration; the SBus master asserts this signal when it wants access to the bus.
SB_CLK	I	SBus clock is generated by the SBus controller. Its rising edge provides the SBus' timing reference and is used to sample synchronous signals.
SB_D[31:0]	I/O	SBus data, primarily a data path, but are also used to transfer virtual addresses to the SBus controller for translation.
SB_DATAPAR	I/O	SBus data parity; is driven so that the total number of signals in the checked group is an odd number. This signal can be generated at any time, but parity errors will only be reported if the data's source also generates parity.
$\overline{\text{SB\_LERR}}$	I	SBus late error; reports errors after an acknowledgment has already been issued. An alternate way to report errors, without generating an error acknowledgment.
SB_PA[27:0]	I/O	SBus physical address; the SBus controller drives the physical address lines with the results of the virtual address translation it performs for the SBus master.

SBus Interface Signals (Continued)

Signal Name	I/O	Description
SB_RD	I/O	SBus direction; is generated by the SBus master. When high during a transfer, this signal indicates a read (data transfer from slave to master) operation is requested. A write (data transfer from master to slave) operation is indicated if the signal is low.
$\overline{\text{SB\_SEL}}$	I	SBus slave select; each slave has its own unique SB_SEL. After the SBus controller has determined which slave is being addressed, it asserts that slave's SB_SEL.
SB_SIZ[2:0]	O	SBus size lines; the master encodes the size of the transfer it is to perform on these three lines. Their decodes, active high, are as follows: 210 000 = Word (4 bytes) transfer 001 = Byte transfer 010 = Half-word (2 bytes) transfer 011 = Extended transfer 100 = Four-word (16 bytes) transfer 101 = Eight-word (32 bytes) transfer 110 = Sixteen-word (64 bytes) transfer 111 = Two-word (8 bytes) transfer

SCSI Interface Signals

Signal Name	Type	Description
SB_SC_INT	O	SCSI interrupt request to the SBus
SCSI_ACK	I/O	SCSI acknowledge; a signal that acknowledges a REQ information transfer handshake
SCSI_ATN	I/O	SCSI attention
SCSI_BSY	I/O	SCSI busy; an OR-tied signal that indicates the bus is being used
SCSI_CD	I/O	SCSI control/data; indicates whether control (active low) or data (active high) information is on the data bus
SCSI_D[15:0]	I/O	SCSI data; 16-data-bit bus, bit 15 is the most significant bit and has the highest priority during the arbitration phase.
SCSI_DP[1:0]	I/O	SCSI data parity; bit 0 is odd parity (active low) for data bits SCSI_D[7:0], bit 1 is odd parity (active low) for SCSI_D[15:8].
SCSI_IO	I/O	SCSI direction; signal that controls the direction of data movement on the data bus with respect to the initiator. True (active low) indicates input.
SCSI_MSG	I/O	SCSI message; signal generated by a target during the message phase of the transfer sequence.
SCSI_REQ	I/O	SCSI request; signal generated by a target indicating a request for an ACK information transfer handshake.
SCSI_RST	I/O	SCSI reset; an OR-tied signal that indicates the RESET condition.
SCSI_SEL	I/O	SCSI select; an OR-tied signal used by an initiator to select a target, or by a target to reselect an initiator.
SCSI_XTAL1	I	Input connection for the 40-MHz crystal used to clock the SCSI controller core (FAS366)
SCSI_XTAL2	O	Output connection for the 40-MHz crystal

Ethernet Interface Signals

Signal Name	Type	Description
ENET_BUFFER_EN_0	O	Ethernet buffer enable; when active high, this signal enables the receive buffer on the board so the devices connected to the MII can be recognized.
ENET_COL	I	Ethernet collision; is set high upon detection of a collision on the medium and remains set while the collision condition persists. Can be set in response to a signal quality error.
ENET_CRS	I	Ethernet carrier sense; is set high when either the transmit or receive function is active. Is always set during a collision. Is cleared when both the transmit and receive functions are idle.
ENET_MDC	O	Ethernet management device clock; when active high, is the timing reference for transfer of information on the MDIO signal.
ENET_MDIO0	I/O	Ethernet management device I/O data for on-board transceiver 0; when active high, it is the transceiver in use.
ENET_MDIO1	I/O	Ethernet management device I/O data for on-board transceiver 1; when active high, it is the transceiver in use
ENET_RX_CLK	I	Ethernet receive clock; is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals.
ENET_RXD[3:0]	I	Ethernet receive data; is a bundle of four data signals which transition synchronously with respect to the RX_CLK. RXD[0] is the least significant bit.
ENET_RX_DV	I	Ethernet receive data valid; when active high, indicates that recovered and decoded nibbles on the RXD[3:0] bundle are being received and that the data is synchronous to RX_CLK.
ENET_RX_ER	I	Ethernet receive error; is set (active high) for one or more RX_CLK periods to indicate that an error (coding, etc.) was detected somewhere in the frame presently being transferred.
ENET_TX_CLK	I	Ethernet transmit clock; is a continuous clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals.
ENET_TX_CLKO	O	Ethernet transmit clock output; this output loops back the clock signal on the ENET_TX_CLK input.
ENET_TXD[3:0]	O	Ethernet transmit data; is a bundle of four data signals which transition synchronously with respect to the TX_CLK. TXD[0] is the least significant bit.
ENET_TX_EN	O	Ethernet transmit enable; when set (active high) indicates that nibbles are being presented on the MII for transmission. It is asserted with the first nibble of the preamble remains set while all nibbles are transmitted.
$\overline{\text{SB\_ET\_INT}}$	O	Ethernet interrupt; Ethernet request to the SBus.

Parallel Port Interface Signals

Signal Name	Type	Description
$\overline{\text{ID\_CS}}$	I/O	ID PROM chip select; selects the FCode PROM if FEPS is mounted on an SBus exapnsion slot.
PP_ACK	I/O	Parallel port acknowledge; is pulsed by the printer when it has received data from the parallel port.
PP_ACKDIR	O	Parallel port ack direction; the signal is high to output acknowledge to the target, low to input acknowledge from the target
PP_AFXN	O	Parallel port audio feed; ALE low address byte; is a dual-function pin. During normal operations, a high indicates autofeed is active. During boot operations, a high indicates the ALE low address byte is enabled for FCode access.
$\overline{\text{PP\_BSY}}$	I/O	Parallel port busy; indicates that the printer cannot accept another character.
PP_BSYDIR	O	Parallel port busy direction; the signal is high to output Busy to the target; low to input busy from the target.
PP_DATA[7:0]	I/O	Parallel port data bus; bidirectional data lines, D0 is the LSB, D7 is the MSB.
PP_DDIR	O	Parallel port data direction; is active high when data is being output to the target, and low when data is being input from the target.
PP_DSDIR	O	Parallel port data strobe direction; is active high when the data strobe is output to the target, and low when the data strobe is input from the target.
PP_ERROR	I	Parallel port error; set high by the printer when it has detected an error.
PP_INIT	O	Parallel port initialize; ALE high address byte; is a dual-function pin. During normal operations, a high indicates port initialization. During boot operations, a high indicates the ALE high address byte is enabled for FCode access.
$\overline{\text{PP\_PE}}$	I	Parallel port paper end; set low by the printer when it is out of paper.
$\overline{\text{PP\_SLCT}}$	I	Parallel port select; set low by the printer when it is selected.
PP_SLCT_IN	O	Parallel port select in; when high, this signal selects the printer.
PP_STB	I/O	Parallel port data strobe; indicates to the printer that valid data is available at the printer port.
$\overline{\text{SB\_PP\_INT}}$	O	Parallel port interrupt; parallel port interrupt request to the SBus.

JTAG/Miscellaneous Signals

Signal Name	Type	Description
CLK_10M	O	10-MHz clock output; sets the ENET clock for a 10-Mbps network with ticks at 200 ms
JTAG_CLK	I	JTAG clock; provides the timing signals during scan mode
JTAG_TDI	I	JTAG test data in; serial-bit stream for JTAG input data
JTAG_TDO	O	JTAG test data out; serial bit stream for JTAG output data
JTAG_TMS	I	JTAG test mode select; serial bit stream for controlling JTAG state machine
$\overline{\text{JTAG\_RST}}$	I	JTAG TAP reset; asynchronous JTAG state machine reset
MODE	I	Mode select; configures the FEPS in stand-alone (forced high to FCode PROM on the FEPS SBus card) mode for compatibility with MACIO and SLAVIO boards, or chipset (forced low to FCode PROM accessed on EBus through a SLAVIO ASIC) mode that will not conflict with the starting address of a PROM connected to SLAVIO.
POD	I	Power-on detect; used to tri-state the SCSI bus to allow FEPS to be power cycled (for example, during “hot plugging”) without generating glitches on the SCSI bus.
STOP_CLOCK	I	Used during testing in scan mode to stop the ENET and SBus clocks. Thereafter the JTAG clocks control the scan timing.

FEPS Address Map

PA[27:00]	Device
000_0000	FCode PROM
880_0000	SCSI channel
8C0_0000	Ethernet channel
C80_0000	Parallel port channel

Total Pin Count

Interface	Pin Count
JTAG/Scan	6
SBus	75
SCSI	30
Ethernet	20
Miscellaneous	28
Subtotal	159
Power/Ground	81
Total pin count	240

SIGNAL TIMING

The following diagrams represent timing conditions for the most common FEPS functions.

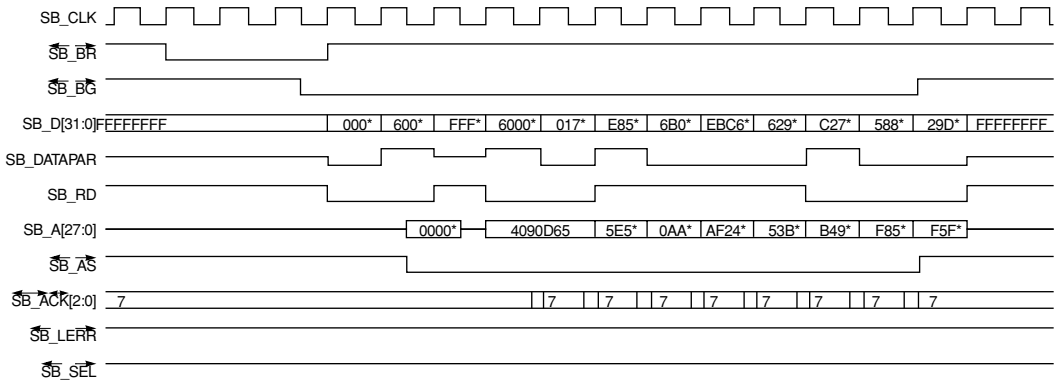


Figure 3. SBus Read

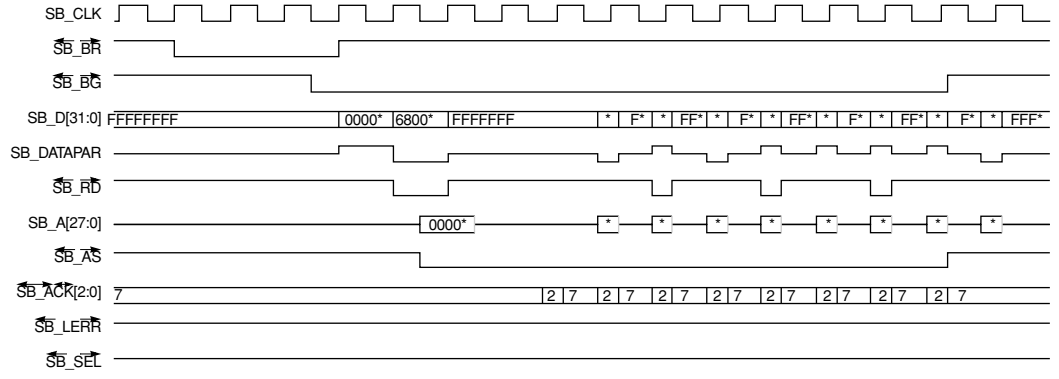


Figure 4. SBus Write

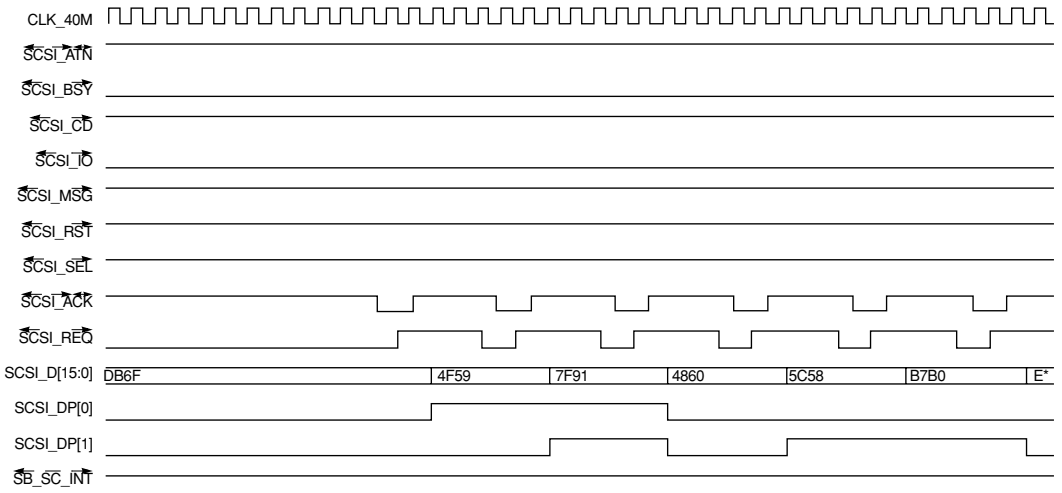


Figure 5. SCSI Asynchronous Read

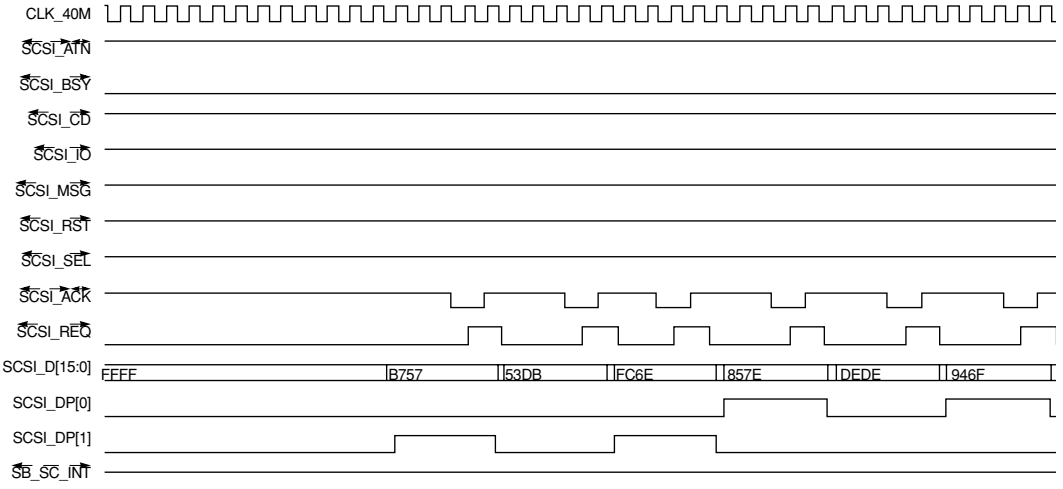


Figure 6. SCSI Asynchronous Write

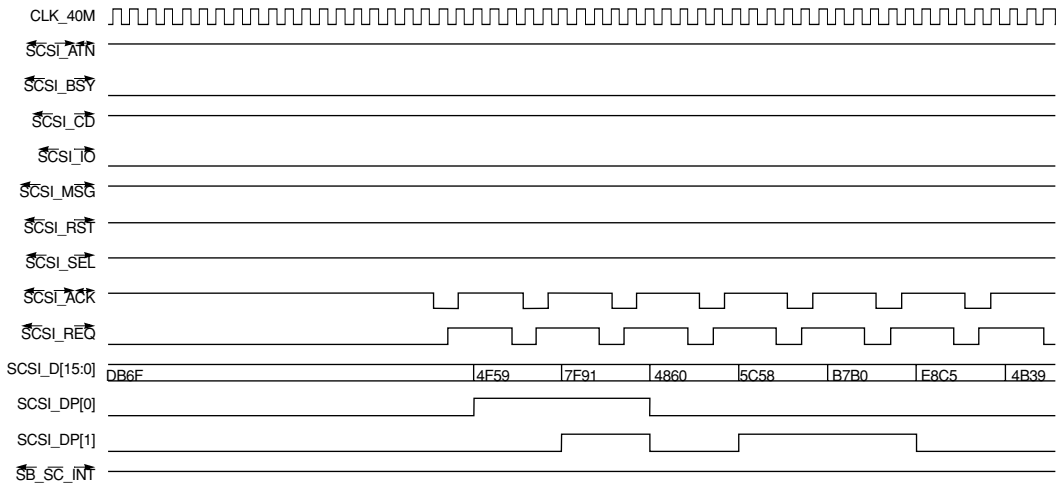


Figure 7. SCSI Synchronous Read

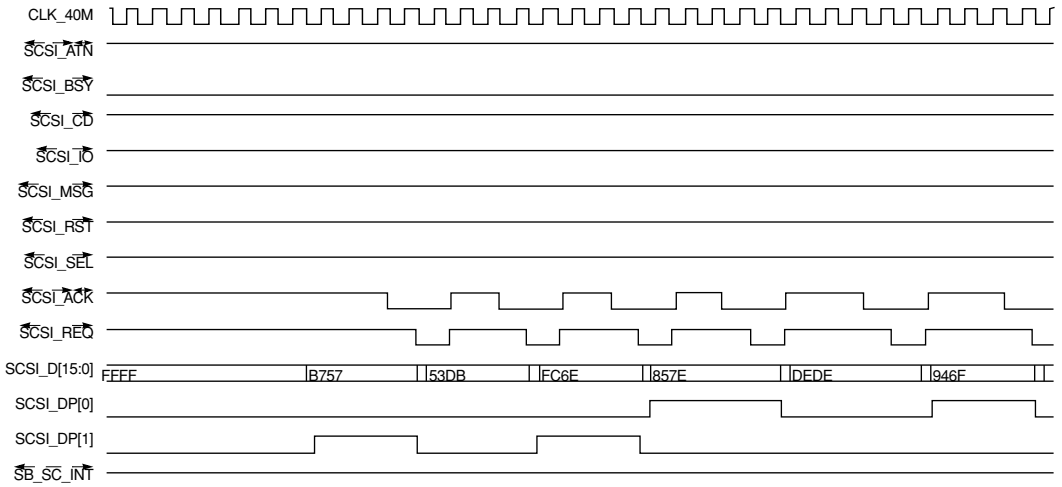


Figure 8. SCSI Synchronous Write

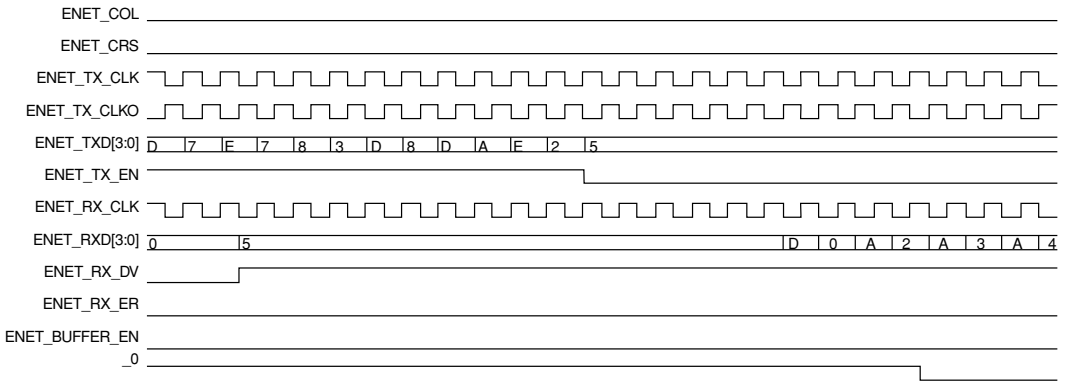


Figure 9. Ethernet Tx and Rx

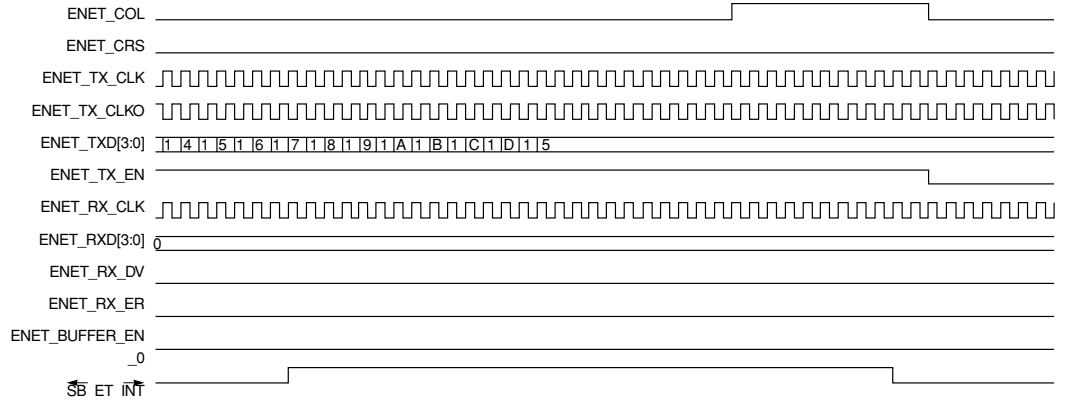


Figure 10. Ethernet–Collision Detected

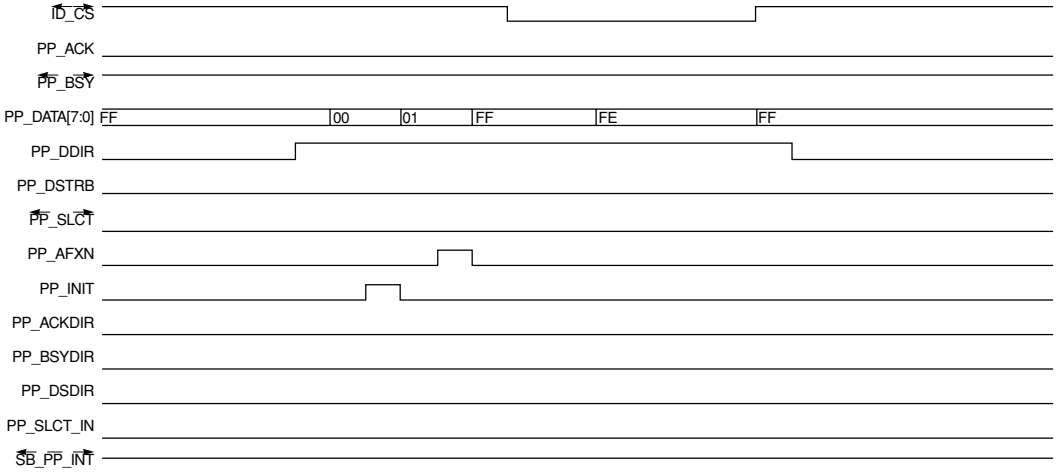


Figure 11. Parallel Port—EPROM Read

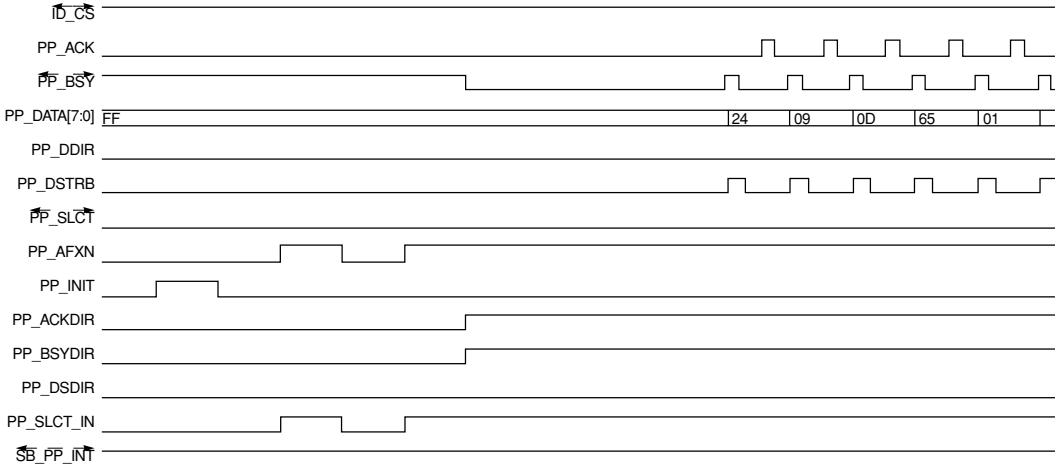


Figure 12. Parallel Port–IBM DMA Read

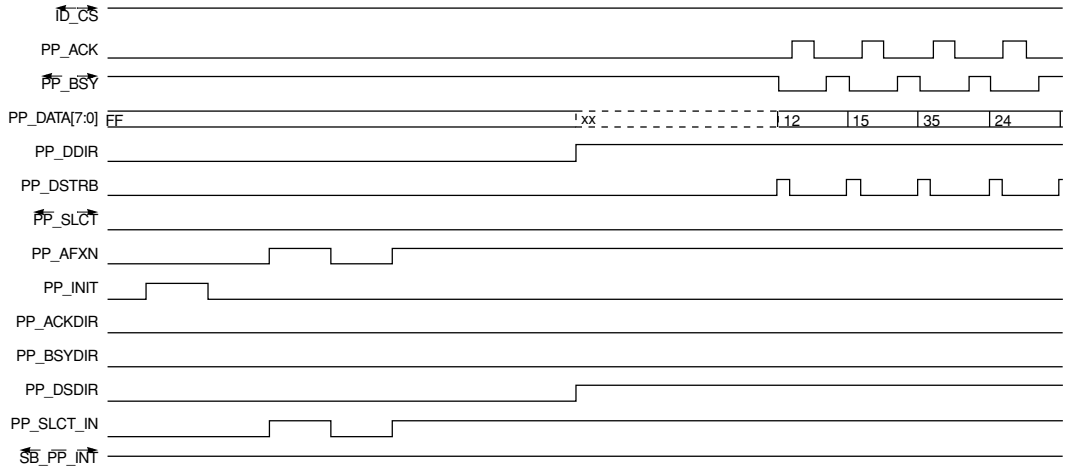


Figure 13. Parallel Port–IBM DMA Write

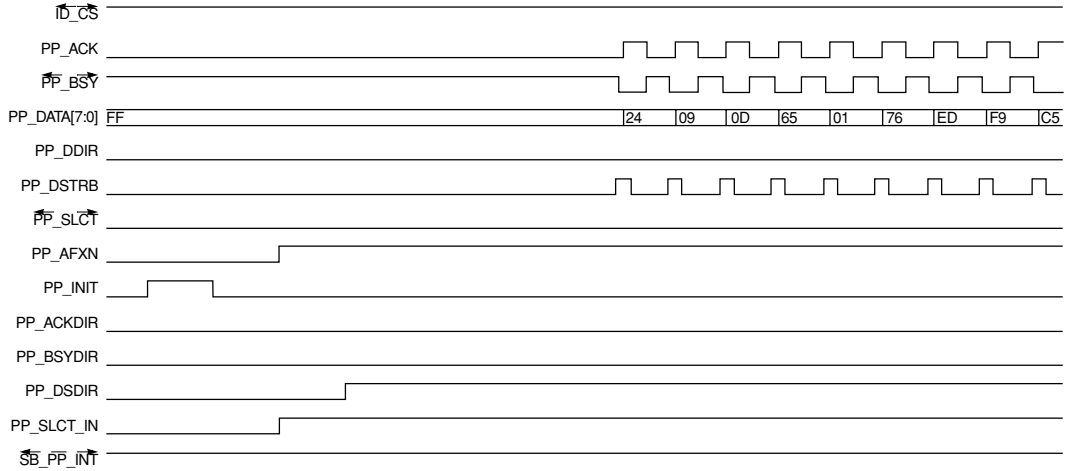


Figure 14. Parallel Port–Xerox DMA Read

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply voltage	–0.5	7	V
V_{IN}	Input voltage range	–0.5	V_{DD} + 0.5	V
I_{IN}	DC input current	–10	10	µA
P_D	Power dissipation	–	1.5	W

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD_CORE	Core DC supply voltage	4.75	5.0	5.25	V
VDD_IO	I/O DC supply voltage	4.75	5.0	5.25	V
V_{IN}	Input voltage	0	–	V_{DD}	V
T_A	Operating temperature at 100 lfm	0	–	70	˚C

DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	Voltage input low	TTL	–	0.80	V
		CMOS	–	$V_{DD} \times 0.3$	
V_{IH}	Voltage input high	TTL	2.0	–	V
		CMOS	$V_{DD} \times 0.7$	–	
V_{T+}	Low-to-high threshold voltage (Schmitt Trigger)	TTL	–	2.0	V
		CMOS	–	3.2	
V_{T-}	High-to-low threshold voltage (Schmitt Trigger)	TTL	0.95	–	V
		CMOS	1.40	–	
Hys	Minimum hysteresis (Schmitt Trigger)	TTL	350	–	mV
		CMOS	700	–	
V_{OL}	Voltage output low (TTL)	I_{OL} = 2 mA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 48 mA		0.4 0.4 0.4 0.4 0.4 0.4	V

DC Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Max	Units
V_{OL}	Voltage output low (CMOS)	I_{OL} = 2 mA		0.5	V
		I_{OL} = 4 mA		0.5	
		I_{OL} = 8 mA		0.5	
		I_{OL} = 16 mA		0.5	
		I_{OL} = 24 mA		0.5	
		I_{OL} = 48 mA		0.5	
V_{OH}	Voltage output high (TTL)	I_{OH} = -2 mA	2.4		V
		I_{OH} = -4 mA	2.4		
		I_{OH} = -8 mA	2.4		
		I_{OH} = -16 mA	2.4		
		I_{OH} = -24 mA	2.4		
		I_{OH} = -48 mA	2.4		
V_{OH}	Voltage output high (CMOS)	I_{OH} = -2 mA	V_{DD} – 0.5		V
		I_{OH} = -4 mA	V_{DD} – 0.5		
		I_{OH} = -8 mA	V_{DD} – 0.5		
		I_{OH} = -16 mA	V_{DD} – 0.5		
		I_{OH} = -24 mA	V_{DD} – 0.5		
		I_{OH} = -48 mA	V_{DD} – 0.5		
Over full process variation, V_{DD} = 4.5 to 5.5 volts					

AC Characteristics

SBus Interface Inputs

Input signals are $\overline{\text{RESET}}$, SB_CLK, $\overline{\text{SB\_SEL}}$, $\overline{\text{SB\_AS}}$, $\overline{\text{SB\_LERR}}$, $\overline{\text{SB\_BG}}$.

SBus Interface Input Signals

Parameter	Reference Signal	Description	Tester Condition	Value (ns)
t_{sck} (min)	SB_CLK	SBus clock period	–	40
t_{ss} (min)	SB_CLK	Setup time	–	15
t_{sh} (min)	SB_CLK	Hold time	–	1

SBus Interface Outputs

Output signals are $\overline{\text{SB\_BR}}$, $\overline{\text{SB\_ET\_INT}}$, $\overline{\text{SB\_SC\_INT}}$, $\overline{\text{SB\_PP\_INT}}$.

SBus Interface Output Signals

Parameter	Reference Signal	Description	Tester Condition (pF)	Value (ns)
t_{sd} (max)	SB_CLK	Propagation delay	30	16
t_{sd} (min)	SB_CLK	Propagation delay	30	2.5

SBus Interface Bidirectionals

Bidirectional signals are SB_D[31:0], SB_SIZ[2:0], SB_RD, $\overline{\text{SB\_ACK}}$[2:0], SB_DTPAR, SB_PA[27:0]. These signals must meet t_{ss} and t_{sh} on inputs. These signals must also meet t_{sd} on outputs.

Ethernet MII Inputs

For the signals ENET_RX_ERR, ENET_RX_DV, and ENET_RXD[3:0] see the Ethernet MII Input Signals table below.

Ethernet MII Input Signals

Parameter	Reference Signal	Description	Tester Condition	Value (ns)
t_{mrs} (min)	ENET_RX_CLK	Setup time	–	8
t_{mrh} (min)	ENET_RX_CLK	Hold time	–	10

ENET_CRS and ENET_COL are asynchronous in the system.

- ENET_RX_CLK input

  ENET_RX_CLK frequency should be equal to 25% of the data rate of the received signal. For example for 100-Mbps traffic, the frequency should be 25 MHz. The accuracy should be ± 5%. The duty cycle should be between 35–65%, both numbers inclusive.

- ENET_TX_CLKI input

  ENET_TX_CLKI frequency should be equal to 25% of the data rate of the transmit data rate. The tolerance is ± 5%. The duty cycle should be between 35% and 65%, both numbers inclusive.

Ethernet MII Outputs

For the signals ENET_TX_EN, ENET_TXD[3:0], and ENET_TX_CLKO, see the Ethernet MII Output Signals table below.

Ethernet MII Output Signals

Parameter	Reference Signal	Description	Tester Condition (pF)	Value (ns)
t_{mxd} (max)	ENET_TX_CLKI	Delay time	30	15
t_{mxd} (min)	ENET_TX_CLKI	Delay time	30	0

For signal $\overline{\text{ENET\_BUFFER\_EN}}$ see the $\overline{\text{ENET\_BUFFER\_EN}}$ Signal table below.

$\overline{\text{ENET\_BUFFER\_EN}}$ Signal

Parameter	Reference Signal	Description	Tester Condition (pF)	Value (ns)
t_{mbd} (max)	ENET_TX_CLKI	Delay time	30	30
t_{mbd} (min)	ENET_TX_CLKI	Delay time	30	0

For the signal ENET_MDC see the ENET_MDC Signal table below.

ENET_MDC Signal

Parameter	Reference Signal	Description	Tester Condition (pF)	Value (ns)
t_{mcd} (max)	SB_CLK	Delay time	30	30

Ethernet MII Bidirectionals

For the signals ENET_MDIO0 and ENET_MDIO1 see the ENET_MDIO0 and ENET_MDIO1 Signals table.

ENET_MDIO0 and ENET_MDIO1 Signals

Parameter	Reference Signal	Description	Tester Condition (pF)	Value (ns)
t_{mcs} (min)	SB_CLK	Setup time	–	8
t_{mch} (min)	SB_CLK	Hold time	–	38
t_{mcd} (max)	SB_CLK	Delay time	30	30
t_{mcd} (min)	SB_CLK	Delay time	30	50

SCSI Interface Clock Timing

For details on timings of the SCSI bus, refer to the FAS366 manual.

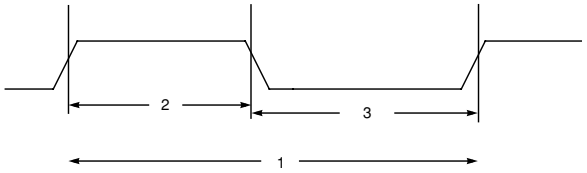


Figure 15. SCSI Clock

FASTCLK Bit Set or Reset

#	Symbol	Description	Min	Max	Unit	Note
1	t_{CP}	Clock period (1/frequency)	25	83.3	ns	–
	t_{CS}	Synchronization latency	t_{cl}	$t_{cl} + t_{cp}$	ns	–

FASTCLK Bit Reset

#	Symbol	Description	Min	Max	Unit	Note
	f_{CPA}	Clock frequency, asynchronous	12	25	MHz	–
	f_{CPS}	Clock frequency, synchronous	20	25	MHz	–
2	t_{CH}	Clock high	14.58	$0.65 \times t_{CP}$	ns	*a
3	t_{CL}	Clock low	14.58	$0.65 \times t_{CP}$	ns	*a

*a: For synchronous SCSI transfers and FASTCLK disabled, the clock must also meet the following requirements: $(2 \times t_{CP} + t_{CL} \geq 97.92$ ns) and $(2 \times t_{CP} + t_{CH} \geq 97.92$ ns).

FASTCLK Bit Set

#	Symbol	Description	Min	Max	Unit
	f_{CPA}	Clock frequency, asynchronous	20	40	MHz
	f_{CPS}	Clock frequency, synchronous	38	40	MHz
2	t_{CH}	Clock high	$0.40 \times t_{CP}$	$0.60 \times t_{CP}$	ns
3	t_{CL}	Clock low	$0.40 \times t_{CP}$	$0.60 \times t_{CP}$	ns

Note: The signal CLK_10M, which is an output from the FEPS, is the SCSI clock divided by 4 signal. So, for a 40-MHz SCSI clock, CLK_10M is a 10-MHz clock signal.

SCSI Interface Asynchronous Output Signals

Parameter	Description	Tester Condition (pF)	Value (ns)
t_{ardso} (min)	Data setup to reqn(out) low	30	60
t_{aadso} (min)	Data setup to ackn(out) low	30	60
t_{arhdo} (min)	Data hold from reqn(in) high	30	20
t_{aahdo} (min)	Data hold from ackn(in) low	30	30

SCSI Interface Asynchronous Input Signals

Parameter	Description	Tester Condition	Value (ns)
t_{arsdi} (min)	Data setup to reqn(in) low	–	0
t_{aadsi} (min)	Data setup to ackn(in) low	–	0
t_{arhdi} (max)	Data hold from reqn(in) low	–	15
t_{aahdi} (max)	Data hold from ackn(in) low	–	15

SCSI Interface Asynchronous Bidirectional Signals

Parameter	Description	Tester Condition (pF)	Value (ns)
t_{aaroh} (max)	ackn(in) low to reqn(out) high	30	50
t_{aarol} (max)	ackn(in) high to reqn(out) low	30	50
t_{araoh} (max)	reqn(in) high to ackn(out) high	30	50
t_{araol} (max)	reqn(in) low to ackn(out) low	30	50

SCSI Synchronous Output Signals

Parameter	Description	Tester Condition (pF)	Value (ns)
t_{sasto} (min)	reqn(out) or ackn(out) assertion period	30	90
t_{snego} (min)	reqn(out) or ackn(out) negation period	30	90
t_{sdso} (min)	Data setup to reqn(out) low or ackn(out) low	30	55
t_{shdo} (min)	Data hold from reqn(out) low or ackn(out) low	30	100

SCSI Synchronous Input Signals

Parameter	Description	Tester Condition	Value (ns)
t_{srasti} (min)	reqn(in) assertion period	–	25
t_{srnegi} (min)	reqn(in) negation period	–	20
t_{saasti} (min)	ackn(in) assertion period	–	20
t_{sanegi} (min)	ackn(in) negation period	–	20
t_{sdsi} (min)	Data setup to reqn(in) or ackn(in) low	–	5
t_{shdi} (min)	Data hold to reqn(in) or ackn(in) low	–	15

SCSI Fast Synchronous Output Signals

Parameter	Description	Tester Condition (pF)	Value (ns)
t_{sasto} (min)	reqn(out) or ackn(out) assertion period	30	30
t_{snego} (min)	reqn(out) or ackn(out) negation period	30	30
t_{sdso} (min)	Data setup to reqn(out) low or ackn(out) low	30	25
t_{shdo} (min)	Data hold from reqn(out) low or ackn(out) low	30	35

SCSI Fast Synchronous Input Signals

Parameter	Description	Tester Condition	Value (ns)
t_{srasti} (min)	reqn(in) assertion period	–	25
t_{srnegi} (min)	reqn(in) negation period	–	20
t_{saasti} (min)	ackn(in) assertion period	–	20
t_{sanegi} (min)	ackn(in) negation period	–	20
t_{sdsi} (min)	Data setup to reqn(in) or ackn(in) low	–	5
t_{shdi} (min)	Data hold to reqn(in) or ackn(in) low	–	15

Parallel Port Inputs

These signals are asynchronous in the system. They are specified for only testing purposes.

For the signals $\overline{\text{PP\_PE}}$, $\overline{\text{PP\_SLCT}}$, PP_ERROR, and MODE see the Parallel Port Input Signals table below.

Parallel Port Input Signals

Parameter	Reference Signal	Description	Tester Condition	Value (ns)
t_{ps}	SB_CLK	Setup time	–	5
t_{ph}	SB_CLK	Hold time	–	10

Parallel Port Outputs

These signals are asynchronous in the system. They are specified for only testing purposes.

For the signals PP_INIT, PP_SLCTIN, PP_AFXN, $\overline{\text{PP\_DSDIR}}$, PP_BSYDIR, PP_ACKDIR, and $\overline{\text{PP\_DDIR}}$ see the Parallel Port Output Signals table below.

Parallel Port Output Signals

Parameter	Reference Signal	Description	Tester Condition (pF)	Value (ns)
t_{pd} (max)	SB_CLK	Delay time	30	25
t_{pd} (min)	SB_CLK	Delay time	30	15

Parallel Port Bidirectionals

For the signals PP_D[7:0], PP_STB, $\overline{\text{PP\_BSY}}$, and PP_ACK, the system must meet the t_{ps} and t_{ph} on inputs and t_{pd} when in output direction.

JTAG Inputs

For the signals $\overline{\text{JTAG\_RST}}$, JTAG_TMS, JTAG_TDI, and STOP_CLK see the JTAG Input Signals table below. The maximum allowable frequency of JTAG_CLK is 10 MHz.

JTAG Input Signals

Parameter	Reference Signal	Description	Tester Condition	Value (ns)
t_{ss} (min)	JTAG_CLK	Setup time	–	15
t_{jh} (min)	JTAG_CLK	Hold time	–	5

$\overline{\text{JTAG\_RST}}$ is an asynchronous signal in the system, the specification applies only when testing on the IC tester.

JTAG Outputs

For the signal JTAG_TDO, the output delay specified with respect to the negative edge of JTAG_CLK clock, see the JTAG Output Signals table below for timing.

JTAG Output Signals

Parameter	Reference Signal	Description	Tester Condition (pF)	Value (ns)
t_{jd} (max)	JTAG_CLK	Delay time	30	20
t_{jd} (min)	JTAG_CLK	Delay time	30	0

Thermal Resistance Versus Air Flow

Approximately Θ_{JA} = 27 ˚C / W at 100 ft / min

PACKAGE INFORMATION

Pin Assignments

The STP2002QFP Pin Assignments table below describes the pin assignments for the STP2002QFP 240-pin PQFP package.

STP2002QFP Pin Assignments

Pin Number	Signal Name	Dual Function (FAS366 Test Mode Only)
1	PP_STB	
2	PP_AFXN	
3	PP_ERROR	I_SCSI_DACKN
4	MODE	I_SCSI_RESETN
5	JTAG_TDI	
6	$\overline{\text{JTAG\_RST}}$	
7	JTAG_CLK	
8	JTAG_TMS	
9	VSS_IO	
10	JTAG_TDO	
11	STOP_CLK	
12	ENET_CRS	I_SCSI_MODE0
13	VDD_IO	
14	ENET_COL	I_SCSI_MODE1
15	VSS_IO	
16	ENET_TXD[3]	
17	ENET_TXD[2]	
18	VSS_IO	
19	ENET_TXD[1]	
20	ENET_TXD[0]	
21	ENET_TX_EN	
22	VSS_IO	
23	ENET_TX_CLK	
24	ENET_TX_CLKO	
25	VDD_IO	
26	ENET_RX_ER	I_SCSI_A1
27	ENET_RX_CLK	I_SCSI_CSN
28	ENET_RX_DV	I_SCSI_A0
29	ENET_RXD[0]	I_SCSI_A2
30	VSS_CORE	
31	ENET_RXD[1]	I_SCSI_A3
32	VDD_CORE	
33	ENET_RXD[2]	I_SCSI_RDN
34	ENET_RXD[3]	I_SCSI_WRN

STP2002QFP Pin Assignments *(Continued)*

Pin Number	Signal Name	Dual Function (FAS366 Test Mode Only)
35	VSS_IO	
36	ENET_BUFFER_EN_0	
37	ENET_MDC	
38	ENET_MDIO0	
39	VDD_IO	
40	ENET_MDIO1	
41	VSS_IO	
42	$\overline{\text{SCSI\_D}}$[11]	
43	$\overline{\text{SCSI\_D}}$[10]	
44	$\overline{\text{SCSI\_D}}$[9]	
45	VSS_IO	
46	$\overline{\text{SCSI\_D}}$[8]	
47	$\overline{\text{SCSI\_IO}}$	
48	$\overline{\text{SCSI\_REQ}}$	
49	VSS_IO	
50	$\overline{\text{SCSI\_CD}}$	
51	$\overline{\text{SCSI\_SEL}}$	
52	$\overline{\text{SCSI\_MSG}}$	
53	VSS_IO	
54	$\overline{\text{SCSI\_RST}}$	
55	$\overline{\text{SCSI\_ACK}}$	
56	$\overline{\text{SCSI\_BSY}}$	
57	VSS_IO	
58	$\overline{\text{SCSI\_ATN}}$	
59	$\overline{\text{SCSI\_SDP}}$[0]	
60	$\overline{\text{SCSI\_D}}$[7]	
61	VSS_IO	
62	$\overline{\text{SCSI\_D}}$[6]	
63	$\overline{\text{SCSI\_D}}$[5]	
64	$\overline{\text{SCSI\_D}}$[4]	
65	VSS_IO	
66	$\overline{\text{SCSI\_D}}$[3]	
67	$\overline{\text{SCSI\_D}}$[2]	
68	$\overline{\text{SCSI\_D}}$[1]	
69	VSS_IO	
70	$\overline{\text{SCSI\_D}}$[0]	
71	$\overline{\text{SCSI\_SDP}}$[1]	
72	$\overline{\text{SCSI\_D}}$[15]	
73	VSS_IO	
74	$\overline{\text{SCSI\_D}}$[14]	
75	$\overline{\text{SCSI\_D}}$[13]	

STP2002QFP Pin Assignments (Continued)

Pin Number	Signal Name	Dual Function (FAS366 Test Mode Only)
76	$\overline{\text{SCSI\_D}}$[12]	
77	VSS_IO	
78	SCSI_XTAL1	
79	SCSI_XTAL2	
80	VDD_IO	
81	Reserved	
82	VSS_IO	
83	POD	
84	CLK_10M	
85	VSS_IO	
86	$\overline{\text{SB\_SC\_INT}}$	
87	$\overline{\text{SB\_ET\_INT}}$	
88	$\overline{\text{SB\_PP\_INT}}$	
89	VSS_IO	
90	SB_CLK	
91	VDD_IO	
92	VDD_CORE	
93	$\overline{\text{SB\_BR}}$	
94	VSS_CORE	
95	VSS_IO	
96	$\overline{\text{SB\_SEL}}$	
97	$\overline{\text{SB\_AS}}$	
98	SB_D[0]	
99	VDD_IO	
100	SB_D[1]	
101	VSS_IO	
102	SB_D[2]	
103	SB_D[3]	
104	VSS_IO	
105	SB_D[4]	
106	SB_D[5]	
107	VDD_IO	
108	SB_D[6]	
109	VSS_IO	
110	SB_D[7]	
111	SB_D[8]	IO_SCSI_DB[8]
112	VSS_IO	
113	SB_D[9]	IO_SCSI_DB[9]
114	SB_D[10]	IO_SCSI_DB[10]
115	VSS_IO	
116	SB_D[11]	IO_SCSI_DB[11]

STP2002QFP Pin Assignments (Continued)

Pin Number	Signal Name	Dual Function (FAS366 Test Mode Only)
117	VDD_IO	
118	SB_D[12]	IO_SCSI_DB[12]
119	SB_D[13]	IO_SCSI_DB[13]
120	$\overline{\text{SB\_BG}}$	
121	VSS_IO	
122	SB_D[14]	IO_SCSI_DB[14]
123	SB_D[15]	
124	VSS_IO	
125	SB_D[16]	
126	VDD_IO	
127	SB_D[17]	
128	VSS_IO	
129	SB_D[18]	
130	SB_D[19]	
131	SB_D[20]	
132	VSS_IO	
133	SB_D[21]	
134	VDD_IO	
135	SB_D[22]	
136	VSS_IO	
137	SB_D[23]	
138	SB_D[24]	
139	VSS_IO	
140	$\overline{\text{SB\_ACK}}$[0]	
141	$\overline{\text{SB\_ACK}}$[1]	
142	VDD_IO	
143	$\overline{\text{SB\_ACK}}$[2]	
144	VSS_IO	
145	SB_D[25]	IO_SCSI_DBP1
146	VDD_CORE	
147	SB_D[26]	
148	VSS_IO	
149	SB_D[27]	
150	VSS_CORE	
151	SB_D[28]	
152	VSS_IO	
153	SB_D[29]	
154	VDD_IO	
155	SB_D[30]	
156	SB_D[31]	
157	VSS_IO	

STP2002QFP Pin Assignments (Continued)

Pin Number	Signal Name	Dual Function (FAS366 Test Mode Only)
158	SB_SIZ[2]	IO_SCSI_DB[07]
159	SB_SIZ[1]	IO_SCSI_DB[06]
160	VSS_IO	
161	SB_SIZ[0]	IO_SCSI_DB[05]
162	VDD_IO	
163	SB_RD	
164	VSS_IO	
165	SB_PA[0]	IO_SCSI_DB[04]
166	SB_PA[1]	IO_SCSI_DB[03]
167	SB_PA[2]	IO_SCSI_DB[02]
168	VSS_IO	
169	SB_PA[3]	IO_SCSI_DB[01]
170	SB_PA[4]	IO_SCSI_DB[00]
171	VSS_IO	
172	SB_PA[5]	IO_SCSI_DBP0
173	VDD_IO	
174	$\overline{\text{SB\_LERR}}$	
175	SB_PA[6]	
176	VSS_IO	
177	SB_PA[7]	
178	SB_PA[8]	
179	VSS_IO	
180	SB_PA[9]	
181	VDD_IO	
182	SB_PA[10]	
183	VSS_IO	
184	SB_PA[11]	
185	SB_PA[12]	
186	VSS_IO	
187	SB_PA[13]	
188	VDD_IO	
189	SB_PA[14]	
190	SB_PA[15]	
191	VSS_IO	
192	SB_PA[16]	
193	SB_PA[17]	
194	VSS_IO	
195	SB_PA[18]	
196	VDD_IO	
197	SB_PA[19]	
198	V_{SS}	

STP2002QFP Pin Assignments *(Continued)*

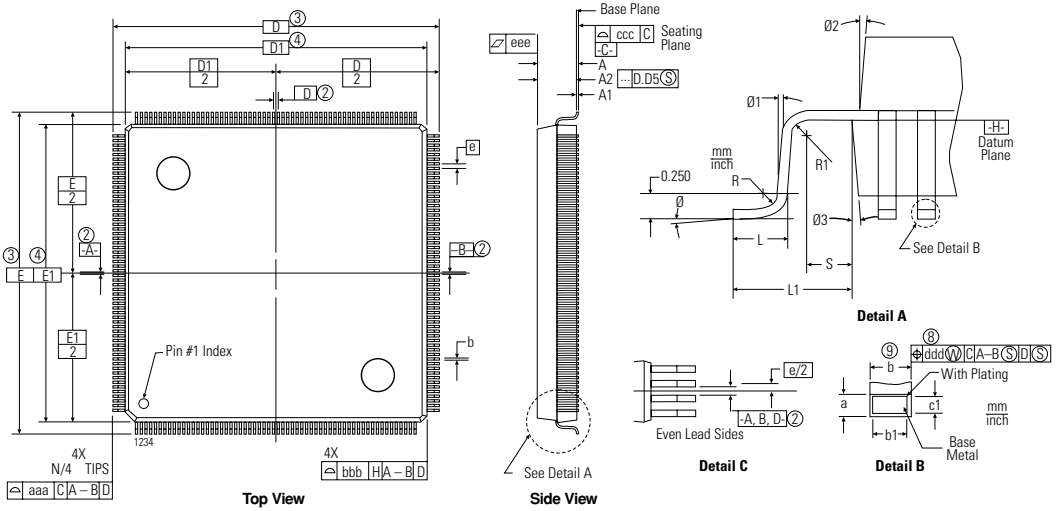
Pin Number	Signal Name	Dual Function (FAS366 Test Mode Only)
199	SB_PA[20]	
200	SB_PA[21]	
201	SB_PA[22]	
202	VSS_IO	
203	SB_PA[23]	
204	VDD_IO	
205	SB_PA[24]	
206	VSS_IO	
207	SB_PA[25]	
208	VDD_CORE	
209	SB_PA[26]	
210	VSS_IO	
211	VSS_CORE	
212	SB_PA[27]	
213	SB_DATPAR	
214	$\overline{\text{RESET}}$	I_SCSI_PAUSE
215	$\overline{\text{ID\_CS}}$	
216	$\overline{\text{PP\_SLCT}}$	I_SCSI_DBWRN
217	$\overline{\text{PP\_PE}}$	I_SCSI_DBRDN
218	VDD_IO	
219	PP_BSYDIR	
220	VSS_IO	
221	$\overline{\text{PP\_BSY}}$	
222	PP_ACKDIR	
223	PP_ACK	
224	PP_DDIR	
225	PP_D[7]	
226	VSS_IO	
227	PP_D[6]	
228	PP_D[5]	
229	VDD_IO	
230	PP_D[4]	
231	PP_D[3]	
232	PP_D[2]	
233	VSS_IO	
234	PP_D[1]	
235	PP_D[0]	
236	PP_SLCT_IN	

STP2002QFP Pin Assignments *(Continued)*

Pin Number	Signal Name	Dual Function (FAS366 Test Mode Only)
237	PP_INIT	
238	VDD_IO	
239	PP_DS_DIR	
240	VSS_IO	

PACKAGE DIMENSION INFORMATION

The FEPS is packaged in a 32×32-mm plastic quad flat pack (PQFP) with 240 leads. Below is the mechanical drawing.



	Dimension (mm)			Dimension (inch)		
	Min	Nom	Max	Min	Nom	Max
A			4.10			0.181
A1	0.25			0.010		
A2	3.20	3.40	3.60	0.126	0.134	0.142
D	34.60 BSC			1.352 BSC		
D1	32.00 BSC			1.260 BSC		
E	34.60 BSC			1.362 BSC		
E1	32.00 BSC			1.260 BSC		
L	0.45	0.60	0.75	0.18	0.024	0.030
L1	1.30 REF			0.052 REF		
N	240			240		
R	0.13	0.19	0.25	0.005	0.007	0.010
R1	0.13			0.005		
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.20	0.004		0.008
c1	0.08		0.15	0.004		0.008
e	0.025 BSC			0.020 BSC		
ddd			0.05			0.003
Ø	0°	2.5°	5°	0°	2.5°	5°
Ø1	0°			0°		
Ø2	5°	10.5°	15°	5°	10.5°	15°

	Dimension (mm)			Dimension (inch)		
	Min	Nom	Max	Min	Nom	Max
Ø3	5°	10.5°	15°	5°	10.5°	15°
aaa			0.20			0.008
bbb			0.20			0.08
ccc			0.10			0.004
S	0.40			0.015		

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datums A–B and -D- to be determined at Datum Plane -H-.
3. To be determined at Seating Plane -C-.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.255 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Controlling dimension: millimeter.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
7. When converting from millimeters to inches, four significant digits to the right of the decimal point are necessary for board layout purposes.
8. Minimum space between lead is 0.15 mm (0.006") regardless of conformance with lead positionaltolerance ddd.
9. This variation is the NCR standard configuration. All other variations are available as options only.

ORDERING INFORMATION

Part Number	Description
STP2002QFP	Fast Ethernet, Parallel Port, SCSI (FEPS)

Document Part Number: STP2002