The UltraSPARC T1 Processor - Reliability, Availability, and Serviceability

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1.0 Introduction

The dramatic increase in reliability, availability, and serviceability (RAS) of CMT systems can be attributed to the CMT processor design approach and enhancements to the processor RAS architecture.

Chip Multithreaded (CMT) processor design promises to deliver many benefits, including the ability to effectively translate the expanded transistor budgets made available by each new generation of semiconductor process technology into higher levels of throughput performance. However, among the more important but perhaps less widely appreciated benefits of CMT design, is a dramatic overall improvement in system reliability, availability, and serviceability (RAS). This latter benefit results from the fact that CMT processor design represents a fundamental shift in the way in which SMP systems are built, internalizing much of the communication that formerly occurred between processors to within a chip. The resulting reduction in part count, combined with enhanced processor RAS features, deliver a highly favorable overall impact on system reliability, availability, and serviceability.

2.0 CMT System Reliability

There is simply less to go wrong in a system with few components than a system with many components.

The first instance of Sun's radical CMT designs is the UltraSPARC T1 processor. When the very high reliability of an UltraSPARC T1 processor is combined with the fact that one radical CMT processor replaces many processors in an equivalent SMP system, system level reliability compounds dramatically with CMT designs. This effect is already visible even in systems based on the first generation of Sun's CMT processors, the UltraSPARC IV processor generation. For the same level of delivered throughput performance, there simply is less to go wrong in an UltraSPARC IV processor-based system than in an UltraSPARC III processor-based system, since the former system is built with just half the number of processor boards (and processor chips) as the latter. Assuming the individual components in two different system are similar in terms of their reliability, on average, the system with the fewer parts can be expected to suffer proportionally fewer failures, corresponding to the difference in their respective part counts.

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For radical CMT processors like the UltraSPARC T1 processor, where one UltraSPARC T1 processor replaces many processors in an equivalent SMP system, the system level reliability effects will be dramatic. As shown in Figure 1, the associated conversion of interchip communication in a traditional SMP system is simplified to intrachip communication in an UltraSPARC T1 processor-based system.

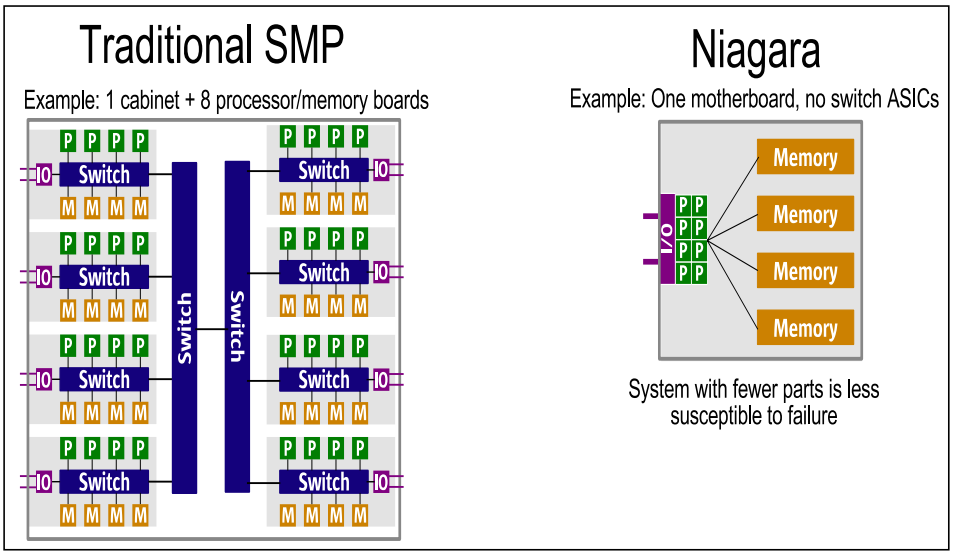

FIGURE 1 System Part Count: Traditional SMP vs. UltraSPARC T1 Processor

The UltraSPARC T1 processor-based system has far less components than the traditional SMP server, reducing its susceptibility to failure.

In Figure 1, the traditional SMP server is housed in a refrigerator-sized cabinet and consists of eight processor/memory boards, each with four processors, memory, and an I/O interface. Each board has switch ASICs to connect the on-board components, and the cabinet has another set of switch ASICs to connect one group of four boards to the other group of four boards. In contrast, the UltraSPARC T1 processor-based system offers a much more integrated and tightly-coupled solution than the traditional SMP by shrinking the eight cell boards into a single chip. Without any need for switch ASICs, the whole system now fits on one motherboard, and has many fewer parts and pins to fail. Moreover, maintaining and servicing the boards was reduced from eight boards to simply one board.

A data center using an SMP server can be replaced with a single UltraSPARC T1 processor-based system while delivering an acceptable level of availability.

To further illustrate this point, suppose a processor is engineered to run 1,000,000 hours on average before it fails. In a 32-processor server, assuming the server requirement is 24x7x365 availability, each server would log more than 280,000 hours of processor time a year. An installation of as few as 4 servers, therefore, would experience 1 or 2 processor-related failures a year, on average; a rate that a server customer well might deem unacceptably high. However, replace the 32 processors with a single UltraSPARC T1 processor engineered to the exactly the same 1,000,000 MTBF (mean time between failure) standard, and the result is a dramatic improvement in system reliability. Even operating on a basis of 24x7x365 constant availability, a large farm of more than 100 UltraSPARC T1 processor-based servers would be expected to have fewer than 1 breakdown a year due to processor failure. Small farms might never experience a processor failure during their useful lifespans.

3.0 UltraSPARC T1 Processor RAS

In addition to the inherent benefits of the CMT processor design, the UltraSPARC T1 processor implements numerous RAS features.

In addition to the inherent RAS benefits of the CMT design approach, the UltraSPARC T1 processor itself implements numerous state-of-the-art RAS features to ensure a system continues to operate, avoid or shorten downtime, and diagnose and fix a broken system. The UltraSPARC T1 processor's RAS highlights include:

- Protection of on-chip memories
- Main memory reliability and availability
- Power and thermal reliability

3.1 Protection of On-Chip Memories

Sun systematically designed the UltraSPARC T1 processor with the appropriate level of protection of its on-chip memories.

As semiconductor technology continues to enable increasing chip densities, the processor has become more susceptible to soft error rates[1] than ever before. Contemporary processors like the UltraSPARC T1 processor, which are manufactured on cutting-edge process technology, are especially prone to these soft errors. With this problem in mind, Sun systematically designed the UltraSPARC T1 processor with the

1. For more information on soft error rates, refer to http://sunsolve.sun.com/data/816/816-5053/pdf/816-5053-10.pdf

appropriate level of protection of its on-chip memories. In general, the UltraSPARC T1 processor protects memory arrays with either single error correction / double error detection (SEC/DED) or parity protection. Redundant arrays are protected with parity, while non-redundant arrays are protected with ECC (Error Correcting Code).

Table 1 lists the UltraSPARC T1 processor's on-chip memories and its corresponding protection mechanism.

TABLE 1 On-Chip Memory Protection

Memory Array	Protection
Integer Register File	ECC
Floating Point Register File	ECC
L1 Instruction Cache - Data	Parity/retry
L1 Instruction Cache - Tag	Parity/retry
Instruction TLB	Parity/retry
Data TLB	Parity/retry
L1 Data Cache - Data	Parity/retry
L1 Data Cache - Tag	Parity/retry
L2 Cache - Data	ECC
L2 Cache - Tag	ECC
L2 Cache Scrubber	Yes

Mainframe-class protection of the UltraSPARC T1 processor's integer and floating point register files prevents an application from crash or silent data corruption.

A notable feature in this schema is the ECC protection of the integer and floating point register files, an extensive level of protection only matched by mainframe-class processors. While processor designs have mainly focused on protecting the datapath, caches, and main memories, the register file has largely been neglected. Since the register file is accessed very frequently, which increases the probability of errors, protecting the register files is critically important. In addition, protecting the register file prevents errors in the register file from quickly spreading to different parts of the system, and prevents an application from crash or silent data corruption.

3.2 Main Memory Reliability and Availability

The UltraSPARC T1 processor protects main memory using Chipkill Technology to correct multi-bit memory errors.

The UltraSPARC T1 processor protects main memory using several mechanisms. “Chipkill” technology is used to withstand multi-bit memory errors within a DRAM device, including a failure that causes incorrect data on all data bits of the device.

The UltraSPARC T1 processor’s Chipkill mechanism[1] can correct any error contained within a single memory nibble (4 bits), and detect any uncorrectable errors contained within any two nibbles. When writing data to the DIMM, data is written in the form of a checksum appended to the data. If a single nibble memory error occurs, then the data is immediately recovered by re-calculating the data from the checksum information. This procedure allows the system to correct not only the single bit errors that standard ECC memory can correct but also 2,3 and 4-bit errors and even a whole DRAM chip failure.

In conjunction with Chipkill, DRAM sparing is implemented in the UltraSPARC T1 processor to map out a failed DRAM chip.

In conjunction with Chipkill, DRAM sparing is implemented in the UltraSPARC T1 processor to improve main memory availability. Where Chipkill detects a failed DRAM chip, DRAM sparing reconfigures a DRAM channel to map out the failed chip, effectively replacing it with a corrected DRAM chip. This technique restores the capability of correcting any random single-nibble error and allows the system to run with minor impaired memory error protection until the DIMM can be replaced.

The UltraSPARC T1 processor implements memory scrubbing to continuously correct memory errors before a soft error impacts a memory row.

Another mechanism implemented in the UltraSPARC T1 processor to ensure main memory reliability is memory scrubbing. Each of the UltraSPARC T1 processor’s four memory controllers has a background error scanner/scrubber to reduce the incidence of multi-nibble errors. The background checker performs reads of main memory and checks for errors on a single memory line (64 bytes). If a correctable error is found, the error is logged, corrected, and written back to memory. In this manner, any single bit or a group of adjacent bits can be corrected *before* a soft error impacts the same memory row. This background checker is even programmable on how often it performs an error scan operation.

1. The UltraSPARC T1 processor’s ECC coding scheme uses Galois Field instead of Hamming in its Chipkill implementation. The Galois Field algorithm provides higher bandwidth than Hamming Chipkill (21.33 GB/s vs. 10.66 GB/s).

3.3 Power and Thermal Reliability

Power and thermal management increases the UltraSPARC T1 processor's reliability and extends its useful lifetime.

Power and thermal management play an important role in the overall RAS architecture of the UltraSPARC T1 processor. By its ability to monitor and control temperature, the UltraSPARC T1 processor reduces the natural wearout and damage of the processor, thereby increasing its reliability and extending its useful lifetime. At the International Reliability Physics Symposium[1], Sun showed that implementing power and thermal management features can dramatically increase both the lifetime and reliability of the device by up to 24 times while maintaining or improving device performance.

The UltraSPARC T1 processor throttles its power consumption by disabling individual threads or disabling cores.

The UltraSPARC T1 processor utilizes two on-chip thermal sensors, located near the cores (the parts of a processor that generate the most heat), enabling system hardware to measure the processor temperature and trigger one of the following "throttling" measures:

- Disable individual threads within a core, effectively forcing the threads to enter an idle state
- Disable entire cores

By reducing processor utilization, throttling reduces power consumption. This active temperature monitor and control allow the UltraSPARC T1 processor to limit its temperature in the case of system failures such as fan failure or other external factors. When conditions return to within the normal range, the idle threads are activated and resume execution.

4.0 Conclusion

Combined with system RAS features such as redundant hot-swap power and cooling, and the Solaris 10 operating system's fault management architecture, next-generation processors like the UltraSPARC T1 processor promise to exhibit very high levels of reliability, availability and serviceability. Moreover, since one radical CMT processor chip replaces what formerly would have been many different parts in an SMP system (including multiple processor boards together with all of their associated

1. International Reliability Physics Symposium, April 2005, Sun Microsystems, Inc., http://www.irps.org/05-43rd/IRPS_Keynote_Yen.pdf

external interconnects), the result will be a dramatic rise in overall system reliability and availability, corresponding to the greatly lowered part count typical of systems built with radical CMT processors.