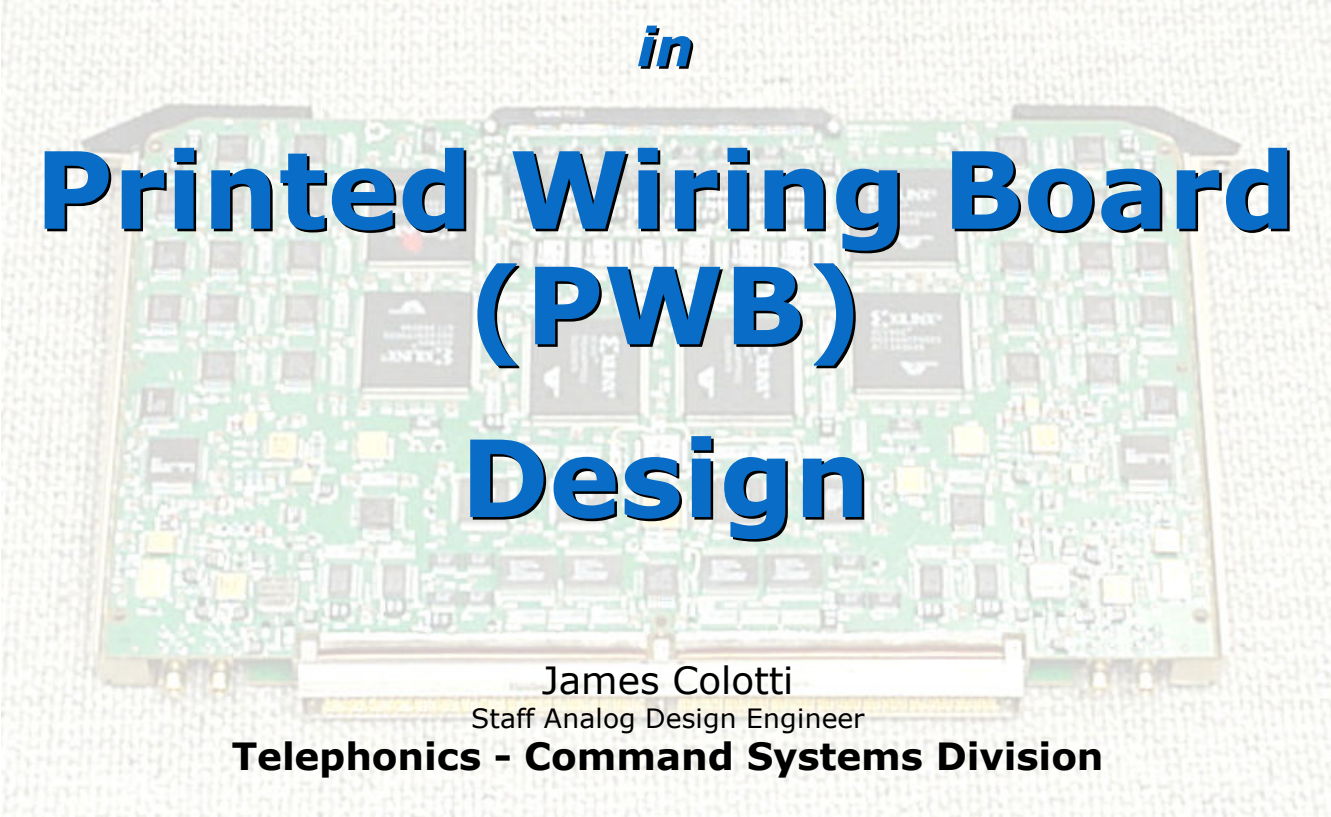


Analog, RF and EMC Considerations

in

Printed Wiring Board (PWB) Design



James Colotti

Staff Analog Design Engineer

Telephonics - Command Systems Division

Introduction

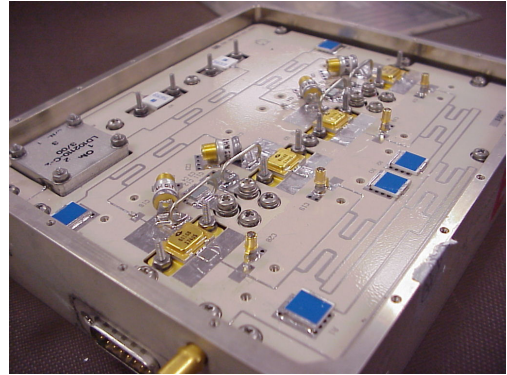
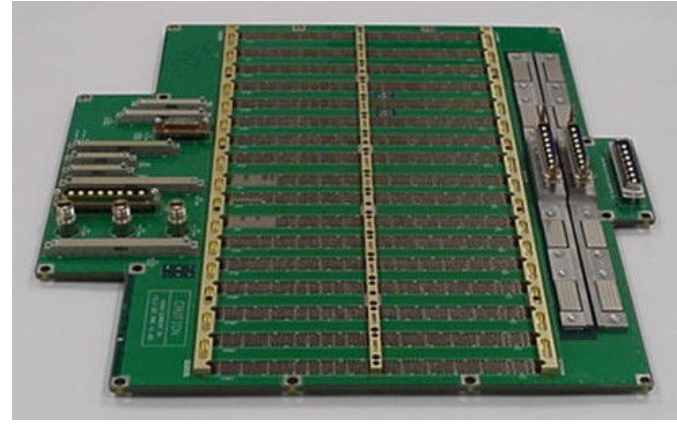
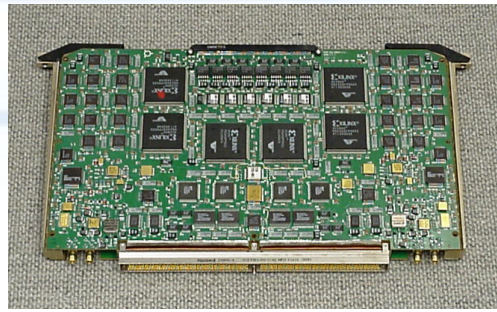
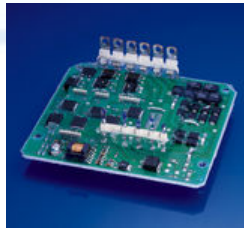
- ◆ Advances in digital and analog technologies present new challenges PWB design
- ◆ Clock frequencies approach the L Band region
 - Dielectric absorption, Skin Depth, Impedances, Dispersion
- ◆ High Power and/or Lower Voltage
 - Power distribution, decoupling
- ◆ High dynamic-range/low-noise analog circuitry
 - Noise immunity, stability
- ◆ High Density Components
 - Xilinx FG1156 Fine Pitch BGA (1.0 mm pitch 39 mils)
 - Finer pitch BGAs 0.8 mm (31 mils) and 0.5 mm (20 mils)
- ◆ Overlap between Disciplines
 - Electrical, Mechanical, Manufacturing, Design/Drafting

Outline

- ◆ PWB Construction
 - Types, Stack-Ups
- ◆ PWB Materials
 - Core/pre-preg, copper weights
- ◆ Signal Distribution
 - Impedance, Coupling, Signal Loss, Delay
- ◆ Power Distribution & Grounding
 - Planes, Decoupling, Power Loss
- ◆ References and Vendors

PWB Construction

PWB/CCA Examples



Types of Rigid PWB

- ◆ Rigid, One Layer, Type 1
- ◆ Rigid, Two Layer, Type 2
- ◆ Rigid, Multi Layer, w/o blind/buried vias, Type 3
- ◆ Rigid, Multi Layer, w/ blind/buried vias, Type 4
- ◆ Rigid, Metal Core, w/o blind/buried vias, Type 5
- ◆ Rigid, Metal Core, w/ blind/buried vias, Type 6

(Per IPC-2222 standard)

Types of Flex PWB

- ◆ Flex, One Layer, Type 1
- ◆ Flex, Two Layer, Type 2
- ◆ Flex, Multi Layer, Type 3
- ◆ Flex, Multi Layer, Rigid/Flex, Type 4

(Per IPC-2223 Standard)

Footnotes on Flex PWBs

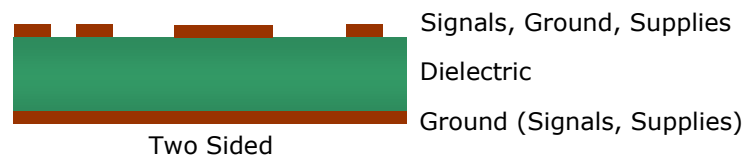
- ◆ Used as alternative to a discrete wiring harness
- ◆ Many similarities to rigid PWBs
- ◆ Typically higher development cost than harness
- ◆ Typically cheaper than harness in production
- ◆ Improved repeatability
- ◆ Improved EMI performance and impedance control when ground layers are used
- ◆ Typically much less real estate needed



PWB Stack-Ups (1 and 2 Layer)



- Inexpensive
- Applicable to straightforward circuits
- Difficult to control EMI without external shield
- Difficult to control impedance



- Inexpensive (slightly more than 1 sided)
- Applicable to more complex circuits
- EMI mitigation with ground plane
- Impedance control simplified with ground plane

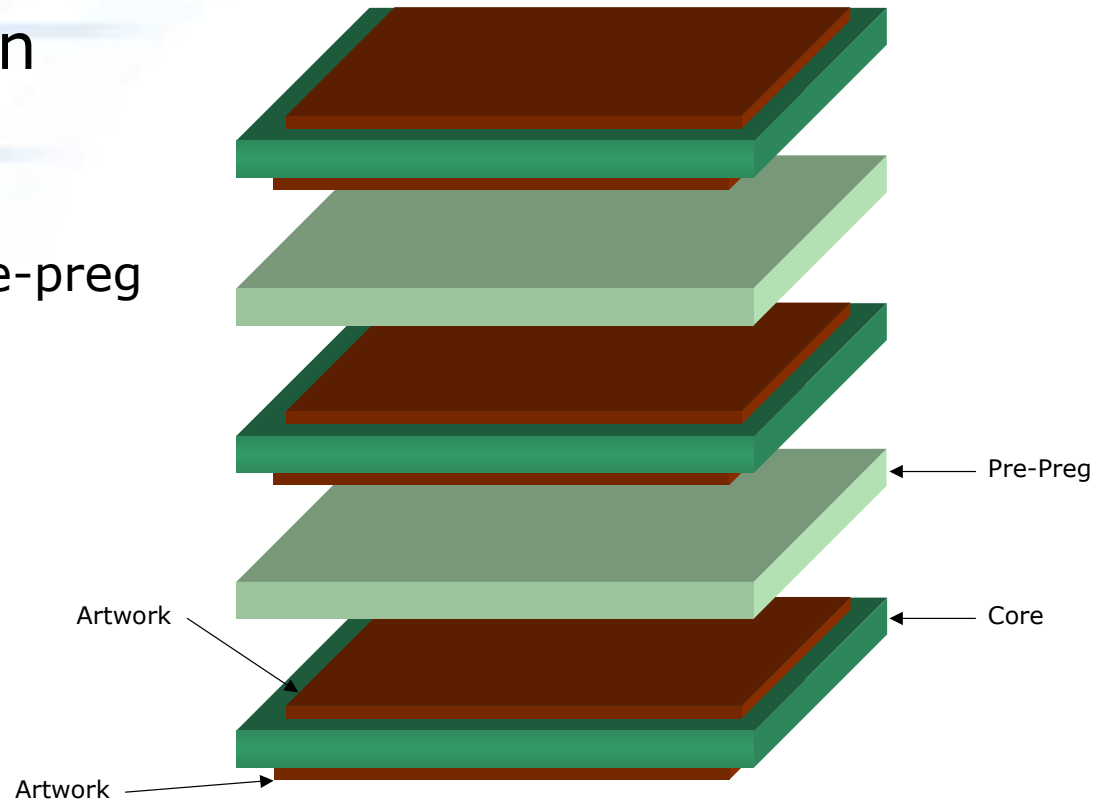


Multi-Layer PWBs

- ◆ Option for dedicating layers to ground
 - Forms reference planes for signals
 - EMI Control
 - Simpler impedance control
- ◆ Option for dedicating layers to Supply Voltages
 - Low ESL/ESR power distribution
- ◆ More routing resources for signals

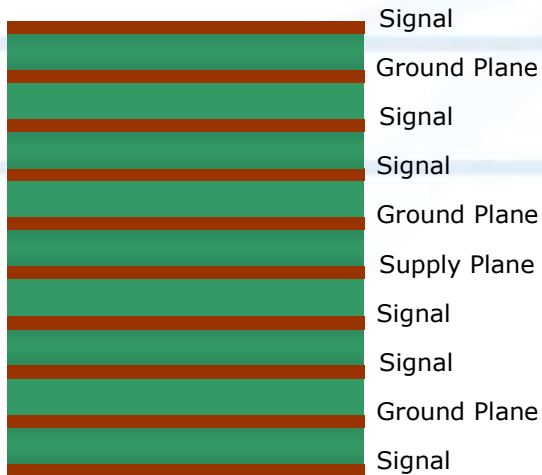
Exploded View of Multi-Layer PWB

- ◆ Core Construction
- As shown
- ◆ Foil Construction
- Reverse core and pre-preg



Multi-Layer Stack-Up Examples

1



High Speed Digital PWB

- High Density
- Ten Layers
- Two Micro-Strip Routing Layers
- Four Asymmetrical Strip-Line Routing Layers
- Single Supply Plane
- Two Sided

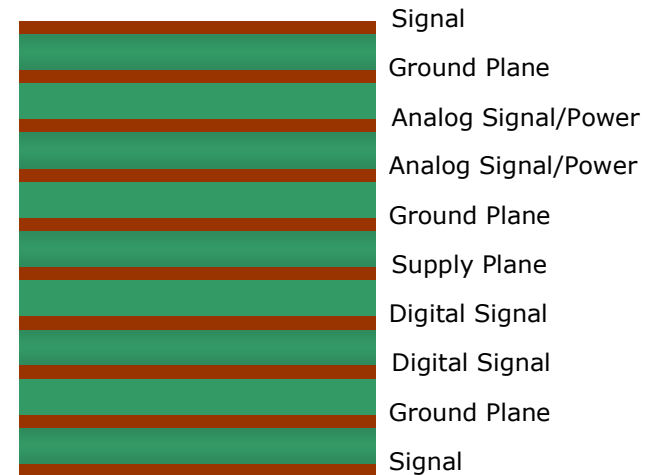
2



High Speed Digital PWB

- Moderate Density
- Six Layers
- Two Micro-Strip Routing Layers
- Two Buried Micro-Strip Routing Layers
- Single Supply Plane
- Two Sided

3



Mixed Analog/RF/Digital PWB

- Moderate Density
- Ten Layers
- Two Micro-Strip Routing Layers
- Four Asymmetrical Strip-Line Routing Layers
- Single Digital Supply Plane
- Analog supplies on inner layers
 - Routing Clearance Considerations
 - Improved isolation
- Two Sided



PWB Stack-Up Guidelines

- ◆ Maximize symmetry to simplify manufacturing and to mitigate warping
- ◆ Even number of layers preferred by PWB manufacturers
- ◆ Asymmetrical strip-line has higher routing efficiency than symmetrical strip-line
- ◆ Supply planes can be used as reference planes for controlled Z (but not preferred for analog)
- ◆ Ideally, supply planes should be run adjacent to ground planes

PWB Materials

PWB Materials

- ◆ Dozens of dielectric materials to chose from
 - Rogers 20 types
 - Taconic 10 types
 - Polyclad 25 types
 - Park Nelco 30 types
- ◆ Several dielectric thickness options
- ◆ Several copper thickness options
- ◆ Two copper plating options
 - Rolled
 - Electro-Deposited

Electrical Considerations in Selecting Material

- ◆ Dielectric Constant (permittivity)
 - The more stable, the better
 - Lower values may be more suitable for high layer counts
 - Higher values may be more suitable for some RF structures
- ◆ Loss Tangent
 - The lower, the better
 - Becomes more of an issue at higher frequencies
- ◆ Moisture Absorption
 - The lower, the better
 - Can effect dielectric constant and loss tangent
- ◆ Voltage Breakdown
 - The higher, the better
 - Typically not an issue, except in high voltage applications
- ◆ Resistivity
 - The higher, the better
 - Typically not an issue, except in low leakage applications

Mechanical Considerations in Selecting Materials

- ◆ Peel Strength
 - The higher, the better
- ◆ Flammability
 - UL Standards
- ◆ Glass Transition Temperature (T_g)
- ◆ Thermal Conductivity
 - Typically PWB material is considered an insulator
 - Thermal Clad (Bergquist)
 - Planes & vias contribute to thermal conductivity
- ◆ Coefficient of Expansion
 - XY matching to components, solder joint stress (LCC)
 - Z axis expansion, via stress
- ◆ Weight (density)
- ◆ Flexibility

PWB Material Examples

Material	Dielectric Constant (ϵ_r)	Loss Tangent ($\tan\delta$)	Notes
FR-4, Woven Glass/Epoxy	4.7 (1 MHz) 4.3 (1 GHz)	0.030 (1 MHz) 0.020 (1 GHz)	Inexpensive, available, unstable ϵ_r , high loss
N7000-1 Polyimide Park-Nelco	3.9 (2.5 GHz) 3.8 (10 GHz)	0.015 (2.5 GHz) 0.016 (10 GHz)	High T_g (260 °C)
CLTE Arlon	2.94 (10 GHz)	0.0025 (10 GHz)	Stable ϵ_r , low loss
RT6010LM Rogers	10.2 (10 GHz)	0.002 (10 GHz)	High ϵ_r , high loss
RO4350B Rogers	3.48 (10 GHz)	0.004 (10 GHz)	Stable ϵ_r , low loss, processing is similar to FR4
RT6002 Rogers	2.94 (10 GHz)	0.0012 (10 GHz)	Stable and accurate ϵ_r , low loss



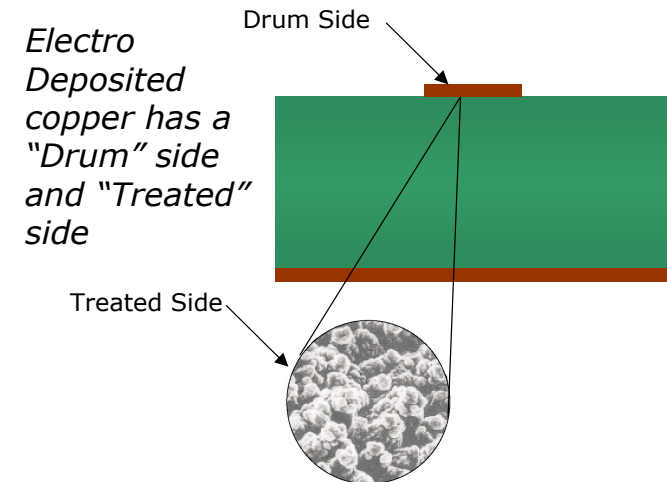
Dielectric, Common Thickness

- ◆ Core Material
 - 0.002, 0.003, 0.004, 0.005, 0.006, 0.007, 0.008, 0.009
 - 0.010, 0.012, 0.014, 0.015, 0.018, 0.020, 0.031
- ◆ Pre-Preg
 - 0.002, 0.003, 0.004, 0.005, 0.008
 - Pre-preg can be stacked for thicker layers
- ◆ Use standard thickness in designing stack-up
- ◆ Work with anticipated PWB vendor(s) when assigning stack-up and selecting material

Copper Options

◆ Common Thickness Options

Weight	Thickness
0.25 oz	0.4 mil (9 μm)
0.5 oz	0.7 mil (18 μm)
1.0 oz	1.4 mil (35 μm)
2.0 oz	2.8 mil (70 μm)



◆ Plating Options

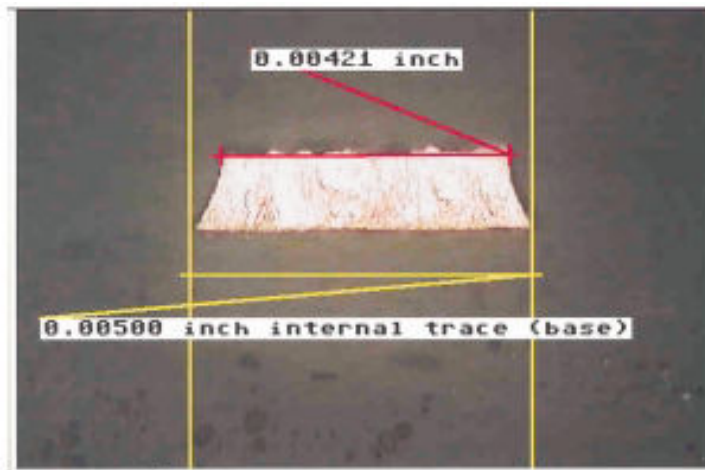
Option	Surface Roughness	Notes
Rolled	55 μin	Lower loss at high frequency (>1 GHz) More precise geometries for critical applications (couplers, distributed filters)
Electro Deposited	75 μin (0.5 oz) 94 μin (1 oz) 120 μin (2 oz)	For Treated (Dendritic) Side Untreated (Drum) Side is 55 μin Less prone to peeling

Considerations in Selecting Copper Thickness & Plating

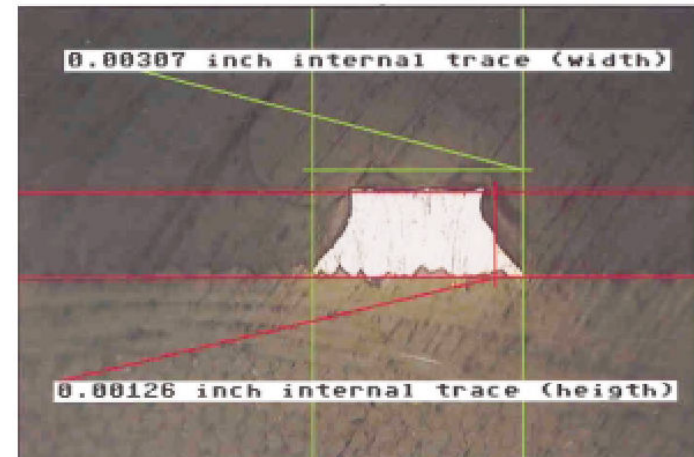
- ◆ Power Handling
 - Current capacity and temperature rise
 - Trace failure due to short
- ◆ Loss
 - Thicker/wider lines reduce DC resistive loss
 - Rolled copper exhibits less loss (>1 GHz)
- ◆ Etch-Back

Etch-Back

- ◆ Actual trace shape is trapezoidal
- ◆ Thinner copper produces more precise geometries with narrow line widths
- ◆ For traces >5 mils, 1 oz is acceptable
- ◆ For traces <5 mils, thinner copper used to limit etch-back
- ◆ Guidelines are vendor dependant



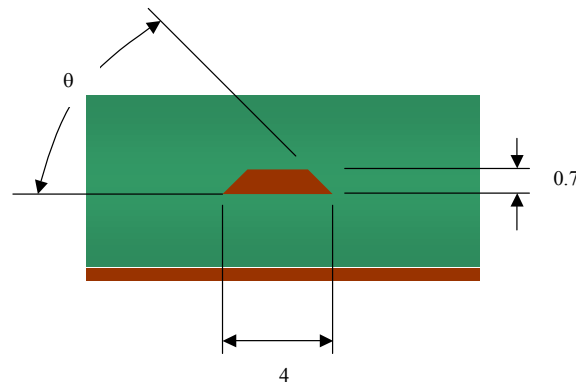
0.005" Trace 1 oz copper



0.003" Trace 1 oz copper

Etch-Back

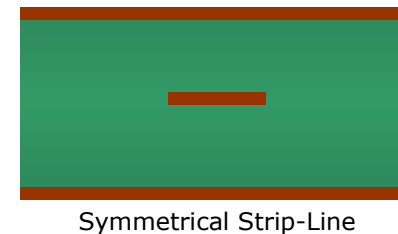
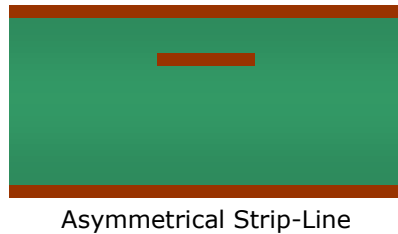
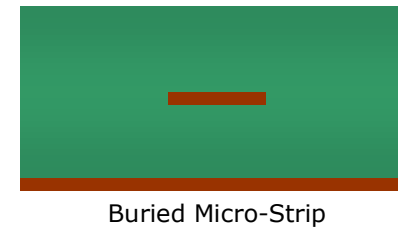
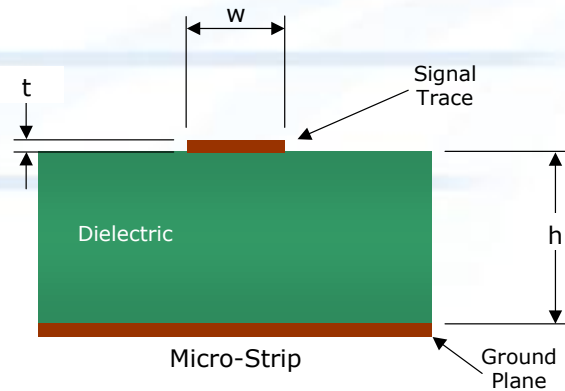
- ◆ Critical in some RF applications
 - Directional Couplers, Distributed Filters
- ◆ Critical in some narrow line width geometries
 - Significantly effects current capacity of trace
 - Significantly effects trace resistance and loss
- ◆ In many applications, effects on Z_o , L, C can be ignored (Buried Micro-Strip Example)



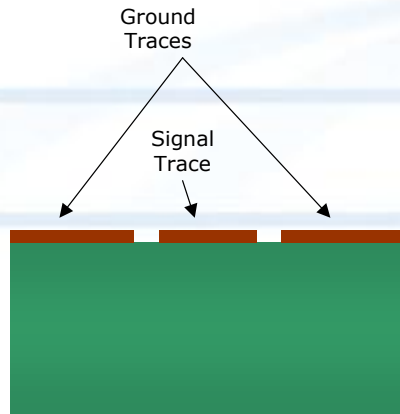
θ	L(nH/in)	C(pF/in)	Z_o (Ω)
90	8.5	3.4	50.0
79	8.6	3.3	50.7
72	8.6	3.3	51.0
60	8.7	3.3	51.5
45	8.8	3.2	52.2

Signal Distribution

Single Ended Structure Examples



Single Ended Structure Examples (continued)



Surface Coplanar Waveguide



Embedded Coplanar Waveguide



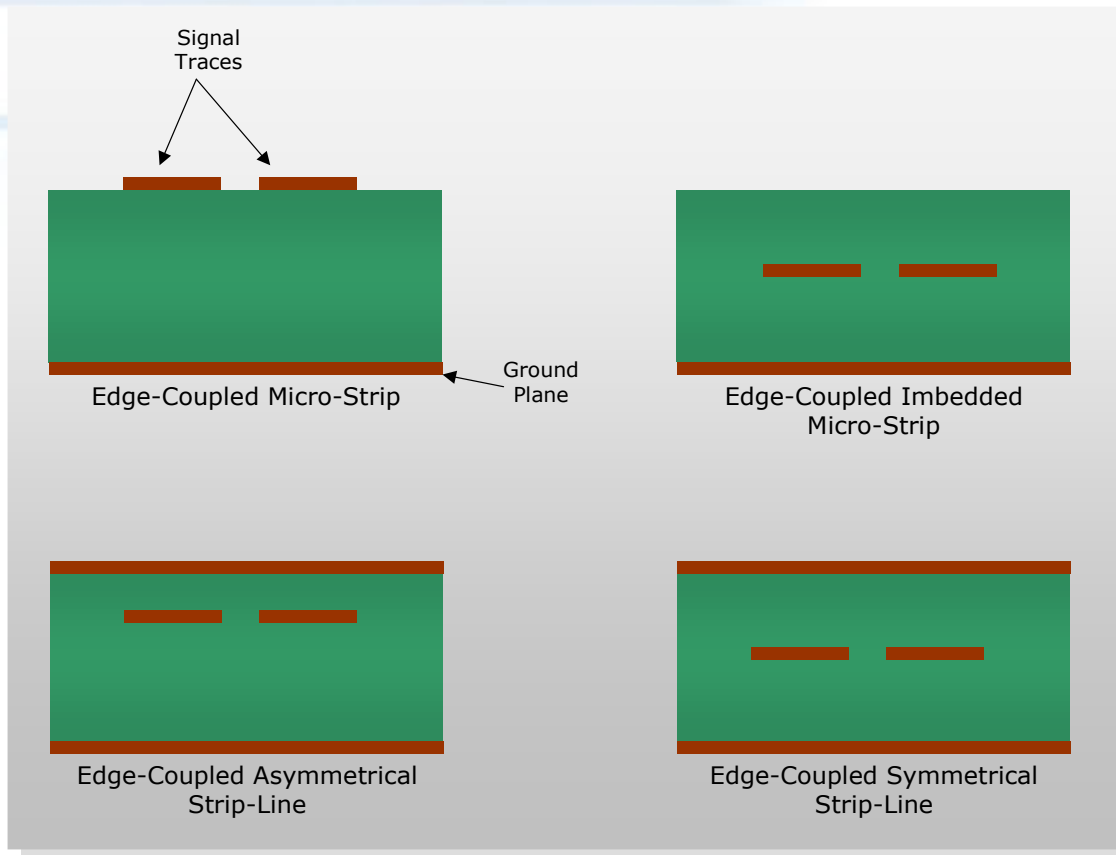
Surface Coplanar Waveguide
with Ground Plane



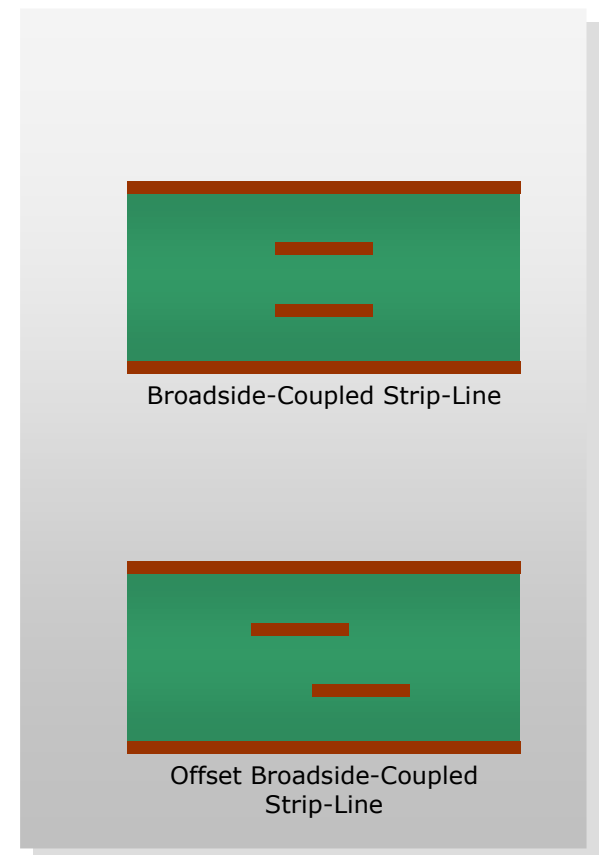
Embedded Coplanar Waveguide
with Ground Plane

Differential Structure Examples

Edge Coupled

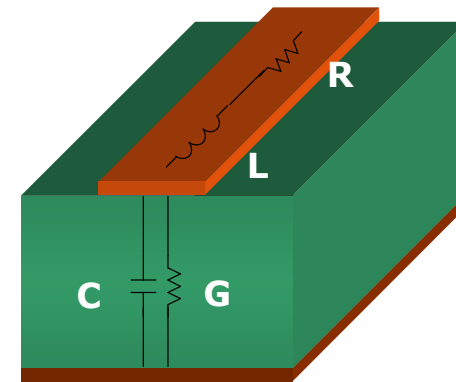


Broadside Coupled

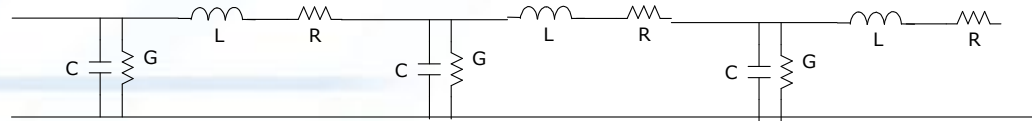


PWB traces as Transmission Lines

- ◆ Signal wavelength approaches component size
- ◆ Dielectric Loss (G)
- ◆ Trace Copper Loss (R)
- ◆ Trace series inductance (L)
- ◆ Trace capacitance (C)



Characteristic Impedance



$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Line impedance in terms of R, L, C and G

$$Z_0 = \sqrt{\frac{L}{C}}$$

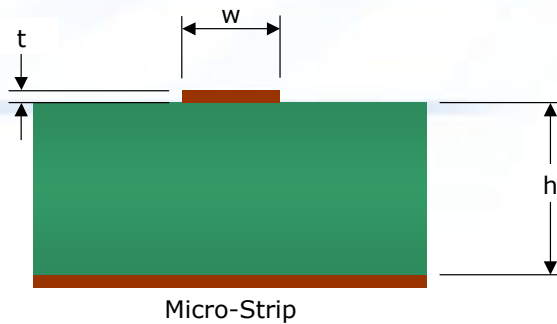
Line Impedance for Lossless line (R and G \Rightarrow 0)

Trace Impedance

- ◆ Impedance Determined By
 - Topology
 - Dielectric constant of PWB material
 - Dielectric height
 - Conductor width
 - Conductor thickness (small extent)

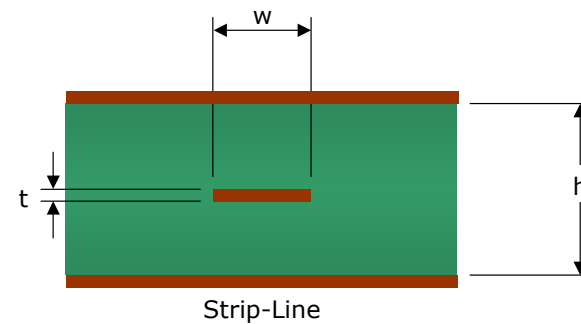
- ◆ Impedance Critical
 - Delivering max power to load
 - Maintaining signal integrity
 - Prevent excessive driver loading

Strip-Line & Micro-Strip Impedance



$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

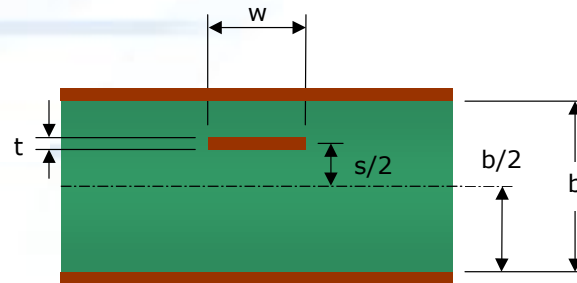
when $0.1 < \frac{w}{h} < 2.0$ and $1 < \epsilon_r < 15$



$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln\left(\frac{1.9b}{0.8w + t}\right)$$

when $\frac{w}{h} < 0.35$ and $\frac{t}{h} < 0.25$

Asymmetrical Strip-Line Impedance



Asymmetrical Strip-Line

$$Z_0 = \frac{\sqrt{\frac{\mu_0}{\epsilon_0}}}{2\pi\sqrt{\epsilon_r}} \cosh^{-1} \left[\sin \left(\frac{\pi(b-s)}{2b} \right) \coth \left(\frac{\pi d_0}{2b} \right) \right]$$

$$d_0 = w \left(0.5008 + 1.0235 \left(\frac{t}{w} \right) - 1.0230 \left(\frac{t}{w} \right)^2 + 1.1564 \left(\frac{t}{w} \right)^3 - 0.4749 \left(\frac{t}{w} \right)^4 \right)$$

$$\text{when } \frac{w}{b-t} < 0.35$$

Impedance Examples

- ◆ Symmetrical Strip-Line

50 Ω , 11 mils wide
(30 mil dielectric)



- ◆ Asymmetrical Strip-Line

50 Ω , 9 mils wide
(10+20=30 mil dielectric)



- ◆ Micro-Strip

50 Ω Micro-Strip, 54 mils wide
(30 mil dielectric)



Notes:

1. Copper: 1 oz, electro-deposited
2. FR4 dielectric constant: 4.50

Loss

- ◆ Loss due to three components
 - Dielectric Loss (loss tangent of PWB material)
 - Conductor Loss (resistive, skin effect, roughness)
 - Radiation Loss (typically negligible)
- ◆ Loss in Digital Applications
 - High Speed
 - Long Trace Runs
 - and/or Fine Width Lines
- ◆ Loss in Analog/RF Applications
 - Gain/Loss budgets in RF and IF paths
 - LO distribution loss
 - Scaling in Video, ADC or DAC applications

Dielectric and Copper Loss Examples

Frequency	FR4			4350		
	Copper Loss	Dielectric Loss	Total Loss	Copper Loss	Dielectric Loss	Total Loss
10 MHz	0.005	0.001	0.006	0.005	0.000	0.005
100 MHz	0.019	0.012	0.031	0.019	0.002	0.021
1 GHz	0.090	0.123	0.213	0.090	0.017	0.107
10 GHz	0.330	1.227	1.557	0.330	0.173	0.503

FR4 dielectric loss exceeds copper loss at 1 GHz

Notes:

1. Copper: 1 oz, electrodeposited, 10 mil width, 50 Ohms, strip-line
2. FR4 dielectric constant: 4.50, loss tangent 0.025, height 28 mils
3. 4350 dielectric constant: 3.48, loss tangent 0.004, height 22 mils
4. Loss units are dB/inch

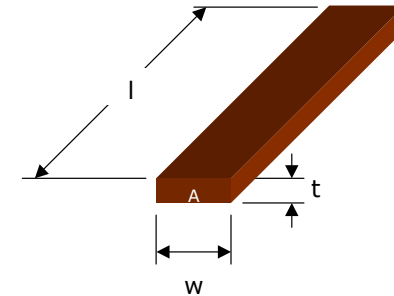
Conductor Loss

DC Resistance

$$R_{DC} = \rho \frac{l}{tw} = \rho \frac{l}{A}$$

$$R_{DC} = 0.679 \mu\Omega - in \frac{12 in}{(0.0014 in)(0.010 in)} = 0.6\Omega$$

$$R_{DC} = 0.679 \mu\Omega - in \frac{12 in}{(0.0007 in)(0.005 in)} = 2.3\Omega$$



Skin Depth

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}}$$

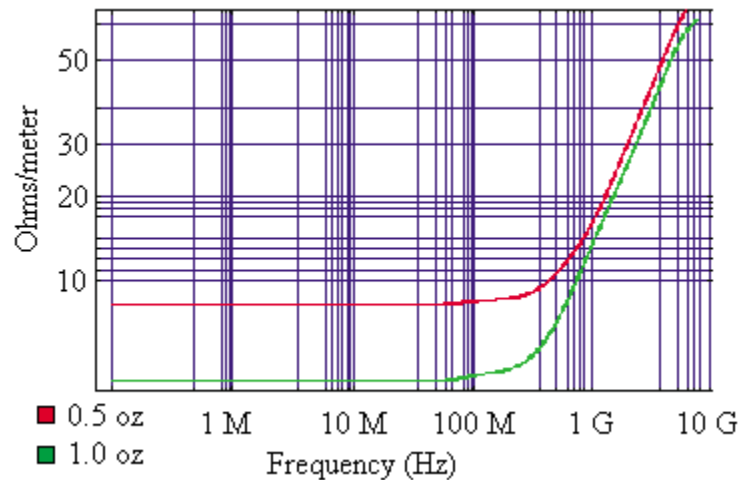
- Current density drops to 37% (1/e)
- Ignore if $t < 2\delta$

$$\delta = \sqrt{\frac{0.0172 \mu\Omega m}{\pi (10 GHz) \left(4\pi \times 10^{-7} \frac{\Omega s}{m} \right)}} = 660 nm = 0.03 mils$$

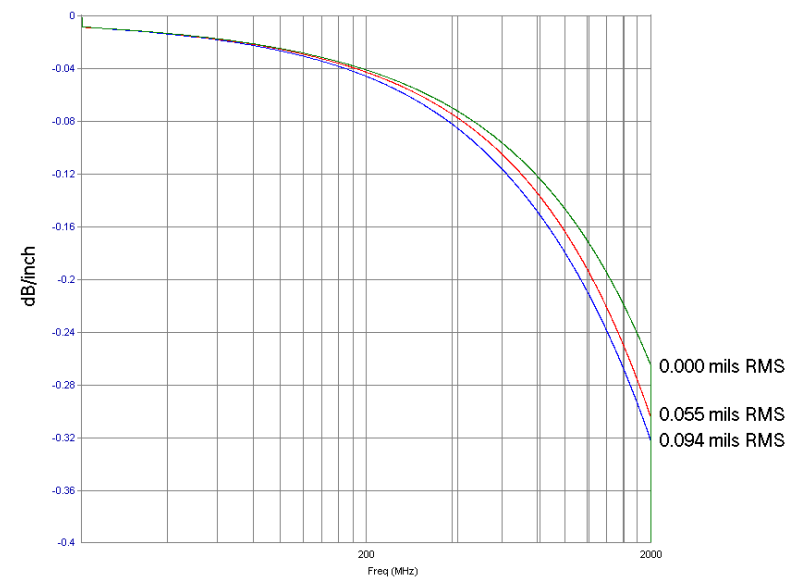
$$\delta = \sqrt{\frac{0.0172 \mu\Omega m}{\pi (10 MHz) \left(4\pi \times 10^{-7} \frac{\Omega s}{m} \right)}} = 21 \mu m = 0.8 mils$$

Loss due to Skin Effect & Roughness

Resistance, 5 mil Line
(on 1 oz and 0.5 oz copper)



Loss Variation, Roughness
(1 oz, 11 mil width)



Time Delay

$$t_d = \sqrt{L_o C_o} = \frac{\sqrt{\epsilon_{r-effective}}}{c} = 85 \sqrt{\epsilon_{r-effective}} \text{ ps/inch}$$

Where:

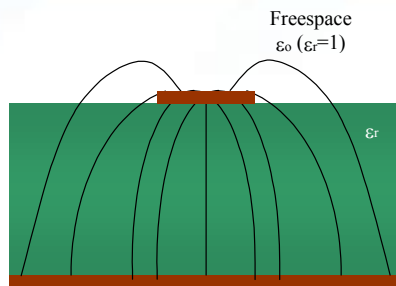
t_d : time delay per unit length

$\epsilon_{r-effective}$: Effective Relative Dielectric constant

C: Speed of Light

L_o : Inductance per unit length

C_o : Capacitance per unit length



Micro-Strip

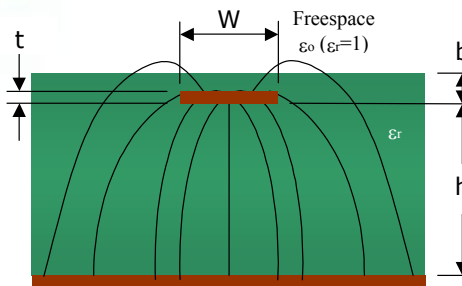
$$\epsilon_{r-effective} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(\frac{1}{\sqrt{1 + \frac{12h}{w}}} \right)$$

when $\frac{w}{h} \geq 1$

$$t_d = 156 \text{ ps/inch}$$

(FR4, $\epsilon_r = 4.5$,

$w = 18\text{mils}, h = 10\text{mils}$)



Buried Micro-Strip

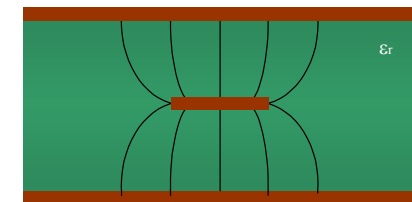
$$\epsilon_{r-effective}(\text{micro-strip})$$

<

$$\epsilon_{r-effective}(\text{buried micro-strip})$$

<

$$\epsilon_r$$



Strip-Line

$$\epsilon_{r-effective}(\text{strip-line}) = \epsilon_r$$

$$t_d = 85 \sqrt{\epsilon_r} \text{ ps per inch}$$

$$t_d = 180 \text{ ps/inch}$$

(FR4, $\epsilon_r = 4.5$)

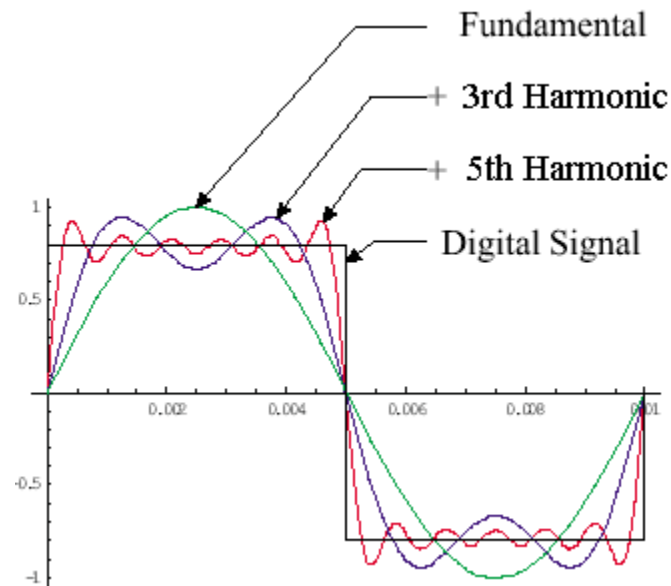
Signal Dispersion

- ◆ Frequency Dependant Dielectric Constant
 - Propagation velocity is frequency dependant
 - PWB acts as a dispersive Medium

- ◆ Becomes Issue
 - Long Trace Runs
 - High Speed Clocks
 - Critical Analog

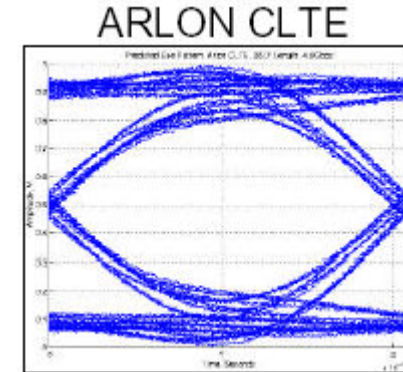
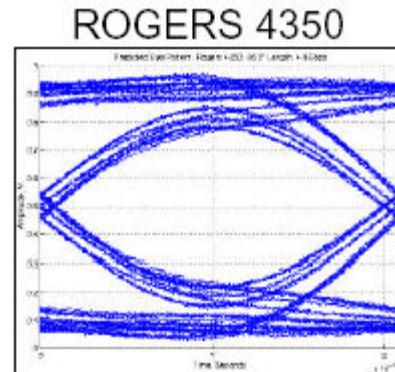
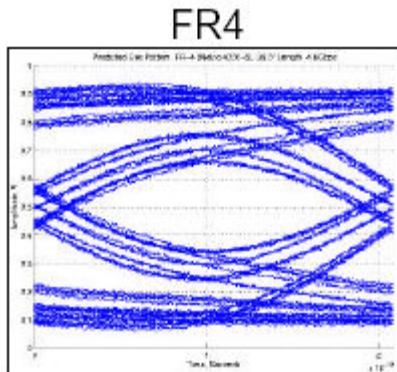
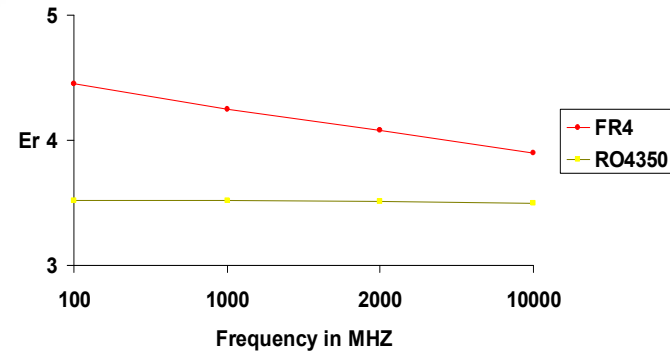
Signal Dispersion

- ◆ Constant time delay is necessary to ensure that signals arrive undistorted at the destination



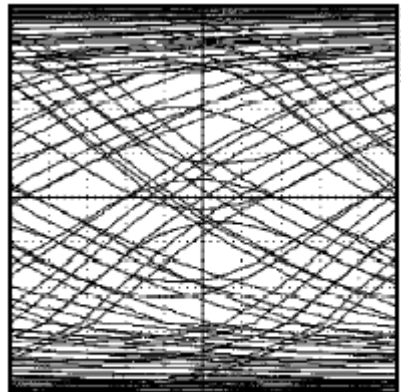
Signal Dispersion Example

- ◆ Eye Diagram
- ◆ 4.8 Gbps
- ◆ 36" trace length

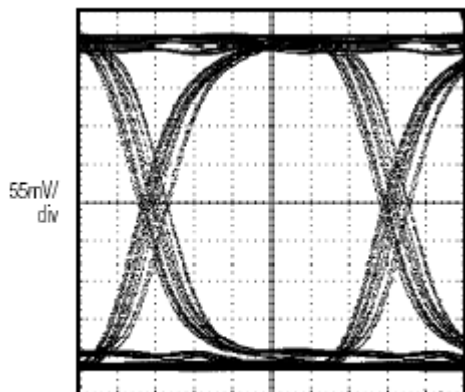


Mitigation of Dispersion

- ◆ More Stable Dielectric
 - Option for new designs
- ◆ Pre-Emphasis Filter
 - Option for new designs or design upgrade
- ◆ Equalizer
 - Option for new designs or design upgrade
 - Maxim MAX3784 (40" length, 6 mil, FR4, 5 Gbps)



32ps/div

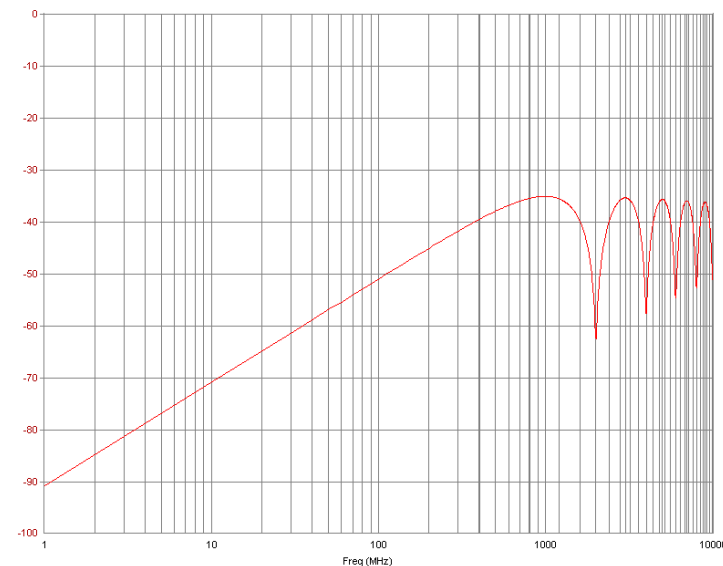
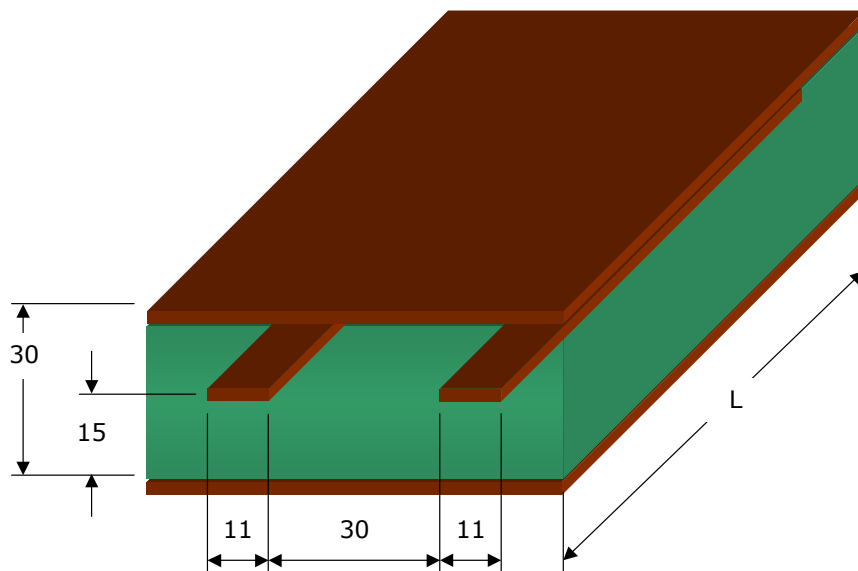


55mV/
div

32ps/div

Coupling

- ◆ Traces run in close proximity will couple
- ◆ Coupling is determined by geometry
 - trace separation, distance to ground(s) & parallel length
 - peaks at $\lambda/4$ and below $\lambda/4$ slope is 20 dB/decade



Notes:

1. Material FR4, $\epsilon_r = 4.5$
2. Parallel length = $\lambda/4 = 1.39''$ at 1 GHz
3. Trace height = 1.4 mils

Coupling Examples

- ◆ Strip-Line
11 mil width
 $\lambda/4 \approx 1.39''$

s	Coupling
0.011"	18 dB
0.030"	35 dB

*Note:
Micro-Strip is more prone
to coupling*

- ◆ Micro-Strip
54 mil width
 $\lambda /4 \approx 1.60''$

s	Coupling
0.030"	18 dB
0.054"	23 dB

Notes:

1. Copper: 1 oz, electrodeposited
2. FR4 dielectric constant: 4.50, height: 30 mils
3. F = 1.0 GHz

Mitigation of Coupling

- ◆ Separation of traces on same layer
- ◆ Reduce length of parallel run
- ◆ Run on separate non-adjacent layers
 - Ground plane in between
- ◆ Orthogonal runs on adjacent layers
- ◆ Run guard trace
 - Ground trace between lines
- ◆ Shield (for micro-strip)
- ◆ Dielectric height allocation



More Coupling

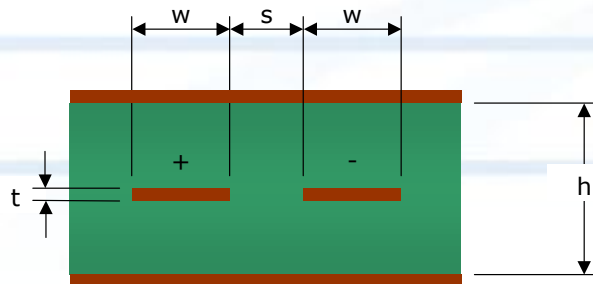


Less Coupling

Differential Pairs

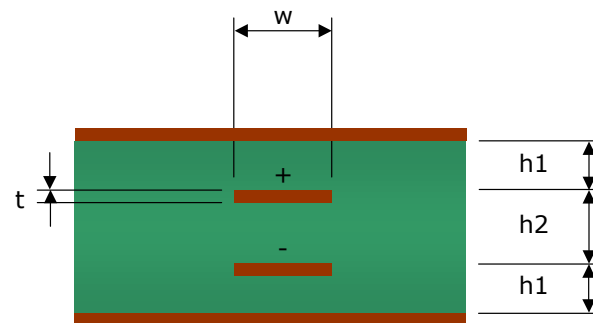
- ◆ Lower Cross-talk, Lower Radiation
- ◆ Common mode noise rejection
- ◆ Reduces ground reference problems
- ◆ High dynamic range analog applications
 - Log Amplifiers
 - High Resolution ADC/DAC
- ◆ Low noise (small signal) analog applications
 - Transducers
- ◆ Critical High Speed Digital Applications
 - Low amplitude clocks
 - Low jitter requirements

Differential Pair Routing Options



Edge Coupled

- ◆ Geometry and spacing defined by artwork
- ◆ High differential impedance easily achievable
- ◆ Impedance reduced as "s" is reduced
- ◆ As "s" is increased, impedance approaches 2x single ended impedance
- ◆ Difficult to rout through fine pitch holes

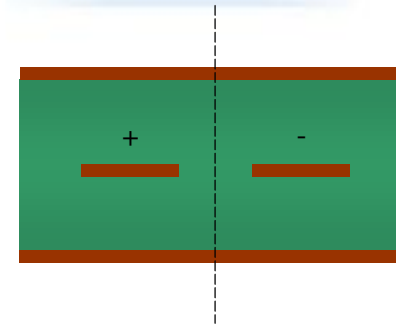


Broadside Coupled

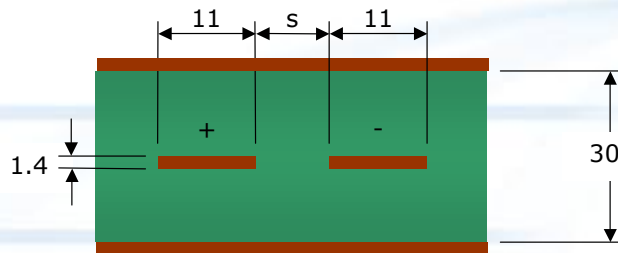
- ◆ Geometry is effected by layer registration
- ◆ Low differential impedance easily achievable
- ◆ Easy to route, easy to maintain matched lengths

Differential Impedance Definitions

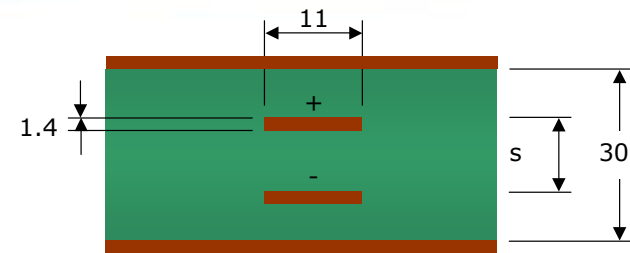
- ◆ **Single-Ended Impedance (Z_0)**
Impedance on a single line with respect to ground when not coupled to another line
 $(Z_0 = \sqrt{Z_{Odd}Z_{Even}})$
- ◆ **Differential Impedance (Z_{DIF})**
The impedance on one line with respect to the coupled line, when the lines are driven by equal and opposite signals
- ◆ **Odd Mode Impedance (Z_{Odd})**
Impedance on a single line with respect to ground when the other coupled line is driven by equal and opposite signals ($Z_{DIF} = 2Z_{Odd}$)
- ◆ **Common Mode Impedance (Z_{CM})**
Impedance of the two lines combined with respect to ground
- ◆ **Even Mode Impedance (Z_{Even})**
The impedance on one line with respect to ground when the coupled line is driven by an equal and in-phase signal ($Z_{Even} = 2Z_{CM}$)



Differential Impedance Examples



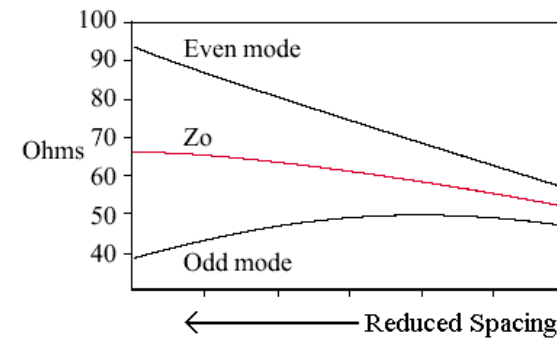
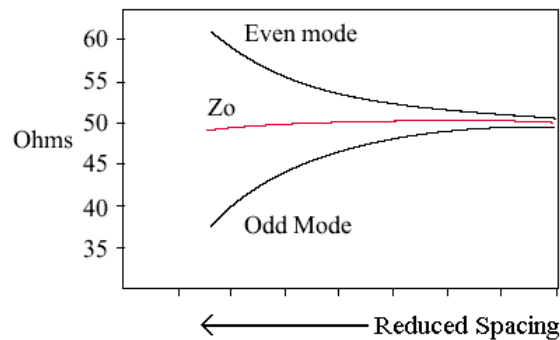
Edge Coupled



Broadside Coupled

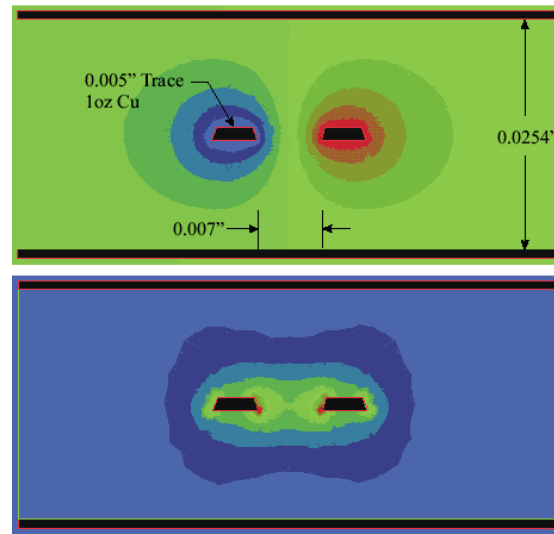
S	Z _{Even}	Z _{Odd}	Z _o	Z _{Diff}
100	49.4	49.4	49.4	98.8
25	50.9	47.9	49.4	95.8
10	56.4	41.9	48.6	83.8

S	Z _{Even}	Z _{Odd}	Z _o	Z _{Diff}
20	41.3	34.7	37.8	69.4
10	68.6	34.7	48.8	69.4



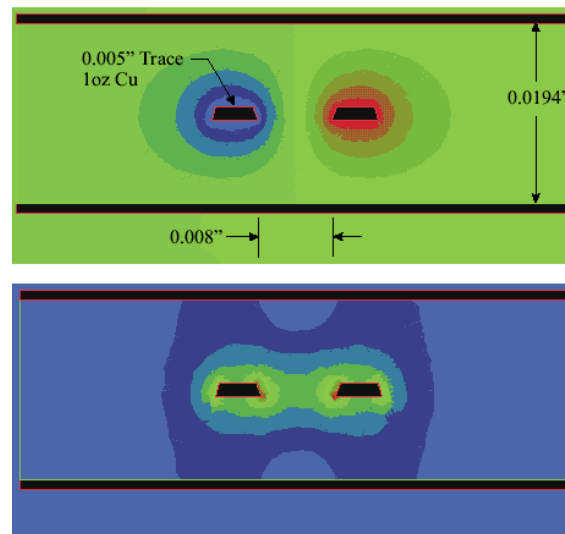
Field Intensity - 1

- ◆ When coupled lines are close, most of the electric field is concentrated between the conductors
 - Low ground currents



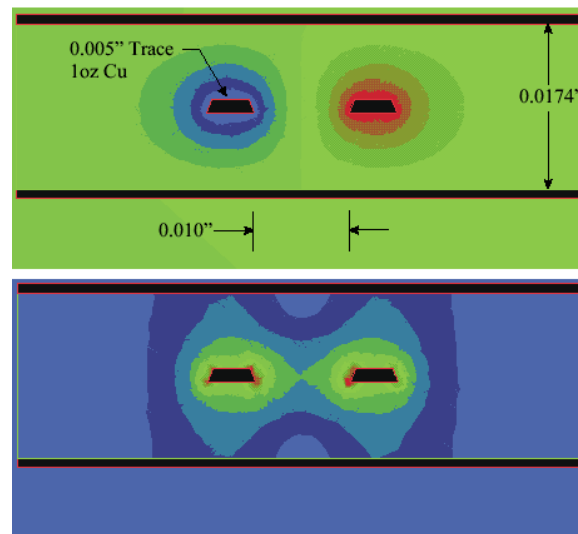
Field Intensity – 2

- ◆ As the coupled lines are separated and/or the ground planes are brought closer, less of the electric field is concentrated between the conductors, and more of the field is concentrated between the ground planes and the conductors



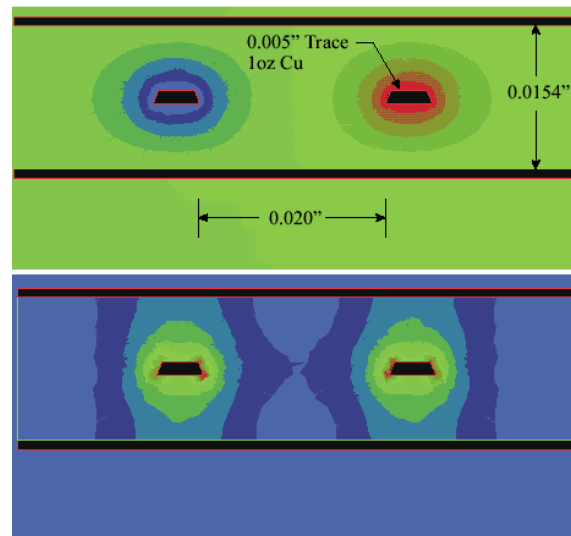
Field Intensity - 3

- ◆ As the coupled lines are separated and/or the ground planes are brought closer, less of the electric field is concentrated between the conductors, and more of the field is concentrated between the ground planes and the conductors



Field Intensity - 4

- ◆ When coupled lines are far apart, most of the electric field is concentrated between the ground planes and the conductors
 - More ground return current



PWB Pad and Trace Parameters

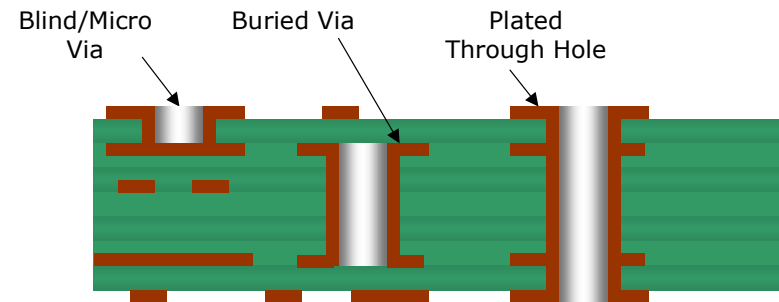
	10 mil trace	20 mil trace	100 mil trace	42 x 42 (\approx 0603)	60 x 60 (\approx 0805)
Capacitance	2.2 pF/in	3.3pF/in	11.6pF/in	0.24 pF	0.45 pF
Inductance	9.9 nH/in	7.2 nH/in	2.4 nH/in	0.19 nH	0.21 nH

Notes:

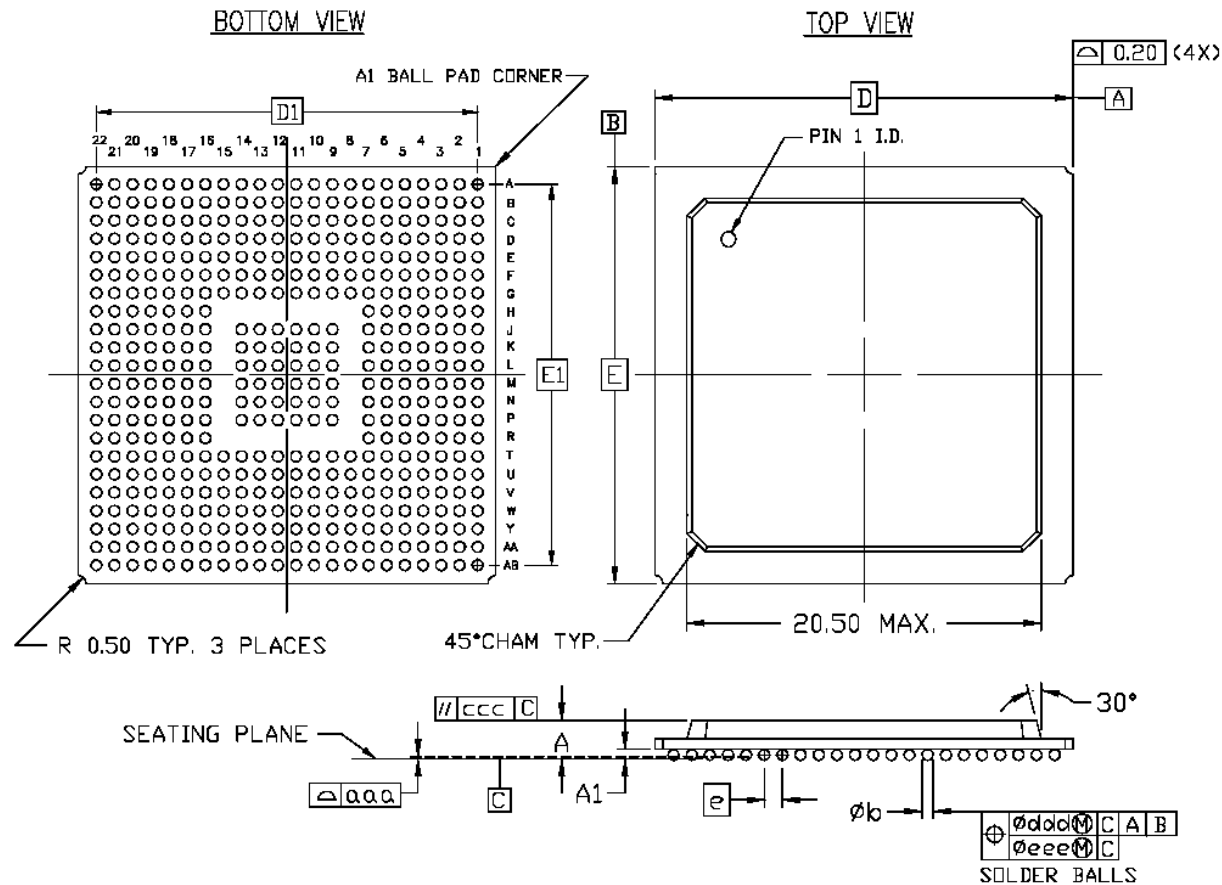
1. Copper: 1 oz, electrodeposited, strip-line.
2. FR4 dielectric constant: 4.50, loss tangent 0.025, height 10 mils.

Vias

- ◆ Needed to interconnect layers
- ◆ Minimize use
 - Introduce discontinuities (R, L, C)
 - “Choke-off” routing
 - Perforate Ground/Supply Planes
- ◆ Traditionally implemented with Plated Through Holes (PTHs)
- ◆ Consider Blind, Buried or Micro (4-6 mils) Vias
 - Escape routing of high density components
 - Additional processing cost can be offset by reduction in layers



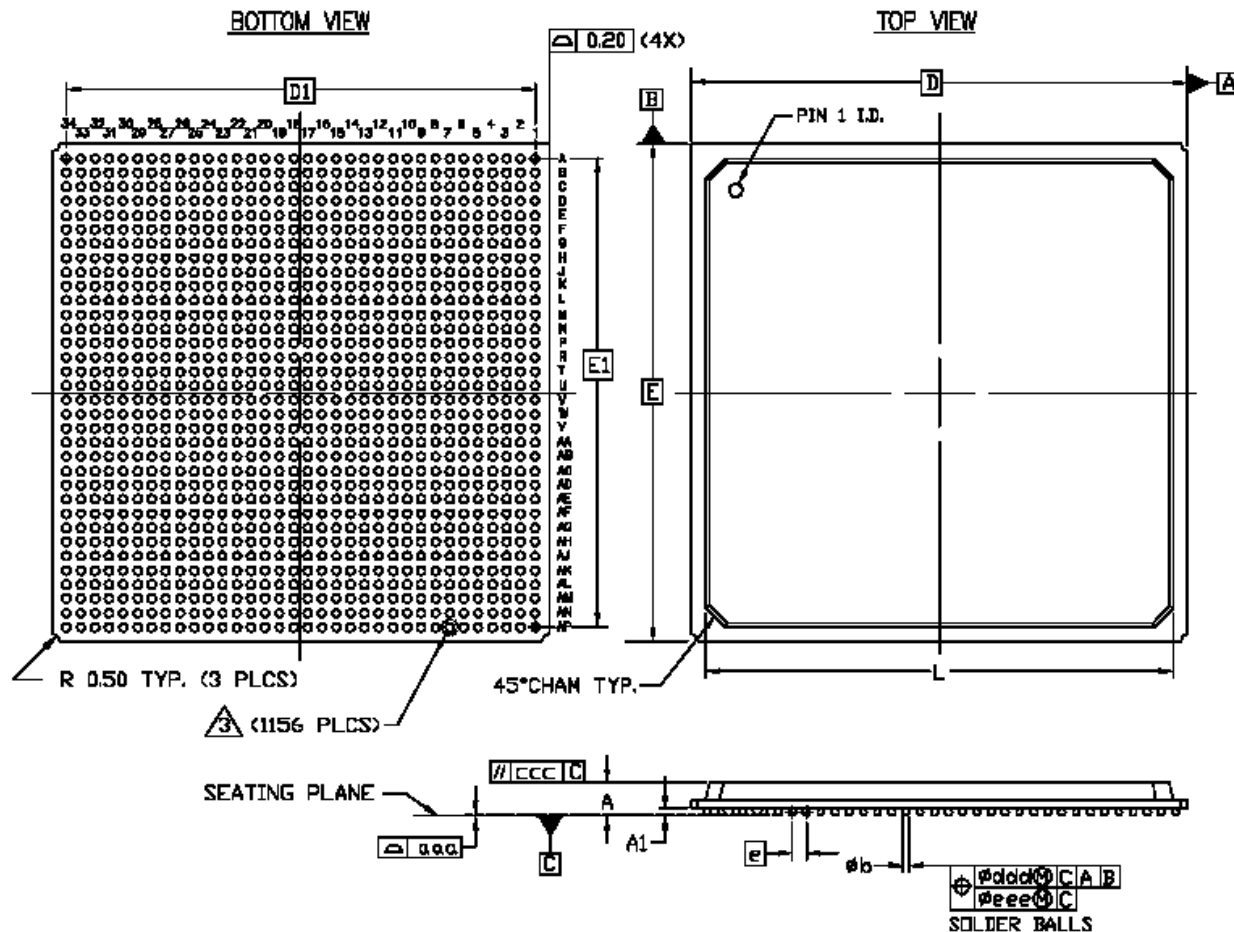
Fine Pitch BGA (FG456) Package



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.20	2.60
A1	0.40	0.50	0.60
D/E	23.00 BSC		
D1/E1	21.00 REF		
e	1.00 BSC		
ϕb	0.50	0.60	0.70
aaa	0.20	0.20	0.20
ccc	0.35	0.35	0.35
ddd	0.30	0.30	0.30
eee	0.10	0.10	0.10
M	22		

Courtesy of
Xilinx

Fine Pitch BGA (FG1156) Package



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	<i>typ</i>	2.33	2.60	
A ₁	0.40	0.50	0.60	
D/E	35.00 BSC			
D ₁ /E ₁	33.00 REF			
e	1.00 BSC			
φb	0.50	0.60	0.70	
φaaa	<i>typ</i>	<i>typ</i>	0.20	
φccc	<i>typ</i>	<i>typ</i>	0.35	
φddd	<i>typ</i>	<i>typ</i>	0.30	
φeee	<i>typ</i>	<i>typ</i>	0.10	
L	<i>typ</i>	<i>typ</i>	33.05	
M	34			2
REF.	JEDEC MS-034-AAR			

Courtesy of
Xilinx

Via Parameters

Via Dia	10			12			15			25		
Pad Dia	22			24			27			37		
Anti-Pad Dia	30			32			35			45		
	R	L	C	R	L	C	R	L	C	R	L	C
Length: 60 Planes: 5	1.55	0.78	0.48	1.25	0.74	0.53	0.97	0.68	0.60	0.57	0.53	0.83
Length: 90 Planes: 7	2.3	1.33	0.66	1.88	1.24	0.69	1.45	1.15	0.78	0.85	0.92	1.08

Notes:

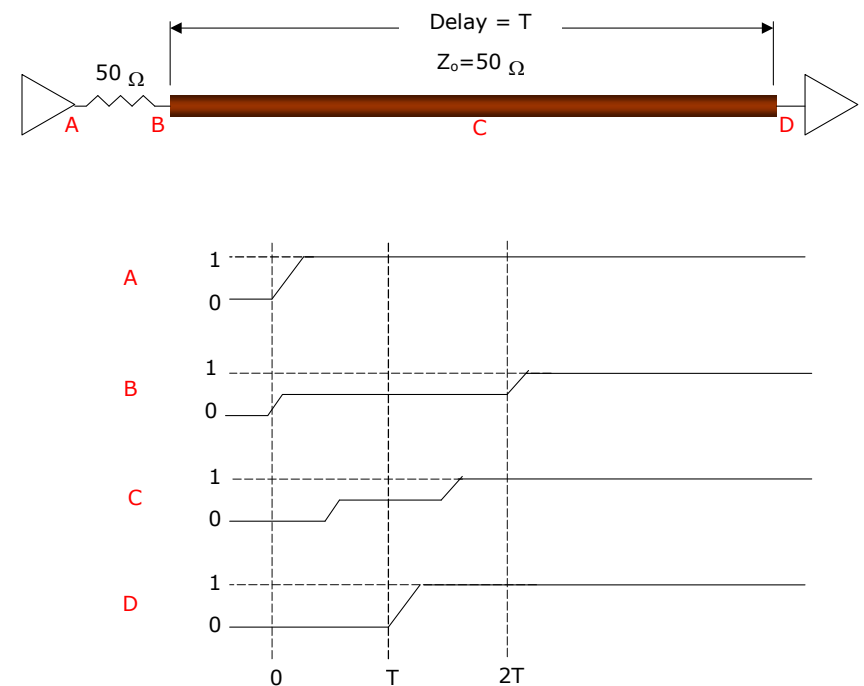
1. R in mΩ , L in nH, C in pF
2. Dimensions are in mils.
3. Planes are evenly spaced.
4. Via inductance can be approximated by:

$$L = 5.08h \left[\ln \left(\frac{4h}{d} \right) - 0.75 \right] \text{ nH}$$

h and d are in inches

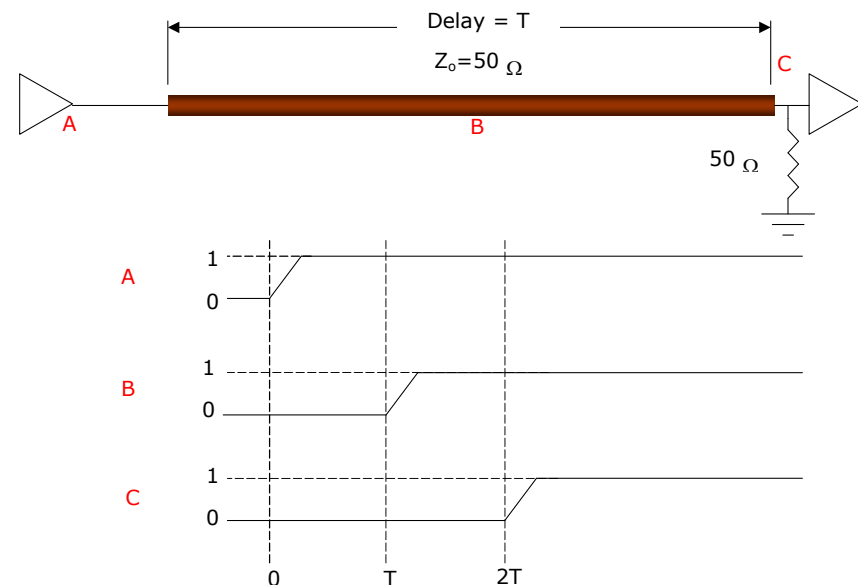
Source Terminations

- ◆ Driving waveform is reduced in half by series resistor at start of propagation
- ◆ Driving signal propagates at half amplitude to end of line
- ◆ At end reflection coefficient is +1
- ◆ Reduced peak current demands on driver
- ◆ Limited use with daisy-chained receivers



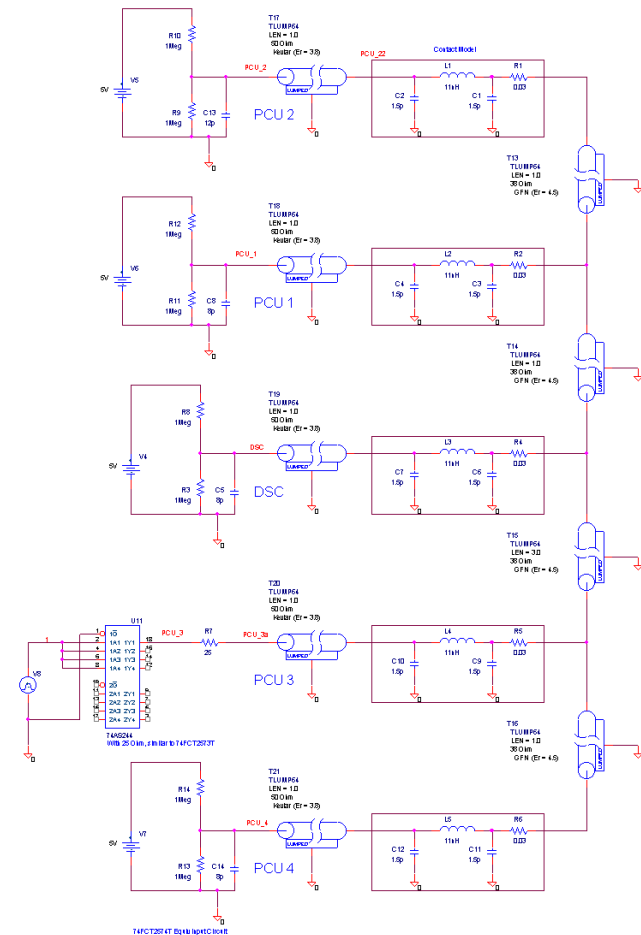
Destination Terminations

- ◆ Driving waveform propagates at full intensity over trace
- ◆ Reflections dampened by terminating resistor(s)
- ◆ Received voltage is equal to transmitting voltage (ignoring losses)
- ◆ Increased peak current demands on driver
- ◆ More applicable to daisy-chained receivers (first incident switching)
- ◆ Thevenin termination reduces steady-state drive current



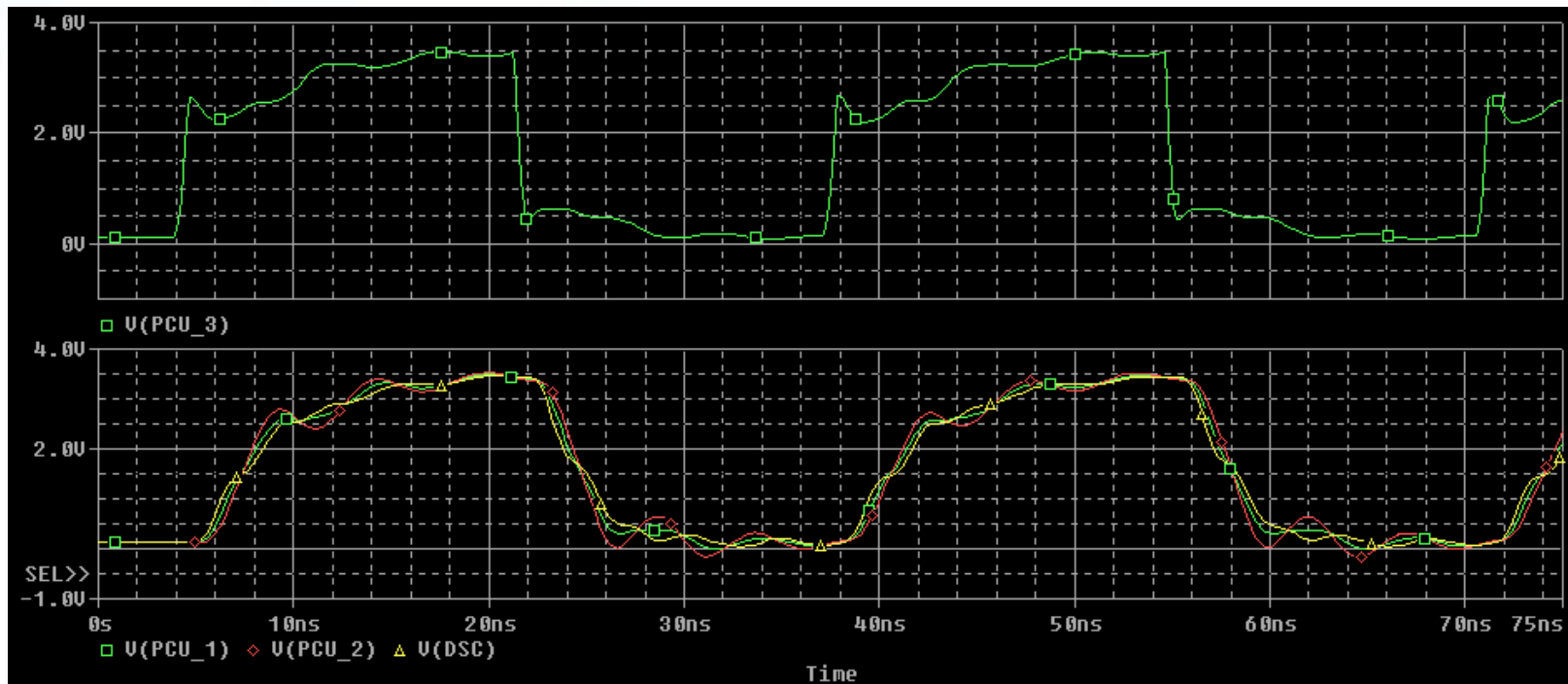
“Intentional” Mismatch Example

- ◆ Five selectable sources
- ◆ Four destinations
- ◆ Modeled signal paths
 - CCA PWB
 - Back Plane PWB
 - Connectors
 - Driver
- ◆ Took advantage of relatively slow clock (30 MHz)



“Intentional” Mismatch Example

- ◆ Allow reflections to dissipate before clocking data (Clocks distributed point-to-point)



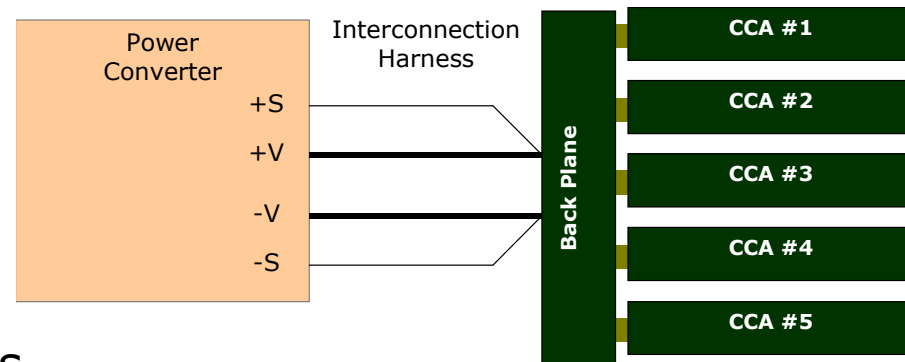
Power Distribution & Grounding

Power Distribution Purpose

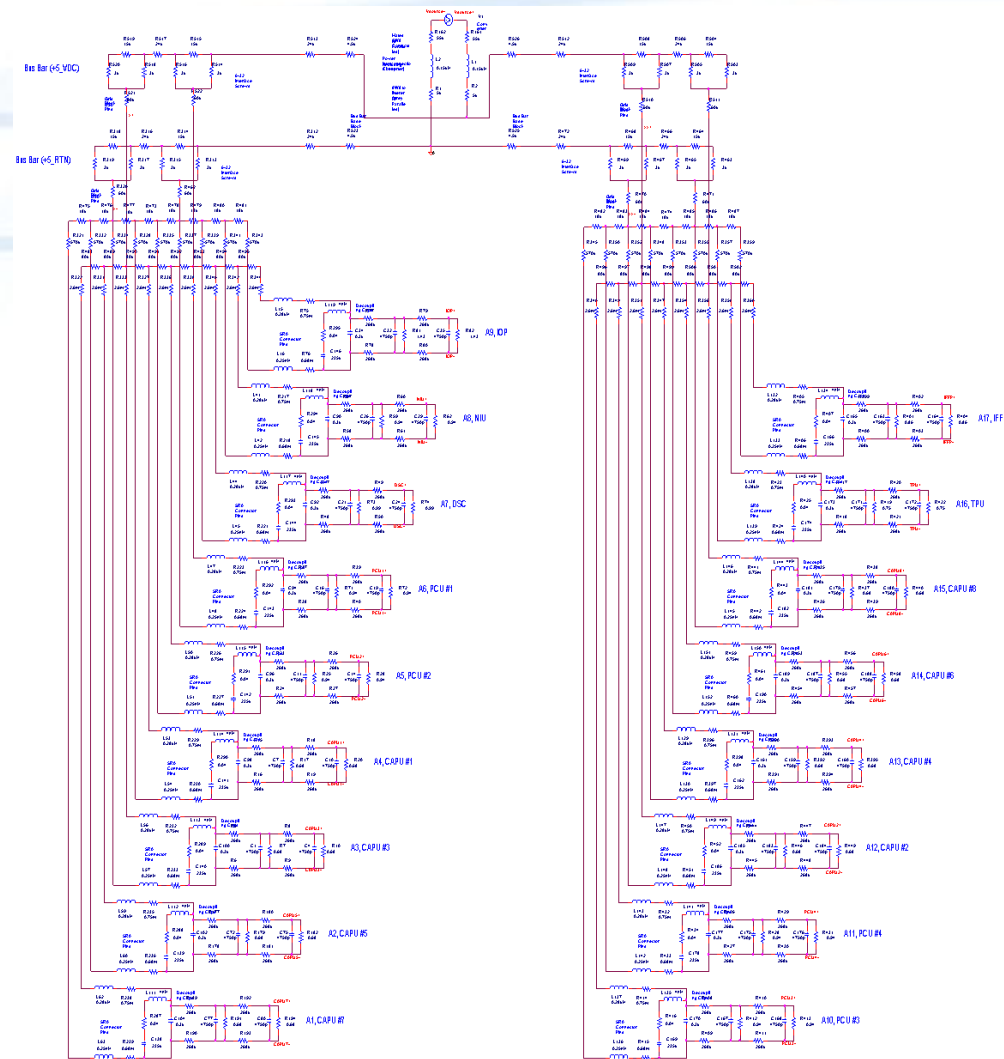
- ◆ To distribute the supply voltages necessary to all components within the required regulation
- ◆ To provide a reliable reference (ground) for all circuitry

Supply Power Loss Budget

- ◆ Distribution loss contributes to supply voltage error delivered to CCA components
- ◆ Complete loss budget needs to be established, especially in high power applications
 - Power Supply Voltage Tolerance
 - Harnessing Loss
 - Connector Loss
 - Back-Plane Loss
 - PWB Loss
- ◆ Remote Sensing
 - Compensate for some losses
 - Location important
 - "Open Sense" protection



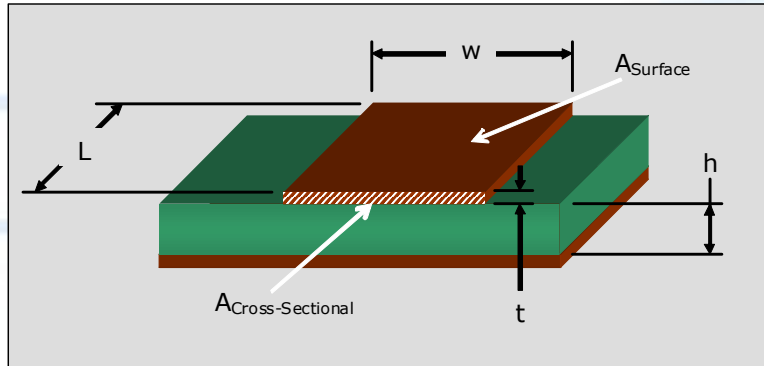
DC Loss Model



Power Distribution Considerations

- ◆ **Dedicated Planes to Ground and Supply**
 - Establishes low inductance distribution (when adjacent)
 - Parallel planes create distributed capacitance (typically not significant except for high ϵ_r and/or thin material)
 - Gould (25 μm , $\epsilon_r = 3.5$)
- ◆ **Through-holes perforate planes**
 - Increases resistance
- ◆ **Distributing localized supplies for analog**
 - A dedicated voltage plane may not be practical or necessary
 - Rout power traces between ground planes as needed for isolation

Plane Capacitance, Inductance, Resistance



Resistance

$$R_{DC} = \rho \frac{l}{A_{Cross-Sectional}} = \rho \frac{l}{tw} \quad \rho = 0.679 \mu\Omega - inch$$

Allowing $l=w$ permits calculation of Resistance per Square.

$$\text{Resistance/Square} = \rho \frac{1}{t} = (0.679 \mu\Omega - in) \frac{1}{0.0014} = 485 \mu\Omega / \text{Square}$$

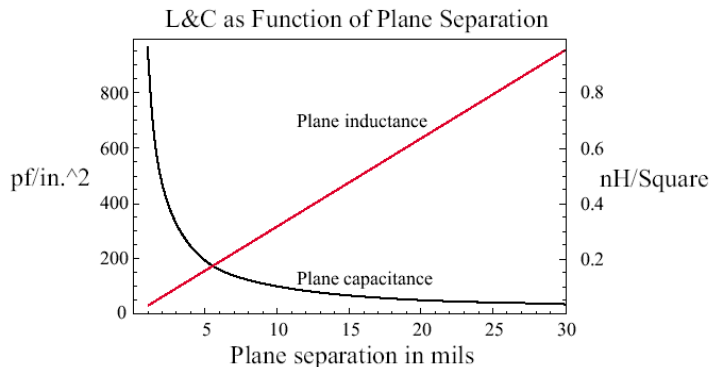
(For 1 ounce copper which is 0.0014" thick)

Inductance

$$L = \mu_0 h \frac{l}{w} \quad \mu_0 = 4\pi \times 10^{-7} \frac{H}{m} = 0.32 \frac{nH}{inch}$$

Capacitance

$$C = \epsilon_0 \epsilon_r \frac{LW}{h} = \epsilon_0 \epsilon_r \frac{A_{Surface}}{h} \quad \epsilon_r = 225 \times 10^{-15} \frac{F}{in}$$



FR4 Dielectric Thickness (mils)	Inductance (pH/square)	Capacitance (pF/inch ²)
8	260	127
4	130	253
2	65	506

Capacitor Parameters

- ◆ Physical capacitors have parasitic elements that limit their ability to stabilize supply lines
- ◆ Equivalent series inductance (ESL)
- ◆ Equivalent Series Resistance (ESR)

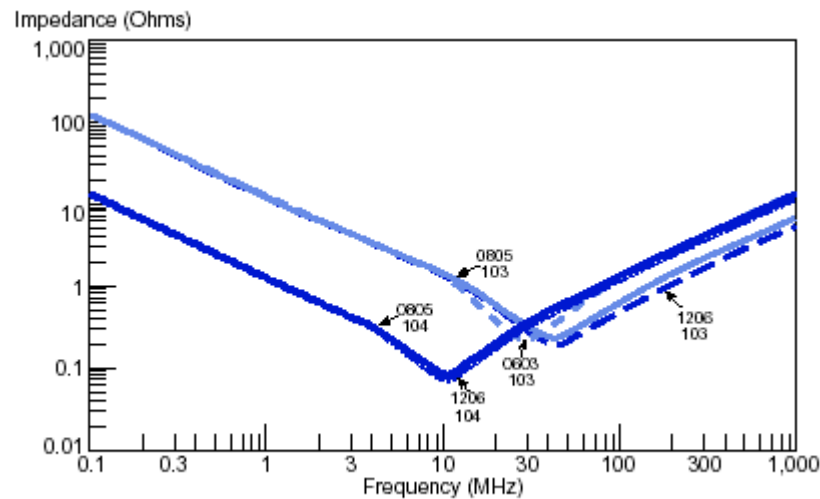
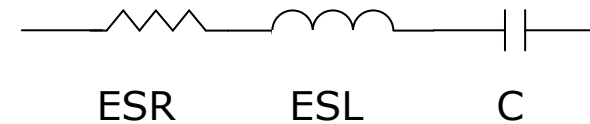


FIGURE 5 Impedance versus Frequency X7R Dielectric

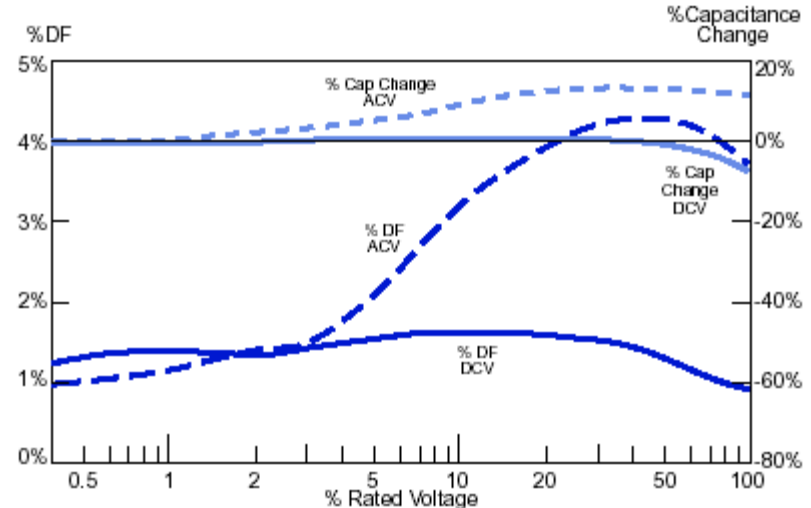


FIGURE 7. X7R Capacitance & DF versus Applied AC/DC Voltages

Plots courtesy of Kemet

Capacitor Parameters

Part Number	Package	Capacitance (uF)	ESL (nH)	ESR (Ω)	SRF (MHz)
C0603C103K5RAC, Kemet	EIA 0603	0.01	1.8	0.25	38
C0805C104K5RAC, Kemet	EIA 0805	0.10	1.9	0.10	12
T491B685K010AS, Kemet	EIA 3528-21	6.8	1.9	0.3	1.4
T494C476K010AS, Kemet	EIA 6032-28	47	2.2	0.2	0.5

$$f_{SRF} = \frac{1}{2\pi\sqrt{LC}}$$

Self Resonant Frequency

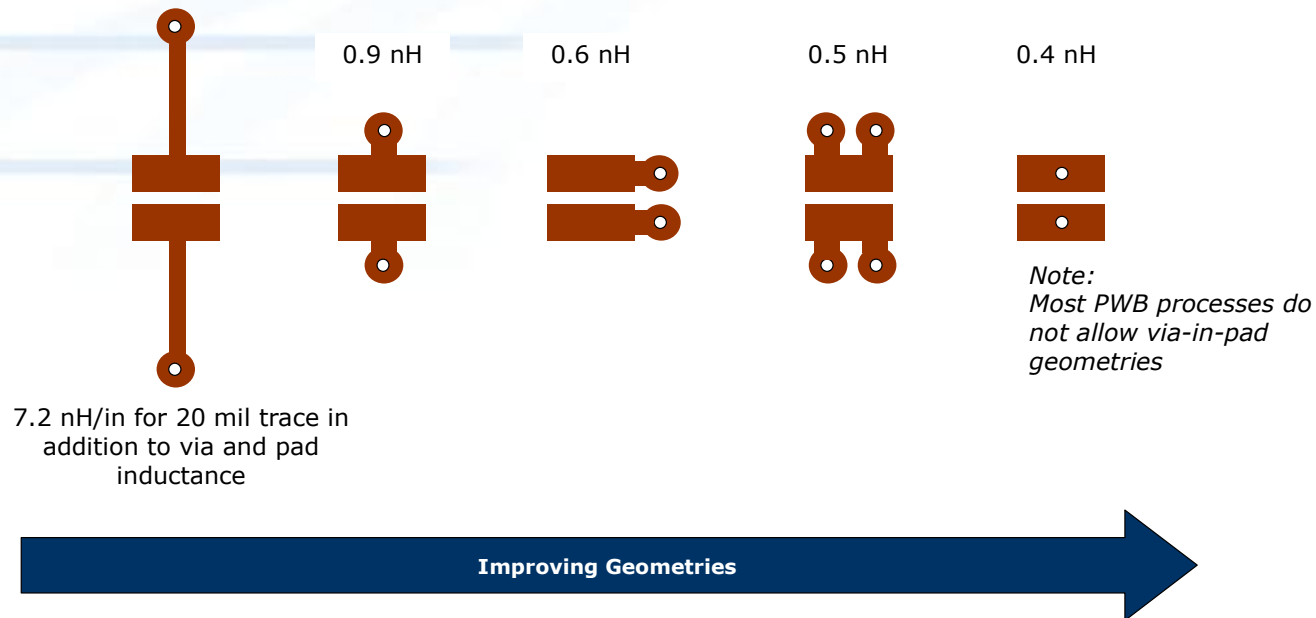
$$Q = \frac{1}{DF} = \frac{X_C}{R} = \frac{1}{2\pi f C R}$$

Quality Factor, Dissipation Factor

Capacitor Guidelines

- ◆ Parasitic inductance is predominantly determined by package size
- ◆ Connect capacitor pads as directly as practical
- ◆ Don't share cap vias

Capacitor Mounting Pads

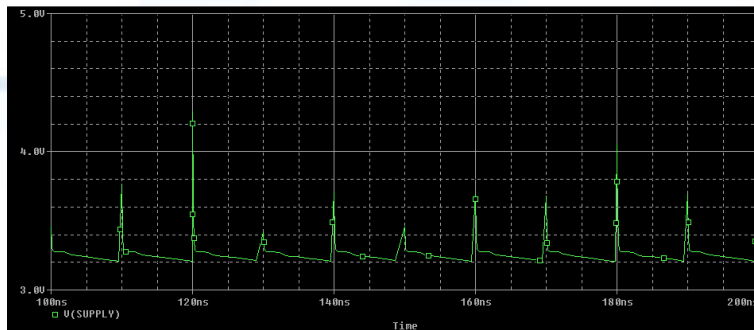


Notes:

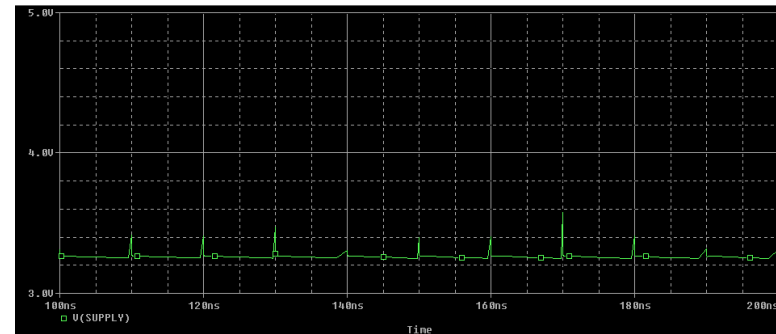
1. Copper: 1 oz, electrodeposited, strip-line
2. FR4 dielectric constant: 4.50, loss tangent 0.025, height 10 mils

Decoupling Examples

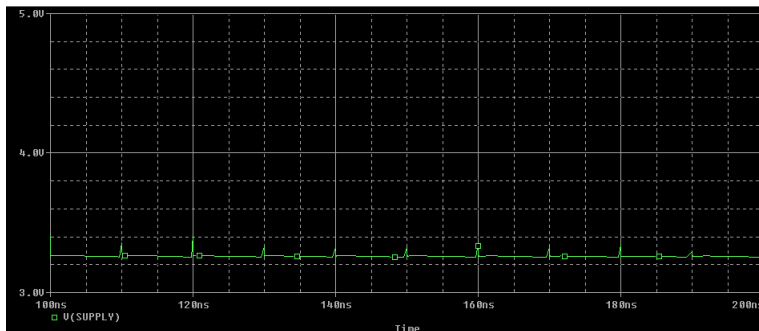
- ◆ 100 MHz Logic Device, 100 mA to 150 mA step load change



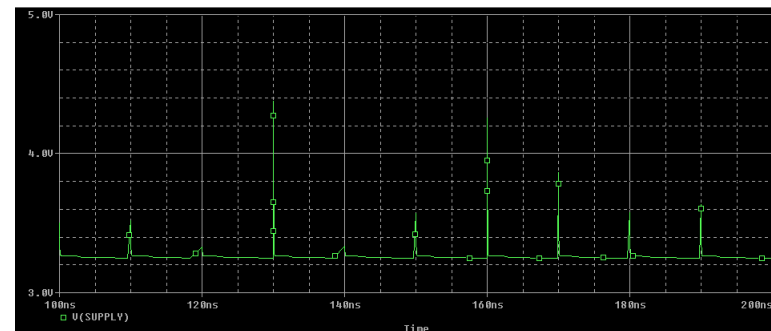
6.8 uF, Ripple: 1 Vpp



6.8 uF + 0.1 uF, Ripple: 0.3 Vpp



*6.8 uF + 0.1 uF + 0.01 uF,
Ripple: 0.1 Vpp*



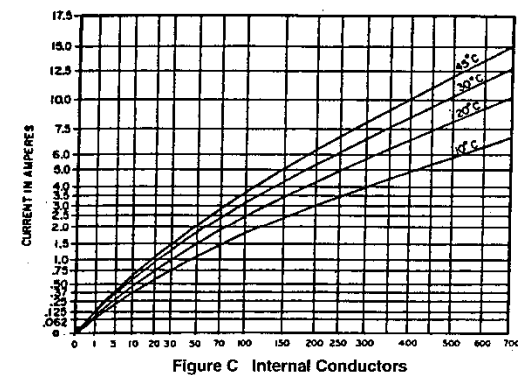
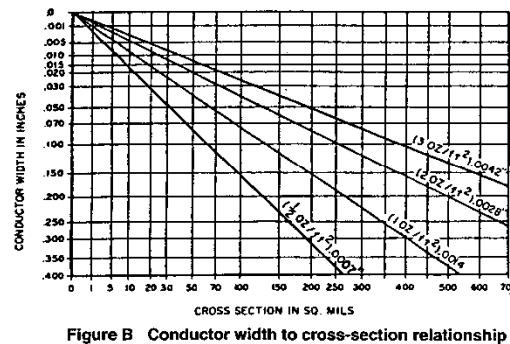
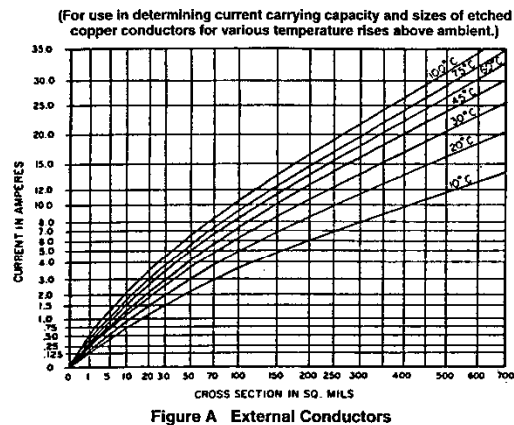
*6.8 uF + 0.1 uF + 0.01 uF w/ long
traces, Ripple: 1.1 Vpp*

Current Carrying Capability of PWB Traces

- ◆ Trace Cross section (w,t)
- ◆ Position of trace (outer layer, inner layer)
- ◆ Maximum acceptable temperature rise
- ◆ IPC-2221, Figure 6-4, can be used as general guideline
- ◆ Thermal modeling may be needed in critical applications

Trace Width Example

- ◆ Application
 - Inner trace, 1 ounce, maximum fault current is 2 Amps
 - Max CCA temp +90 °C, max PWB temp +150 °C, Margin 30 °C
 - Allowable Temp rise = 150 – 90 – 30 = 30 °C
- ◆ Determine Cross Section from "C" is 56 sq mils
- ◆ Determine width from "B" to be 40 mils



References and Vendors

References

- ◆ IPC-2221 Generic Standard on Printed Board Design
- ◆ IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards
- ◆ IPC-2223 Sectional Design Standard for Flexible Printed Boards
- ◆ IPC-4101 Specification for Base Materials for Rigid and Multi-Layer Printed Boards
- ◆ IPC-6012 Qualification and Performance Specification for Rigid Printed Boards
- ◆ IPC-SM-782 Surface Mount Design & Land Pattern Standard
- ◆ High Speed Digital Design, Howard W Johnson
- ◆ Even Mode Impedance, Polar Instruments, Application Note AP157

References (continued)

- ◆ Effect of Etch Factor on Printed Wiring, Steve Monroe, 11th Annual Regional Symposium on EMC
- ◆ Transmission Line Design Handbook, Brian C Wadell
- ◆ The Impact of PWB Construction on High-Speed Signals, Chad Morgan AMP/Tyco
- ◆ Transmission Line RAPIDESIGNER Operation and Applications Guide (AN-905) National Semiconductor
- ◆ PWB Design and Manufacturing Considerations for High Speed Digital Interconnection, Tom Buck, DDI
- ◆ Power Distribution System Design (XAPP623) Mark Alexander, Xilinx
- ◆ Surface Mount Capacitors, Kemet, Catalog F-3102G

Material Suppliers

- ◆ Arlon, www.ArlonMed.com
- ◆ Bergquist, www.BergquistCompany.com
- ◆ Isola, www.Vonrollisola.com
- ◆ Park-Nelco, www.ParkNelco.com
- ◆ Polyclad, www.Polyclad.com
- ◆ Rogers, www.Rogers-Corp.com
- ◆ Taconic, www.Taconic-add.com

PWB Fabricators

- ◆ DDI, www.DDIglobal.com
- ◆ Parlex, www.Parlex.com
- ◆ Tyco, www.PrintedCircuits.TycoElectronics.com

Design Tools

- ◆ Ansoft

www.Ansoft.com



- ◆ Cadance

www.Cadence.com



- ◆ Eagleware

www.EagleWare.com



- ◆ Polar Instruments

www.PolarInstruments.com



Viewgraphs Are Online

- ◆ **Visit the IEEE Long Island Website
www.IEEE.LI**
- ◆ **Click on Electromagnetic Compatibility Page**
- ◆ **Scroll down to the Viewgraphs
*Analog, RF & EMC Considerations in Printed
Wiring Board Design***

Thank You!