

Fully-Differential Amplifiers

James Karki
AAP Precision Analog

ABSTRACT

Differential signaling has been commonly used in audio, data transmission, and telephone systems for many years because of its inherent resistance to external noise sources. Today, differential signaling is becoming popular in high-speed data acquisition, where the ADC's inputs are differential and a differential amplifier is needed to properly drive them.

Two other advantages of differential signaling are reduced even-order harmonics and increased dynamic range.

This report focuses on integrated, fully-differential amplifiers, their inherent advantages, and their proper use. It is presented in three parts: 1) Fully-differential amplifier architecture and the similarities and differences from standard operational amplifiers, their voltage definitions, and basic signal conditioning circuits; 2) Circuit analysis (including noise analysis), provides a deeper understanding of circuit operation, enabling the designer to go beyond the basics; 3) Various application circuits for interfacing to differential ADC inputs, antialias filtering, and driving transmission lines.

Contents

1	Introduction	3
2	What Is an Integrated, Fully-Differential Amplifier?	3
3	Voltage Definitions	5
4	Increased Noise Immunity	5
5	Increased Output Voltage Swing	6
6	Reduced Even-Order Harmonic Distortion	6
7	Basic Circuits	6
8	Circuit Analysis and Block Diagram	8
9	Noise Analysis	13
10	Application Circuits	15
11	Terminating the Input Source	15
12	Active Antialias Filtering	20
13	V_{OCM} and ADC Reference and Input Common-Mode Voltages	23
14	Power Supply Bypass	25
15	Layout Considerations	25
16	Using Positive Feedback to Provide Active Termination	25
17	Conclusion	27

List of Figures

1	Integrated Fully-Differential Amplifier vs Standard Operational Amplifier	4
2	Simplified Fully-Differential Amplifier	4
3	Fully-Differential Amplifier Voltage Definitions	5
4	Fully-Differential Amplifier Noise Immunity	5
5	Differential Output Voltage Swing	6
6	Amplifying Differential Signals	7
7	Converting Single-Ended Signals to Differential Signals	7
8	Analysis Circuit	8
9	Block Diagram	9
10	Single-Ended-to-Differential Amplifier	11
11	Circuit With $\beta_1 = 0$	11
12	Circuit With $\beta_2 = 0$	12
13	Circuit With $\beta_2 = 1$	12
14	Circuit With $\beta_1 = 0$ and $\beta_2 = 1$	12
15	Noise Analysis Circuit	13
16	Block Diagram of the Amplifier's Input-Referred Noise	14
17	Terminating a Differential Input Signal	16
18	Differential Termination Impedance	16
19	Differential Thevenin Equivalent	16
20	Differential Solution for Gain = 1	17
21	Terminating a Single-Ended Input Signal	17
22	Single-Ended Termination AC Impedance	18
23	Single-Ended Thevenin Equivalent	18
24	Single-Ended Solution for Gain = 1	19
25	Balance vs Unbalanced Amplifiers	20
26	First-Order Active Low-Pass Filter	21
27	First-Order Active Low-Pass Filter With Passive Second Pole	21
28	Third-Order Low-Pass Filter Driving an ADC	22
29	1-MHz, Second-Order Butterworth Low-Pass With Real Pole at 15.9 MHz	23
30	Internal Reference Circuit of the ADS809 and Recommended Bypass Scheme	24
31	V_{OCM}	24
32	Using Positive Feedback to Provide Active Termination	26
33	Output Waveforms With Active and Standard Termination	27

1 Introduction

Why use integrated fully-differential amplifiers?

- Increased immunity to external noise
- Increased output voltage swing for a given voltage rail
- Ideal for low-voltage systems
- Integrated circuit is easier to use
- Reduced even-order harmonics

Professional audio engineers use the term *balanced* to refer to differential-signal transmission. This conveys the idea of symmetry, which is very important in differential systems. The driver has balanced outputs, the line has balanced characteristics, and the receiver has balanced inputs.

There are two methods commonly used to manipulate differential signals: electronic and transformer.

- Electronic methods have advantages, such as lower cost, small size and weight, and wide bandwidth.
- Transformers offer very good CMRR vs frequency, galvanic isolation, no power consumption (efficiencies near 100%), and immunity to very-hostile EMC environments.

This report focuses on electronic methods for signal conditioning differential signals using integrated, fully-differential amplifiers—such as the THS41xx and THS45xx families of high-speed amplifiers from Texas Instruments.

2 What Is an Integrated, Fully-Differential Amplifier?

An integrated, fully-differential amplifier is very similar in architecture to a standard, voltage-feedback operational amplifier, with a few differences as illustrated in Figure 1. Both types of amplifiers have differential inputs. Fully differential amplifiers have differential outputs, while a standard operational amplifier's output is single-ended. In a fully-differential amplifier, the output is differential and the output common-mode voltage can be controlled independently of the differential voltage. The purpose of the V_{ocm} input in the fully-differential amplifier is to set the output common-mode voltage. In a standard operational amplifier with single-ended output, the output common-mode voltage and the signal are the same thing. There is typically one feedback path from the output to the negative input in a standard operational amplifier. A fully-differential amplifier has multiple feedback paths, which is discussed in detail in this report.

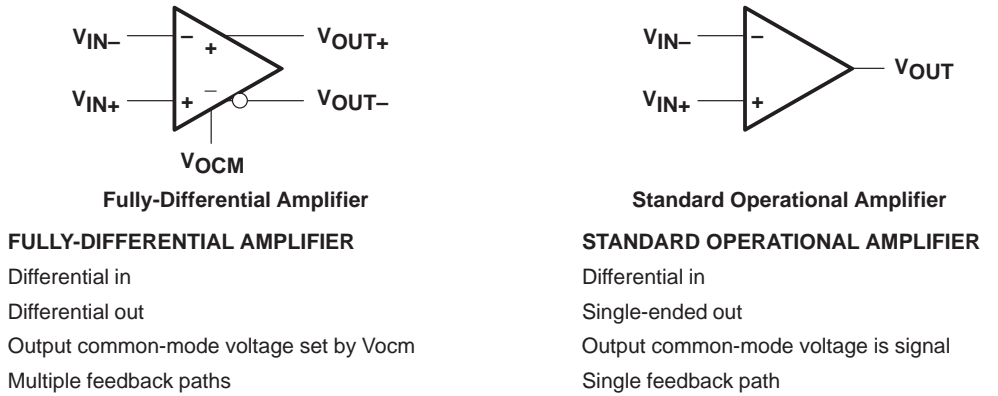


Figure 1. Integrated Fully-Differential Amplifier vs Standard Operational Amplifier

Figure 2 shows a simplified version of an integrated, fully-differential amplifier (representative of the THS41xx or the THS45xx). Q1 and Q2 are the input differential pair. In a standard operational amplifier, output current is taken from only one side of the input differential pair and used to develop a single-ended output voltage. In a fully-differential amplifier, currents from both sides are used to develop voltages at the high-impedance nodes formed at the collectors of Q3/Q5 and Q4/Q6. These voltages are then buffered to the differential outputs OUT+ and OUT-.

At first analysis, voltage common to IN+ and IN- does not produce a change in the current flow through Q1 or Q2 and thus produces no output voltage—it is rejected. The output common-mode voltage is not controlled by the input. The Vocm error amplifier maintains the output common-mode voltage at the same voltage applied to the Vocm pin by sampling the output common-mode voltage, comparing it to the voltage at Vocm, and adjusting the internal feedback. If not connected, Vocm is biased to the midpoint between VCC and VEE by an internal voltage divider.

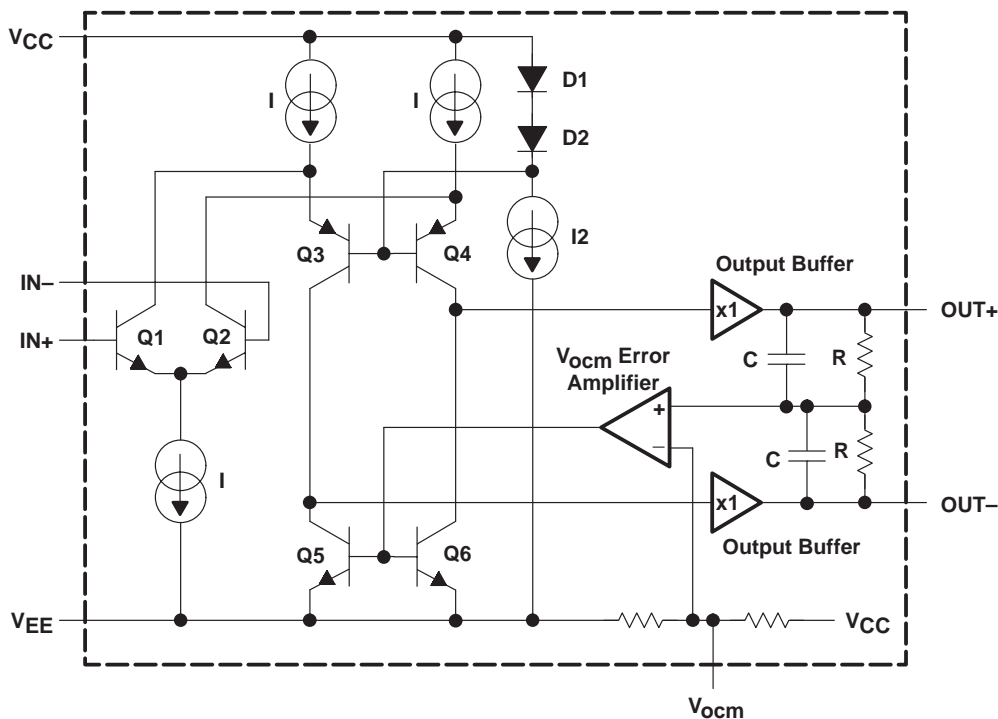


Figure 2. Simplified Fully-Differential Amplifier

3 Voltage Definitions

To understand the behavior of a fully-differential amplifier, it is important to understand the voltage definitions used to describe the amplifier. Figure 3 shows a block diagram used to represent a fully-differential amplifier and its input and output voltage definitions.

The voltage difference between the plus and minus inputs is the input differential voltage, V_{id} . The average of the two input voltages is the input common-mode voltage, V_{ic} .

The difference between the voltages at the plus and minus outputs is the output differential voltage, V_{od} . The output common-mode voltage, V_{oc} , is the average of the two output voltages, and is controlled by the voltage at V_{ocm} .

With $a(f)$ as the frequency-dependant differential gain of the amplifier, then $V_{od} = V_{id} \times a(f)$.

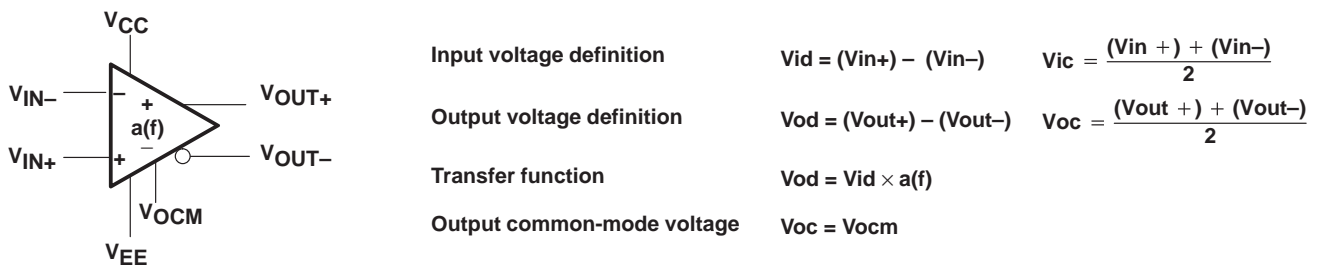


Figure 3. Fully-Differential Amplifier Voltage Definitions

4 Increased Noise Immunity

Invariably, when signals are routed from one place to another, noise is coupled into the wiring. In a differential system, keeping the transport wires as close as possible to one another makes the noise coupled into the conductors appear as a common-mode voltage. Noise that is common to the power supplies also appears as a common-mode voltage. Since the differential amplifier rejects common-mode voltages, the system is more immune to external noise. Figure 4 illustrates the noise immunity of a fully-differential amplifier.

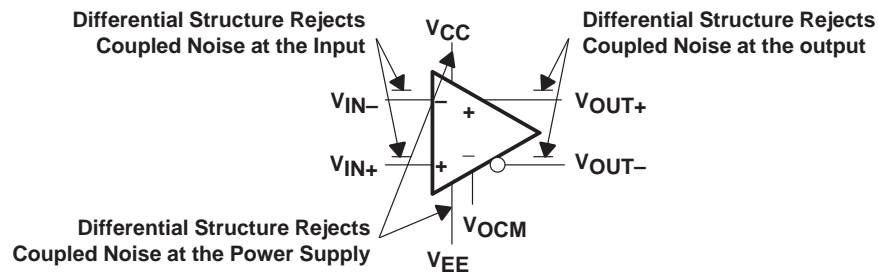
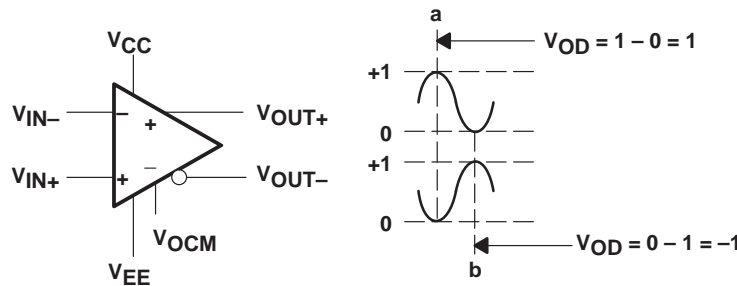


Figure 4. Fully-Differential Amplifier Noise Immunity

5 Increased Output Voltage Swing

Due to the change in phase between the differential outputs, the output voltage swing increases by a factor of 2 over a single-ended output with the same voltage swing. Figure 5 illustrates this. This makes them ideal for low voltage applications.



Differential Output Results in $V_{OD} p-p = 1 - (-1) = 2 \times SE$ Output

Figure 5. Differential Output Voltage Swing

6 Reduced Even-Order Harmonic Distortion

Expanding the transfer functions of circuits into a power series is a typical way to quantify the distortion products.

Taking a generic expansion of the outputs and assuming matched amplifiers, we get:

$$V_{out+} = k_1 V_{in} + k_2 V_{in}^2 + k_3 V_{in}^3 + \dots, \text{ and}$$

$$V_{out-} = k_1(-V_{in}) + k_2(-V_{in})^2 + k_3(-V_{in})^3 + \dots$$

$$V_{od} = 2k_1 V_{in} + 2k_3 V_{in}^3 + \dots, \text{ where } k_1, k_2 \text{ and } k_3 \text{ are constants.}$$

The quadratic terms gives rise to second-order harmonic distortion, the cubic terms gives rise to third-order harmonic distortion, and so on.

In a fully-differential amplifier, the odd-order terms retain their polarity, while the even-order terms are always positive. When the differential is taken, the even order terms cancel.

Real life is not quite this perfect. Lab testing of the THS4141 at 1 MHz shows that the second harmonic at the output is reduced by approximately 6 dB when measured differentially as compared to measuring either output single-ended. The third harmonic is unchanged between a differential and single-ended measurement.

7 Basic Circuits

In a fully-differential amplifier, there are two possible feedback paths in the main differential amplifier, one for each side. This naturally forms two inverting amplifiers, and inverting topologies are easily adapted to fully-differential amplifiers. Figure 6 shows how to configure a fully-differential amplifier with negative feedback to control the gain and maintain a balanced amplifier.

Symmetry in the two feedback paths is important to have good CMRR performance. CMRR is directly proportional to the resistor matching error—a 0.1% error results in 60 dB of CMRR.

The Vocm error amplifier is independent of the main differential amplifier. The action of the Vocm error amplifier is to maintain the output common-mode voltage at the same level as the voltage input to the Vocm pin. With symmetrical feedback, output balance is maintained, and Vout+ and Vout- swing symmetrically around the voltage at the Vocm input.

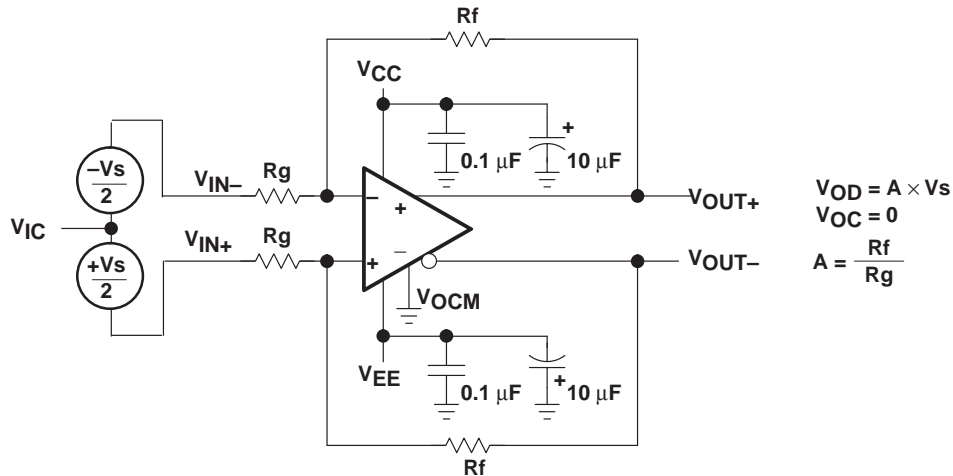


Figure 6. Amplifying Differential Signals

Generation of differential signals has been cumbersome in the past. Different means have been used, requiring multiple amplifiers. The integrated fully-differential amplifier provides a more elegant solution. Figure 7 shows an example of converting single-ended signals to differential signals.

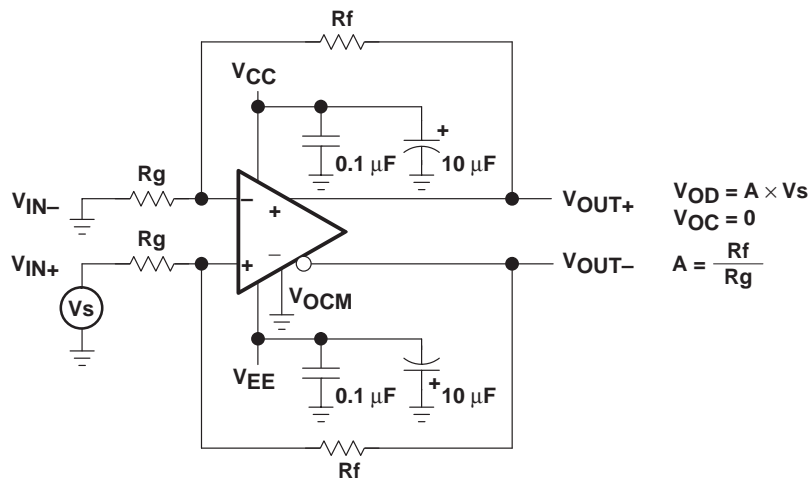


Figure 7. Converting Single-Ended Signals to Differential Signals

8 Circuit Analysis and Block Diagram

Circuit analysis of fully-differential amplifiers follows the same rules as normal single-ended amplifiers. However, subtleties are present that may not be fully appreciated until a full analysis is done. The analysis circuit shown in Figure 8 is used to derive a generalized circuit formula and a block diagram from which specific circuit configurations can easily be solved. The voltage definitions are similar to the circuit shown in Figure 3, but are changed to reflect the use of feedback. These definitions are required to arrive at practical solutions.

The open-loop differential gain of the amplifier is represented by $a(f)$ such that $(V_{out+}) - (V_{out-}) = a(f)(V_p - V_n)$. This assumes that the gains of the two sides of the differential amplifier are well matched, and variations are insignificant. With negative feedback, this is typically the case when $a(f) \gg 1$. However, $a(f)$ is a function of frequency, falling -20 dB/dec over most of the usable bandwidth of the amplifier due to dominant-pole compensation.

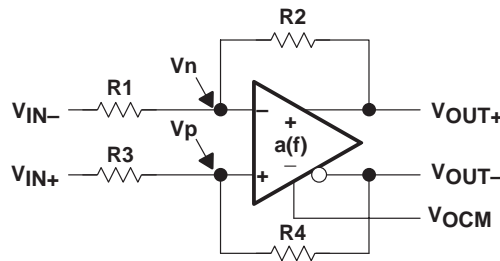


Figure 8. Analysis Circuit

Input voltage definitions:

$$V_{id} = (V_{in+}) - (V_{in-}) \quad (1)$$

$$V_{ic} = \frac{(V_{in+}) + (V_{in-})}{2} \quad (2)$$

Output voltage definitions:

$$V_{od} = (V_{out+}) - (V_{out-}) \quad (3)$$

$$V_{oc} = \frac{(V_{out+}) + (V_{out-})}{2} \quad (4)$$

$$(V_{out+}) - (V_{out-}) = a(f)(V_p - V_n) \quad (5)$$

$$V_{oc} = V_{ocm} \quad (6)$$

Referring back to the simplified schematic shown in Figure 2, the first thing to realize is that there are two amplifiers: the main differential amplifier from V_{in} to V_{out} , and the V_{ocm} error amplifier. The operation of the V_{ocm} error amplifier is the simpler of the two and is considered first.

V_{out+} and V_{out-} are filtered and summed by the internal RC network connected between the output terminals so the voltage at the positive terminal of the V_{ocm} amplifier is:

$$\frac{(V_{out+}) + (V_{out-})}{2},$$

which is V_{oc} by definition. The V_{ocm} error amplifier's output drives the base of Q5 and Q6. Going from base to collector provides the signal inversion required for negative feedback in the loop. Thus, the *error* voltage of the V_{ocm} error amplifier (the voltage between the input pins) is driven to zero, and $V_{oc} = V_{ocm}$. This is the basis of the voltage definition given by equation 6.

There is no simple way to analyze the main differential amplifier except to write down some node equations and then reduce them algebraically into a practical form. A solution is first derived based solely on nodal analysis. Then the voltage definitions given above are used to derive solutions for the output voltages taken as single ended outputs, that is, V_{out+} and V_{out-} . These definitions are then used to calculate V_{od} .

Solving the node equations at V_n and V_p yields:

$$V_n = (V_{in-}) \left(\frac{R_2}{R_1 + R_2} \right) + (V_{out+}) \left(\frac{R_1}{R_1 + R_2} \right), \text{ and}$$

$$V_p = (V_{in+}) \left(\frac{R_4}{R_3 + R_4} \right) + (V_{out-}) \left(\frac{R_3}{R_3 + R_4} \right). \text{ By setting } \beta_1 = \left(\frac{R_3}{R_3 + R_4} \right) \text{ and}$$

$$\beta_2 = \left(\frac{R_1}{R_1 + R_2} \right), V_n \text{ and } V_p \text{ can be rewritten as:}$$

$$V_n = (V_{in-}) (1 - \beta_2) + (V_{out+}) (\beta_2), \text{ and} \tag{7}$$

$$V_p = (V_{in+}) (1 - \beta_1) + (V_{out-}) (\beta_1) \tag{8}$$

A block diagram of the main differential amplifier like that shown in Figure 9 can be constructed using equations 7 and 8. Block diagrams are useful tools to understand circuit operation, and investigate other variations.

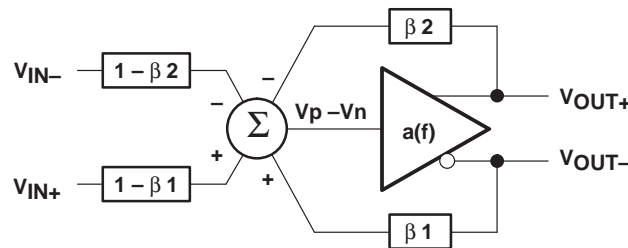


Figure 9. Block Diagram

By using the block diagram, or combining equations 7 and 8 with equation 5 the input-to-output relationship can be found to be:

$$(V_{out+}) (1 + a(f)\beta_2) - (V_{out-})(1 + a(f)\beta_1) = a(f)[(V_{in+})(1-\beta_1) - (V_{in-})(1-\beta_2)] \tag{9}$$

Although accurate, equation 9 is somewhat cumbersome when the feedback paths are not symmetrical. More practical formulas can be derived by using the voltage definitions given in equations 1 through 4 and equation 6.

Substituting: $(V_{out-}) = 2V_{oc} - (V_{out+})$, and $V_{oc} = V_{ocm}$, it becomes:

$$(V_{out+}) (2 + a(f)\beta_1 + a(f)\beta_2) - 2V_{ocm}(1 + a(f)\beta_1) = a(f)[(V_{in+})(1-\beta_1) - (V_{in-})(1-\beta_2)]$$

$$(V_{out+}) = \frac{1}{(\beta_1 + \beta_2)} \frac{(V_{in+})(1-\beta_1) - (V_{in-})(1-\beta_2) + 2V_{ocm} \left(\frac{1}{a(f)} + \beta_1 \right)}{\left(1 + \frac{2}{a(f)\beta_1 + a(f)\beta_2} \right)} \tag{10}$$

Using the *ideal* assumption: $a(f)\beta_1 \gg 1$ and $a(f)\beta_2 \gg 1$, equation 10 reduces to:

$$(V_{out+}) = \frac{(V_{in+})(1 - \beta_1) - (V_{in-})(1 - \beta_2) + 2V_{ocm}\beta_1}{(\beta_1 + \beta_2)} \quad (11)$$

V_{out-} is derived in a similar manner:

$$(V_{out-}) = \frac{1}{(\beta_1 + \beta_2)} \frac{-[(V_{in+})(1 - \beta_1) - (V_{in-})(1 - \beta_2)] + 2V_{ocm}\left(\frac{1}{a(f)} + \beta_2\right)}{\left(1 + \frac{2}{a(f)\beta_1 + a(f)\beta_2}\right)} \quad (12)$$

Again, assuming $a(f)\beta_1 \gg 1$ and $a(f)\beta_2 \gg 1$ this reduces to:

$$(V_{out-}) = \frac{-[(V_{in+})(1 - \beta_1) - (V_{in-})(1 - \beta_2)] + 2V_{ocm}\beta_2}{(\beta_1 + \beta_2)} \quad (13)$$

To calculate $V_{od} = (V_{out+}) - (V_{out-})$, subtract equation 12 from equation 10:

$$V_{od} = \frac{1}{(\beta_1 + \beta_2)} \frac{2[(V_{in+})(1 - \beta_1) - (V_{in-})(1 - \beta_2)] + 2V_{ocm}(\beta_1 - \beta_2)}{\left(1 + \frac{2}{a(f)\beta_1 + a(f)\beta_2}\right)} \quad (14)$$

Again, assuming $a(f)\beta_1 \gg 1$ and $a(f)\beta_2 \gg 1$ this reduces to:

$$V_{od} = \frac{2[(V_{in+})(1 - \beta_1) - (V_{in-})(1 - \beta_2)] + 2V_{ocm}(\beta_1 - \beta_2)}{(\beta_1 + \beta_2)} \quad (15)$$

It can be seen from equations 11, 13, and 15, that even though it is obvious that a fully-differential amplifier should be used with symmetrical feedback, the gain can be controlled with only one feedback path.

Using matched resistors, $R_1 = R_3$ and $R_2 = R_4$, in the analysis circuit of Figure 8, the feedback paths are balanced so that $\beta_1 = \beta_2 = \beta$, and the transfer function is:

$$\frac{(V_{out+}) - (V_{out-})}{(V_{in+}) - (V_{in-})} = \frac{(1 - \beta) a(f)}{(1 + a(f)\beta)} = \frac{1 - \beta}{\beta} \times \frac{1}{\left(1 + \frac{1}{a(f)\beta}\right)}$$

The common-mode voltages at the input and output do not enter into the equation— V_{ic} is rejected and V_{oc} is set by the voltage at V_{ocm} . The ideal gain (assuming $a(f)\beta \gg 1$) is set by the ratio: $\frac{1 - \beta}{\beta} = \frac{R_2}{R_1}$. Note that the normal inversion that might be expected with inverting amplifiers is accounted for by the output voltage definitions resulting in a positive gain.

Many applications require that a single-ended signal be converted to a differential signal. The circuits below show various approaches. Circuit solutions are easily derived using equations 11, 13, and 15.

With a slight variation of Figure 8, as shown in Figure 10, single-ended signals can be amplified and converted to differential signals. V_{in-} is now grounded and the signal applied is V_{in+} . Substituting $V_{in-} = 0$ in equations 11, 13, and 15 results in:

$$(V_{out+}) = \frac{(V_{in+})(1-\beta_1) + 2V_{ocm}\beta_1}{(\beta_1 + \beta_2)}, \quad (V_{out-}) = \frac{2V_{ocm}\beta_2 - (V_{in+})(1-\beta_1)}{(\beta_1 + \beta_2)}, \quad \text{and}$$

$$V_{od} = \frac{2(V_{in+})(1-\beta_1) + 2V_{ocm}(\beta_1 - \beta_2)}{(\beta_1 + \beta_2)}$$

If the signal is not referenced to ground, the reference voltage is amplified along with the desired signal, reducing the dynamic range of the amplifier. To strip unwanted dc offsets, use a capacitor to couple the signal to V_{in+} . Keeping $\beta_1 = \beta_2$ prevents V_{ocm} from causing an offset in V_{od} .

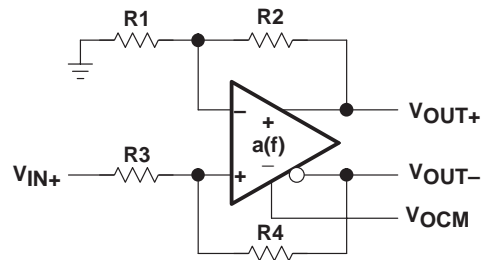


Figure 10. Single-Ended-to-Differential Amplifier

The following four circuits use nonsymmetrical feedback. This causes V_{ocm} to influence V_{out+} and V_{out-} differently, resulting in V_{ocm} showing up in V_{od} . This unbalances the operating points between the internal nodes in the differential amplifier, and degrades the matching of the open-loop gains. CMRR is not a real issue with single ended inputs, but the analysis points out that CMRR is severely compromised when nonsymmetrical feedback is used. In the noise analysis section it is shown that nonsymmetrical feedback also increases the noise introduced at the V_{ocm} pin. For these reasons the circuits shown in Figures 11, 12, 13, and 14 are presented mainly for instructional purposes, and are not recommended without further testing.

In the circuit shown in Figure 11, $V_{in-} = 0$ and $\beta_1 = 0$. The output voltages are:

$$(V_{out+}) = \frac{(V_{in+})}{\beta_2}, \quad (V_{out-}) = 2V_{ocm} - \frac{(V_{in+})}{\beta_2}, \quad \text{and} \quad V_{od} = \frac{2(V_{in+})}{\beta_2} - 2V_{ocm}.$$

With $\beta_1 = 0$, this circuit is similar to a noninverting amplifier, but has twice the normal gain.

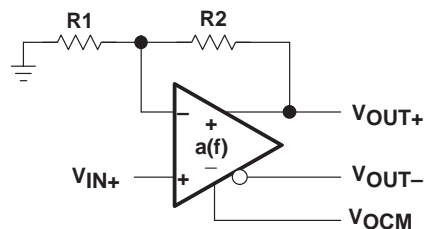


Figure 11. Circuit With $\beta_1 = 0$

In the circuit shown in Figure 12, $V_{in-} = 0$ and $\beta_2 = 0$. The output voltages are:

$$(V_{out+}) = \frac{(V_{in+})(1-\beta_1)}{\beta_1} + 2V_{ocm}, \quad (V_{out-}) = \frac{-(V_{in+})(1-\beta_1)}{\beta_1}, \quad \text{and}$$

$$V_{od} = \frac{2(V_{in+})(1-\beta_1)}{\beta_1} + 2V_{ocm}. \quad \text{With } \beta_2 = 0, \text{ the gain is twice that of an inverting amplifier (without the minus sign).}$$

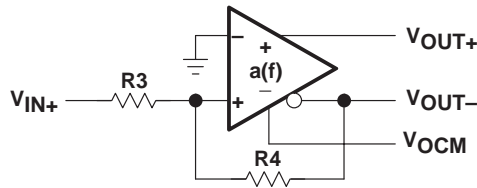


Figure 12. Circuit With $\beta_2 = 0$

In the circuit shown in Figure 13, $V_{in-} = 0$ and $\beta_2 = 1$. The output voltages are:

$$(V_{out+}) = \frac{(V_{in+})(1-\beta_1) + 2V_{ocm}\beta_1}{\beta_1 + 1}, \quad (V_{out-}) = \frac{2V_{ocm} - (V_{in+})(1-\beta_1)}{\beta_1 + 1}, \quad \text{and}$$

$$V_{od} = \frac{2(V_{in+})(1-\beta_1) + 2V_{ocm}(\beta_1 - 1)}{(\beta_1 + 1)}. \quad \text{The gain is 1 with } \beta_1 = 0.333; \text{ with } \beta_1 = 0.6, \text{ the gain becomes } 1/2.$$

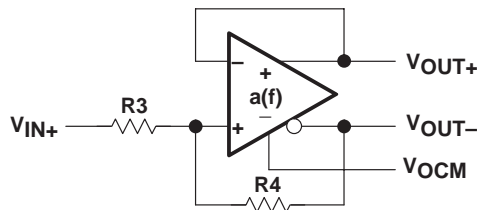


Figure 13. Circuit With $\beta_2 = 1$

In the circuit shown in Figure 14, $V_{in-} = 0$, $\beta_1 = 0$, and $\beta_2 = 1$. The output voltages are: $(V_{out+}) = (V_{in+})$, $(V_{out-}) = 2V_{ocm} - (V_{in+})$, and $V_{od} = 2[(V_{in+}) - V_{ocm}]$. This circuit realizes a resistorless gain of 2.

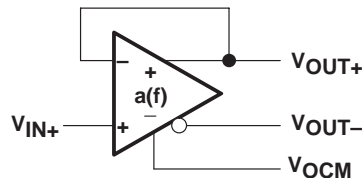


Figure 14. Circuit With $\beta_1 = 0$ and $\beta_2 = 1$

9 Noise Analysis

The noise sources are identified in Figure 15. The analysis uses the definitions shown in this figure.

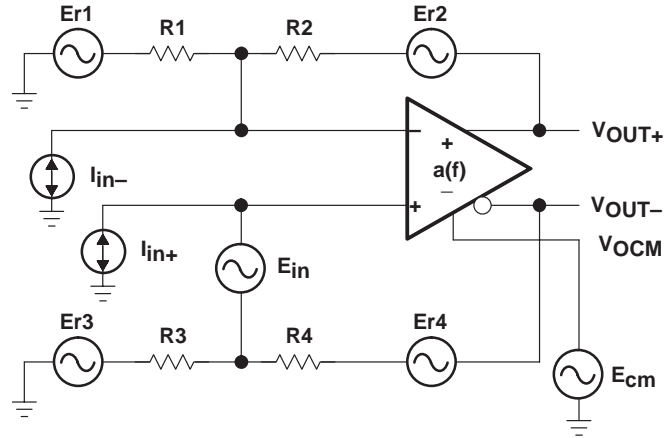


Figure 15. Noise Analysis Circuit

E_{in} is the input-referred RMS noise voltage of the amplifier: $E_{in} \approx e_{in} \times \sqrt{ENB}$ (assuming the $1/f$ noise is negligible), where e_{in} is the input white-noise spectral density in volts per square root hertz, and ENB is the effective noise bandwidth. E_{in} is modeled as a differential voltage at the input.

I_{in+} and I_{in-} are the input-referred RMS noise currents that flow into each input. They are considered to be equal and called I_{in} . $I_{in} \approx i_{in} \times \sqrt{ENB}$ (assuming the $1/f$ noise is negligible), where i_{in} is the input white-noise spectral density in amps per square root hertz, and ENB is the effective noise bandwidth. I_{in} develops a voltage in proportion to the equivalent input impedance seen from the input nodes. Assume the equivalent input impedance is dominated by the parallel combination of the gain setting resistors: $Req1 = \frac{R1R2}{R1 + R2}$ and $Req2 = \frac{R3R4}{R3 + R4}$.

E_{cm} is the RMS noise at the Vocm pin taking into account the spectral density and bandwidth, as with the input-referred noise sources. Proper bypassing of the Vocm pin reduces the effective bandwidth, so this voltage is negligible.

$Er1 - Er4$ is the RMS noise voltage from the resistors. It is calculated by: $Ern = \sqrt{4kTR \times ENB}$, where n is the resistor number, k is Boltzmann's constant ($1.38 \times 10^{-23} \text{J/K}$), T is the absolute temperature in Kelvin (K), R is the resistance in ohms (Ω), and ENB is the effective-noise bandwidth.

E_{od} is the differential RMS-output-noise voltage. $E_{od} = A(E_{id})$, where E_{id} is a single-input noise source, and A is the gain from the source to the output. One-half of E_{od} is attributed to the positive output $\left(\frac{+E_{od}}{2}\right)$, and 1/2 is attributed to the negative output $\left(\frac{-E_{od}}{2}\right)$. Therefore, $\left(\frac{+E_{od}}{2}\right)$ and $\left(\frac{-E_{od}}{2}\right)$ are correlated to one another and to the input source, and can be directly added together, that is, $\left(\frac{+E_{od}}{2}\right) - \left(\frac{-E_{od}}{2}\right) = E_{od} = A(E_{id})$.

Independent noise sources are typically not correlated. To combine noncorrelated noise voltages, a sum-of-squares technique is used. The total RMS voltage squared is equal to the square of the individual RMS voltages added together. The output-noise voltages from the individual noise sources are calculated one at a time and then combined in this fashion.

The block diagram shown in Figure 16 helps in the analysis of the amplifier's noise sources.

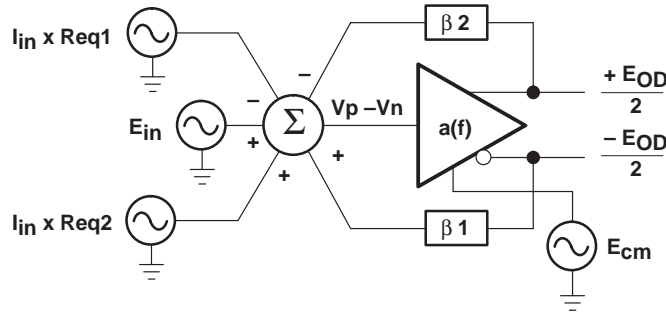


Figure 16. Block Diagram of the Amplifier's Input-Referred Noise

Considering only E_{in} , from the block diagram we can write:

$$E_{od} = a(f) \left[E_{in} + \frac{(-E_{od})\beta_1}{2} - \frac{(+E_{od})\beta_2}{2} \right]. \text{ Solving: } E_{od} = \left(\frac{2E_{in}}{\beta_1 + \beta_2} \right) \left[\frac{1}{1 + \frac{2}{a(f)(\beta_1 + \beta_2)}} \right]$$

Assuming $a(f)\beta_1 \gg 1$ and $a(f)\beta_2 \gg 1$: $E_{od} = \frac{2E_{in}}{(\beta_1 + \beta_2)}$. Given $\beta_1 = \beta_2 = \beta$ (symmetrical

feedback): $E_{out} = \frac{E_{in}}{\beta}$, the same as a standard single-ended voltage feedback operational amplifier.

Similarly, the noise contributions from $I_{in} \times Req1$ and $I_{in} \times Req2$ are: $\frac{2I_{in} \times Req1}{(\beta_1 + \beta_2)}$ and

$\frac{2I_{in} \times Req2}{(\beta_1 + \beta_2)}$ respectively.

The V_{ocm} error amplifier produces a common-mode noise voltage at the output equal to E_{cm} . Due to the feedback paths, β_1 and β_2 , a noise voltage is seen at the input which is equal to $E_{cm}(\beta_1 - \beta_2)$. This is amplified, just as an input, and seen at the output as a differential noise

voltage equal to $\frac{2E_{cm}(\beta_1 - \beta_2)}{(\beta_1 + \beta_2)}$. Noise gain from the V_{ocm} pin ranges from 0 (given $(\beta_1 = \beta_2)$) to a

maximum absolute value of 2 (given $\beta_1 = 1$ and $\beta_2 = 0$, or $\beta_1 = 0$ and $\beta_2 = 1$).

Noise from resistors R1 and R3 appears as signals at V_{in+} and V_{in-} in Figure 8. From the circuit analysis presented in section 8, Circuit Analysis and Block Diagram, the differential output noise

contributions from R1 and R3 are: $\frac{2(Er1)(1-\beta_2)}{(\beta_1 + \beta_2)}$ and $\frac{2(Er3)(1-\beta_1)}{(\beta_1 + \beta_2)}$, respectively.

Noise from resistors R2 and R4 is imposed directly on the output with no amplification. Their contributions are E_{r2} and E_{r4} .

Adding the individual noise sources, the total output differential noise is:

$$E_{od} = \sqrt{\frac{(2E_{in})^2 + (2I_{in} \times R_{eq1})^2 + (2I_{in} \times R_{eq2})^2 + (2E_{cm}(\beta_1 - \beta_2))^2 + (2(E_{r1})(1 - \beta_2))^2 + (2(E_{r3})(1 - \beta_1))^2}{(\beta_1 + \beta_2)^2} + E_{r2}^2 + E_{r4}^2}$$

The individual noise sources are added in sum-of-squares fashion. Input-referred terms are amplified by the noise gain of the circuit: $G_n = \frac{2}{(\beta_1 + \beta_2)}$. If symmetrical feedback is used,

where $\beta_1 = \beta_2 = \beta$, the noise gain is: $G_n = \frac{1}{\beta} = 1 + \frac{R_f}{R_g}$, where R_f is the feedback resistor and R_g is the input resistor, the same as a standard single-ended voltage-feedback amplifier.

10 Application Circuits

Having covered the basic circuit operation and dealt with analysis techniques to take you beyond the basics, we next investigate some typical applications like driving ADC inputs and transmission lines. We assume that the amplifier is being used at frequencies where $a(f) \gg 1$, and do not include its effects in the following formulas. Also, assume that symmetrical feedback is being used where $\beta_1 = \beta_2 = \frac{R_g}{R_g + R_f}$. Before going into the application circuits, we detour briefly into source termination and its implications in keeping the feedback symmetrical.

11 Terminating the Input Source

Double termination is typically used in high-speed systems to reduce transmission line reflections and improve signal integrity. With double termination, the driving source's output impedance and the far-end termination are matched to the transmission line impedance. Common values are 50 Ω , 75 Ω , 100 Ω , and 600 Ω . When the source is differential, the termination is placed across the line. When the source is single-ended, the termination is placed from the line to ground.

Figure 17 shows an example of terminating a differential signal source. The situation depicted is balanced so that $1/2 V_s$ and $1/2 R_s$ are attributed to each side, with V_{ic} being the center point. R_s is the source impedance and R_t is the termination resistor. The transmission line is not shown. The circuit is balanced, but there are two issues to resolve: 1) proper termination, and 2) gain setting.

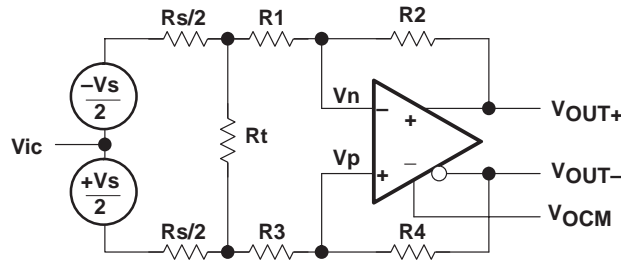


Figure 17. Terminating a Differential Input Signal

As long as $a(f) \gg 1$ and the amplifier is in linear operation, the action of the amplifier keeps $V_n \approx V_p$. Thus, to first order approximation, a virtual short is seen between the two nodes as shown in Figure 18. The termination impedance is the parallel combination: $R_t \parallel (R_1 + R_3)$. The

value of R_t for proper termination is calculated by: $R_t = \frac{1}{\frac{1}{R_s} - \frac{1}{(R_1 + R_3)}}$.

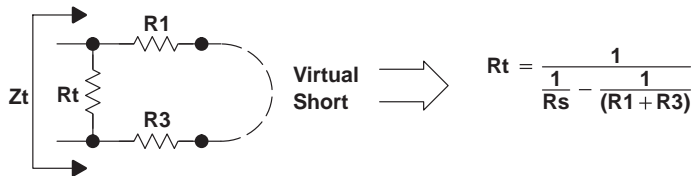


Figure 18. Differential Termination Impedance

Once R_t is found, the required gain is found by Thevenizing the circuit. The circuit is broken between R_t and the amplifier input resistors R_1 and R_3 . V_{ic} does not concern us at this point, so we leave it out and combine the $1/2 V_s$'s. Then, $V_{th} = V_s \times \frac{R_t}{R_t + R_s}$ and $R_{th} = R_s \parallel R_t$ ($1/2$ is attributed to each side). The resulting Thevenin equivalent is shown in Figure 19. The proper

gain is calculated by: $\frac{V_{od}}{V_{th}} = \frac{R_f}{R_g + \frac{R_s \parallel R_t}{2}}$. Substituting for V_{th} , this becomes :

$\frac{V_{od}}{V_s} = \frac{R_f}{R_g + \frac{R_s \parallel R_t}{2}} \times \frac{R_t}{R_s + R_t}$, where R_f is the feedback resistor (R_2 or R_4), and R_g is the input resistor (R_1 or R_3). Remember to keep $R_2 = R_4$ and $R_1 = R_3$ for symmetry.

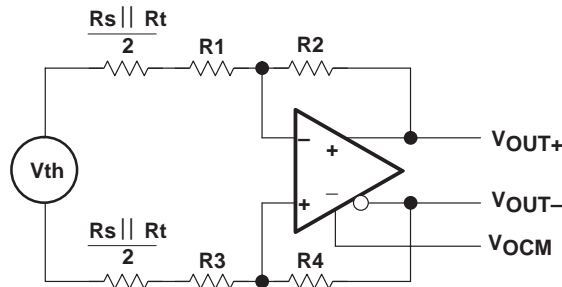


Figure 19. Differential Thevenin Equivalent

As an example, suppose you are terminating a 50Ω differential source that is balanced, and want an overall gain of one from the source to the differential output of the amplifier. Start the design by first choosing the values for R_1 and R_3 , then calculate R_t and the feedback resistors.

With the voltage divider formed by the termination, it is reasonable to assume that a gain of about two is required of the amplifier. Also, feedback resistor values of approximately 500 Ω are reasonable for a high-speed amplifier. Using these starting assumptions, choose R1 and R3 equal to 249 Ω. Next calculate Rt from the formula:

$$R_t = \frac{1}{\frac{1}{R_s} - \frac{1}{(R_1 + R_3)}} = \frac{1}{\frac{1}{50} - \frac{1}{(249 + 249)}} = 55.6 \Omega \text{ (the closest standard 1\% value is 56.2 } \Omega \text{)}$$

The gain is now set by calculating the value of the feedback resistors:

$$R_f = \left(\frac{V_{out}}{V_s}\right) \left(R_g + \frac{R_s \parallel R_t}{2}\right) \left(\frac{R_s + R_t}{R_t}\right) = (1) \left(249 + \frac{50 \parallel 56.2}{2}\right) \left(\frac{50 + 56.2}{56.2}\right) = 495.5 \Omega \text{ (the closest standard 1\% value is 499 } \Omega \text{)}$$

The solution is shown in Figure 20 with standard 1% resistor values.

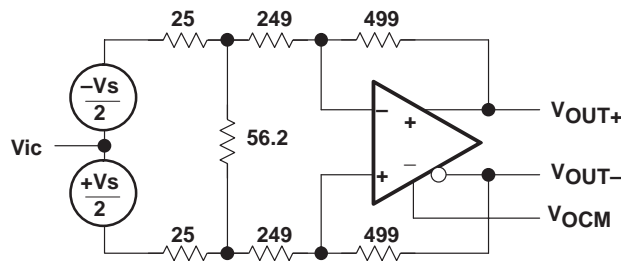


Figure 20. Differential Solution for Gain = 1

Figure 21 shows an example of terminating a single-ended signal source. Rs is the source impedance and Rt is the termination resistor. The transmission line is not shown. The circuit is not balanced, so there are three issues to resolve: 1) proper termination, 2) gain setting, and 3) balance.

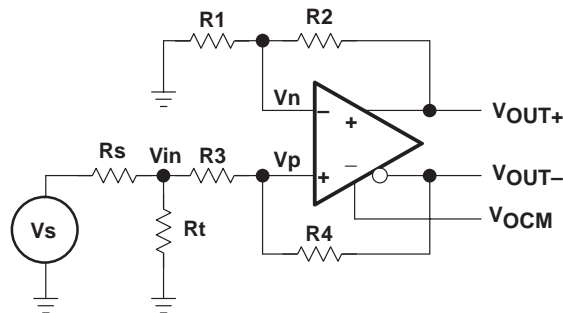


Figure 21. Terminating a Single-Ended Input Signal

To determine the termination impedance seen from the line looking into the amplifier's input at V_{in} , remove V_s and R_s and short all other sources. As long as $a(f) \gg 1$ and the amplifier is in linear operation, the action of the amplifier keeps $V_n \approx V_p$. V_n sees the voltage at V_{out+} times the resistor ratio $\frac{R_1}{R_1 + R_2}$. Assuming the amplifier is balanced: $V_{out+} = K \times \frac{V_{in}}{2}$, where K is the closed loop gain of the amplifier ($V_{ocm} = 0$). The termination impedance is the parallel combination: R_t in parallel with $\frac{V_{in}}{I_{R3}} = \frac{R_3}{1 - \frac{K}{2 \times (1+K)}}$. The value of R_t for proper termination is

then calculated by: $R_t = \frac{1}{\frac{1}{R_s} - \frac{1 - \frac{K}{2 \times (1+K)}}{R_3}}$.

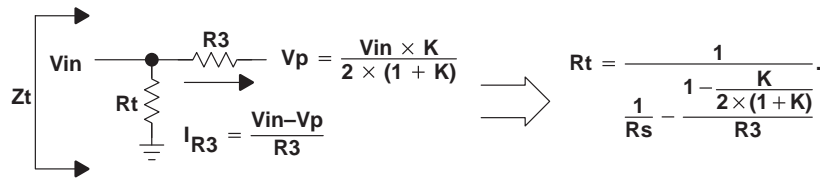


Figure 22. Single-Ended Termination AC Impedance

Once R_t is found, the required gain is found by Thevenizing the circuit. The circuit is broken between R_t and the amplifier's input resistors R_1 and R_3 . $V_{th} = V_s \times \frac{R_t}{R_t + R_s}$, and $R_{th} = R_s \parallel R_t$. The resulting Thevenin equivalent is shown in Figure 23.

With proper symmetry, $R_2 = R_4$ and $R_1 = R_3 + (R_s \parallel R_t)$, the Thevenin gain is given by

$\frac{V_{od}}{V_{th}} = \frac{R_2}{R_1} = \frac{R_4}{R_3 + (R_s \parallel R_t)}$. Substituting for V_{th} , the circuit gain is:

$\frac{V_{od}}{V_s} = \frac{R_2}{R_1} \times \frac{R_t}{R_s + R_t} = \frac{R_4}{R_3 + (R_s \parallel R_t)} \times \frac{R_t}{R_s + R_t}$.

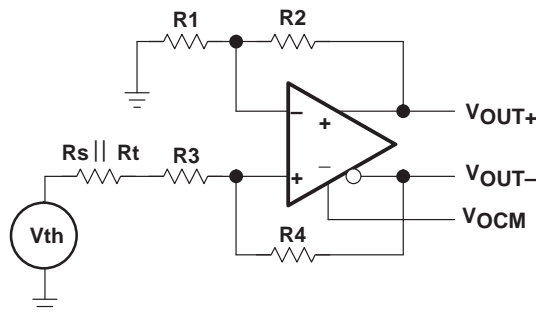


Figure 23. Single-Ended Thevenin Equivalent

As an example, suppose you are terminating a 50- Ω single-ended source, and want an overall gain of one from the source to the differential output of the amplifier. Start the design by first choosing the value for R_3 , then calculate R_t and the feedback resistors. This becomes an iterative process starting with some initial assumptions and then refining it.

Start with the assumption that $R_t = 50 \Omega$ and a gain of two is required of the amplifier. Also, feedback resistor values of approximately 500Ω are a reasonable value for a high-speed amplifier. Using these starting assumptions, choose $R_1 = 249 \Omega$ and $R_3 = R_1 - R_s \parallel R_t = 249 \Omega - 25 \Omega = 224 \Omega$. Next, calculate R_t from the formula:

$$R_t = \frac{1}{\frac{1}{R_s} - \frac{1 - \frac{K}{2(1+K)}}{R_3}} = \frac{1}{\frac{1}{50} - \frac{1 - \frac{2}{2(1+2)}}{224}} = 58.7 \Omega.$$

Now calculate the value of the feedback resistors:

$$R_2 = \left(\frac{V_{od}}{V_s}\right)(R_1)\left(\frac{R_s + R_t}{R_t}\right) = (1) \times (249) \times \left(\frac{50 + 58.7}{58.7}\right) = 460.9 \Omega, \text{ and}$$

$$R_4 = \left(\frac{V_{od}}{V_s}\right)(R_3 + R_s \parallel R_t)\left(\frac{R_s + R_t}{R_t}\right) = (1) \times (224 + 50 \parallel 58.7) \times \left(\frac{50 + 58.7}{58.7}\right) = 464.7 \Omega.$$

It can be seen that the process is iterative because the gain is not 2, but rather $\frac{460.9}{249} = 1.85$, and R_t calculated to be 58.7Ω not 50Ω . Iterating through the calculations two more times results in: $R_3 = 221.9 \Omega$ (the closest standard 1% value is 221Ω), $R_t = 59.0 \Omega$ (which is a standard 1% value), and $R_2 = R_4 = 460.9 \Omega$ (the closest standard 1% value is 464Ω). The solution is shown in Figure 24 using standard 1% resistor values.

Use of a spread sheet makes the iterative process described above a very simple manner. Also, component values can be easily adjusted to find a better fit to the standard available values.

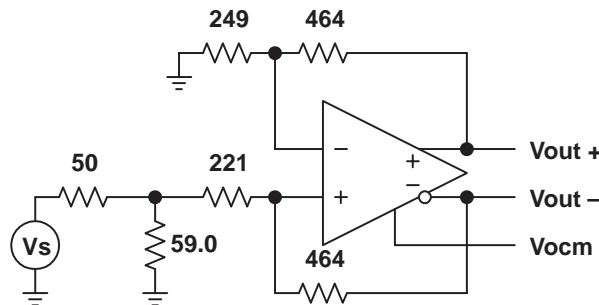


Figure 24. Single-Ended Solution for Gain = 1

Figure 25 shows the output voltages of a balanced vs an unbalanced single-ended-to-differential amplifier where $V_{ocm} = 2.5 \text{ V}$.

The balanced amplifier reflects the values calculated in the previous example.

For the unbalanced amplifier: $R_t = 59 \Omega$, $R_1 = R_3 = 249 \Omega$, and $R_2 = R_4 = 499 \Omega$.

Note the unequal feedback factors in the unbalanced amplifier lead to V_{ocm} causing an offset in the differential output. Dynamic range is lost if used to drive an ADC.

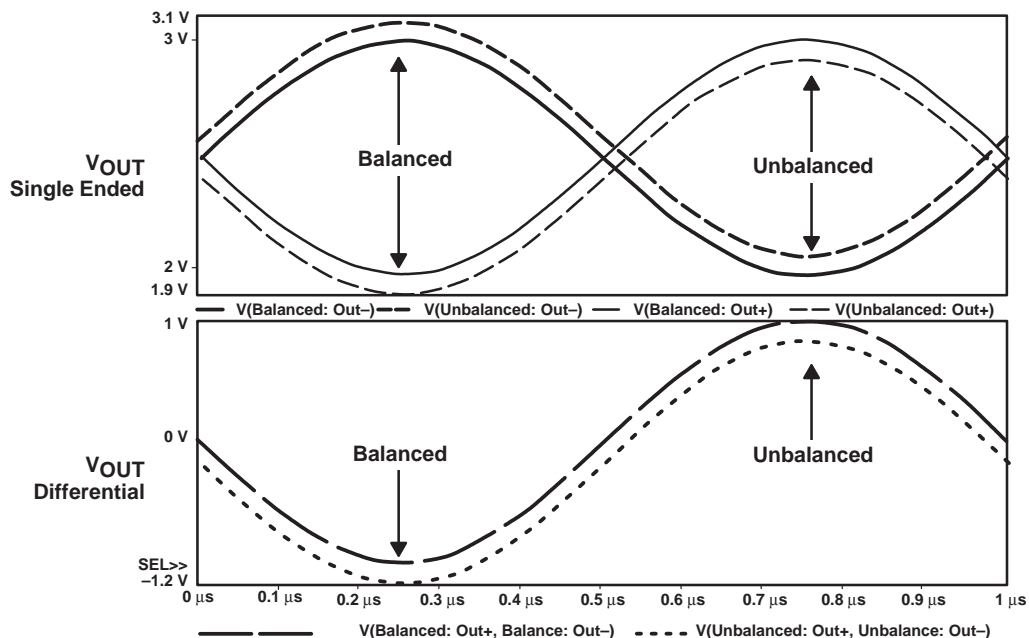


Figure 25. Balance vs Unbalanced Amplifiers

From the foregoing analysis, it is seen that although the idea of line termination may seem trivial, a bit of work is required to get it right.

12 Active Antialias Filtering

A major application of fully-differential amplifiers is in low-pass antialias filters for ADCs with differential inputs.

Creating an active first-order low-pass filter is easily accomplished by adding capacitors in the feedback loop, as shown in Figure 26. With balanced feedback, the transfer function is:

$$\frac{V_{od}}{V_{id}} = \frac{R_f}{R_g} \times \frac{1}{1 + j2\pi f(R_f C_f)}$$

The pole created in the transfer function is a real pole on the negative real axis on the s-plane.

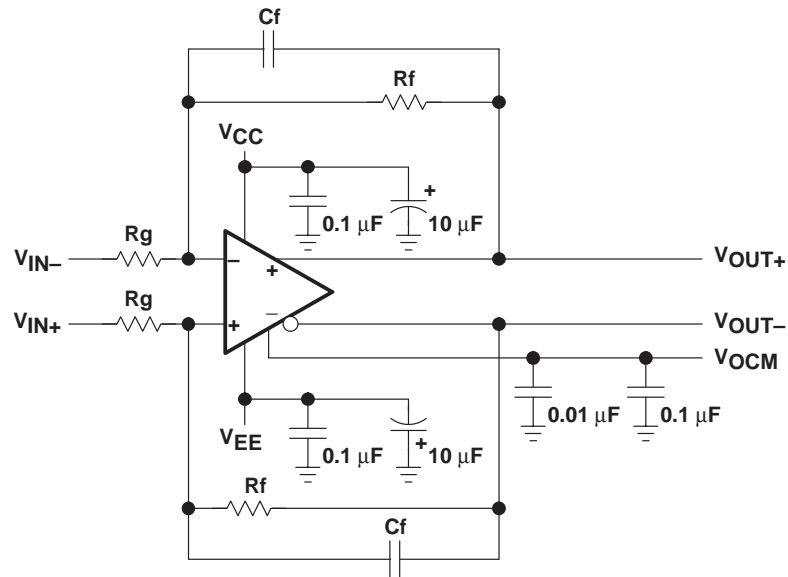


Figure 26. First-Order Active Low-Pass Filter

To create a two-pole low-pass filter, another passive real pole can be created by placing R_o and C_o in the output as shown in Figure 27. With balanced feedback, the transfer function is:

$$\frac{V_{od}}{V_{id}} = \frac{R_f}{R_g} \times \frac{1}{1 + j2\pi f(R_f C_f)} \times \frac{1}{1 + j2\pi f \times 2 \times R_o C_o}$$

The second pole created in the transfer function is also a real pole on the negative real axis on the s-plane. The capacitor, C_o , can be placed differentially across the outputs as shown in solid lines, or two capacitors (of twice the value) can be placed between each output and ground as shown in dashed lines. Typically, R_o is a low value and, at frequencies above the pole frequency, the series combination with C_o loads the amplifier. The additional loading causes more distortion in the amplifier's output. To avoid this, you might stagger the poles so that the $R_o C_o$ pole is placed at a higher frequency than the $R_f C_f$ pole.

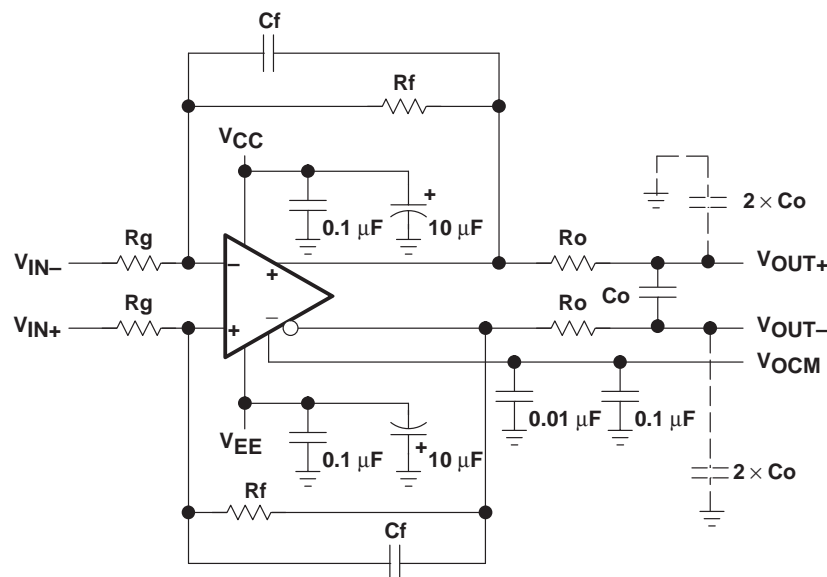


Figure 27. First-Order Active Low-Pass Filter With Passive Second Pole

The classic filter types like Butterworth, Bessel, Chebyshev, etc. (second order and greater) cannot be realized by real poles—they require complex poles. Multiple feedback (MFB) topology is used to create a complex-pole pair, and is easily adapted to fully-differential amplifiers as shown in Figure 28. A third-order filter is formed by adding R4(s) and C3 at the output.

Capacitors C2 and C3 can be placed differentially across the inputs and outputs as shown in solid lines. Alternatively, for better common-mode noise rejection, two capacitors of twice the value can be placed between each input or output and ground as shown in dashed lines.

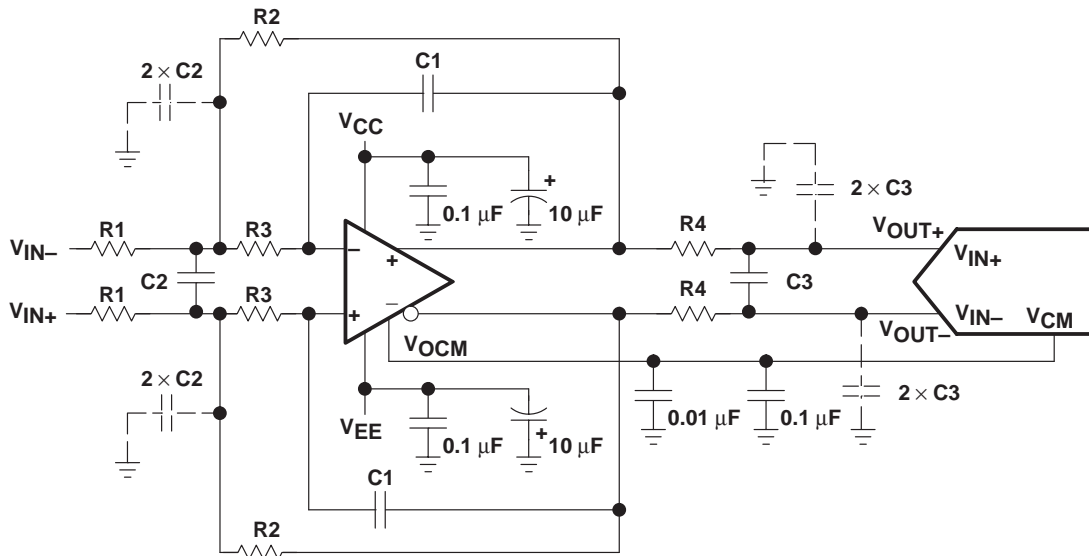


Figure 28. Third-Order Low-Pass Filter Driving an ADC

The transfer function for this filter circuit is:

$$\frac{V_{od}}{V_{id}} = \left[\frac{K}{-\left(\frac{f}{\text{FSF} \times f_c}\right)^2 + \frac{1}{Q} \frac{jf}{\text{FSF} \times f_c} + 1} \right] \times \left(\frac{1}{1 + j2\pi f \times 2 \times R_4 C_3} \right),$$

$$\text{where } K = \frac{R_2}{R_1}, \text{FSF} \times f_c = \frac{1}{2\pi\sqrt{2 \times R_2 R_3 C_1 C_2}}, \text{ and } Q = \frac{\sqrt{2 \times R_2 R_3 C_1 C_2}}{R_3 C_1 + R_2 C_1 + K R_3 C_1}.$$

K sets the pass-band gain, f_c is the cutoff frequency of the filter, FSF is a frequency-scaling

factor, and Q is the quality factor. $\text{FSF} = \sqrt{\text{Re}^2 + |\text{Im}|^2}$, and $Q = \frac{\sqrt{\text{Re}^2 + |\text{Im}|^2}}{2\text{Re}}$, where Re is the real part, and Im is the imaginary part of the complex-pole pair. Setting $R_2=R$, $R_3=mR$,

$$C_1=C, \text{ and } C_2=nC, \text{ results in: } \text{FSF} \times f_c = \frac{1}{2\pi RC \sqrt{2n \times m}}, \text{ and } Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)}.$$

It is easiest to start the design by choosing standard capacitor values for C1 and C2. This gives a value for n. Then determine if there is a value for m that results in the required Q of the filter with the desired gain. If not, use another capacitor combination and try again. Once a suitable combination of m and n are found, use the value for C to calculate R based on the desired f_c . It may take a few tries to obtain reasonable component values.

R4 and C3 are chosen to set the real pole in a third-order filter. Care should be exercised with setting this pole. Typically, R4 is a low value and, at frequencies above the pole frequency, the series combination with C3 loads the amplifier. The extra loading causes additional distortion in the amplifier's output. To avoid this, place the real pole at a higher frequency than the cutoff frequency of the complex pole pair.

Figure 29 shows the gain and phase response of a second-order Butterworth low-pass filter with corner frequency set at 1 MHz, and the real pole set by R4 and C3 at 15.9 MHz. The components used are: R1 = 787 Ω , R2 = 787 Ω , R3 = 732 Ω , R4 = 50 Ω , C1 = 100 pF, C2 = 220 pF, C3 = 100 pF, and a THS4141 fully-differential amplifier. At higher frequencies, parasitic elements allow the signal to feed-through.

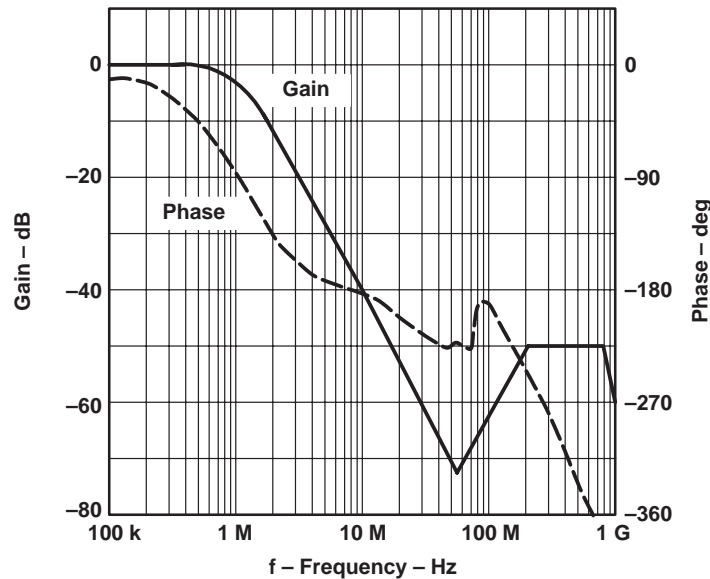


Figure 29. 1-MHz, Second-Order Butterworth Low-Pass With Real Pole at 15.9 MHz

13 V_{OCM} and ADC Reference and Input Common-Mode Voltages

Figure 30 shows the internal reference circuit that is published in the ADS809 ADC data sheet. The reference voltages, REFT and REFB, determine the input voltage range of the converter. The voltage CM is at the midpoint between REFT and REFB. The input signal to the ADC must swing symmetrically about CM to utilize the full dynamic range of the converter. This means the output common-mode voltage of the amplifier must match this voltage.

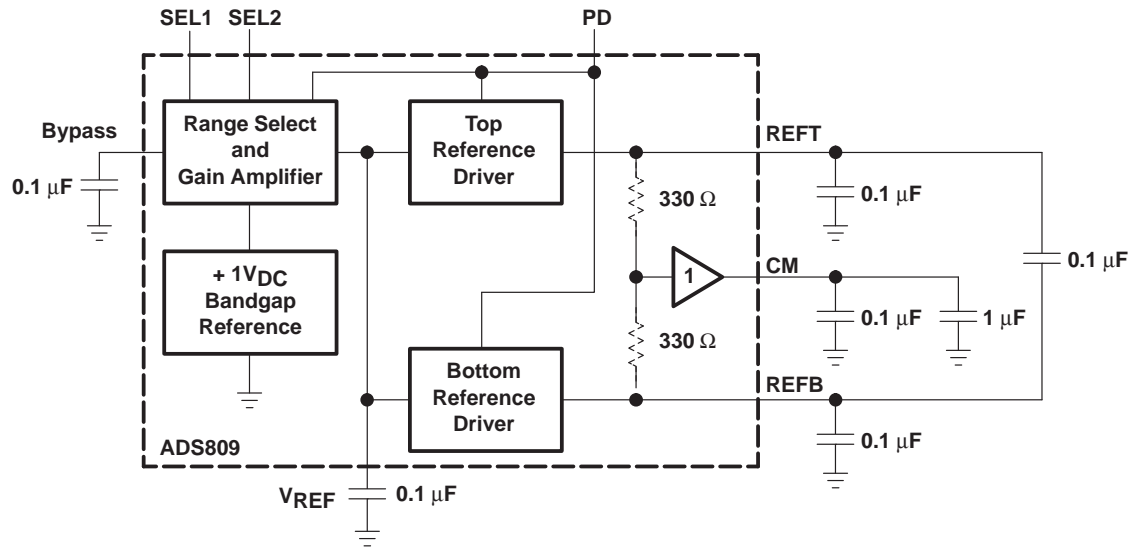


Figure 30. Internal Reference Circuit of the ADS809 and Recommended Bypass Scheme

The V_{OCM} input on the THS45xx is provided specifically for this purpose. Internal circuitry forces the output common-mode voltage to equal the voltage applied to V_{OCM} . Thus, V_{OUT+} and V_{OUT-} swing symmetrically about V_{OCM} . In many cases, all that is required is to tie CM to V_{OCM} with bypass capacitor(s) to ground (typically 0.1 μF to 10 μF) to reduce noise.

Figure 31 shows a simplified schematic of the V_{OCM} input on the THS45xx. With V_{OCM} unconnected, the resistor divider sets the voltage half way between the power supply voltages. The equation shows how to calculate the current required from an external source to overdrive this voltage. Internal circuitry is used to cancel the bias current (I_{EA}) drawn by the V_{OCM} error amplifier. It is easy to see that if the desired V_{OCM} is half way between the power supply voltages (as in a single +5-V supply application) no external current is required. On the other hand, assuming that the amplifier is being powered from $\pm 5\text{ V}$ and the desired V_{OCM} is +2.5 V, the external source needs to supply 100 μA . Depending on the CM output drive from the ADC, a buffer may be required to supply this current.

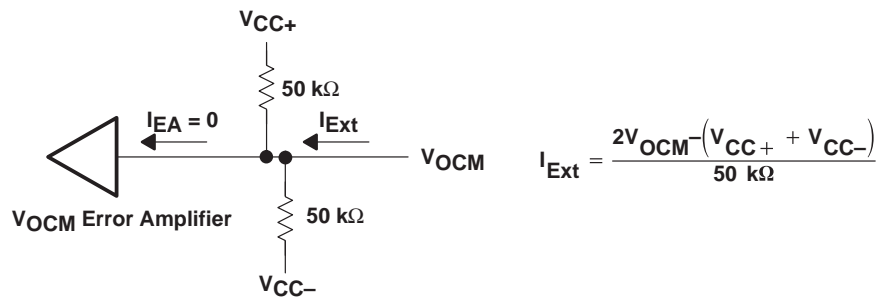


Figure 31. V_{OCM}

All high-performance ADCs using differential inputs that I have seen have an output for setting the common-mode voltage of the drive circuit. Different manufacturers use different names for it. I have seen CM, REF, V_{REF} , V_{CM} , and V_{OCM} . Whatever it is called, the important things to remember are:

- Make sure the amplifier has enough output drive current if V_{OCM} is not at mid-rail
- Use bypass capacitors to reduce common-mode noise

14 Power Supply Bypass

Each power rail should have 6.8 μF to 10 μF tantalum capacitors located within a few inches of the amplifier to provide low-frequency power supply bypassing. A 0.01 μF to 0.1 μF ceramic capacitor should be placed within 0.1 inch of each power pin on the amplifier to provide high-frequency power supply bypassing.

15 Layout Considerations

As with all high-speed amplifiers, care should be taken with regard to parasitic capacitance at the amplifier's input by removing the ground plane near the pins and any interconnecting circuit traces. Also, minimize trace routing and use surface mount components.

16 Using Positive Feedback to Provide Active Termination

Driving transmission lines differentially is a typical use for fully differential amplifiers. By using positive feedback, the amplifiers can be used to provide active termination as shown in Figure 32. The positive feedback makes the value of the output resistor appear larger than what it actually is when viewed from the line. Still, the voltage dropped across the resistor depends on its actual value, resulting in increased efficiency.

To reiterate, it is important to use symmetrical feedback with this application.

With double termination, the output impedance of the amplifier, Z_o , equals the characteristic impedance of the transmission line, and the far end of the line is terminated with the same value resistor i.e., $R_t = Z_o$. For proper balance, $1/2 Z_o$ is placed in each half of the differential output, so that $Z_o = 2 \times Z_{o\pm}$.

To calculate the output impedance, ground the inputs, insert either a voltage or current source between V_{out+} and V_{out-} , and calculate the impedance from the circuit's response.

Due to symmetry, $Z_{o+} = Z_{o-}$, $V_{out+} = -(V_{out-})$, and $V_{o+} = -(V_{o-})$. Calculating the impedance of one side provides the solution.

$$Z_{o+} = \frac{V_{out+}}{I_{out+}}, \quad I_{out+} = \frac{(V_{out+}) - (V_{o+})}{R_o}, \quad \text{and } V_{o+} = (V_{out-}) \times \left(\frac{-R_f}{R_p} \right).$$

Looking back into the amplifier's outputs, the impedance seen by each side of the line is the value of R_o divided by 1 minus the gain from the other side of the line:

$$Z_{o\pm} = \frac{R_o}{1 - \frac{R_f}{R_p}} \quad (16)$$

The positive feedback also affects the forward gain. Accounting for this effect and for the voltage divider between R_o and $R_t \parallel 2R_p$, the gain from $V_{in} = (V_{in+}) - (V_{in-})$ to $V_{out} = (V_{out+}) - (V_{out-})$ is:

$$A = \frac{V_{out}}{V_{in}} = \frac{R_f}{R_g} \times \frac{1}{\frac{2R_o + R_t \parallel 2R_p}{R_t \parallel 2R_p} - \frac{R_f}{R_p}} \quad (17)$$

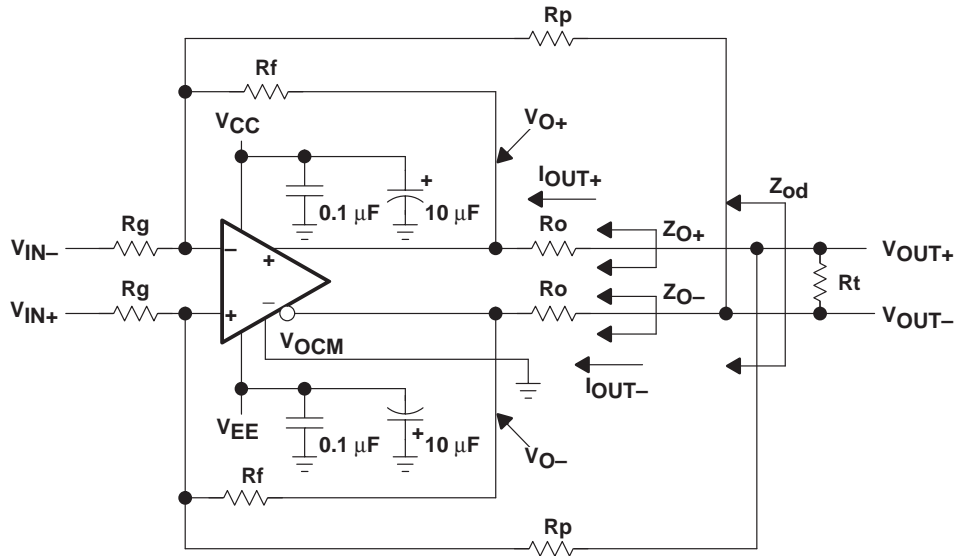


Figure 32. Using Positive Feedback to Provide Active Termination

The design is easily accomplished by first choosing the value of R_f and R_o and then calculating the required value of R_p to obtain the desired Z_o . R_g is then calculated for the required gain.

For example:

Given a desired gain of 1, it is desired to properly terminate a 100- Ω line with $R_f = 1 \text{ k}\Omega$ and $R_o = 10 \text{ }\Omega$. The proper value for $Z_{o\pm}$ and R_t is 100 Ω ($Z_{o\pm} = 50 \text{ }\Omega$). Rearranging equation 1:

$$R_p = \frac{R_f}{1 - \frac{R_o}{Z_{o\pm}}} = \frac{1 \text{ k}\Omega}{1 - \frac{10 \text{ }\Omega}{50 \text{ }\Omega}} = 1.25 \text{ k}\Omega.$$

Then, rearranging equation 2:

$$R_g = \frac{R_f}{A} \times \frac{1}{\frac{2R_o + R_t \parallel 2R_p}{R_t \parallel 2R_p} - \frac{R_f}{R_p}} = \frac{1 \text{ k}\Omega}{\frac{20 \text{ }\Omega + 100 \text{ }\Omega \parallel 2.5\text{K}}{100 \text{ }\Omega \parallel 2.5\text{K}} - \frac{1 \text{ k}\Omega}{1.25 \text{ k}\Omega}} = 2.45 \text{ k}\Omega.$$

The circuit is built and tested with the nearest standard values to those computed above: $R_f = 1 \text{ k}\Omega$, $R_p = 1.24 \text{ k}\Omega$, $R_g = 2.43 \text{ k}\Omega$, $R_t = 100 \text{ }\Omega$, and $R_o = 10 \text{ }\Omega$. Compare the output voltage waveforms ($V_{out} = 2V_{p-p}$) with the active and standard terminations shown in Figure 33 ($V_o = (V_{o+}) - (V_{o-})$ and $V_{out} = (V_{out+}) - (V_{out-})$). For standard termination, $R_f = 1 \text{ k}\Omega$, $R_p = \text{open}$, $R_g = 499 \text{ }\Omega$, $R_t = 100 \text{ }\Omega$, and $R_o = 50 \text{ }\Omega$.

With standard termination, 20 mW of power is dissipated in the output resistors, as opposed to 6.25 mW with active termination. That is, 69% less power is wasted with the active termination.

Another characteristic of the active termination that is very attractive, especially in low-voltage applications, is the effective increase in output voltage swing for a given supply voltage.

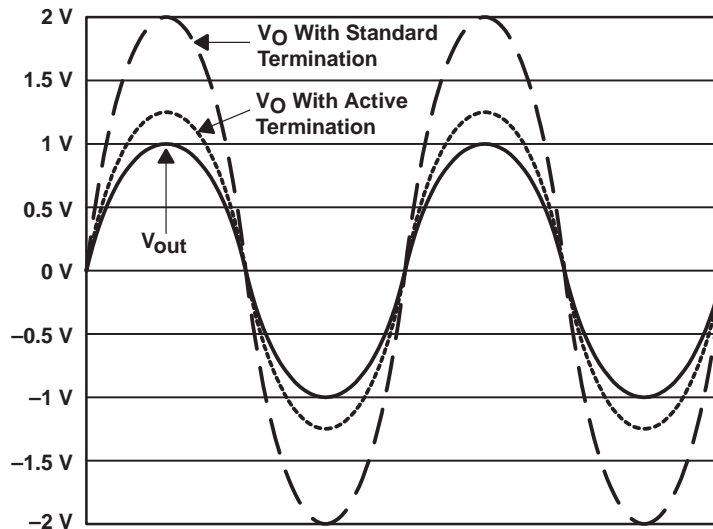


Figure 33. Output Waveforms With Active and Standard Termination

17 Conclusion

Integrated fully-differential amplifiers are very similar to standard single-ended operational amplifiers, except that output is taken from both sides of the input differential pair to produce a differential output.

Differential systems provide increased immunity to external common-mode noise, reduced even-order harmonics, and twice the output swing for a given voltage limit when compared to single-ended systems.

Inverting amplifier topologies are easily adapted to fully-differential amplifiers by implementing two symmetric feedback paths. The best performance is achieved using symmetrical feedback.

In high-speed systems, line termination must be taken into account to maintain symmetric feedback. This is accomplished by taking into account the termination resistors and adjusting the gain-setting resistors accordingly.

Integrated fully-differential amplifiers are well suited for driving differential ADC inputs. They provide easy means for antialias filtering and setting of the common-mode voltage.

Integrated fully-differential amplifiers are also well suited for driving differential transmission lines, and active termination provides increased efficiency and reduces power supply requirements.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated