# IP7500 Media Processor Family

IP7500 Family

The Ubicom IP7500 Media Processor family provides highly flexible interfaces coupled with broad multimedia capabilities and integrated networking. Utilizing 12 multi-threaded thread-CPUs (tCPUs), the IP7500 provides flexible, software-configurable interfaces capable of supporting numerous protocols, enabling unparalleled flexibility in connecting to peripheral devices. Integrated networking and multimedia capabilities make the IP7500 processor family ideal for the next generation of networked, consumer media devices such as networked audio players and digital photo frames.
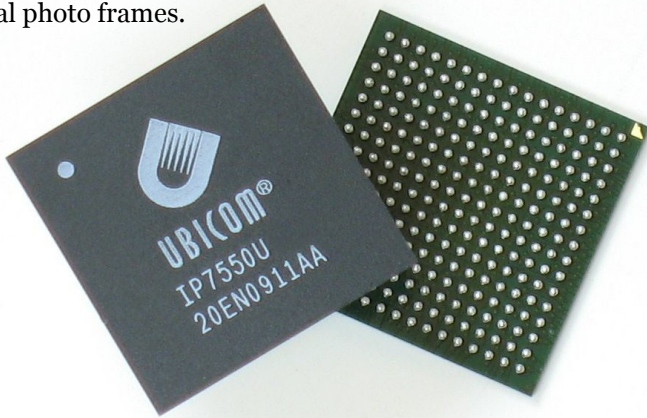
Key Features

Flexible, Software-Configurable I/O

Ubicom's unique architecture is equipped with a highly flexible set of interfaces, capable of supporting a wide variety of protocols through a combination of hardware controllers and software configurable interfaces. The IP7500 processor family features high-speed, hardware peripheral interfaces such as 66MHz PCI and Gigabit Ethernet, a programmable, low-latency interface for fast parallel interfaces like LCD or IDE, and the ability to use any pin as a software controlled I/O. This capability enables the IP7500 series of processors to utilize its I/Os to interface to a large variety of protocols including serial (I²S, I²C, others) and memory (CF, SDIO, others) formats. Integrated PWM-capable pins provide control over backlights, speakers, or motors.

Real-Time Processing

The IP7500 family includes a hardware thread manager that enables developers to set hard, real-time performance levels for specific tasks. These processes can include user interface responsiveness, codec processing (for media applications), and any other interface protocol that requires specific or deterministic timing. This functionality enables a higher level of integration for designs that require an additional FPGA or CPLD to achieve deterministic timing for synchronization and codec processing functions, allowing the IP7500 to integrate those functions into a real-time process. Additionally, designs that require guaranteed user interface responsiveness can use this hardware to prioritize user interface processes ahead of other, background operations.

Flexible Multimedia

The integrated video block offers motion compensation and iDCT acceleration (with a dedicated 16 x 16 multiplier) for decoding MPEG and similar video formats, while the pixel processing pipeline provides hardware support for color space conversion, alpha blending, and scaling. High-fidelity on-chip audio decode and encode are enabled through deterministic hardware threads (tCPUs). These blocks free the CPU core from MIPS-intensive processes, thus enabling greater processing efficiency and additional functionality in the same processing budget.

Integrated Security

Products within the IP7500 processor family include hardware acceleration for Digital Rights Management (DRM) cryptographic functions up to AES 256-bit encryption. This offload engine enables the processor to provide real time DRM-equipped media decryption while simultaneously freeing the main processing pipeline to perform other duties. This hardware block is also capable of providing the cryptographic functions necessary for secure networking.

Product	Applications	Features	Max. CPU Clock
IP7560	Digital Media Player	LCD, Video Acceleration (D1), DRM Acceleration, Audio	550 MHz
IP7550	Digital Photo Frame	LCD, Video Acceleration (D1), Audio	500 MHz
IP7540	Networked Audio Device	LCD, Audio Processing	400 MHz

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Features

Ubicom32™ 32-bit Processor Core

- Up to 550 MHz
- 12 Multithreaded tCPUs (hardware threads)
- Programmable, deterministic execution on all threads with zero-overhead context switching
- 16KB instruction and data caches
- 240KB On-chip memory for high performance accesses
- 32 x 32-bit multiplier
- Nominal core voltage of 1.0 or 1.2V
- DDR1 or DDR2 SDRAM I/O
- 3.3V Standard I/O
- Watchdog timer

Highly Configurable, Software-Controlled I/O

- USB 2.0 OTG controller with PHY
- Up to 225 MHz DDR1, DDR2
- 2x 10/100/1000 Integrated Ethernet MACs
  - MII/TMII/GMII/RMII/RGMII Interfaces
- PCI host for wireless and peripheral interface
- 2×SD/SDIO/MMC for wireless and memory interface
- 3×PWM-enabled interfaces
- Configurable Serial Controller (SPI, UART, I²C, I²S)
- Programmable low-latency I/O (PLIO)
  - Programmable controller configurable for parallel interfaces (LCD, IDE, etc...)
- Up to 152 software-controlled GPIO configured as:
  - Serial – N×SPI, N×I²S, N×I2C, N×PCM, N×S/PDIF, N×UART
  - Memory – CF, MS, NAND
  - Peripheral – PCMCIA
  - Many other interfaces

Integrated Security Engine

- AES 128-bit, 192-bit and 256-bit encryption/decryption in hardware for advanced DRM
- True random number generator (32-bit seed)

Programmable Media Acceleration

- Deterministic, on-chip audio decode/encode
- Hardware-enabled up to D1 (720 x 480) video playback
  - MJPEG, MPEG1/2/4, H.263, H.264, WMV
  - Independent 16 x 16 multiplier
- LCD controller with 16-bit color and up to 1280 x 720 LCD resolution
- Color space conversion
- Gamma correction
- Alpha-blending
- Scaler

Packaging

- 256 ball PBGA, 14 × 14 mm package, 0.8 mm ball pitch
- Available in commercial (0-70C) and industrial (-20C to 85C) temperature ranges
- All processors in the IP7500 family are pin-for-pin compatible, enabling multiple price-performance points from a single board design and layout

IP7500 Block Diagram