SoC 설계와 검증

On-Chip Buses/Networks for SoC

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References

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Contents

Introduction to SoC Bus

Introduction

- Interconnection of functional units in SoC
  - Communication architecture is a crucial element in SoC.
  - General solution for interconnection suitable for arbitrary applications is very complex.
- Standardization of On-Chip Bus (OnCB)
  - Design reuse and Intellectual Property (IP) is a MUST in the design of SoC.
  - VSIA (Virtual Socket Interface Alliance) founded in 1996 was the first step towards IP-based design.
  - VSIA aims to develop standards for integration and reuse of IP blocks.

Design Methodology

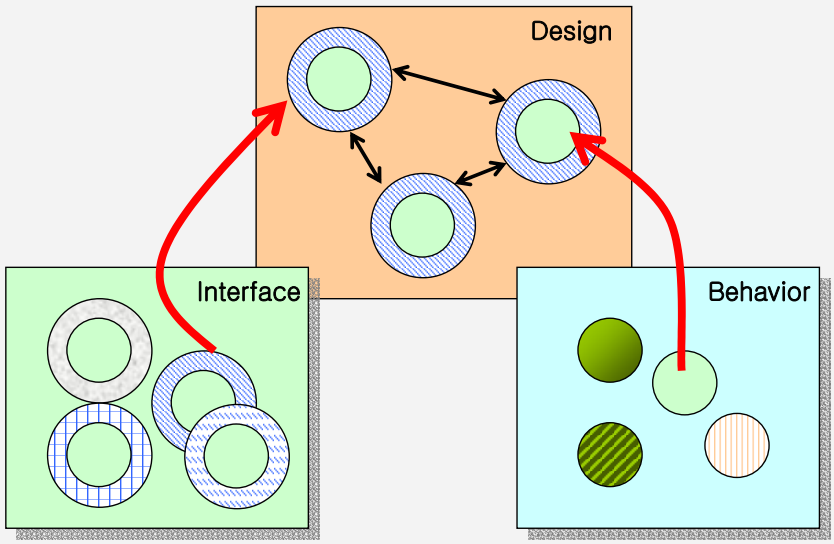
- Interface-based design
  - Through the separation of IP behavior from the communication gadgets, design reuse and verification has become easier in designing SoC.
- Platform-based design
  - The basic platform of SoC integration is fixed such as Software-API-Hardware platform, although certain degree of parameterization is possible.

Interface-Based Design

- Motivation
  - Communication among modules can be specified independently of the modules constituting the design.
- Design Procedure
  - 1) Expression of system behavior making use of models of computation.
  - 2) Design then becomes the arbitration of communication among different models of computation

Interface-based Design

- Method of describing designs focusing on how the modules interface with each other.
- Interface and behavior is separated completely.

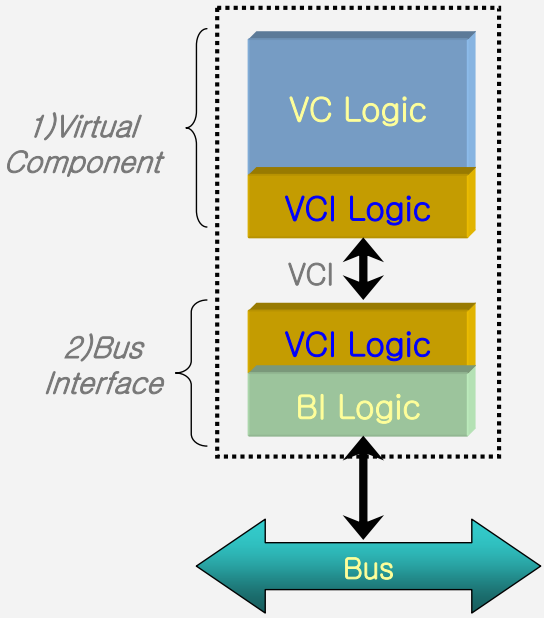


Interface-based Design

- Concept of VSIA's VCI (Virtual Component Interface)
  - Mix and match of "virtual components" from multiple sources on a single silicon chip.
  - "Virtual components" obey the standards as provided by VSIA.
- Challenges
  - Many on-chip bus standards exist, but no single bus can satisfy all the requirements from varying situations.

Interface-based Design

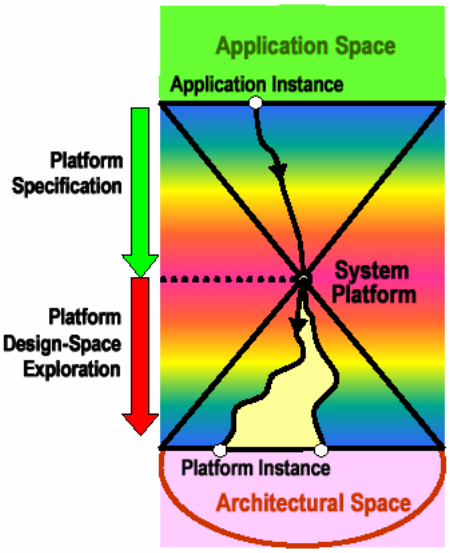
- How to solve it?
  - VCI (Virtual Component Interface) specification to which proprietary buses can interface.
  - 1)VC, designed with one interface, i.e., VCI can be integrated with different buses to meet different system performance requirements.
  - 2)The proprietary bus provider or VC designer should provide "Bus Interface" for integration



Platform-based Design

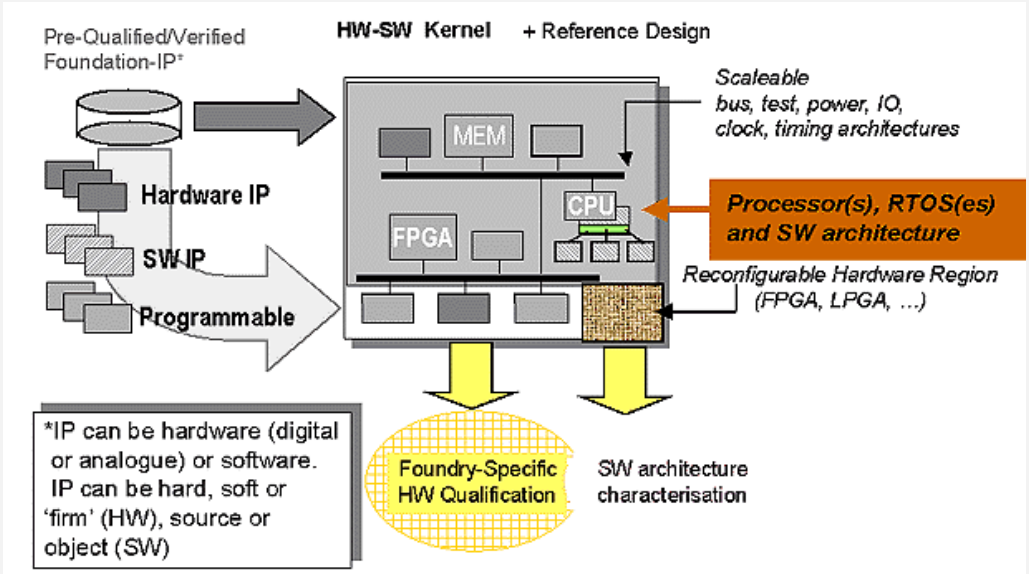
- What is it?
  - Substantial reuse of design implies that the basic implementation of SOC remains "fixed".
  - Certain degree of parameterization is possible.
- "Platform-based Design" is SOC design platform proposed by GSRC
  - GSRC, Gigascale Silicon Research Center
  - http://www.gigascale.org

What is SOC Integration Platform?



A platform is a coordinated family of hardware-software architectures, that satisfy a set of architectural constraints, imposed to allow the reuse of hardware and software components. This is called a "System Platform"

Hardware-Centric View of Platform



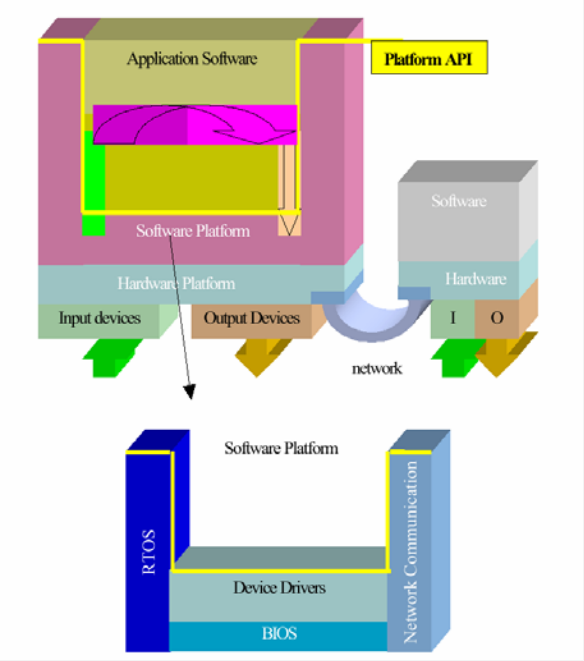
Micro-Architecture

- Definition of micro-architecture
  - The implementation of functionality as a composition of modules and components along with associated software
  - Ex.
    - Instruction set of microprocessor defines architecture.
    - The hardware organization defines micro-architecture.
- Micro-architecture as a set of interconnected components
  - Set of microprocessors, peripherals, dedicated logic blocks and memories

Mapping & Implementation

- 1)Functions are mapped onto micro-architecture
- 2)After the mapping, estimation of performance and cost is made.
- 3)Mapped micro-architecture is iteratively refined.
- 4)After the mapping with design constraints satisfied, each component is linked to the real hardware implementation or software component.

Software-Centric View of Platform



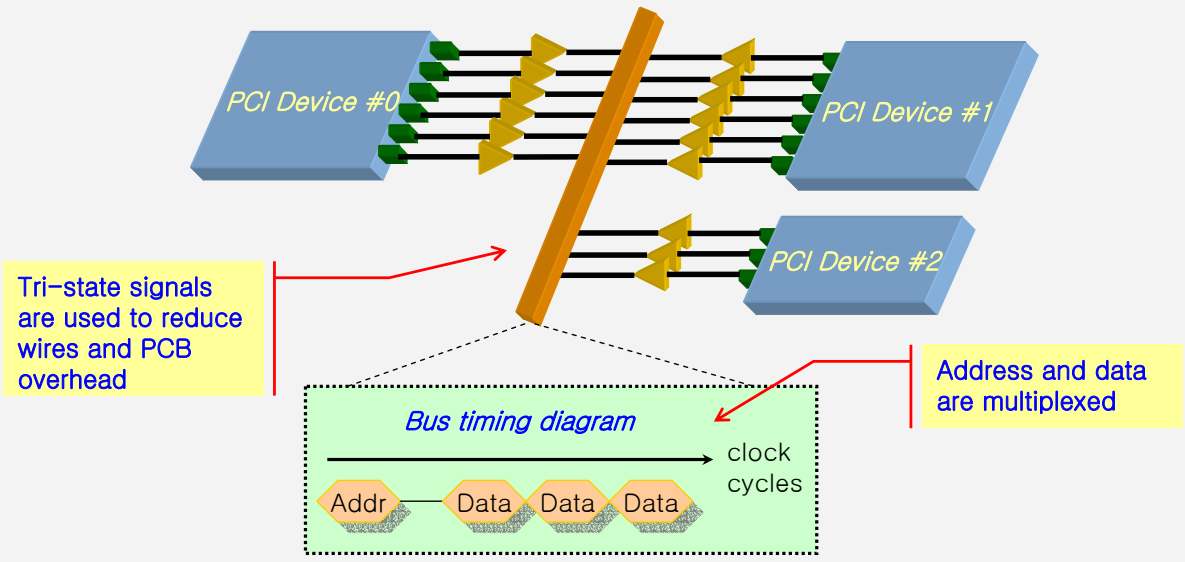
- Abstraction of the under-lying hardware present to the software designers a conceptual application programmer's interface (API)
- The platform services are offered to the software designers in the form of RTOS, special software stacks, and what is called middleware.

On-Chip Bus

Off-Chip Bus

- Features
  - PCI, ISA, … are off-chip buses
  - Connection of discrete chips on a PCB.
- Design Criteria
  - High-speed communication between discrete devices. (about 30MHz-100MHz)
  - Minimizing the number of bus signals, i.e., pins for reducing the cost of PCB
  - Tri-state signaling for add-in cards and extensions to disconnect the non-active cards.
  - PCI uses multiplexed signals for address and data.

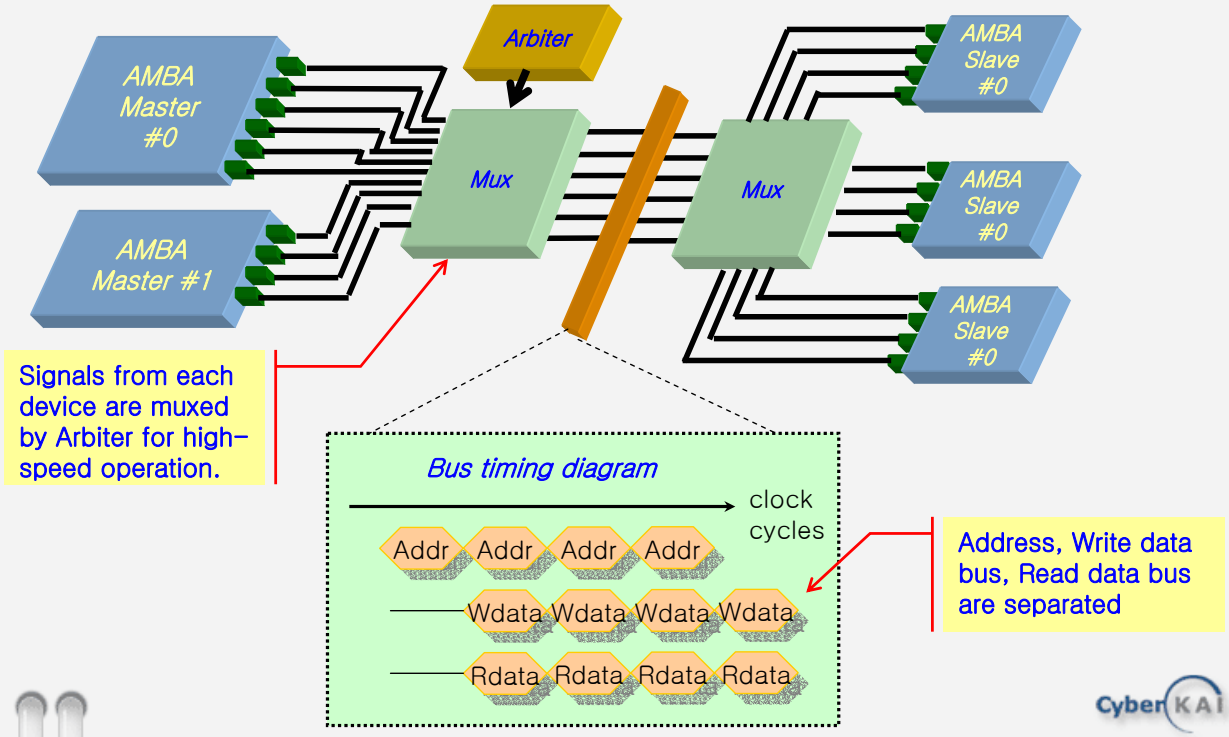
Limitation of Off-Chip Bus



What Features on OnCB?

- On-Chip Buses
  - Routing cost is not so important.
  - No use of tri-state signals : Tri-state bus is difficult for static timing analysis as the bus loading is only identified through dynamic simulation.
  - High-performance transaction schemes
    - Point-to-point protocol
    - Split transaction (Transaction is started on receiving the RSVP signal from the requested device.)
    - Efficient arbitration schemes are adopted.

On-Chip Bus

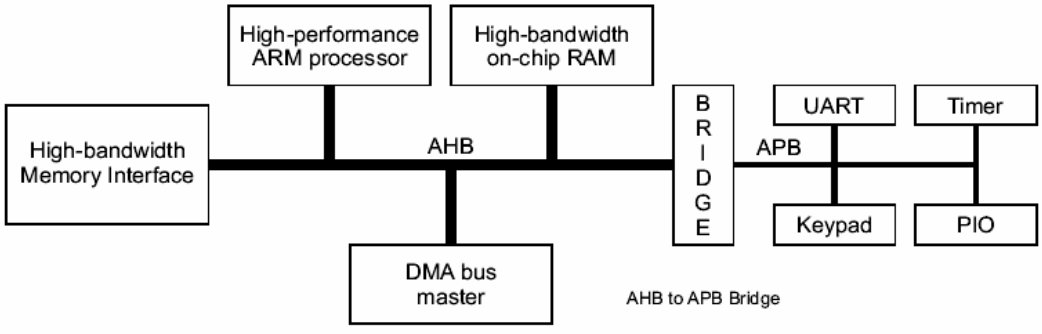


AMBA

- ARM
  - *Advanced Microcontroller Bus Architecture* for ARM-based System-on-Chip
  - Widely used for fast development of embedded microcontroller products with CPUs or DSPs
- Bus Transaction
  - Standard bus transactions are implemented (ex.; ERROR, RETRY, SPLIT)
  - Multiplexer interconnection scheme. (Arbiter and Decoder selects the master and the target through multiplexer.)

AMBA

- System backbone bus (AHB or ASB)
  - CPU/DMA/Memory
  - Pipelined/Burst transfer, Multiple bus master
- Peripheral bus (APB)
  - Simple interface
  - Suitable for many peripherals

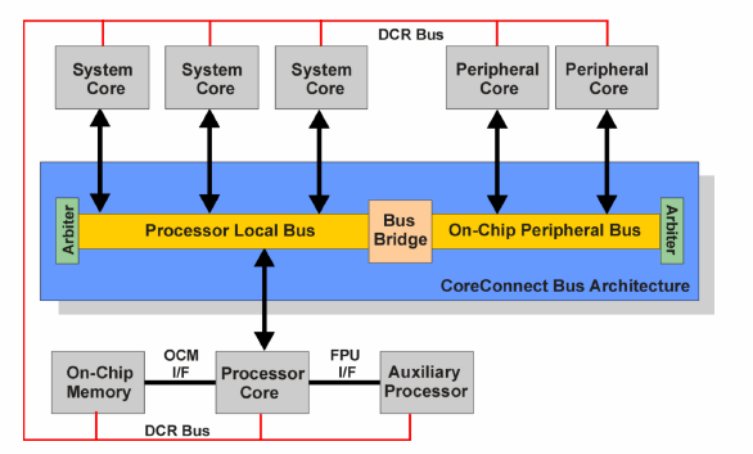


CoreConnect

- IBM's CoreConnect
  - Base bus scheme for the IBM Blue Logic Core Library
  - Consists of PLB(Processor Local Bus), OPB(On-Chip Periperahl Bus), DCR(Device Control Register) bus.
- Features
  - Standard bus transactions (Burst/DMA/Split/Pipelined)
  - DCR bus for movement of GPR (General Purpose Register) data between CPU and slave logic.

CoreConnect

- PLB
  - Separate read/write data bus for overlapped transactions.
  - DMA/Processor/Cache-line transfer
- OPB
  - On-Chip peripheral bus

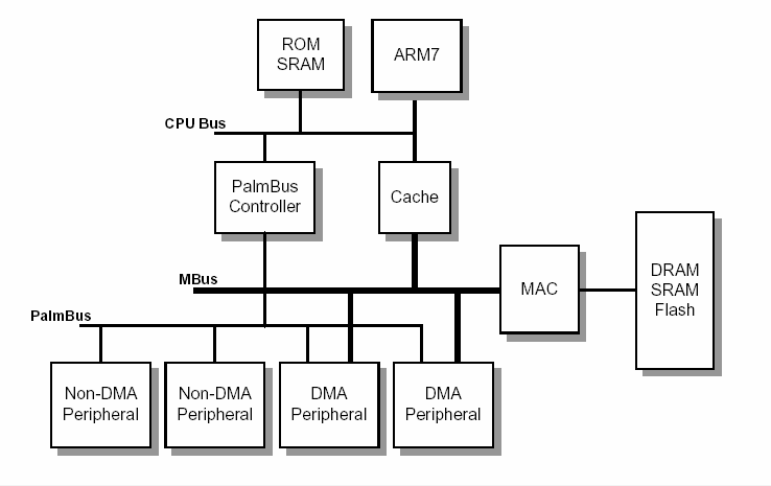


CoreFrame

- Palmchip Corporation
  - Simple protocol for reduced gate count
  - Positive-edge clocking only
  - Support for latch-based slave peripherals for low-power
- Buses
  - PalmBus
    - Peripheral bus
    - Interface between CPU and peripherals
  - MBus
    - DMA bus with pipelined address and control
    - DMA peripherals are connected to MBus
  - MAC (Memory Address Controller) connects MBus to external memories(DRAM, SRAM, Flash)

CoreFrame

- CoreFrame architecture
  - CPU bus for CPU and cache
  - MBus for high-performance operation
  - PalmBus for peripheral devices.

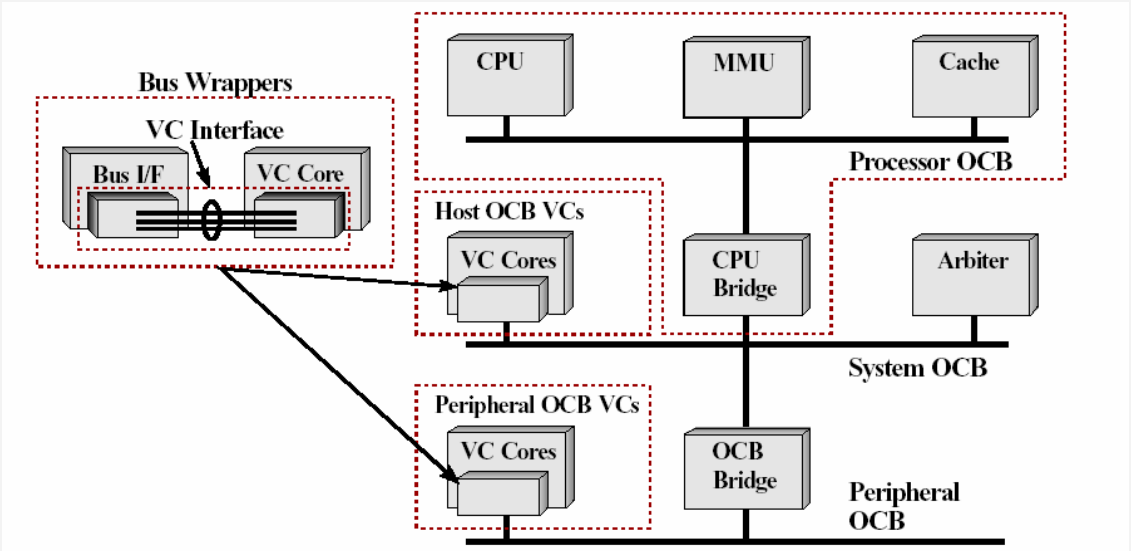


VCI

- VSIA's On-Chip Bus Development Working Group
  - VC interface
    - OnCB standard virtual component interface for communication between bus and component.
  - Bus Wrapper
    - Logic between bus & VC interface or component & VC interface
- Bus hierarchy
  - Processor OnCB : Processor/Cache
  - System OnCB : RISC/DSP/DMA
  - Peripheral OnCB

VCI

- VC Core and Bus I/F interfaces through bus wrappers.



Others

- OCP
  - Open Core Protocol by OCP-IP Corporation
- Wishbone
  - SiliCore Corporation
- FPI
  - Infineon

Summary

	AMBA	CoreConnect	Core Frame	VCI	Wish bone
Hierarchical	O	O	O	X	?
Uni/Bidirectional	Uni	Uni	Uni	Uni	Uni/Bi
Shared/P2P	Shared	Shared	P2P	?	Shared
Synchrouns/Async	S	S	S	S	S
Multiple clock	?	?	O	O	O
Handshaking	O	O	O	O	O
Split transfer	O	?	?	O	?
Pipelined transfer	O	O	?	O	X
Broadcast	?	?	?	X	?
Pipelined Arbitration	O	O	O	X	?
Centralized/Distributed	Cent	Cent	Cent	Cent	Cent

Summary

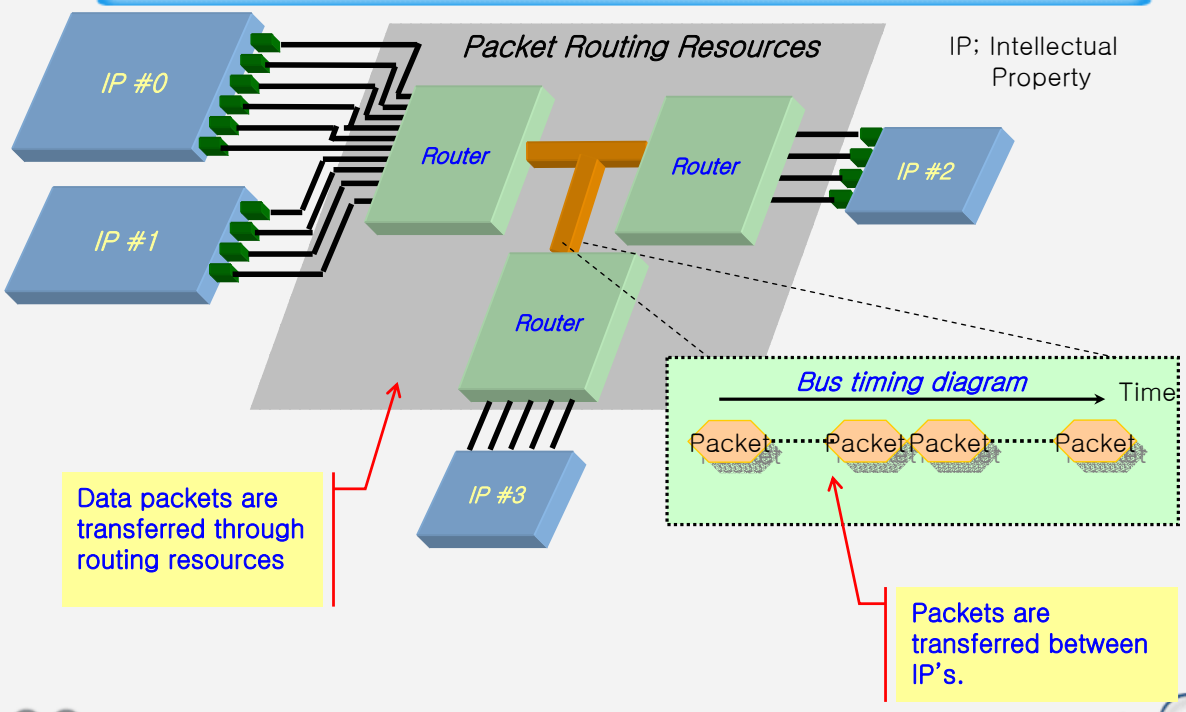
- (Normal) On-chip Bus has
  - Unidirectional bus with multiplexed master/slave & without tri-state bus
  - Shared bus with the exception of CoreFrame(P2P).
  - Supports handshaking, split transfer, pipelined transfer (possible when address and data use separate buses) for high-performance transaction
  - Pipelined arbitration scheme can be additionally used for high-performance arbitration.

On-Chip Network

Why On-Chip Network?

- Limitation of Bus-based OnCB
  - Lack of Software interface (only low-level hardware interface available)
  - Lack of SW Interrupt handling (only low-level hardware interrupt available)
  - Lack of Debugging features
  - Lack of interfacing with off-chip bus
  - Lack of Error detection/correction
- Network-oriented On-Chip Bus
  - Layered network OnCB
  - Route-Packet based OnCB
  - Micro-network for separation of computation and interface

Network Concept on OCB



Network-on-Chip(NOC)

- Proposed by GSRC (Gigascale Silicon Research Center)
- Layered communication architecture
  - Similar to OSI Reference Model in the communication networks community
  - Overcomes the ad hoc design methodology of the previous OCB design.
  - Provides a programmer with an abstraction of the underlying communication network.

Network-on-Chip

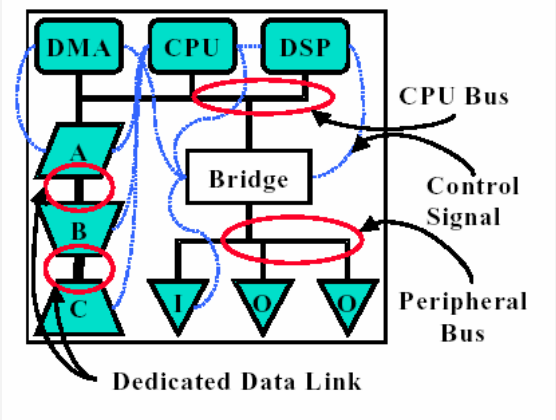
- OSI Reference Model Applied to NOC
  - Physical
    - Signal voltage, timing, bus widths, pulse shape.
    - Synchronization of signals is done in this layer for IP's at different clock frequency.
    - Power/Delay estimation is difficult.
  - Data Link
    - Reliable data transfer over the physical link
    - Error detection/correction is implemented.
  - Network
    - Topology-independent view of the end-to-end communication

Network-on-Chip

- Transport
  - Establish & maintain end-to-end connection.
  - Flow control for packet segmentation and assembly
- Session
  - Add state to the end-to-end connection
  - Common session protocol is synchronous messaging which requires the sending and receiving components rendezvous as the message is passed.
- Presentation
  - Conversion of data into compatible formats (byte orderings..etc.)
- Application
  - Define a function using lower stack layers.

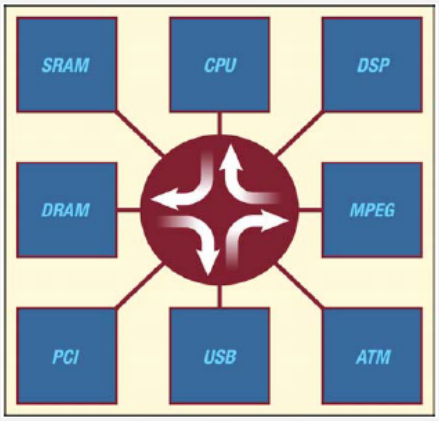
MicroNetwork

- Background;
  - Generally, separation between computation and communication is poor in OnCB scheme.
  - Direct connections between cores requires detailed prior knowledge of timing, protocol, and performance characteristics.



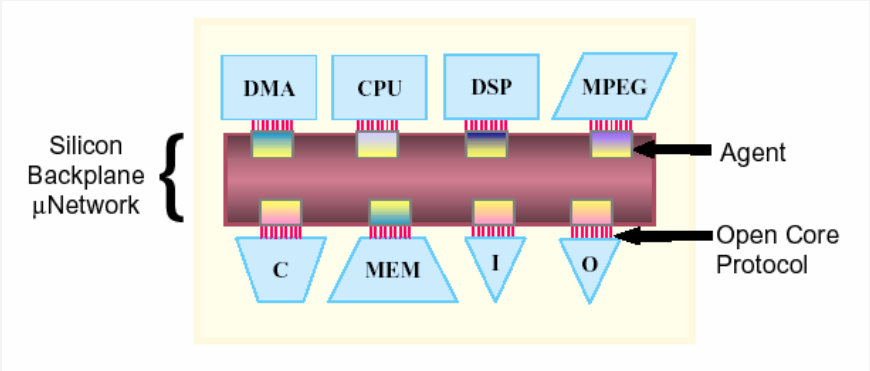
MicroNetwork

- Sonics, Inc.'s μNetworks
  - Combination of TDMA (Time Division Multiple Access) bandwidth scheme with fully pipelined/fixed-latency bus (due to non-hierarchical nature of the bus).
  - Configurable communication system that simultaneously incorporates data, test, and control traffic.
  - Design and verification efforts are reduced due to flat bus structure.



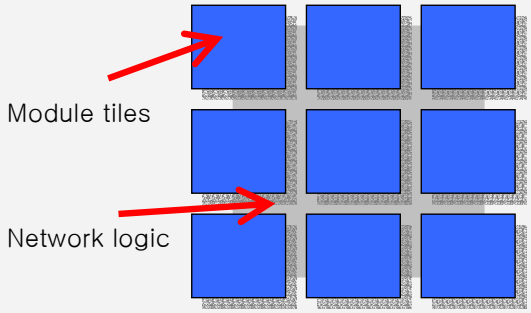
MicroNetwork

- μNetworks Components
  - Each IP core communicates with "Agent" through *OpenCore Protocol Interface*.
  - Agents communicate with each other, on the other end, through the network with TDMA bus, which is Si-Backplane μNetwork.



Route Packets

- Presented by Stanford Computer Systems Laboratory.
- Network to replace global wiring
  - Concentrates on the wiring problem in the SoC back-end design.
  - Use of route packets for communication for IP interconnection in SoC instead of global wires
  - Low & predictable cross-talk



Summary

- The network connection throughout the chip
  - Application of network-area concepts to the on-chip bus.
  - Simplified verification of interconnection problems between IP's.
  - Wire load and delay are more predictable.