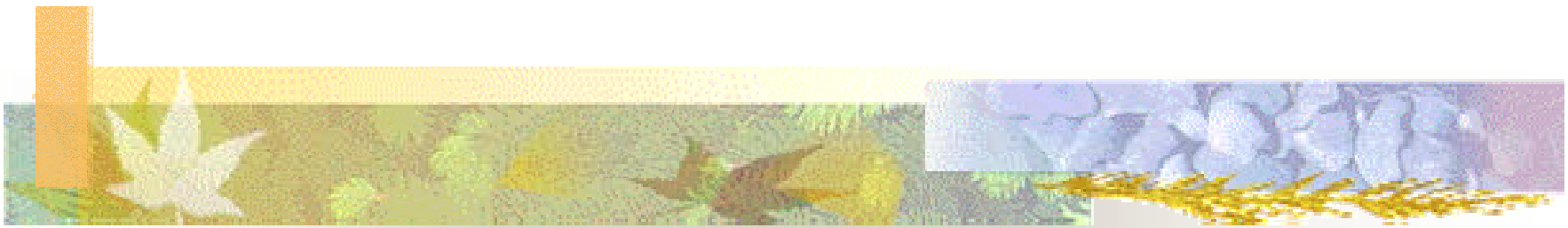
MOS OP AMP DESIGN:

A Tutorial Overview

(PAUL R. GRAY & ROBERT G. MEYER)



Presented by:

HARSH KULKARNI

KUNAL PATEL

About the Paper……..

- Overview of CMOS OP AMP design techniques
- PART I:
  - Performance of a basic two-stage OP-AMP
  - Design issues, constraints, tradeoffs discussed
- PART II:
  - Alternative architectures for improved performance
  - Design of output stages

Introduction

- Relevance of OP AMP design
- Designing OP AMPS for single-chip analog subsystems
  - (VS stand-alone CMOS amplifiers)
  - Designing for well-defined loads
- Internal Amplifiers VS Output Buffers

Design Issues

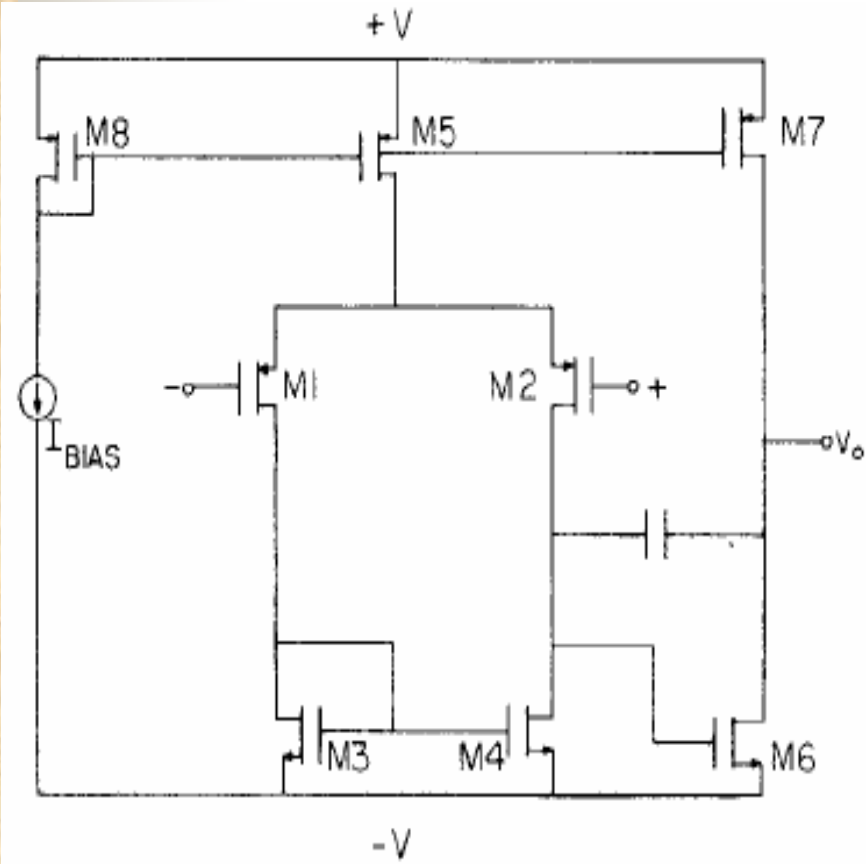
TYPICAL SPECS

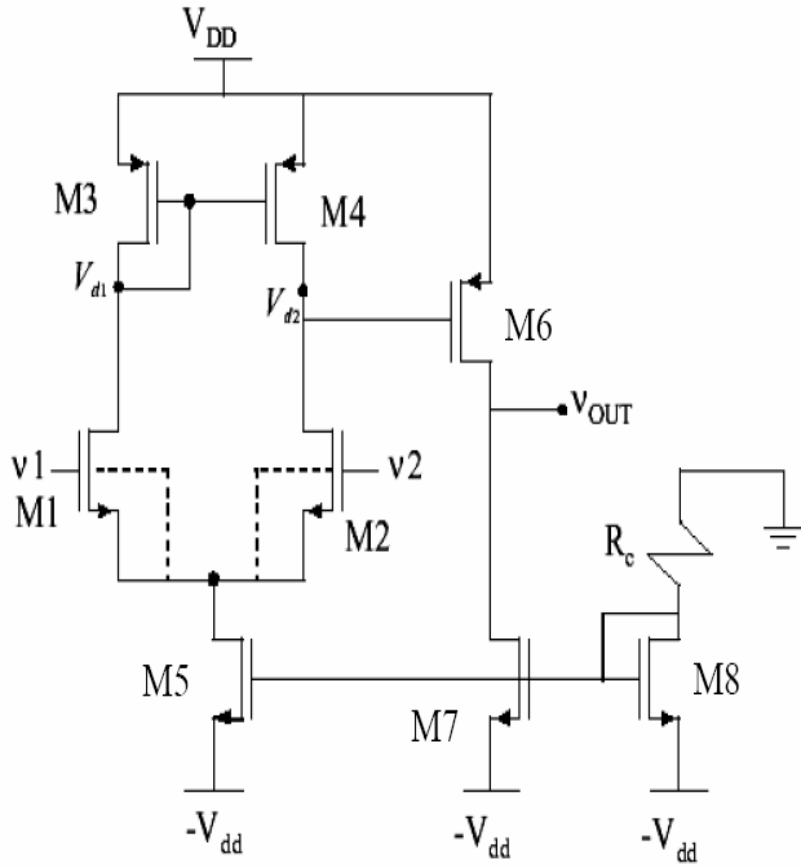
- DC Gain (Av)
- Unity Gain Bandwidth
- Power Dissipation
- Slew Rate
- Input Offset Voltage
- PSRR
- Output Voltage Swing
- ICMR
- CMRR

DESIGN FACTORS

- Frequency Response
- Phase Margin
- Load Capacitance
- Compensation
- Nulling Resistor
- Noise Performance
- Device Dimensions

Basic Two Stage OP AMP





Input Transistors: PMOS

(Discussed in the paper)

Input Transistors: NMOS

(Discussed in the class)

Open Circuit Voltage Gain

$$A_v = g_m r_o = \frac{2I_D}{V_{GS} - V_T} \cdot \frac{1}{\lambda I_D}$$

$$A_v = \frac{2L}{V_{GS} - V_T} \cdot \left(\frac{dx_d}{dV_{ds}} \right)^{-1}$$

$$A_v = \frac{2\sqrt{\mu_n C_{OX} . W . L}}{\sqrt{2I_D}} \cdot \left(\frac{dx_d}{dV_{DS}} \right)^{-1}$$

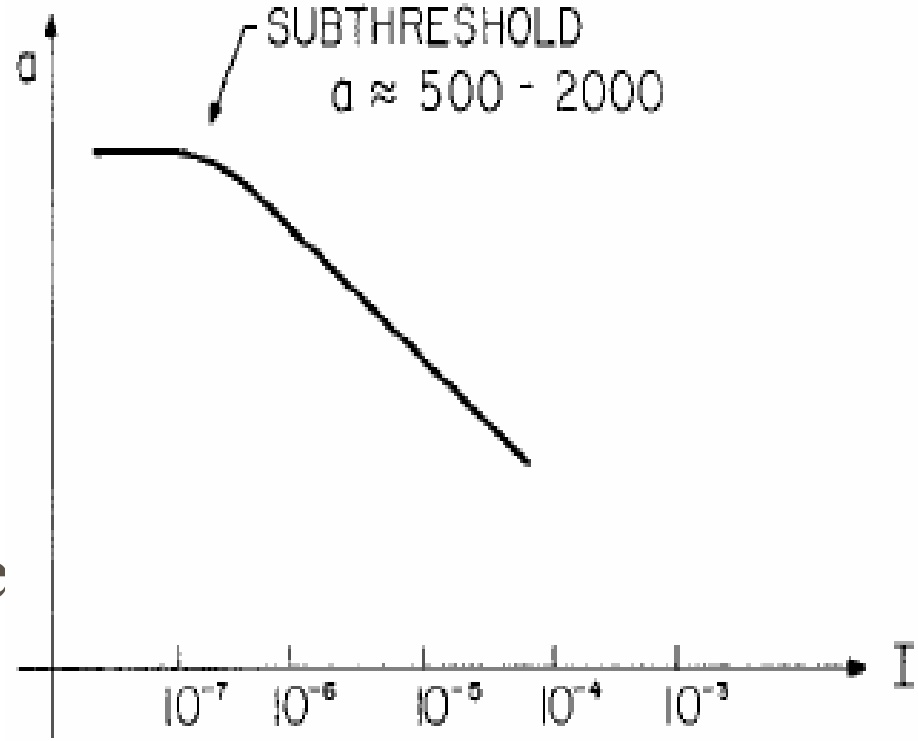
- Gain is directly proportional to the square root of W and L
  - *Decides minimum size of transistors*
- Gain is an increasing function of substrate doping
  - $\left(\frac{dx_d}{dV_{DS}} \right)$ *decreases with increasing doping*

Gain VS Bias Current

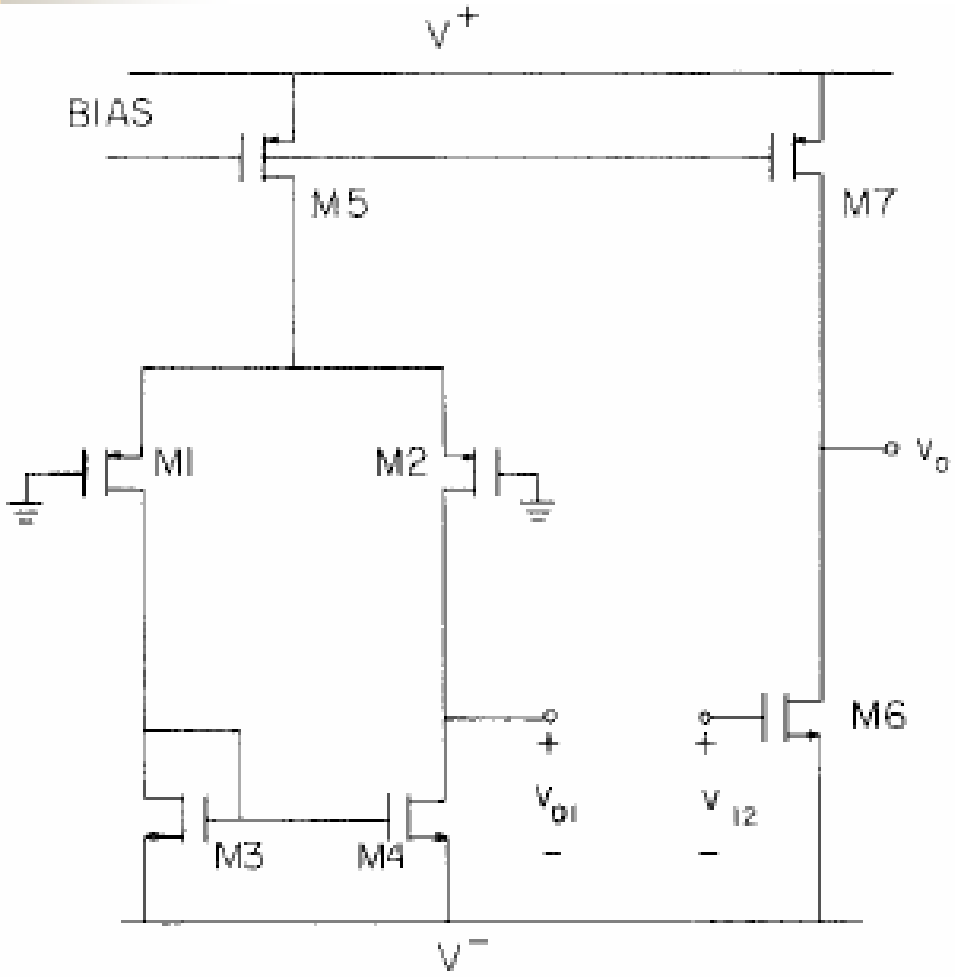
For constant device geometry:

$$A_v = \frac{2\sqrt{\mu_n C_{OX} .W .L}}{\sqrt{2 I_D}} . \left(\frac{dx_d}{dV_{DS}} \right)^{-1}$$

- Gain is inversely proportional to the square root of the drain current



Input Offset Voltage



- Systematic Offset Voltage: Results from Design of circuit and is present even when all matched devices are indeed identical

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \left(\frac{1}{2}\right)\frac{(W/L)_5}{(W/L)_7}$$

- Choose same channel lengths for M3, M4, M6 to counter process induced variations in L

Random Input Offset Voltage

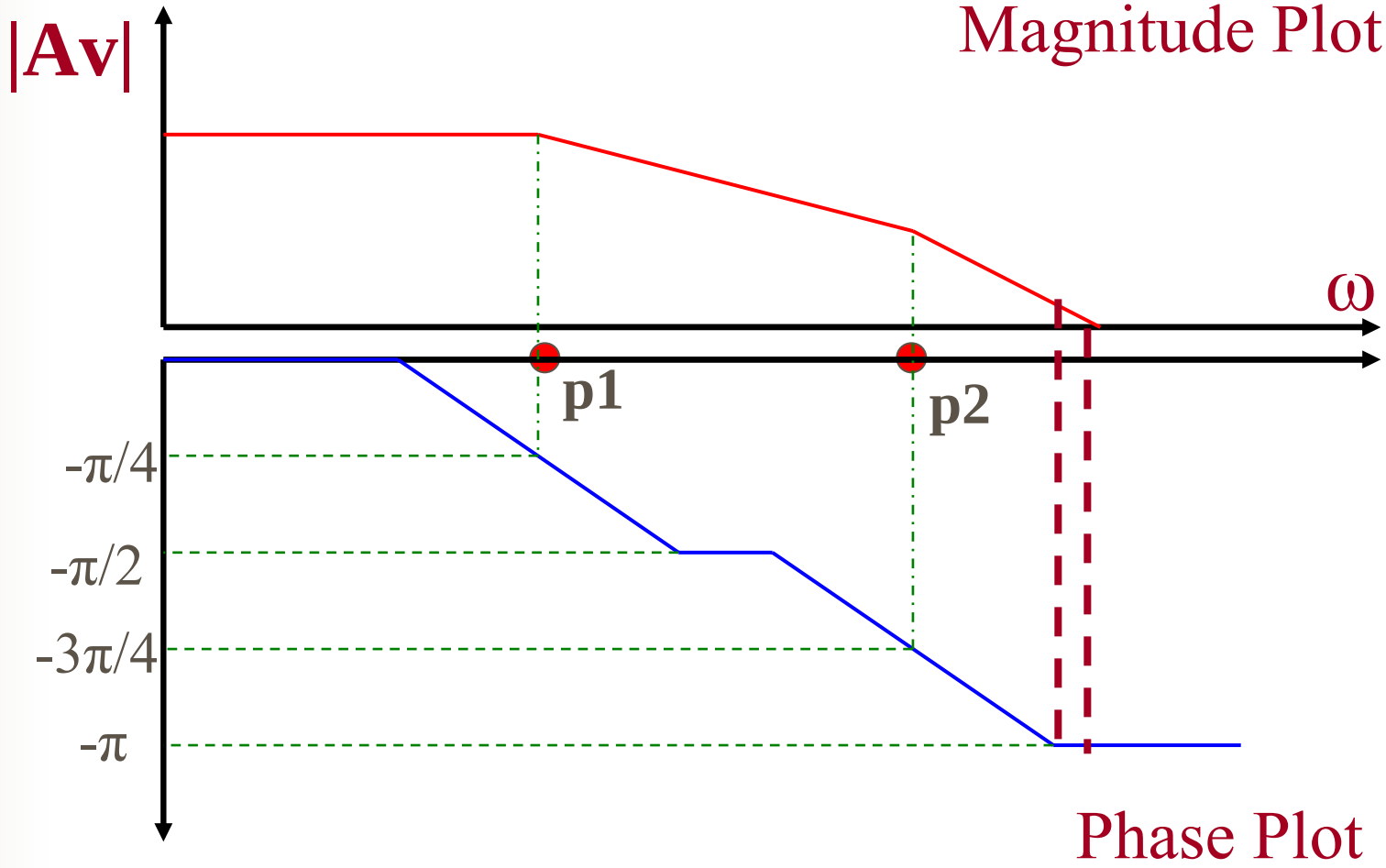
- Results from mismatches in supposedly identical pairs of devices.
- If the load elements of the OP AMP mismatch by Δ, the for V_{out} to be zero, the absolute difference in the two currents must be ΔI. This requires that the DC input difference voltage to be applied be:

$$V_{gs} = \frac{I}{g_m}\Delta = \frac{(V_{gs} - V_T)}{2}\Delta$$

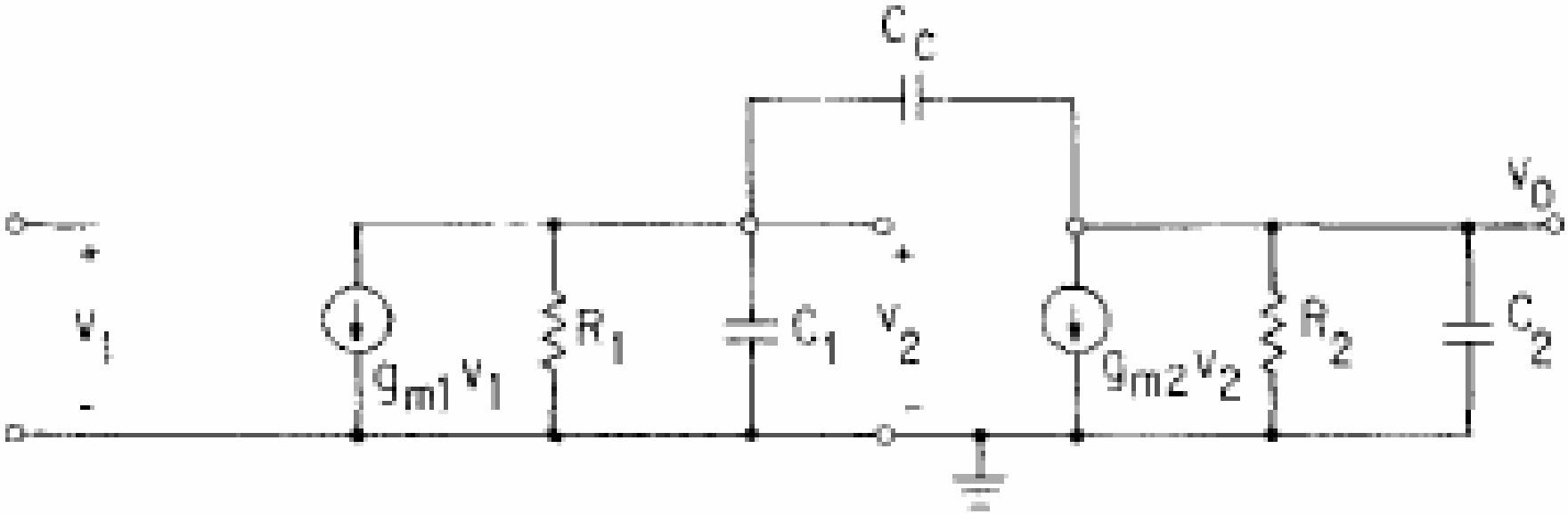
- Thus Input offset depends on I/gm ratio and the fractional mismatch Δ.
- Mismatch can be reduced by operating at low values of V_{gs}.

- THRESHOLD MISMATCH: Independent of bias parameters
  - *Improved by Common Centroid Geometries*

Frequency Response



Compensation & Pole Splitting



$$p_1 = \frac{-1}{(1+g_{m2}R_2)C_cR_1}$$

$$p_2 = \frac{-g_{m2}C_c}{C_2C_1 + C_2C_c + C_cC_1}$$

$$z = +\frac{g_{m2}}{C_c}.$$

p1: Pole due to capacitive loading of the first stage by the second

p2: Pole due to capacitance of the output node of the second stage

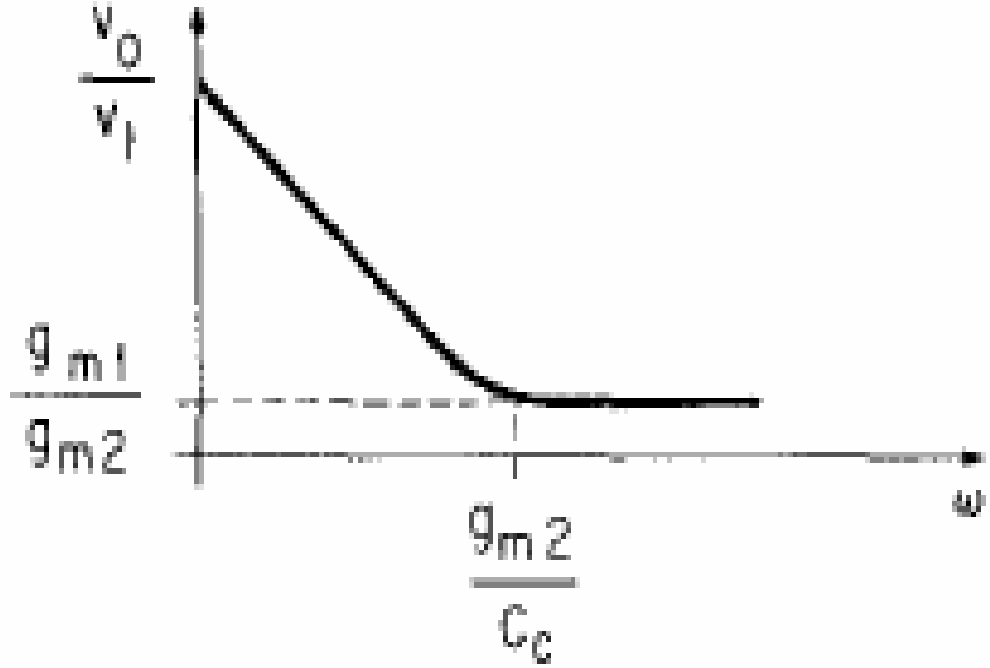
Cc: Compensation capacitance

Problem of Pole Splitting

Assume $C_1 << C_2, C_c$

$$\left|\frac{p_2}{\omega_1}\right| = \frac{g_{m2}C_c}{g_{m1}C_2}$$

$$\left|\frac{z}{\omega_1}\right| = \frac{g_{m2}}{g_{m1}}.$$

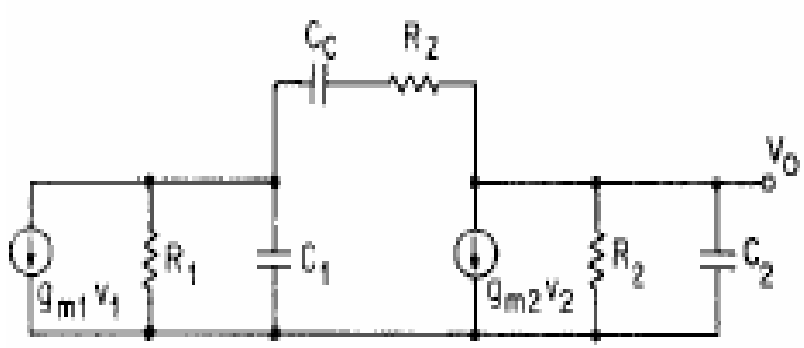


$$GB(\omega) = \frac{g_{m1}}{C_C}$$

- At HF, Cc behaves like a short circuit => $Gain = g_{m1}.\left(1/g_{m2}\right)$
- The polarity of this gain is opposite to that at low frequencies
- Hence negative feedback => positive feedback

Nulling Resistor Design

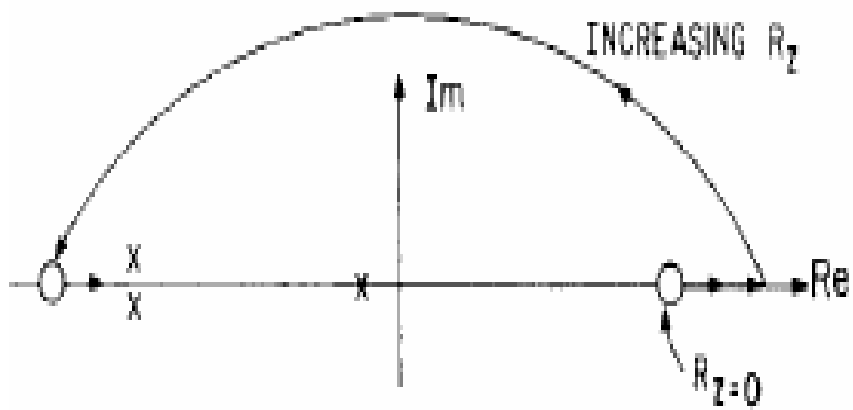
- Hence the need for a Nulling Resistor
- R_z connected in series with C_c



- At HF, the O/P current from the 1st stage now flows as drain current in the 2nd stage transistor

$$z = \frac{1}{C_c\left(\frac{1}{g_{m2}} - R_z\right)}$$

- Rz can be increased to make z negative, i.e. push the zero in the left-half plane to improve the phase margin



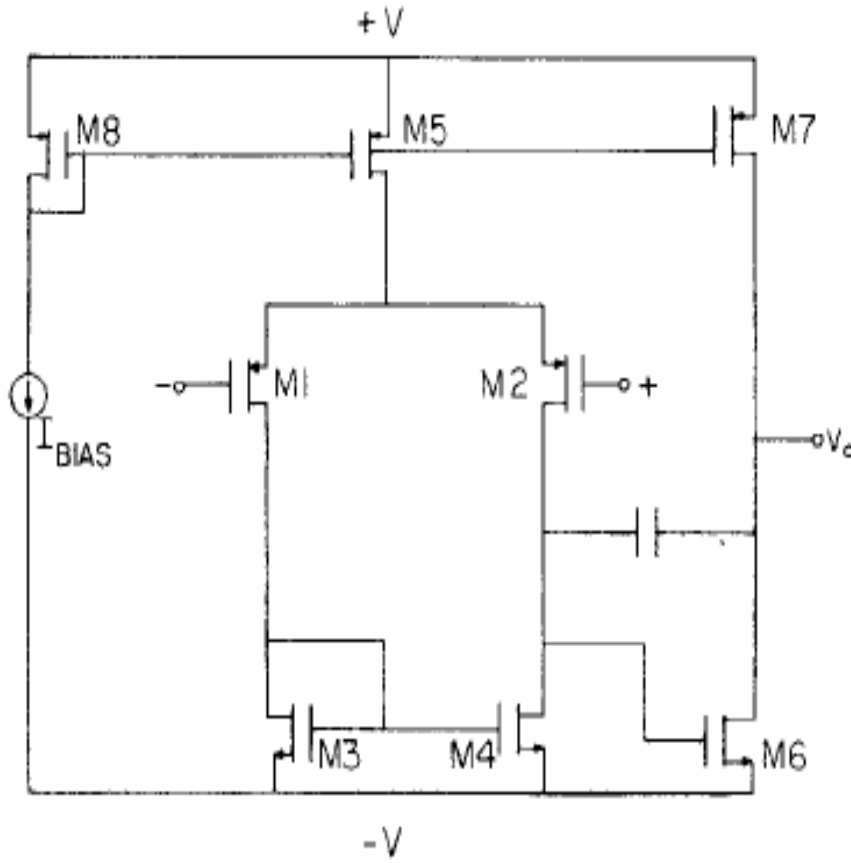
Slew Rate

$$SR = \frac{I_{D5}}{C_C} = \frac{2I_{D1}}{C_C}$$

$$C_C = \frac{g_{m1}}{GB(\omega)}$$

$$SR = \frac{2I_{D1}.\omega}{g_{m1}}$$

$$SR = (V_{gs} - V_T)_1.\omega_1$$

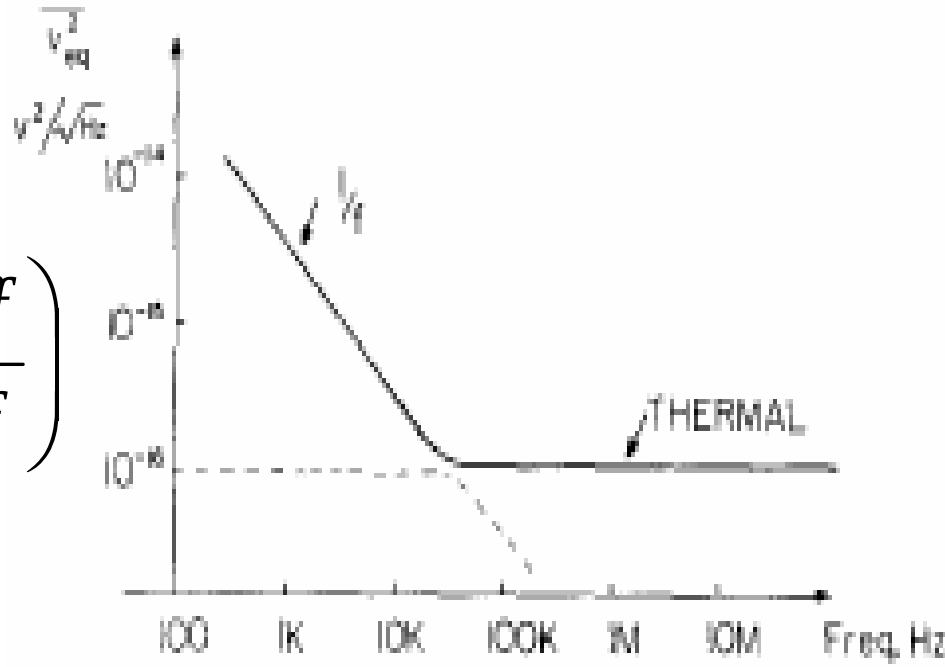


- $(V_{gs} - V_T)_1$ is the range of differential input voltage for which the input stage stays in the active region
- For constant BW, the slew rate is directly proportional to this range

Noise Performance

- **Input Referred 1/f noise**

$$V_{1/f}^2 = \frac{2K_p}{W_1 L_1 C_{ox}} \cdot \left(1 + \frac{K_n \mu_n L_1^2}{K_p \mu_p L_3^2}\right) \cdot \left(\frac{\delta f}{f}\right)$$



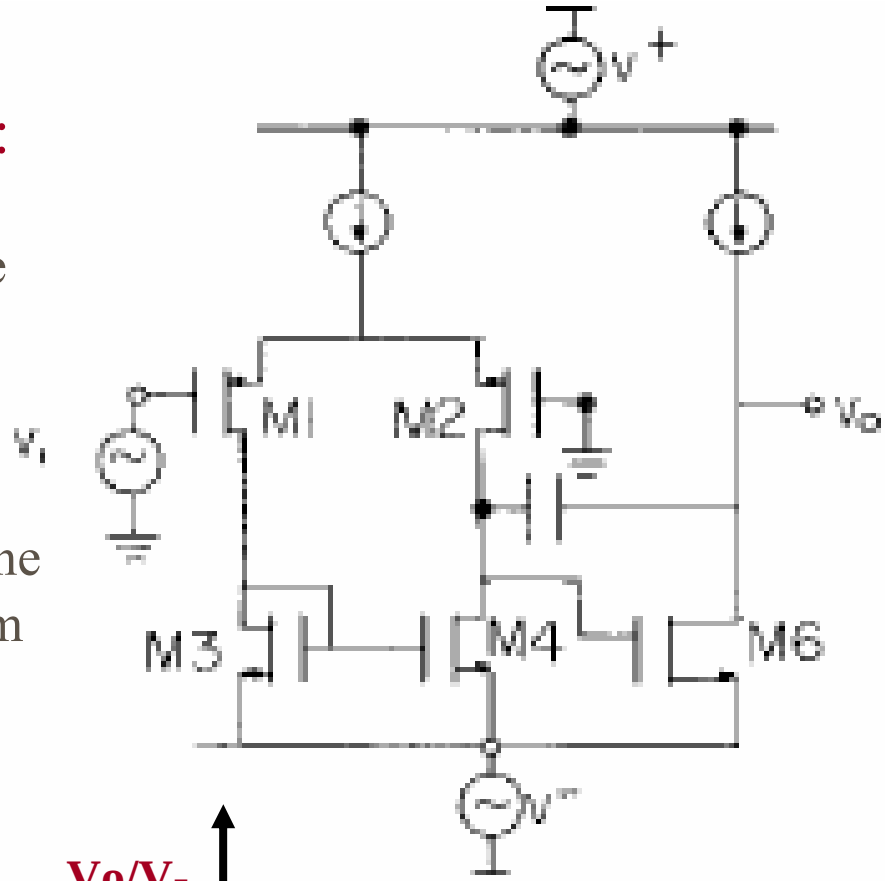
- **Thermal Noise**

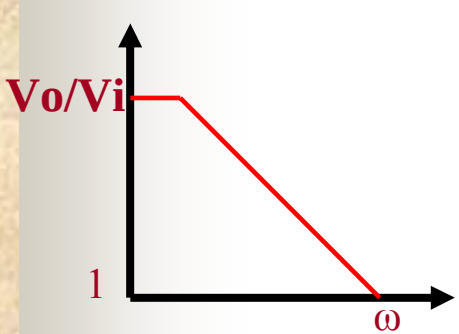
$$V_{eq}^2 = 4kT \frac{4}{3\sqrt{2\mu_p C_{ox} (W/L)_1 I_D}} \left(1 + \sqrt{\frac{\mu_n (W/L)_3}{\mu_p (W/L)_1}}\right)$$

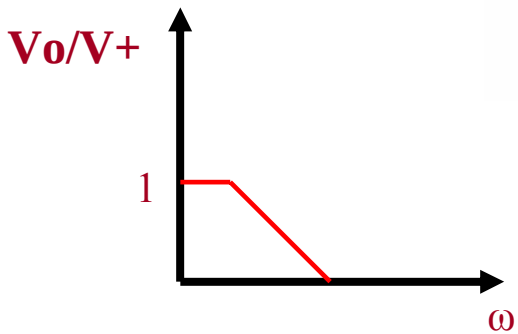
Power Supply Rejection

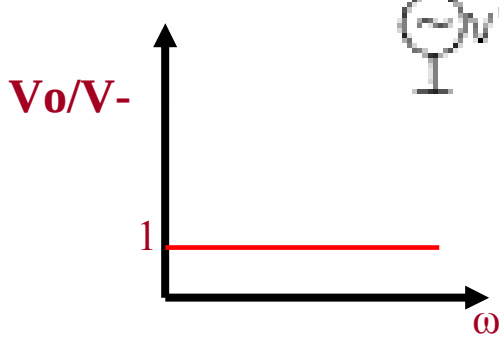
•Need for Power Supply Rejection:
We need high PSRR in complex A-D systems, to avoid coupling of digital noise into analog supplies

•PSRR: Ratio of the voltage gain from the input to the output (open loop) to that from the supply to the output.



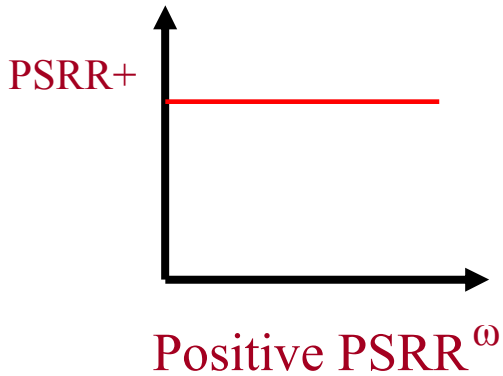






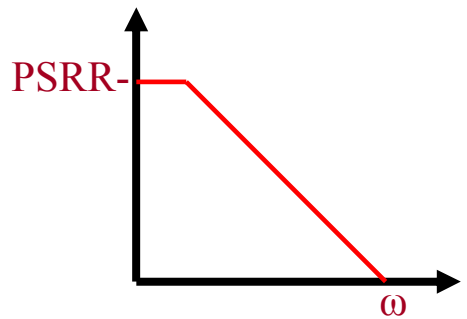
PSRR continued…….

$$PSRR^{+} = \left[\frac{\left\{ \frac{V_0}{V_i}(\omega) \right\}}{\left\{ \frac{V_0}{V^{+}}(\omega) \right\}} \right]$$



Positive PSRR

$$PSRR^{-} = \left[\frac{\left\{ \frac{V_0}{V_i}(\omega) \right\}}{\left\{ \frac{V_0}{V^{-}}(\omega) \right\}} \right]$$



Negative PSRR

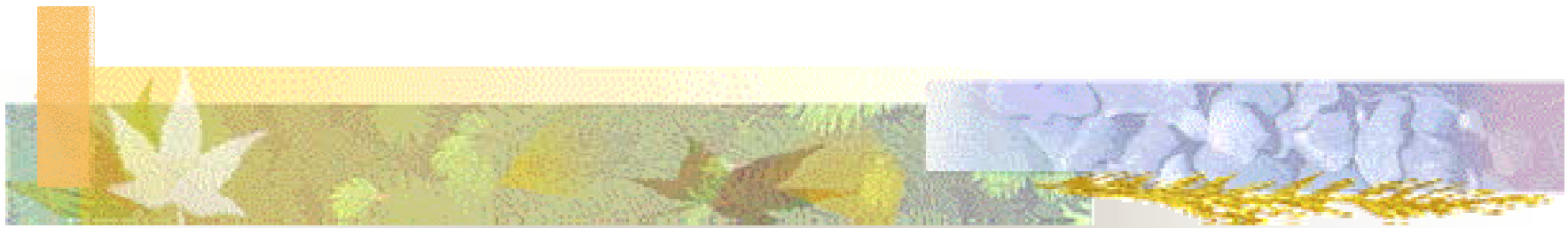
- Alternative Architectures have been developed to alleviate the problem. *(discussed later)*

Summary: PART I

- Relevance of OP AMP Design
- Performance Objectives for MOS OP AMPS
- Basic two-stage CMOS OP-AMP Architecture
- Analysis of Performance Parameters
  - Voltage Gain
  - Input Offset Voltage
  - Frequency Response, Compensation and Slew Rate
  - Noise Performance
  - Power Supply Rejection

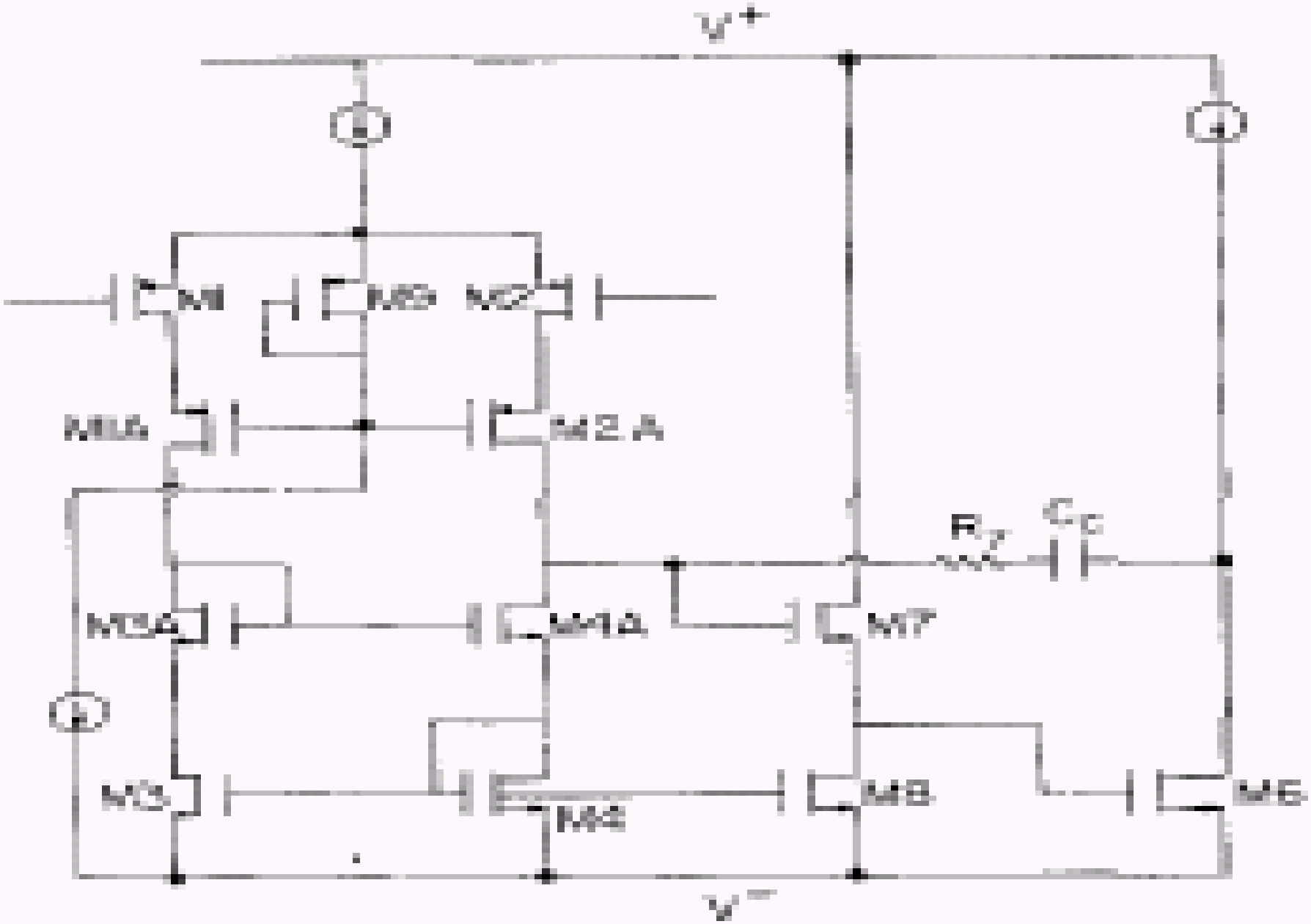
Part II

ALTERNATIVE ARCHITECTURES FOR IMPROVED PERFORMANCE



Need for Alternative Architecture

- High performance that is superior over the basic circuit
- Improved closed loop voltage gain
- Improved stable bandwidth
- Better power-supply rejection ratio

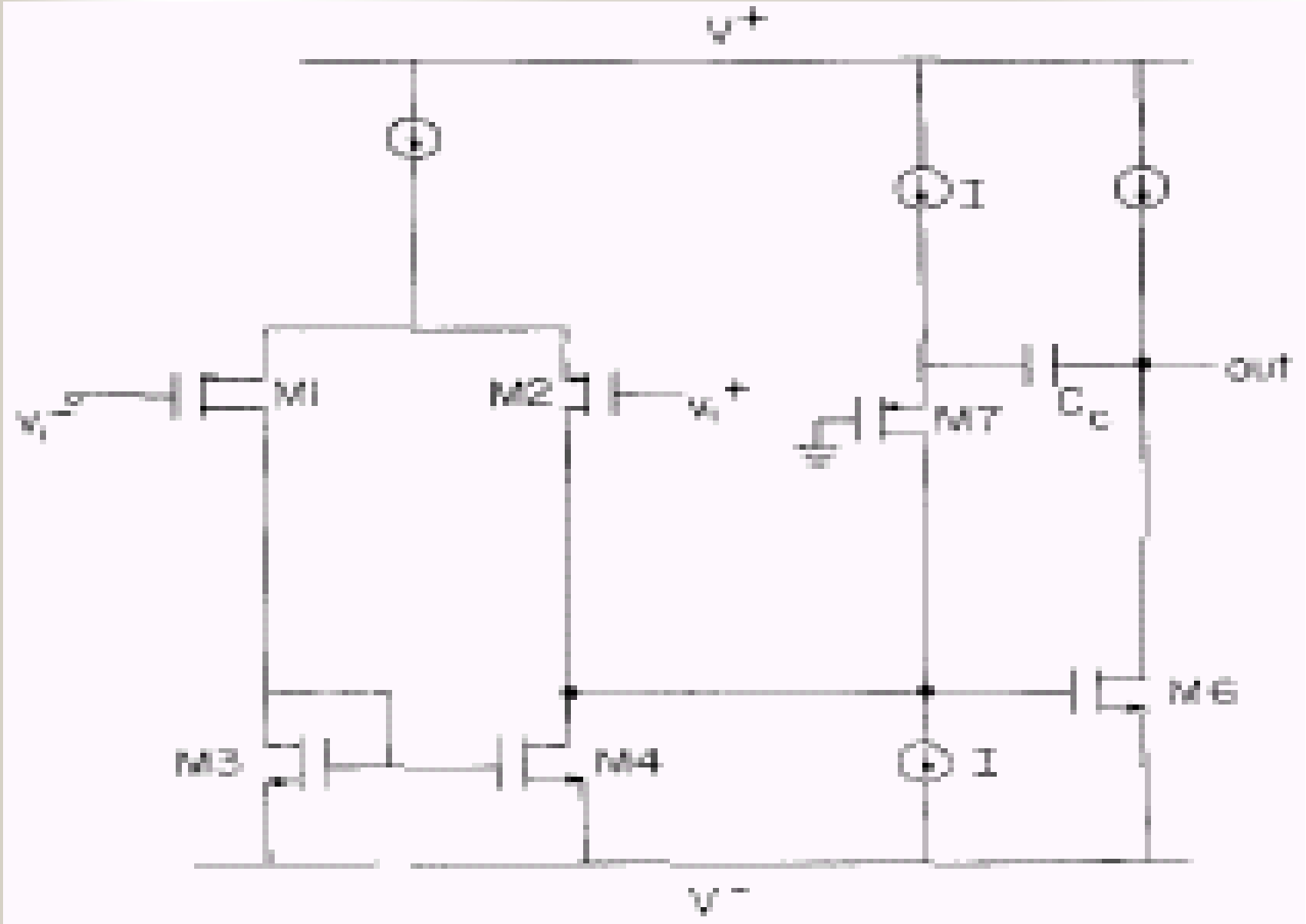

V+
M1
M3
M2
M1A
M2A
M4A
M1A
M7
R
C
M3
M4
M8
M6
V−

Use of Cascode for Improved Voltage Gain

- Basic 2 stage op-amp suffers from inadequate voltage gain.
- Approach: Add a common gate and common source, cascode.
- M1A and M2A input cascade.
- M3A and M4A cascade of current mirror.
- M9 and a current source biases the gates of M1A and M2A.
- M7 and M8 act as level shifters.

Two-stage amplifier with cascoded first stage

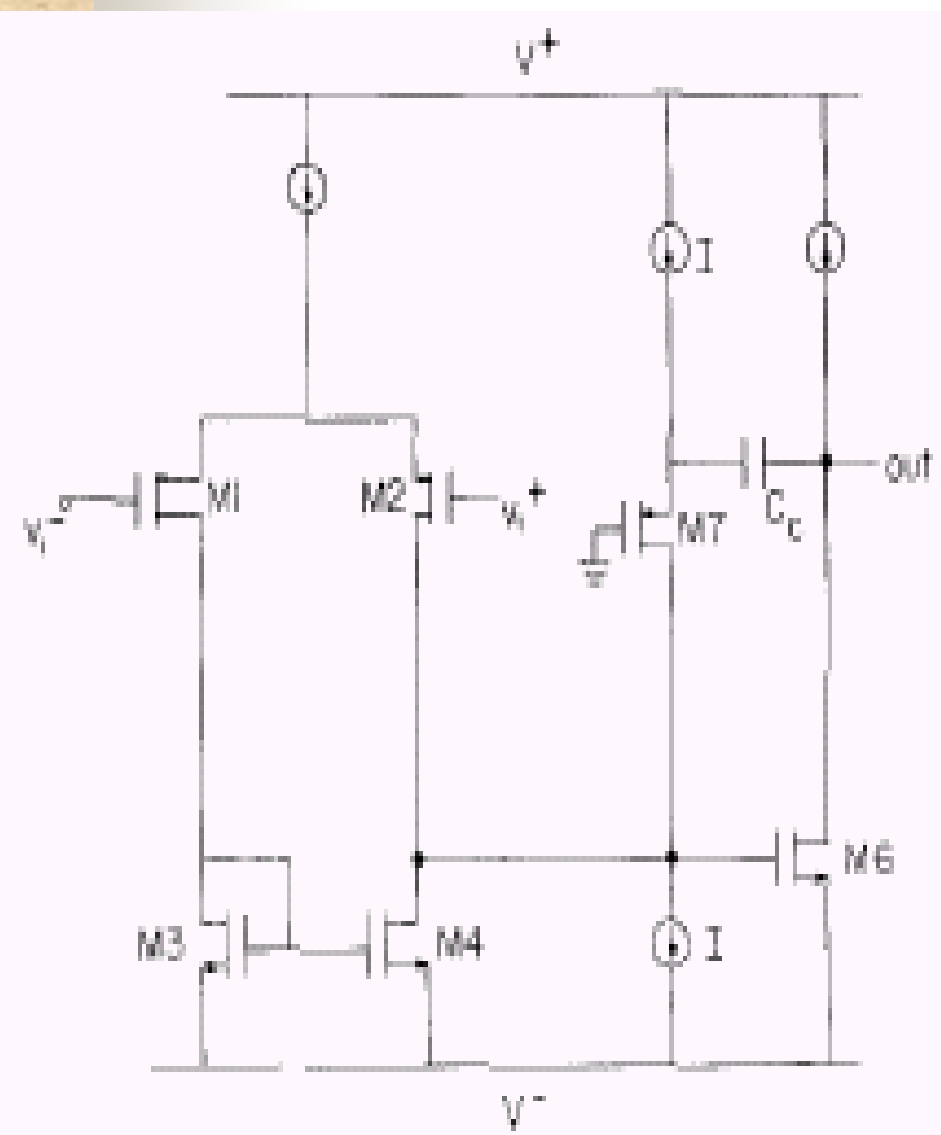
- Advantage:
- Increase gain.
- Increase output resistance.
- Disadvantage: Reduction in ICMR.
- Tradeoff: Improve ICMR by adding cascode to second stage with decrease in output swing.


V+
I
I
M1
M2
M7
Cc
out
M6
M3
M4
I
V-

Improved PSRR Grounded-Gate Cascode Compensation

- Basic 2 stage op-amp suffers from reduced PSRR.
- Cause: Variation in negative supply of power.
- Effect: Change in output with change in supply voltage.
- This can be overcome by using cascode.

Basic amplifier with cascode feedback compensation



- Connect the left end of the capacitor to virtual ground.
- No change in capacitor voltage with change in supply
- Output independent on supply variations.
- Current source and sink is added to bias M7 in active region.

Tradeoff

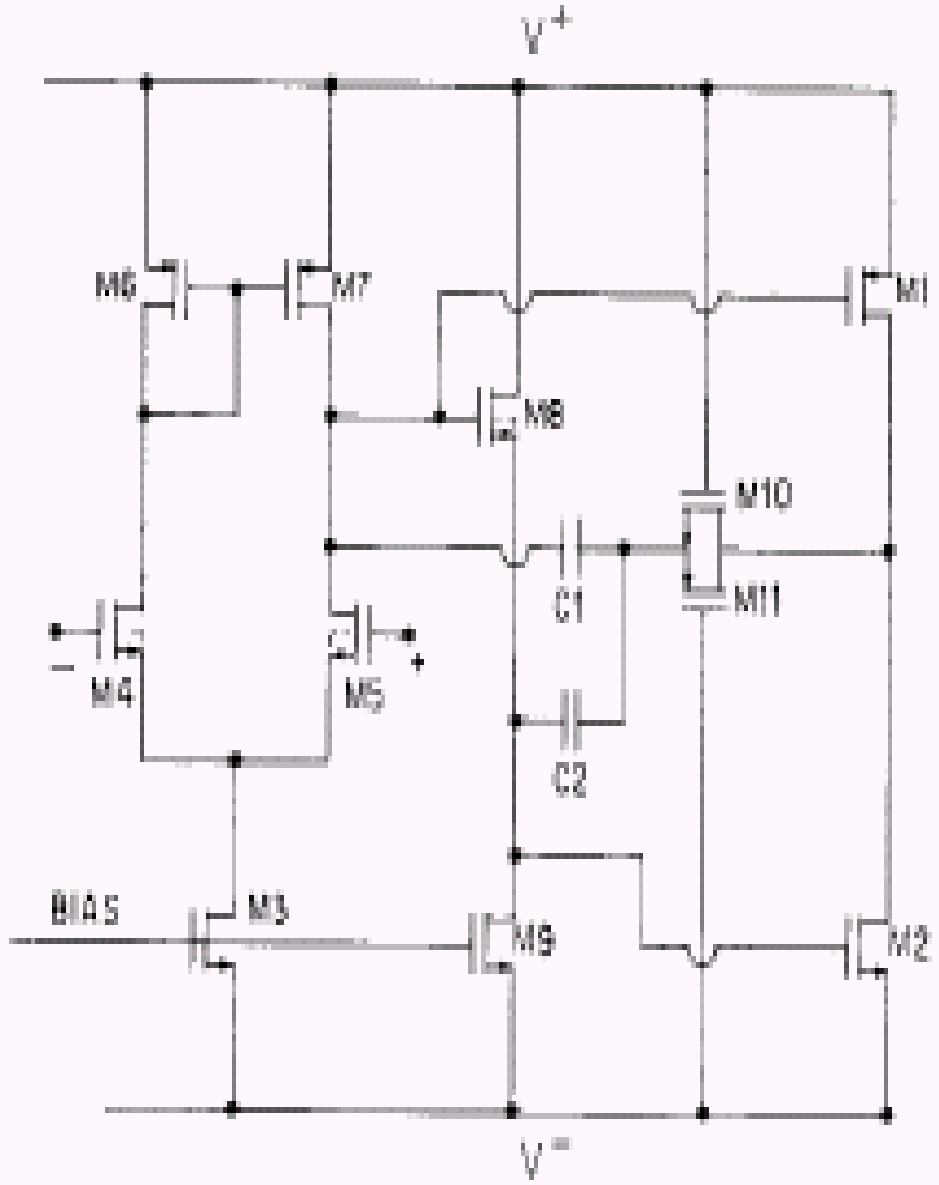
- Improved PSRR with slight increase in complexity, random offset and noise.

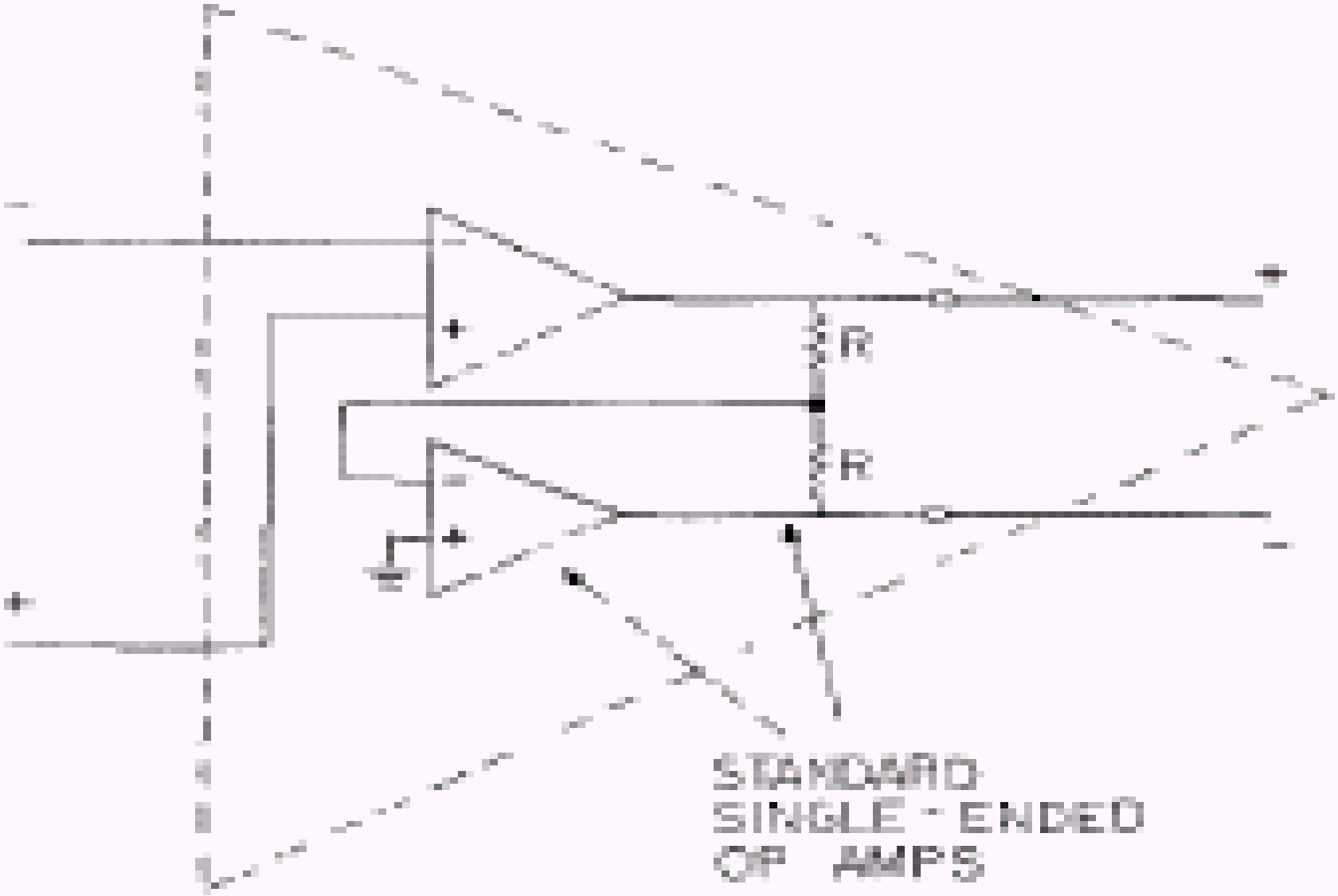
Class AB Amplifiers

- Most MOS analog circuits commercially produced utilize class AB circuitry in some form.
- Mainly used in output buffers.
- Used as internal amplifiers if minimization of chip power is the objective.
- Less power consumption and reduced cross over distortion is obtained using *Class* AB.

Class AB Amplifier

- Gate of M2 is connected to a level-shifted version of the stage input voltage.
- During positive half cycle M2 forces Vo to follow.
- During negative half cycle M1 conducts delivering the required current.
- M8 and M9 are level shifters.




R
R
STANDARD
SINGLE - ENDED
OP AMPS

Differential Output Amplifier

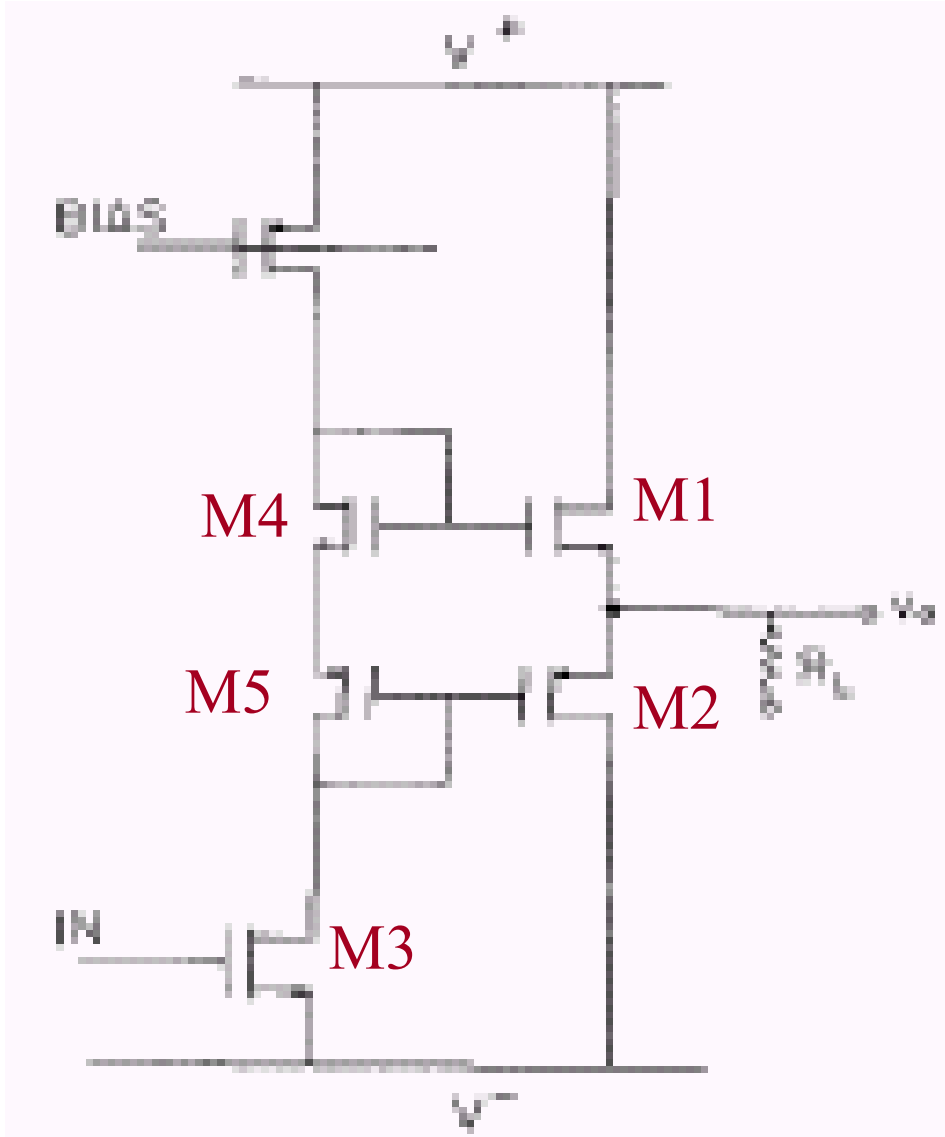
- Definition: Represent the signal by the difference between two inputs.
- It amplifies the difference between the two signal and rejects common components.
- Advantage: Provides a large output voltage swing.

Output Buffers

- Careabouts of an output stage :
- Large signal swing
- Avoid signal distortion
- Provide sufficient output power
- Have high Efficiency
- Provide protection from abnormal conditions

Complementary source follower CMOS output stage

- $V_{GS4} + V_{SG5} = V_{GS1} + V_{SG2}$
- M4 and M5 are biased by M3, $V_{GS4} + V_{SG5}$ is constant , which implies $V_{GS1} + V_{SG2}$ is constant.
- Drawback: Limitation in output voltage swing.



Summary

- Alternative architectures improve the performance and important parameters like voltage gain, PSRR and output resistance.
- However, it comes with the cost of increase complexity and noise.

References

- P.R. Gray and R.G. Meyer, " MOS Operational Amplifier Design- A Tutorial Overview," *IEEE Journal of Solid-State Circuits*, VOL.SC-17, NO. 6; pp. 969-982, December 1982.
- P.R. Gray and R.G. Meyer, Analysis and Design of Analog Integrated Circuits. New York: Wiley, 2001.
- Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design. New York: Oxford University Press, 2002.

Acknowledgements

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