SuperSpeed USB Developers Conference

Tokyo, Japan
May 20-21, 2009

USB 3.0 Architecture Overview

Bob Dunstan
USB 3.0 Technical Workgroup Chair
Intel Corporation

Agenda

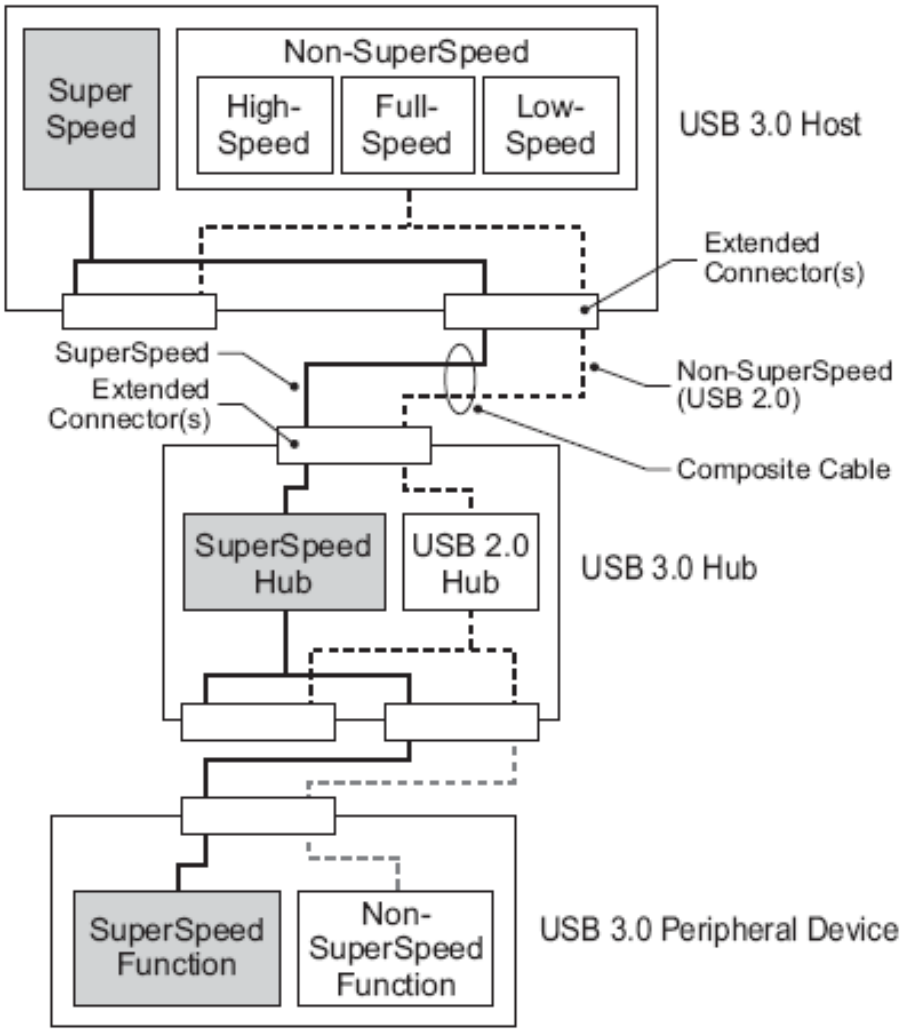
- What is SuperSpeed (USB 3.0)
- Connectors/cables
- Physical Layer
- Link Layer
- Protocol Layer
- Power Management
- Summary

USB 3.0 Features

- 10x performance increase over USB 2.0
- Backward compatible
  - Legacy devices continue to work when plugged into new host connector
  - New devices work when plugged in legacy systems albeit at USB 2.0 speeds
  - Existing class drivers continue to work
- Same USB Device Model
  - Pipe Model
  - USB Framework
  - Transfer types
- Power Efficient
  - Provides excellent power characteristics (especially for idle links)
    - Both on the device and the platform
  - Eliminate need for polling
- Extensible
  - Protocol designed to efficiently scale up

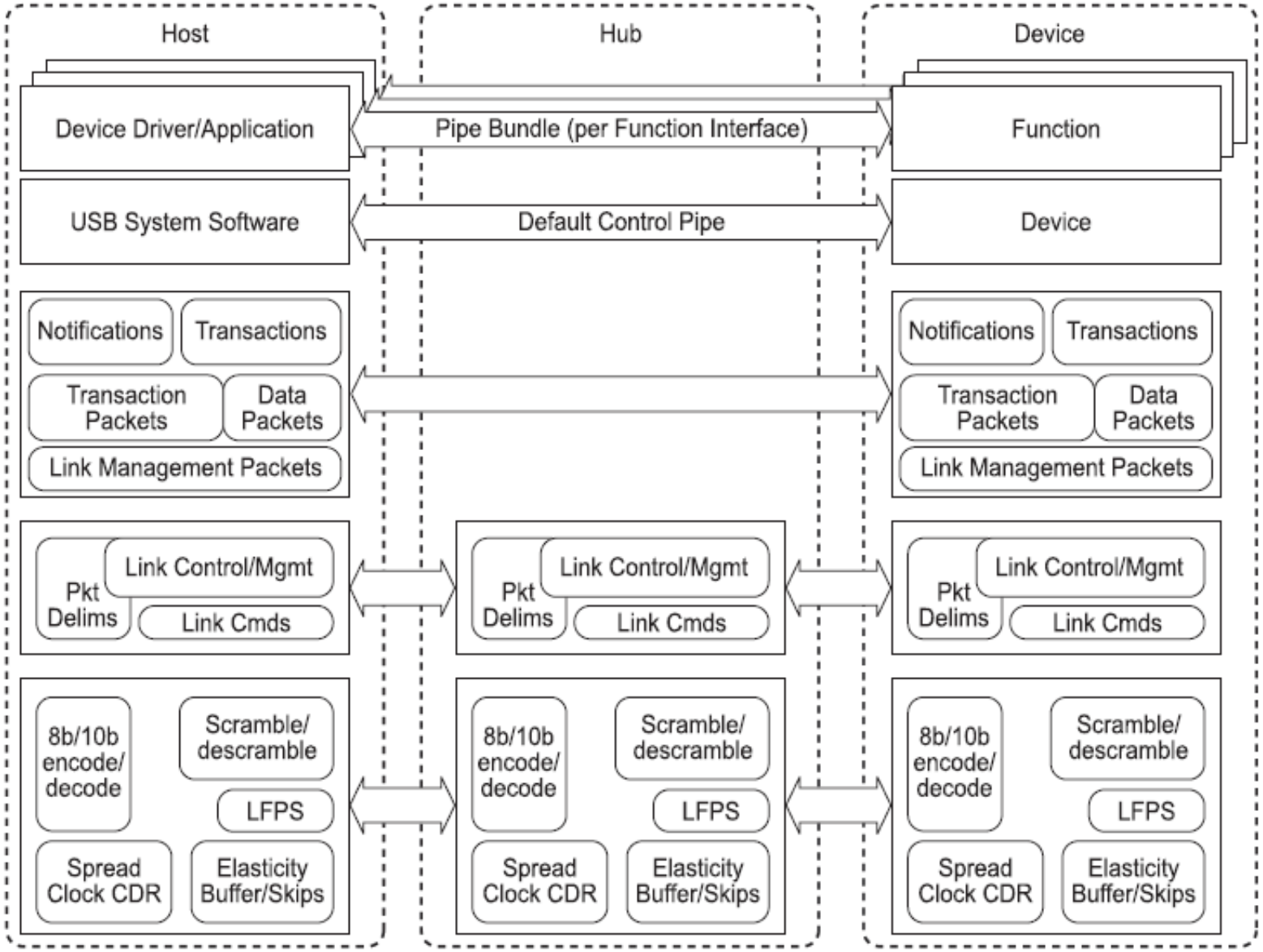
USB 3.0 Bus Architecture

- Dual-bus architecture SuperSpeed bus operates concurrently with USB 2.0
  - Electrically/mechanically backward & forward compatible
  - Devices discovered/configured at fastest signaling rate
  - Hubs provide additional connection points
- SuperSpeed USB
  - Dual simplex signaling
  - Packets routed to device
  - Hubs store and forward
  - Asynchronous notifications



Note: Simultaneous operation of SuperSpeed and non-SuperSpeed modes is not allowed for peripheral devices.

SuperSpeed Layered Architecture



USB 3.0 Connector & Cable Goals and Objectives

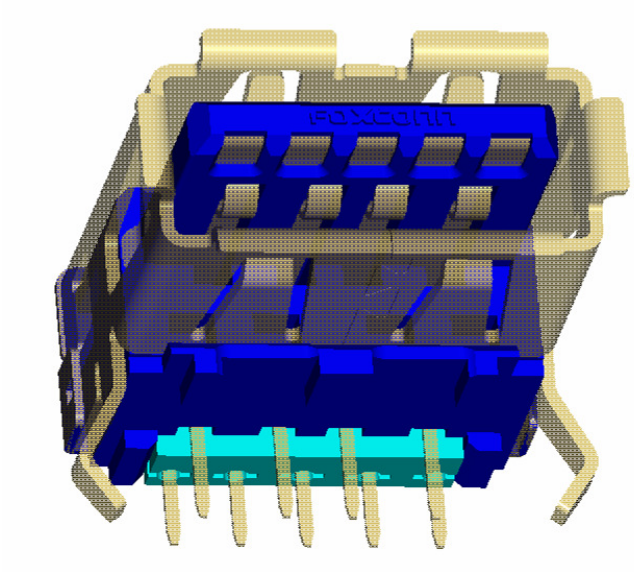
- Deliver low cost connectors and cable assemblies solutions to meet USB 3.0 architecture and performance needs
  - Support 5 Gbps data rate
  - Manage compatibility with USB 2.0
  - Minimize connector form factor variations
  - Contain EMI
  - Comprehend ease-of-use aspects

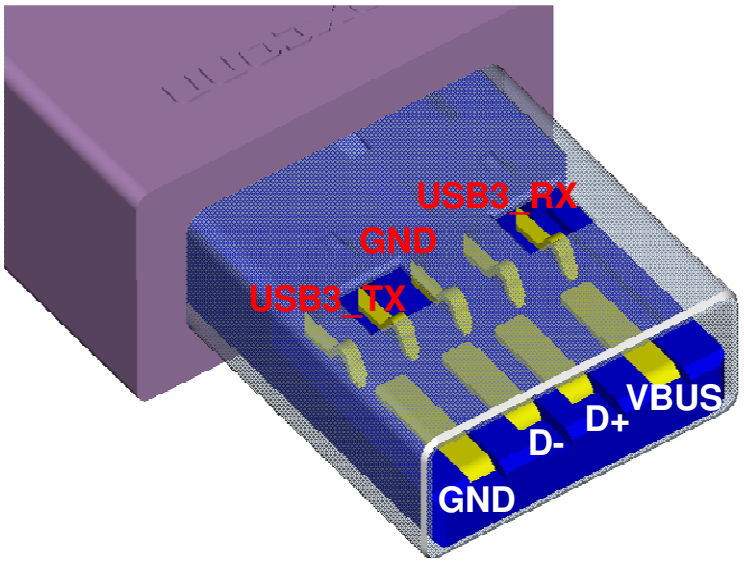
Connector Interoperability Summary

Receptacle	Plugs Accepted
USB 2.0 Standard-A	USB 2.0 Standard-A or USB 3.0 Standard-A
USB 3.0 Standard-A	USB 3.0 Standard-A or USB 2.0 Standard-A
USB 2.0 Standard-B	USB 2.0 Standard-B
USB 3.0 Standard-B	USB 3.0 Standard-B or USB 2.0 Standard-B
USB 3.0 Powered-B	USB 3.0 Powered-B, USB 3.0 Standard-B, or USB 2.0 Standard-B
USB 2.0 Micro-B	USB 2.0 Micro-B
USB 3.0 Micro-B	USB 3.0 Micro-B or USB 2.0 Micro-B
USB 2.0 Micro-AB	USB 2.0 Micro-B or USB 2.0 Micro-A
USB 3.0 Micro-AB	USB 3.0 Micro-B, USB 3.0 Micro-A, USB 2.0 Micro-B, or USB 2.0 Micro-A

USB 3.0 Standard-A Connector

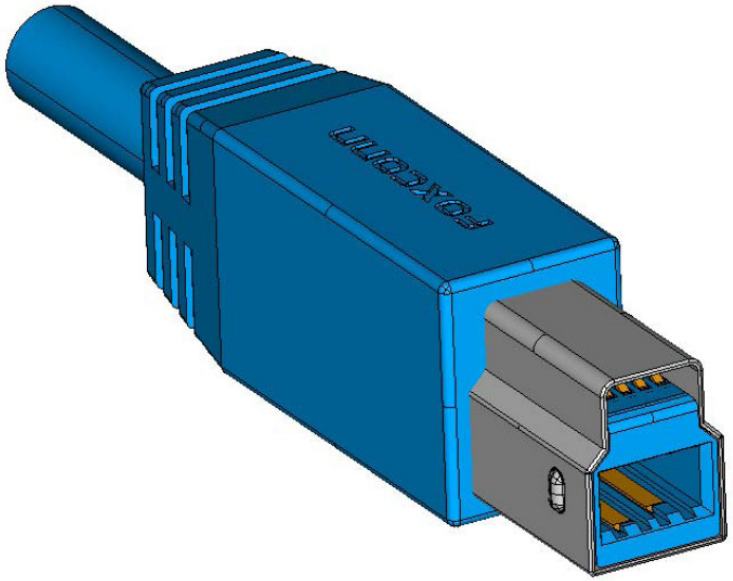
- Same interface as the USB 2.0 Standard-A connector, but with added pins for SuperSpeed USB signals
- Complete compatibility with USB 2.0 Standard-A connector
- Double-stacked connectors supported

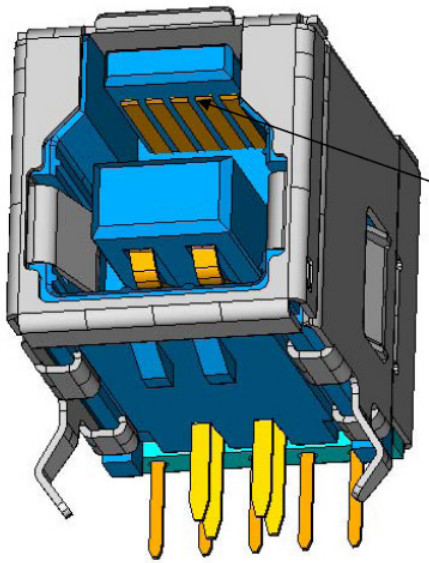




USB 3.0 Standard-B Connector

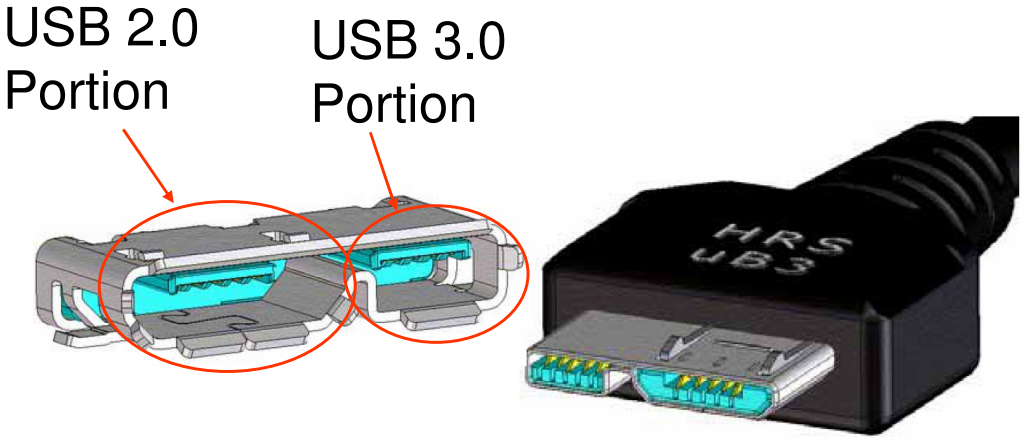
- Defined for relatively large, stationary peripherals such as hard drives and printers
- Visually different from USB 2.0 Standard-B connector
  - But the receptacle accepts a USB 2.0 Standard-B plug



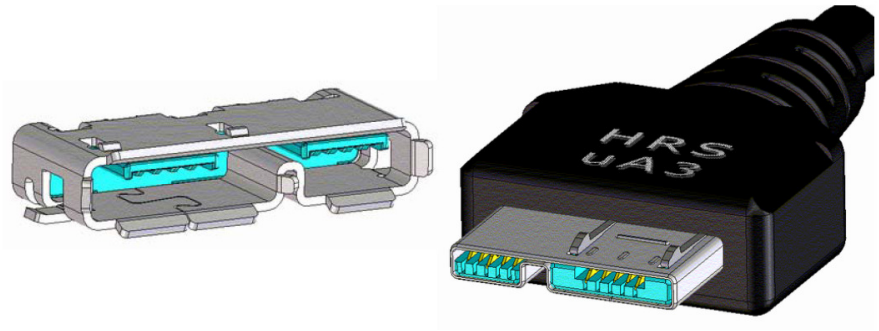


USB 3.0 Micro Connector Family

- Defined for hand held devices
- Backward compatible with USB 2.0 Micro connectors
- Based on USB 2.0 Micro-B connector with an extended portion for the SuperSpeed USB signals
- USB 3.0 Micro-A and –AB connectors are identical to USB 3.0 Micro-B connector except for different keying



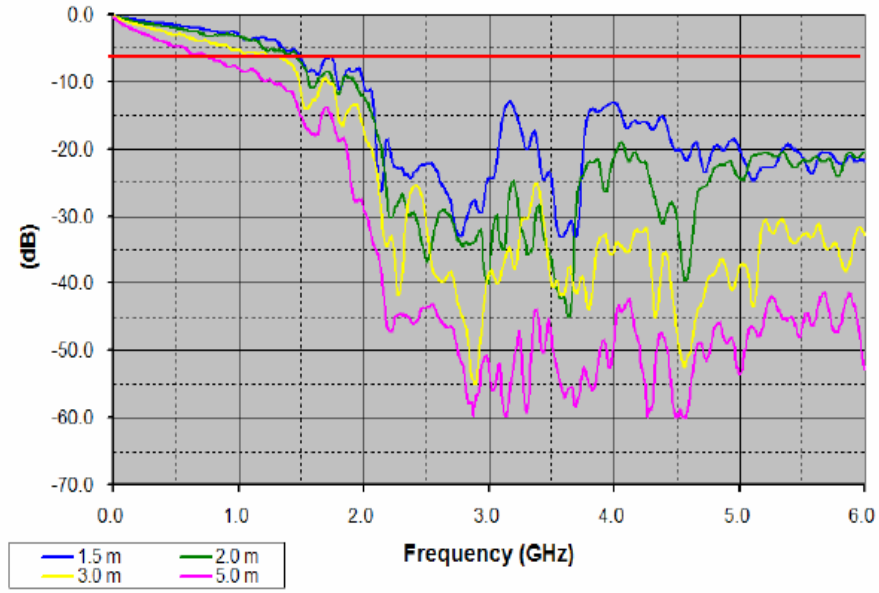
Micro-B

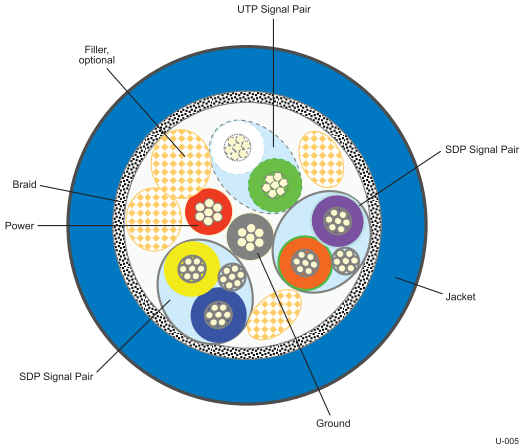


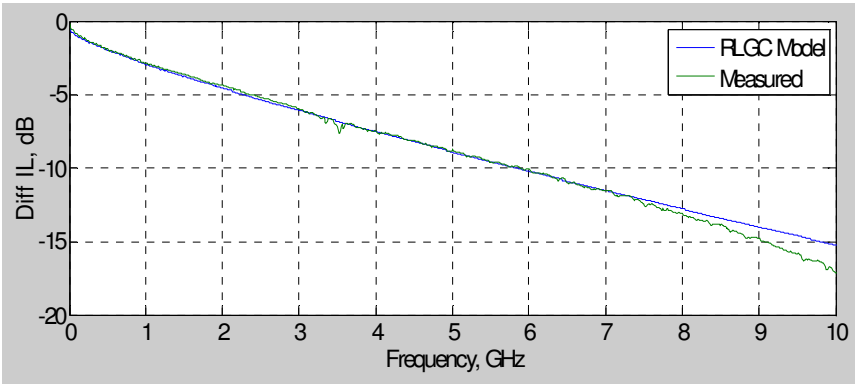
Micro-AB/A

Cables

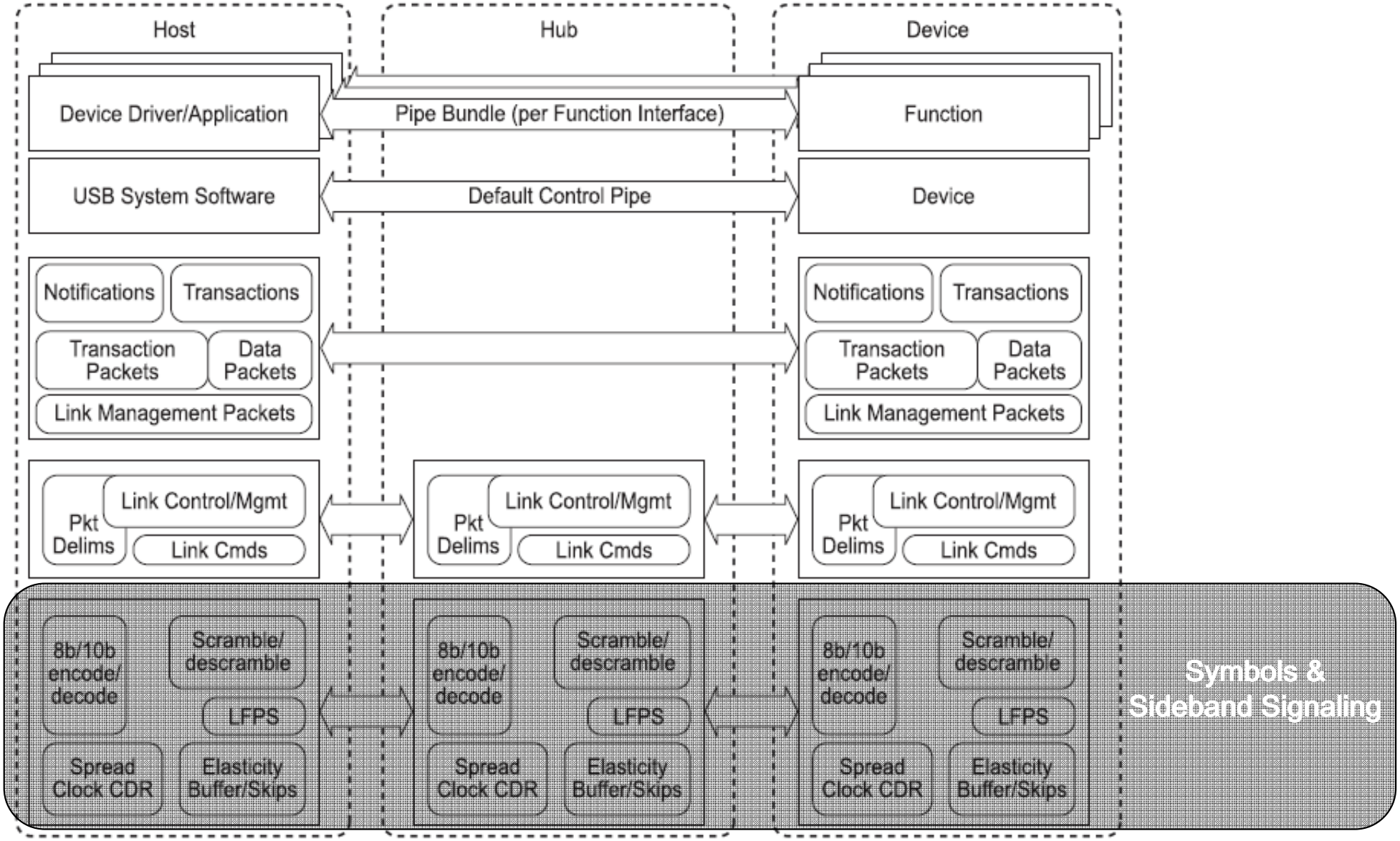
- Unshielded twisted pair (UTP) cable used for USB 2.0 cannot be used for SuperSpeed USB
- Shielded differential pair (SDP, twisted or twinax) is needed for SuperSpeed USB
  - Signal integrity and EMI containment







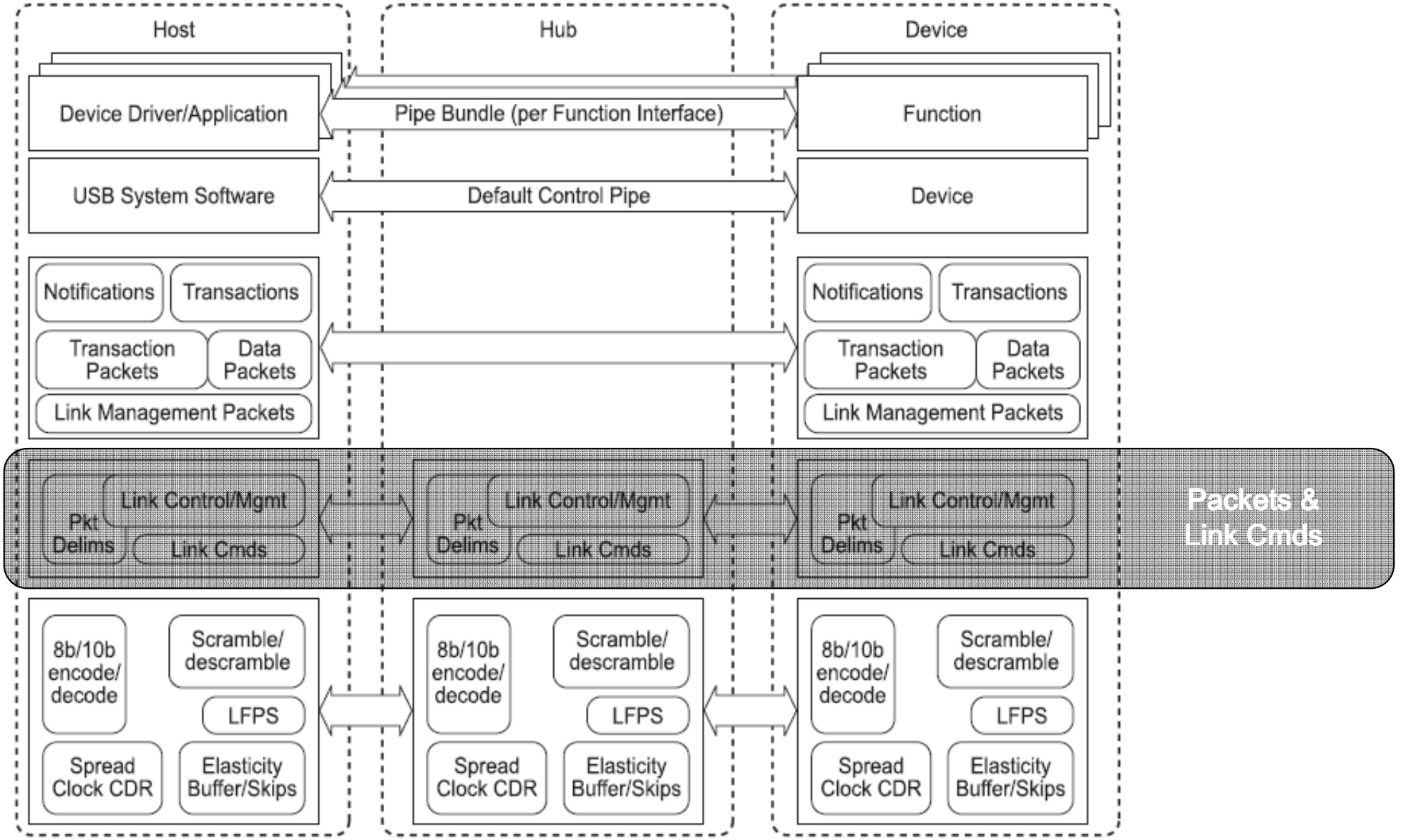
SuperSpeed Physical Layer



Physical Layer

- Support up to a 3 Meter cable
- Based on existing specs
  - Signaling similar to mix of high-speed serial buses (PCIe/SATA)
    - 2 differential pairs – dual simplex
  - Retain sideband functionality (e.g. reset, wake) without additional wires
    - Low Frequency Periodic Signaling (LFPS) – similar to PCIe beaconing
- Retain USB Hot Plug functionality
  - Rx termination for connect/disconnect detect

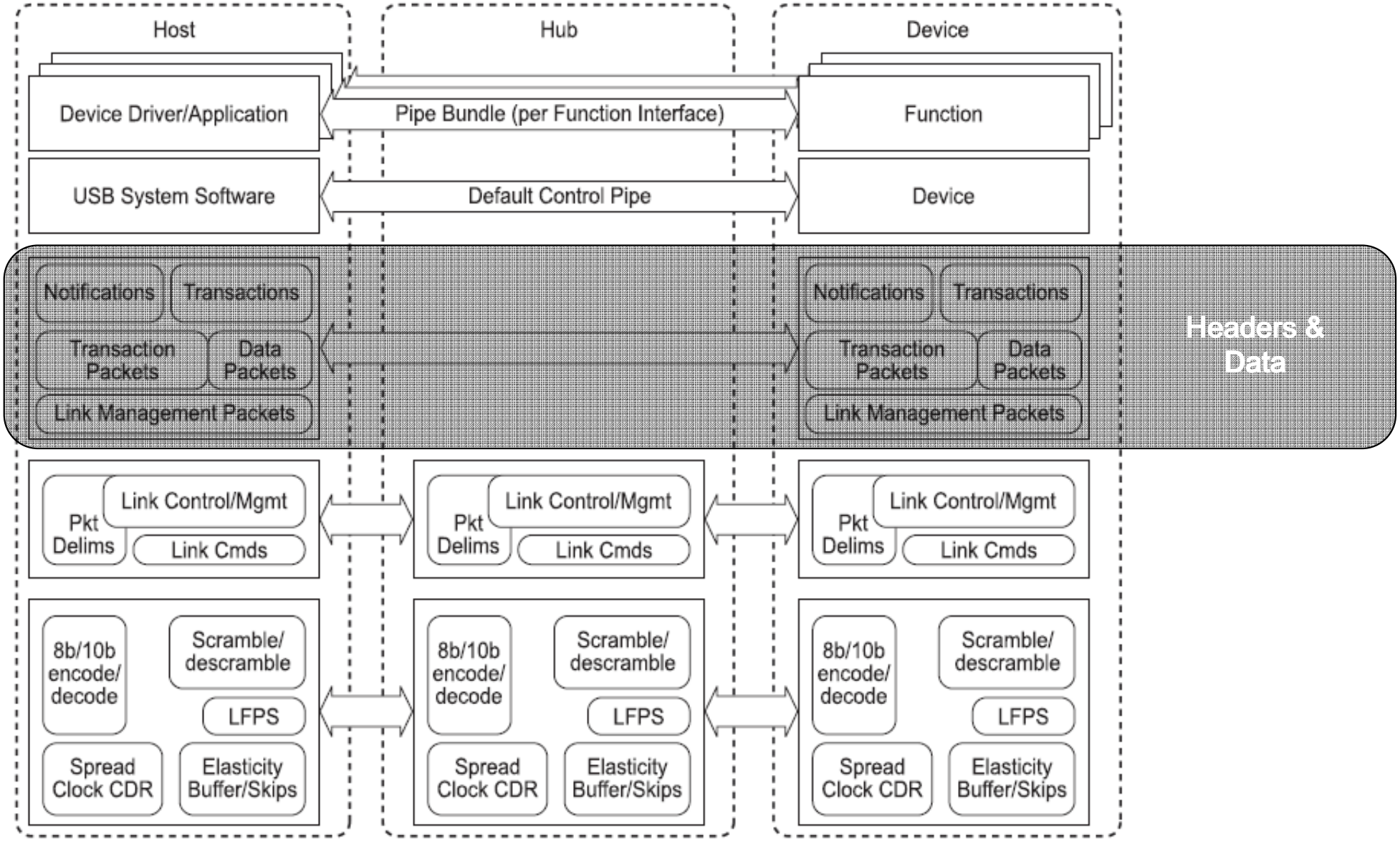
SuperSpeed Link Layer



Link Layer

- Robust & Reliable
  - Redundancy, advanced encoding techniques and retries
  - >10^{-20} undetectable error rate for link commands
- Effective Power Management
  - Four link power states
  - Either port can initiate link power state change
  - Low Frequency Periodic Signaling (LFPS)
- Link Commands
  - Link flow control
  - Link power state change
- Packets
  - Header Packets
    - Store and forward
    - Link level retries guarantee reliability
    - Contain information consumed by link or host or device
  - Data Packet
    - Compound packet contains header plus data payload

SuperSpeed Protocol Layer



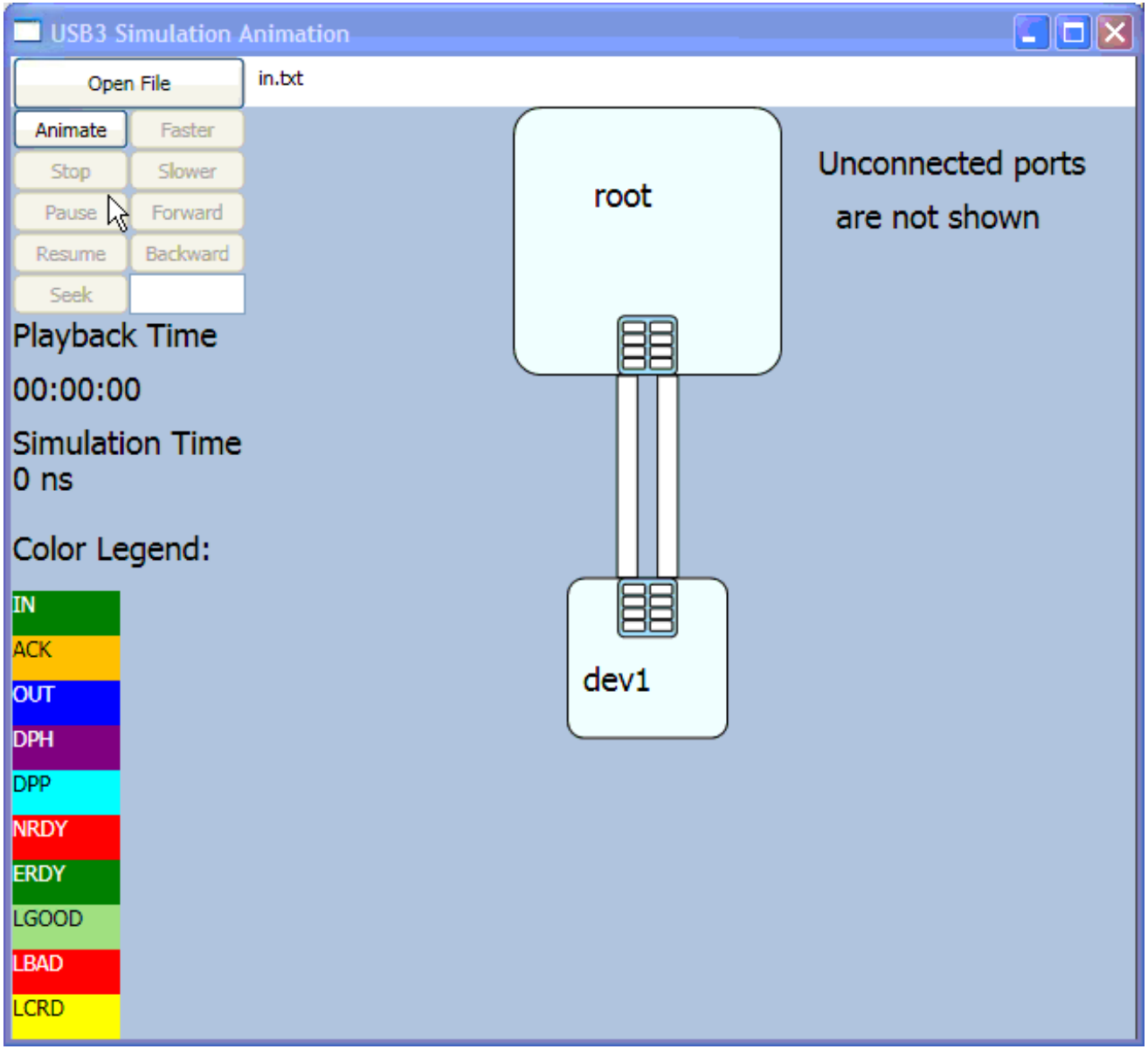
Protocol Layer

- Preserved legacy SW stack
  - USB 2.0 transfer types (bulk, control, interrupt, isochronous)
- Streams enhance bulk's capabilities
  - Multiple commands on a pipe
  - Out of order completion
- Optimized for good power management
  - Routable Packet Architecture
  - Asynchronous notifications
- Efficient use of bandwidth
  - Simultaneous IN / OUTs

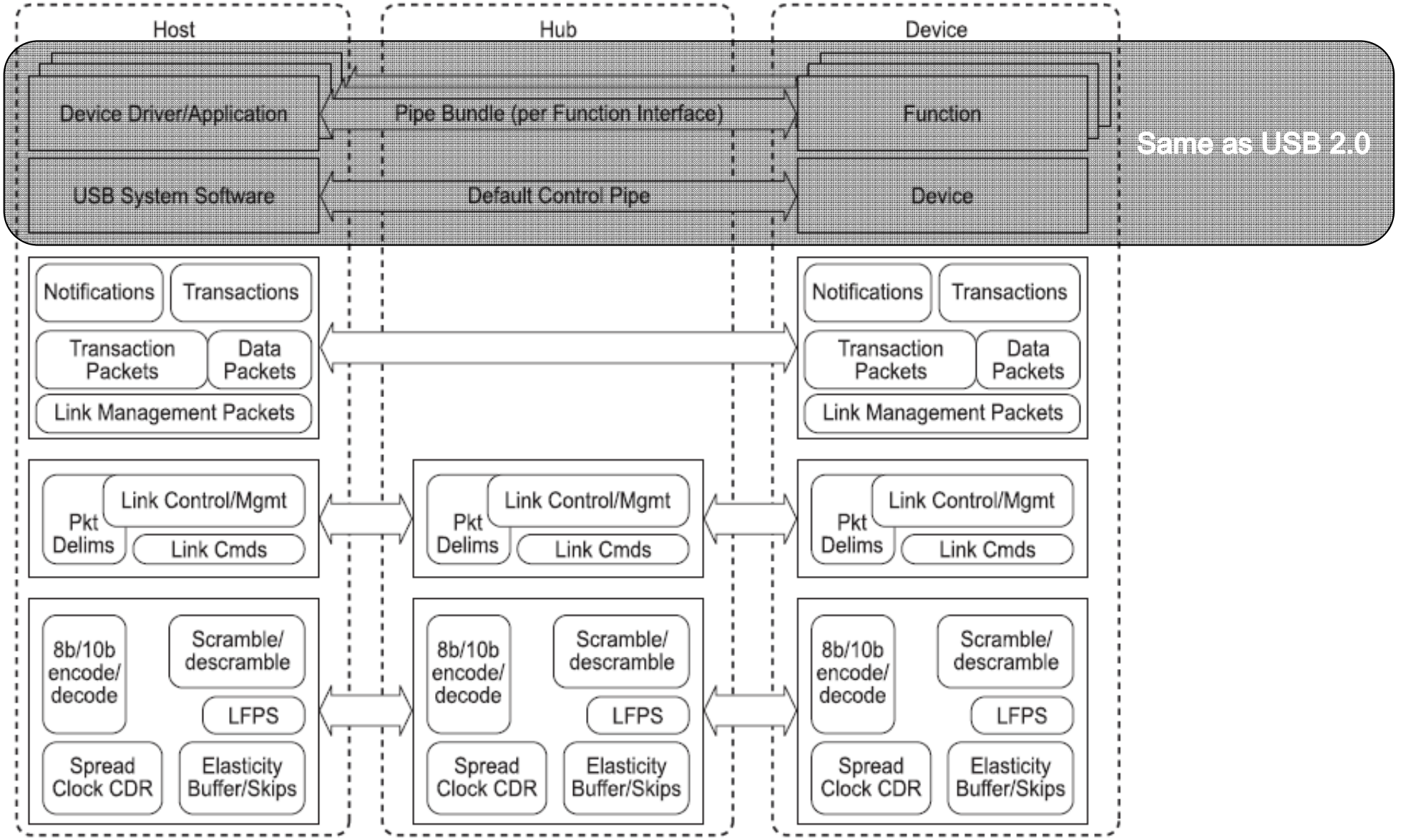
Packet Basics

- Header & Data Packets
  - Move between host and device
  - Address triple: device address, endpoint number, direction
  - Route String describes path between host and device
- Host initiates ALL data transfers
- Devices
  - Either respond immediately or defer the packet
  - Hubs proxy for target device by deferring packets routed to a downstream port whose link is not active
- Deferred requests restarted asynchronously
  - Device notifies host which responds with a new transfer request
- Bus active only when moving data

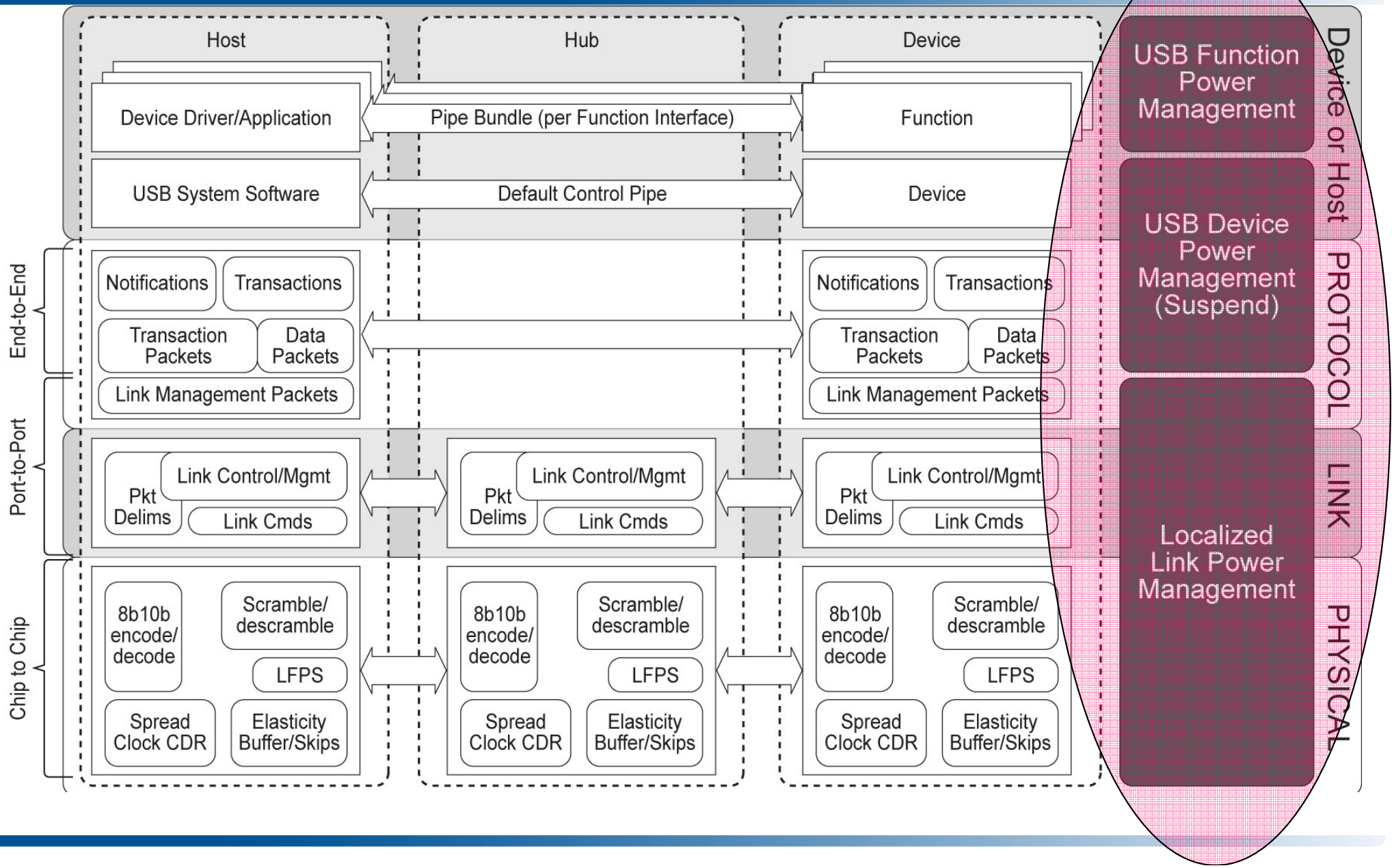
Example IN Transaction



SuperSpeed USB
Application Layer



Power Management Overview



Power Management Overview

- Power Management is at all levels
  - PHY layer, e.g. remote wakeup signaling
  - Link layer, e.g. low power link state entry & exit
  - Protocol layer, e.g. endpoint busy / ready notifications
  - Devices, e.g. function suspend
  - Hubs, e.g. “bubble up” link PM
  - Hosts, e.g. ping / ping response messaging
- Power efficiency at *system* level
  - Async endpoint busy / ready notifications – no polling
  - Packets routed, not broadcast
  - Low power link states entered automatically when idle

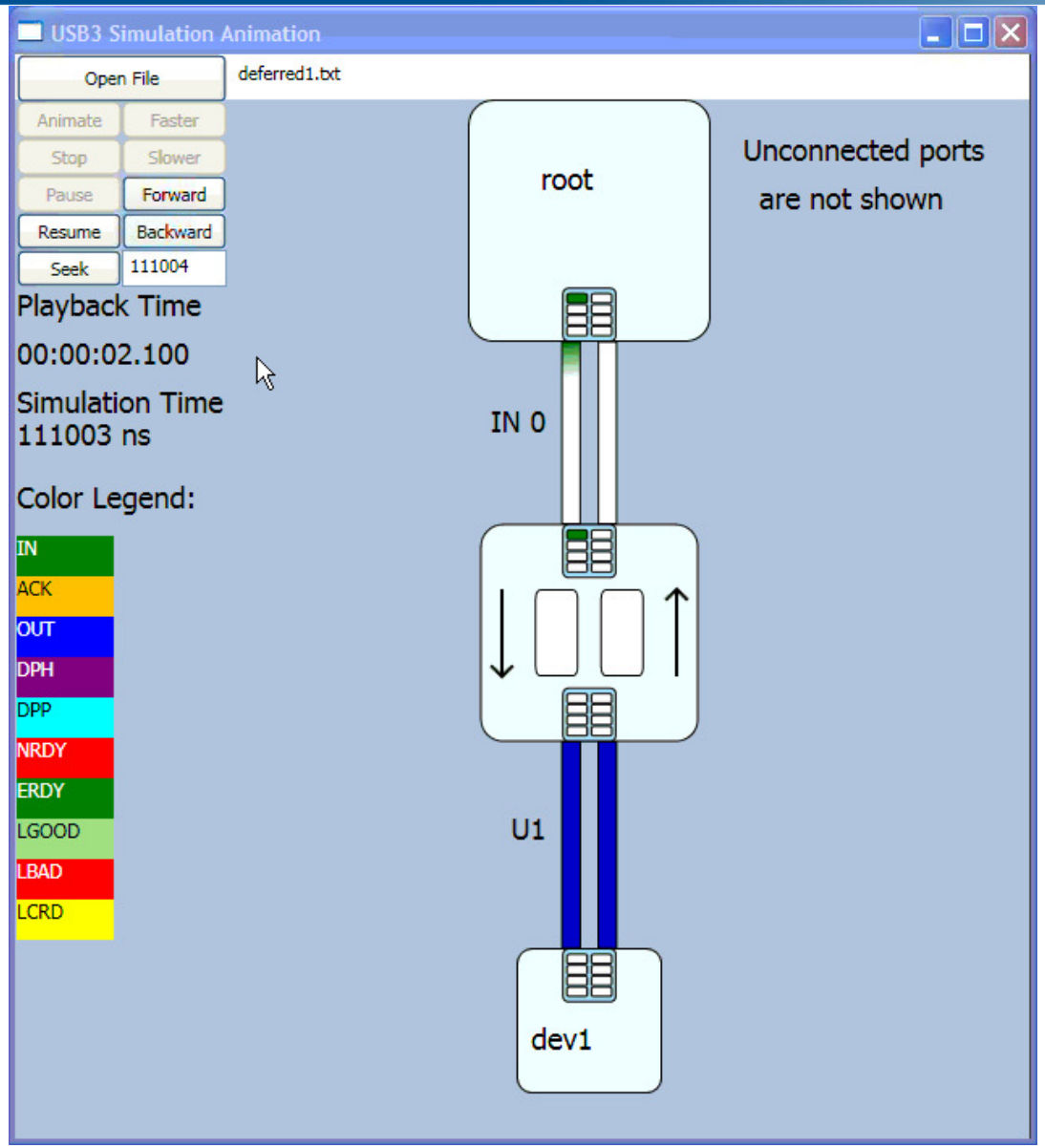
SuperSpeed USB
Power Management Primitives

- Physical Layer
  - Lower power per bit
  - Dual simplex - don't need to turn around the bus
  - Low Frequency Periodic Signaling
- Link Layer
  - Four Link States - trade lower power for increased latency
    - U0: operational, U1: link idle with fast exit (PLL remains on)
    - U2: link idle with slow exit (PLL may be off), U3: suspend
- Protocol Layer
  - Deferring & asynchronous device notifications
  - Packets Pending flag
  - Ping/Ping Response
  - Selective Suspend
  - Isochronous Timestamp packets
  - Latency Tolerance Message

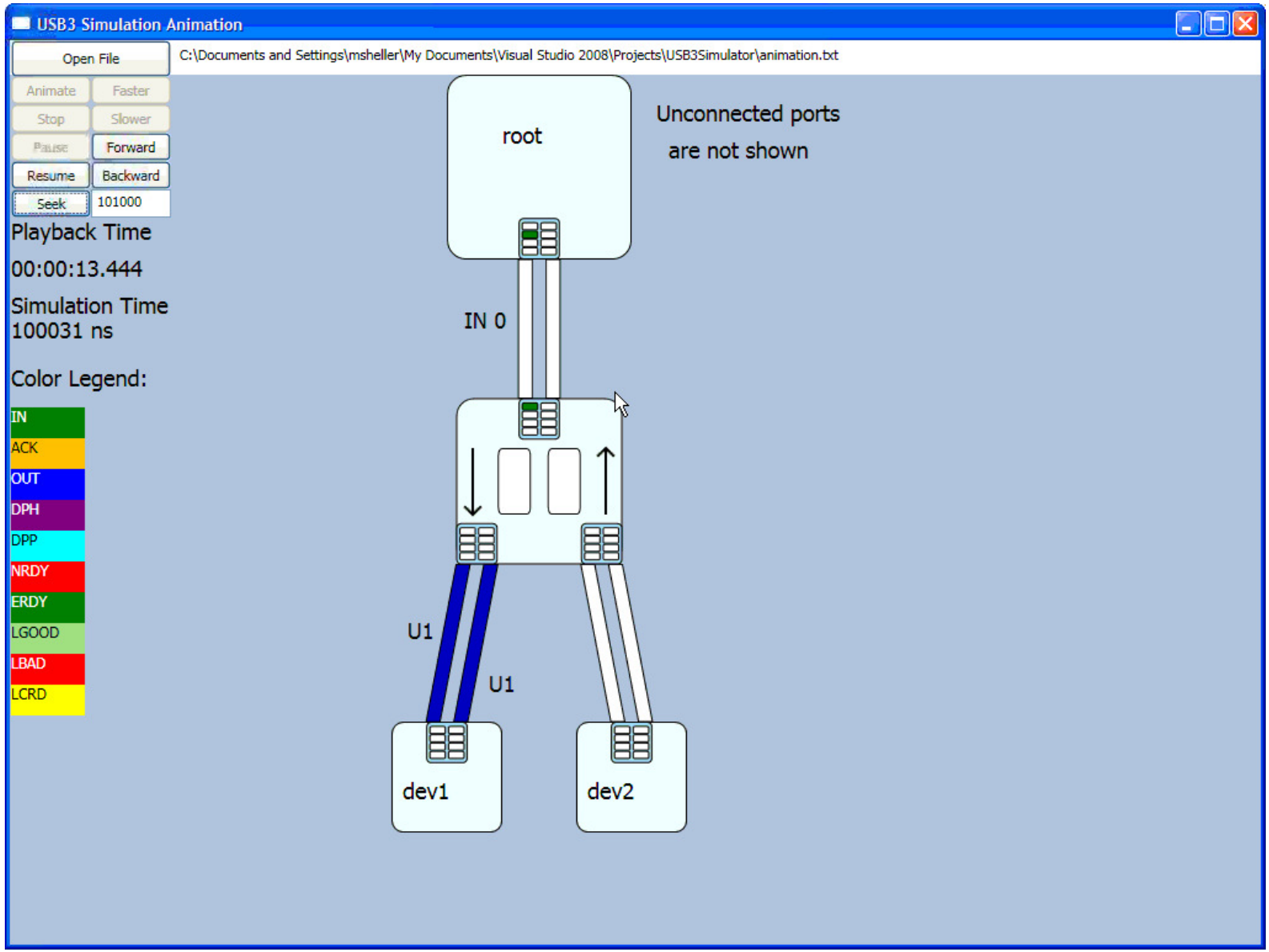
USB 3.0 SuperSpeed Hubs

- SuperSpeed hubs are more than port expanders
- Hubs central to SuperSpeed USB power management
  - A hub adjusts its upstream port link state based in its downstream ports' link state
  - A hub routes a downstream flowing packet only to the specified port
  - A hub defers packets directed to ports whose links are not in the active state
  - A hub has programmable inactivity timers on its downstream ports
  - A hub only forwards multicast timestamp packets to downstream ports whose link is active
  - A hub marks timestamp packets that are delayed

Simple Deferring Example



Deferring Balances Performance with Power Management



Host Support for Bus Power Management - Interrupt Endpoints

- Interrupt transfers must get completed within service interval
  - Devices may use U1 / U2
  - Host sends transfer far enough ahead of time to compensate for worst case link exit latency
- Host stops interrupt endpoint activity upon receipt of an NRDY
  - Resumes upon receipt of an ERDY
  - No polling – links can enter U1 / U2 when there is no activity

Host Support for Bus Power Management Isochronous Endpoints and Timestamp TPs

- Isochronous transfers must get completed within service interval
  - Devices want to use U1 / U2 for improved power efficiency
  - Devices must comprehend U1 / U2 exit latencies
- Ping / ping response messaging
  - Host sends a ping to isochronous device ahead of an isoch transfer
    - Gets all links in path to device back to U0 prior to transfer
  - Device responds with a ping response to host
    - Host then schedules isochronous transfer
    - Device keeps link in U0 until transfer occurs
  - Host can perform other transfers while waiting for ping response
- Timestamp packets sent at bus interval boundaries
  - Only sent on downstream ports in U0
  - U1 / U2 link inactivity timers ignore timestamp packets

Function Suspend and Device Suspend

- Function suspend
  - Individual functions* placed into *function* suspend independently
  - Controlled by FUNCTION_SUSPEND feature selector
- Device suspend
  - Device-wide state coupled to U3
    - Entered / exited intrinsically as a result of U3 entry / exit
      - SetPortFeature(PORT_LINK_STATE U3)
  - Device suspend entered regardless of function suspend state
- Selective suspend also supported
  - System software may initiate device suspend when all of a device's functions are in function suspend

* Composite devices contain multiple functions

SuperSpeed USB Power Management

- Fine grain power management controlled by devices
  - Devices control their own link state
    - Host provides ‘packets pending transfer’ information to device
    - When no transfers are pending, devices can put their link into a reduced power management state
  - Hubs play key role
    - Propagate link state upwards
    - Forward packets only to the link in the direct path
    - Forward Isochronous Timestamp packets only to active links and do not effect inactivity timers
- Default power management policy
  - Systems set by inactivity timers in downstream ports

System Level Power Management Latency Tolerance Messaging

- LTM enables system to enter deeper power saving states with cooperation of devices
- Devices report the latency they can tolerate from the system in response to a request
  - Send host LTM notification packet with latency value
- Allows system to enter deeper sleep states when devices in system can tolerate it

Summary

- Physical layer is based on existing industry specs
- Maintained backwards compatibility
  - Cabling/connector
    - Standard A receptacles backward compatible with USB 2.0
    - New B and Micro AB receptacles backward compatible with USB 2.0
  - Devices – USB 2.0 support remains
  - Software – Existing device drivers just work
  - Hubs support both USB 2.0 & SuperSpeed devices
- Link and Protocol optimized for Power Management
  - U0-U3 link states
  - Devices drive own link state, hubs propagate up
  - Deferring and asynchronous notifications maximize opportunities for PM
  - Hub inactivity timers provide coarser, but effective default PM

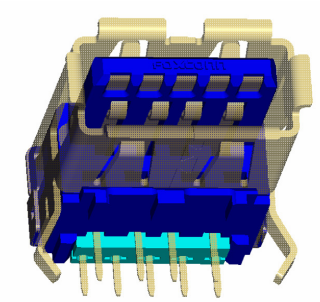
Call to Action

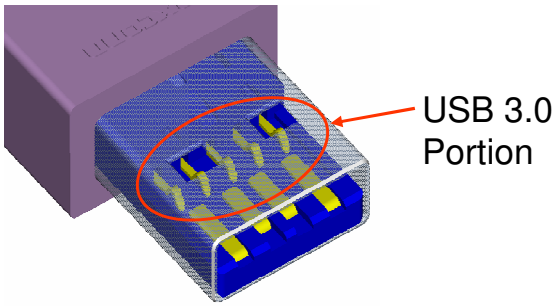
- Download & Review USB 3.0 Material
  - USB 3.0 Version 1.0 Specification
  - Referenced documents
  - Pipe Spec (www.developers.intel.com)
- Tell us about your product plans

Backup

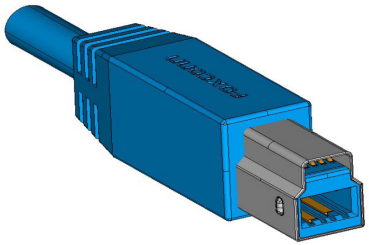
USB 3.0 Connector & Cable

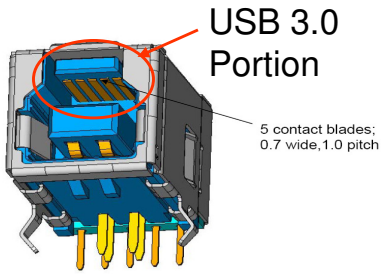
- Std A - Same interface as USB 2.0 Standard-A connector, but with added pins for USB 3.0 Super-Speed signals
- Complete compatibility with USB 2.0 Standard-A connector



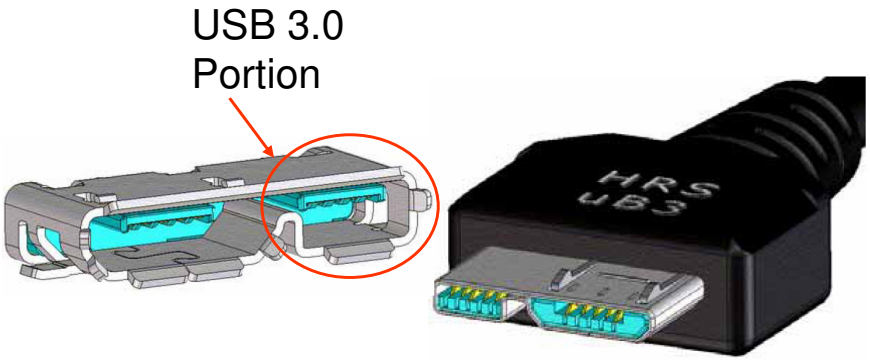


- Std B - Defined for relatively large, stationary peripherals such as hard drives and printers
- Powered version variant is a defined
- Visually different from USB 2.0 Standard-B connector



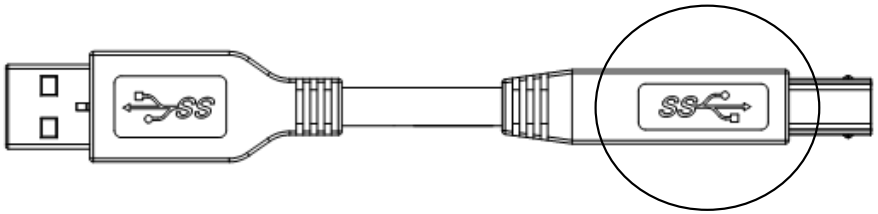


- Micro B - Based on the proven USB 2.0 Micro-B connector design with an extended portion for the Super-Speed signals
- USB 3.0 Micro-A and –AB connectors are identical to USB 3.0 Micro-B connector except for keying/profile differences



Defined Cable Assemblies

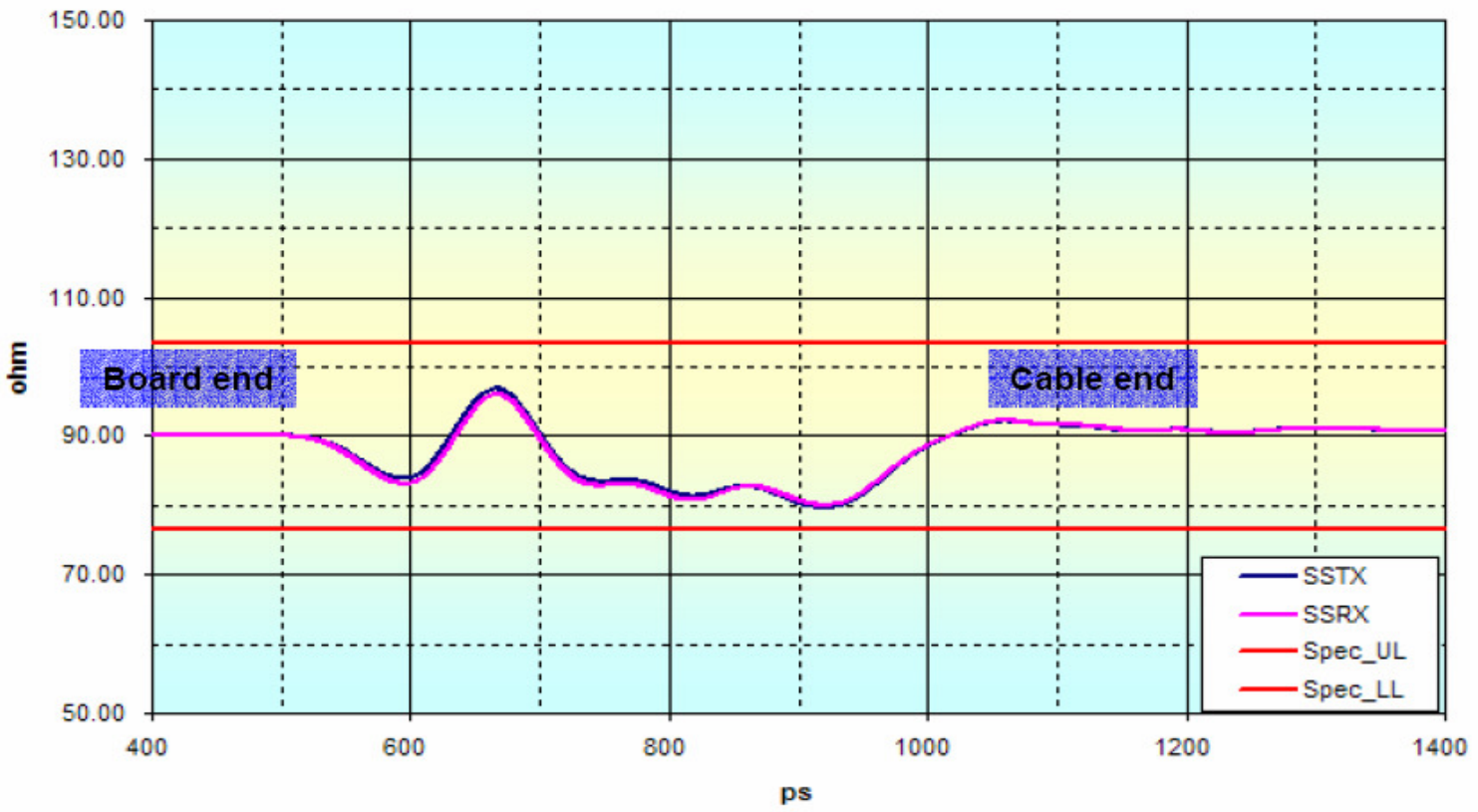
- Compliance cable assemblies:
  - USB 3.0 Standard-A plug to USB 3.0 Standard-B plug
  - USB 3.0 Standard-A plug to USB 3.0 Micro-B plug
  - USB 3.0 Standard-A plug to USB 3.0 Standard-A plug
  - USB 3.0 Micro-A plug to USB 3.0 Micro-B plug
  - USB 3.0 Micro-A plug to USB 3.0 Standard-B plug
  - Captive cable with USB 3.0 Standard-A plug
  - Permanently attached cable with USB 3.0 Micro-A plug
  - Permanently attached cable with USB 3.0 Powered-B plug



TDR of Mated Connectors

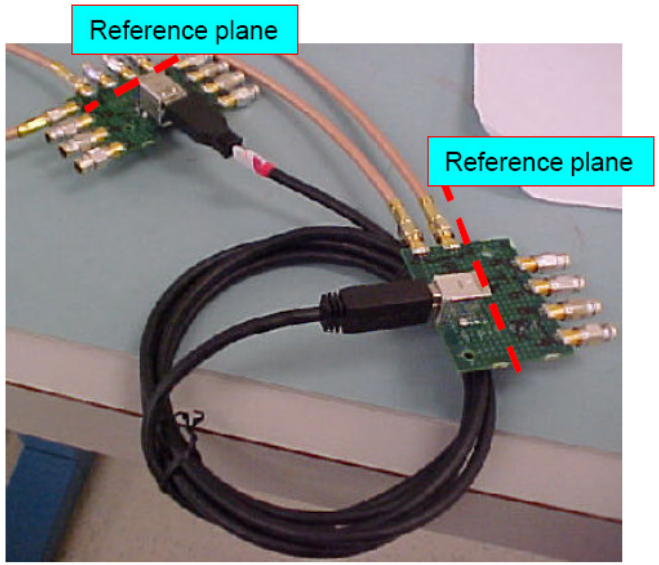
- TDR with a 50 ps (20-80%) rise time
  - 90+/-15 ohms- required for all USB 3.0 mated connectors

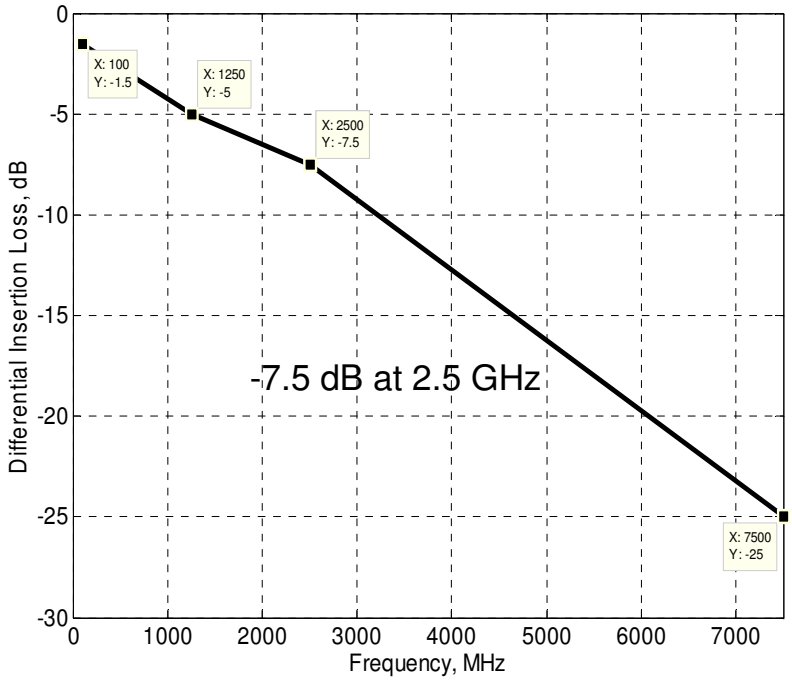
Example: USB 3.0 Standard-B Mated Connector

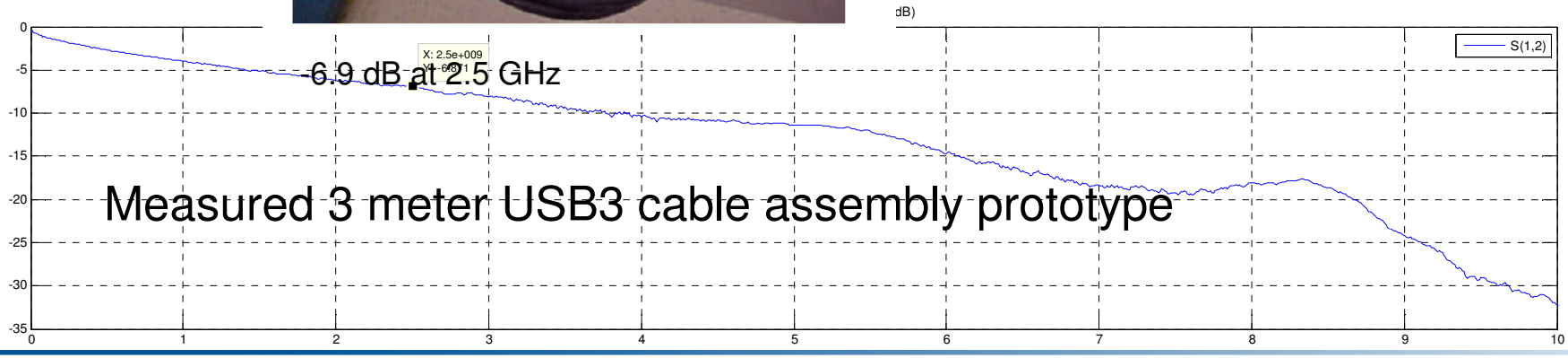


Cable Assembly – SDD21

- Differential insertion loss is a key requirement
  - Supports 3 meter long cable assembly
    - With 26 AWG wire



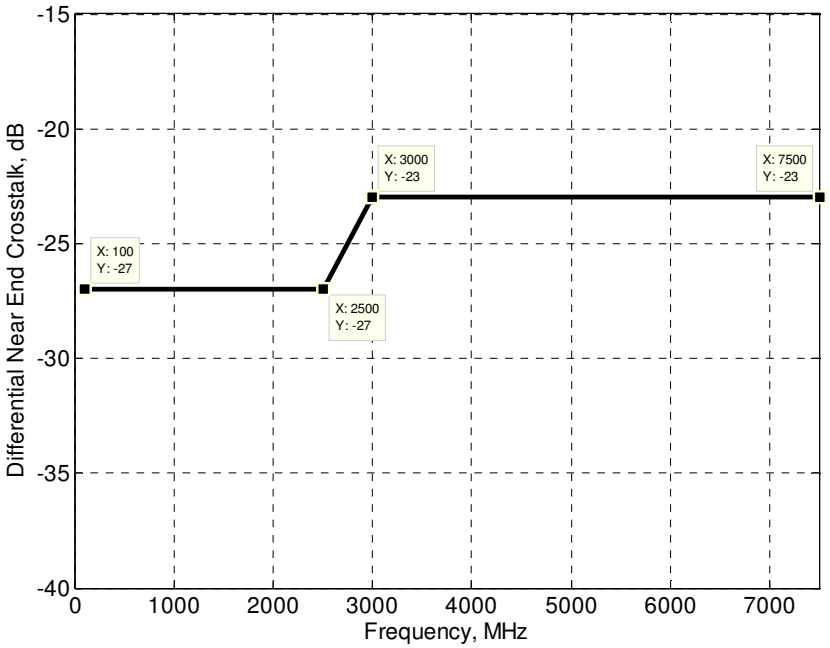


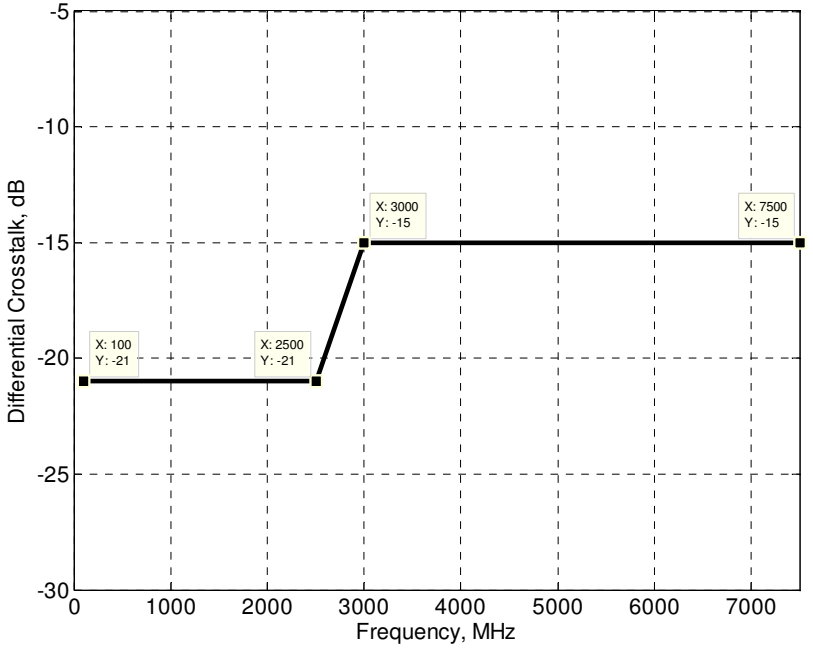


Measured 3 meter USB3 cable assembly prototype

Cable Assembly - Crosstalk

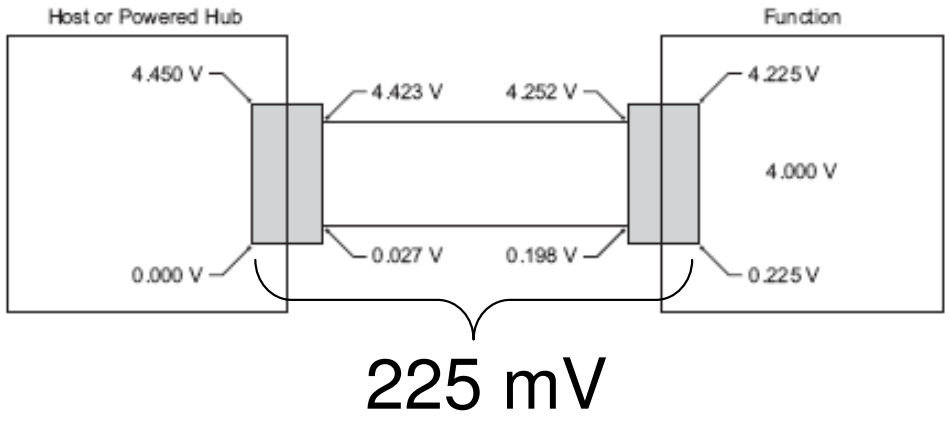
- Differential NEXT is specified for USB3-to-USB3 pairs
- Differential NEXT and FEXT are specified for USB2-to-USB3 pairs
  - Due to the internal construction of the USB 3.0 Standard-A connector, we have to tolerate a quite large crosstalk between USB 3.0 and USB 2.0 pairs
    - This is a problem only when USB 2.0 and USB 3.0 signals are running simultaneously (only allowed for hubs)





Key Mechanical Requirements

- Durability
  - Micro family: 10,000 cycles
  - All other connectors
    - Standard durability class: 1500 cycles
    - High durability class: 5000 cycles
- Unmating force
  - 10N min initial, 8N min EOL
- 4-Axis continuity
  - Required for Micro connector family
- Mated cable Assembly voltage drop (Vbus and GND, respectively)
  - 225mV max with a 900mA current



Attention Required

- Great attention must be paid to electrical design details to minimize TDR Impedance mismatch, crosstalk between SuperSpeed USB pairs and crosstalk between SuperSpeed USB and D+/D- pairs
  - The cable termination management is particularly important
- Unintended shorting in Standard-A connectors between pins during insertion/extraction must be avoided
  - USB 3.0 plug with USB 2.0 receptacle
  - USB 2.0 plug with USB 3.0 receptacle
- Exposed contact (to human fingers) is not allowed
- Appropriate (friction) latch design is important to connection robustness