Space Radiation Effects in Advanced Flash Memories†

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I. INTRODUCTION

Memory storage requirements in space systems have steadily increased, much like storage requirements in terrestrial systems. Large arrays of dynamic memories (DRAMs) have been used in solid-state recorders, relying on a combination of shielding and error-detection-and correction (EDAC) to overcome the extreme sensitivity of DRAMs to space radiation. For example, a 2-Gbit memory (with 4-Mb DRAMs) used on the Clementine mission functioned perfectly during its moon mapping mission, in spite of an average of 71 memory bit flips per day from heavy ions.

Although EDAC worked well with older types of memory circuits, newer DRAMs use extremely complex internal architectures which has made it increasingly difficult to implement EDAC. Some newer DRAMs have also exhibited catastrophic latchup.

Flash memories are an intriguing alternative to DRAMs because of their nonvolatile storage and extremely high storage density, particularly for applications where writing is done relatively infrequently. This paper discusses radiation effects in advanced flash memories, including general observations on scaling and architecture as well as the specific experience obtained at the Jet Propulsion Laboratory in evaluating high-density flash memories for use on the NASA mission to Europa, one of Jupiter's moons. This particular mission must pass through the Jovian radiation belts, which imposes a very demanding radiation requirement.

The natural space radiation environment can affect flash memories in four basic ways:

(1) Macroscopic ionization damage from the interaction of many electrons and protons, producing a buildup of charge in gate and isolation oxides;

(2) Transient effects from the interaction of a single galactic cosmic ray or high-energy proton, causing upsets in the state machine, buffer or other digital regions of the flash memory (this is analogous to upset effects from alpha particles, but the particles in space produce far more intense track densities);

(3) Microscopic *ionization* damage from the charge produced by a single cosmic-ray heavy-ion in the gate region; and

(4) Microscopic *catastrophic* damage from high energy protons or galactic cosmic ray particles which can permanently increase the leakage current of the floating gate.

The first two mechanisms have been observed in older flash memory technologies [1-3], as well as in conventional memories and CMOS integrated circuits. Evidence for the last two mechanisms has been seen in evaluations of other memory technologies (particularly DRAMs), but they have not been examined in detail for flash memories

II. FLASH TECHNOLOGY EVOLUTION

Flash memory applications can be divided into two basic categories: *code storage*, which requires fast, random access to all memory locations; and *file storage*, which mainly requires access to sequential data. Code storage flash memories usually use NOR architecture, with independent read access for each internal storage location. The cell size of a conventional NOR flash cell with LOCOS isolation is ≈ 10-11 F^2, where F is the feature size of the technology. Modern NOR flash devices use multi-level storage (storing 3 different levels within each cell and providing 2 binary bits) in order to improve the effective storage density. This decreases the effective cell size to approximately $6F^2$, taking into account the requirement for additional circuitry. Multi-level storage reduces the margin between the threshold voltage of the various levels in the floating gate, and also requires a more sophisticated readout technology that can recognize the different charge levels within the floating gates.

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File storage flash memories use NAND architecture, which stacks n cells together to form a NAND logic array that can only be accessed sequentially. Sixteen or 32 cells are typically used, along with two control transistors [4]. The basic NAND cell occupies only about 50% of the area of a corresponding NOR cell (without considering multi-level storage) because the NAND cell does not require separate access to the source and drain regions of individual transistors in the NAND memory stack.

Scaling in both technologies is limited by the requirement for relatively high voltages for erase and write functions (12-20 V). An internal charge pump is nearly always used to provide those voltages. Special transistors with thicker gate oxides are required within the charge pump as well as in the control logic for writing and erasing.

NOR flash memories have been produced with multi-level storage since 1998. Currently 64-Mb devices are available, fabricated with a 0.25 µm process, and higher density devices are in development using a process with a feature size of 0.18 µm [5].

NAND flash memory trends are shown in Figure 1, adapted from Coi, et al. [6]. There are two "steps" in cell size trends that have reduced the cell size. The first is due to shallow trench isolation in 1998; the second is due to the anticipated use of multi-level cell technologies by mid-2001. NOR cell sizes are shown for comparison. Multi-level cell technology was introduced in the NOR technology in 1999. Dashed lines in the figure show anticipated trends during the next year.

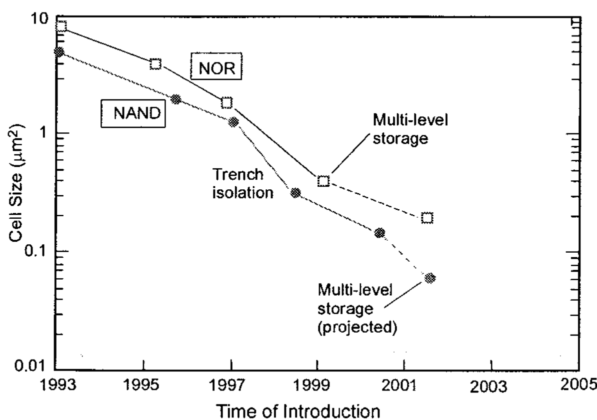

Figure 1. NAND flash memory evolution. The effective cell size decreases by a factor of four when multi-level cell structures are introduced. NOR flash trends are shown for general comparison

III. Global Ionization Damage

A. Basic Issues

Ionization from high-energy electrons and protons in space produces electron-hole pairs within gate and isolation oxides of MOS devices. Some of the excess charge is trapped at the interface region, changing the threshold voltage of the transistor. For basic MOS transistors the shift in threshold voltage scales with the square of the oxide thickness [7], which has generally reduced the importance of total dose damage in highly scaled devices.

Although this same scaling scenario applies to flash memories, the internal transistors used for the charge pump and erase/write control have much thicker oxides because of the requirement for high voltage. This causes flash devices to be considerably more sensitive to total dose damage compared to other ULSI technologies. It also implies that write and erase functions will be the first parameters to fail from total dose.

Figure 2 shows the results of probe measurements of the internal charge pump for a 128-Mb NAND flash device. The charge pump voltage starts to degrade at about 6 krad(Si), and falls rapidly at higher levels. At about 8 krad(Si) the device can no longer be erased. The shaded region in the figure shows the range of failure levels for different units from the same group of devices.

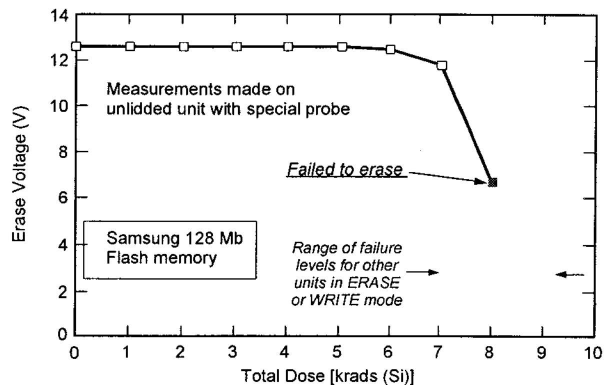

Figure 2. Degradation of the internal charge pump of a 128-Mb NAND flash memory after irradiation with gamma rays.

The gate oxide thickness of high-voltage transistors in this device is nominally 200 A. At 8 krad(Si), the shift in threshold voltage is about 70 mV, assuming 50% hole trapping.

Flash memories will work at much higher radiation levels in the read mode. Figure 3 shows test results for an older NOR flash device that compares functional operation for biased and unbiased devices (charge trapping is reduced when no electric field is applied during exposure). When

the device is biased, field oxide inversion causes a highly nonlinear increase in power supply current at about 20 krad(Si).

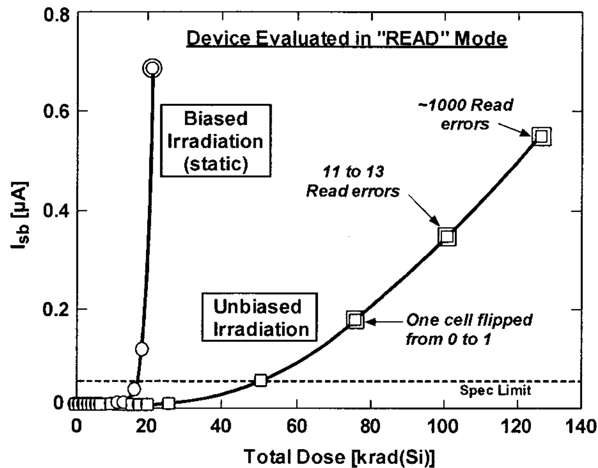

Figure 3. Effect of ionizing radiation on read mode operation of a 16-Mb NOR flash memory. The large increase in power supply current at low total dose levels is due to inversion of the LOCOS field oxide structure.

Trench isolation is used in more advanced flash devices. Similar isolation leakage effects can occur in trench isolation structures. Processing details play a large role in determining their sensitivity to radiation damage.

IV. Single-Event Upset Effects

A. Basic Issues

Single-event upset sensitivity of flash memories is highly dependent upon the operating mode. If an ion strike causes the internal state machine to be altered, then the device will no longer work properly. This type of functional error is very difficult to categorize because of the limited information on the state machine that can be inferred from external pins. Read, write and erase functions can all be affected. In addition to the state machine, errors can also be introduced into buffers or other active internal memory regions.

Although many different operating conditions can be used for radiation testing, most tests are done with the device in the read mode after a specific pattern is loaded (this assumes that write operations are done infrequently, and that the probability of an ion strike hitting a sensitive node during write or erase operations is small). After the device is exposed to a flux of ions, the memory contents are read out to see if the data has been altered or if the device will still operate without being shut down and reinitialized.

B. Representative Test Results (Static Mode)

Tests on 16-Mb NAND flash technology with the device in a static mode during irradiation are shown in Figure 4. The ion used for these tests has an ionization track density that is slightly above the "iron threshold" in the distribution of galactic cosmic rays, and thus is a reasonable measure of the device sensitivity to galactic cosmic ray effects. The same fluence (10^6 ions/cm^2) was used for each of the four test runs.

Two points can be made concerning these data. First, functional operation was only affected during two of the four test runs. When functional errors occurred, they could either affect readout of the memory or other internal operation of the device in the read mode (such as page-mode errors). However, because the results are inconsistent from run to run, it is not possible to get the same statistical precision about error rates compared with tests that show less ambiguous results.

Second, during the test run there were abrupt increases and decreases in the power supply current. The current changes are likely due to upsets in control logic which cause conflicts in bidirectional logic. The presence of the current steps indicate that many internal regions are affected. However, upsets in regions of the device that affect write or erase functions will not be detected by post-irradiation tests in the read mode.

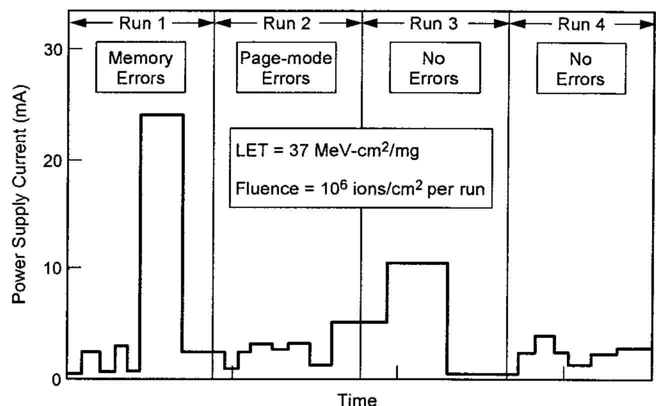

Figure 4. Steps in power supply current during a heavy ion test of a 16-Mb flash memory.

Fortunately the cross section for upsets in the state machine is relatively small compared to the total device area. The lower curve in Figure 5 shows the upset cross section for a 16-Mb flash memory, dominated by upsets in the controller. Because of the small cross section, the error rate in space is relatively low, corresponding to one error in time periods of several days to weeks (depending on the particular orbit and other application details). The

upper curve in Figure 5 shows the upset cross section for the buffer in a more advanced 256-Mb flash memory [3]. Unlike the lower curve which was a total device cross section, this curve represents the error rate for a page buffer that stores 528 bits. Thus, the cross section is much larger than that of the older 16-Mbit device, and roughly scales with the size of the memory.

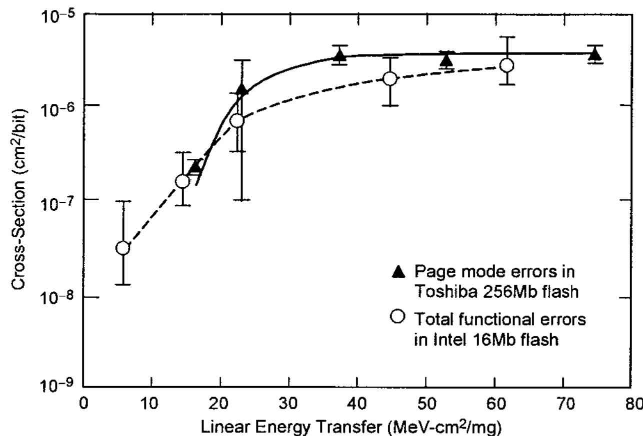

Figure 5. Upset cross section for an older 16-Mb and a more advanced 256-Mb flash memory. The lower curve is a total device cross section, whereas the upper curve for page-mode errors in the 256-Mb device represents errors per bit for a buffer that stores 528 bits.

C. Dealing with the Upset Problem

It is very difficult to detect whether internal errors have occurred in flash memory state machines and control logic because of the "closed" nature of flash memory designs. It is not possible to use address lines, status lines or operational flags that are used for conventional microcontrollers because those functions are buried internally within the flash memory device. Consequently, it is necessary to periodically reinitialize these devices as data is read out. It is also possible to incorporate error-detection techniques to aid in interpreting data validity providing data within a single word is distributed over different chips.

Some visibility can be obtained on internal errors by monitoring selected status lines, such as the page mode information that is present on larger flash devices. However, this does not provide information on overall operational errors, which are usually due to errors in the controller.

V. Microscopic Ionization Effects

Microscopic ionization damage from heavy ions was analyzed by Oldham, et al. in DRAMs in 1993 [8], where it caused increases in cell leakage current that depends on operating conditions (including the refresh rate). The most straightforward way to study microscopic damage effects in DRAMs is to examine the threshold voltage distribution within a device before and after irradiation. Figure 6 shows an example for a dynamic memory where the retention time distribution was used to infer internal threshold voltage after total dose irradiation [9]. The mean value of the retention time changes, but there is a much larger effect on cells at the "tail" of the retention time distribution which have lower threshold voltage, causing the retention time to be more affected by radiation damage (processing variations, including the statistical distribution of dopant atoms in the channel, cause the threshold voltage to vary somewhat for different cell locations).

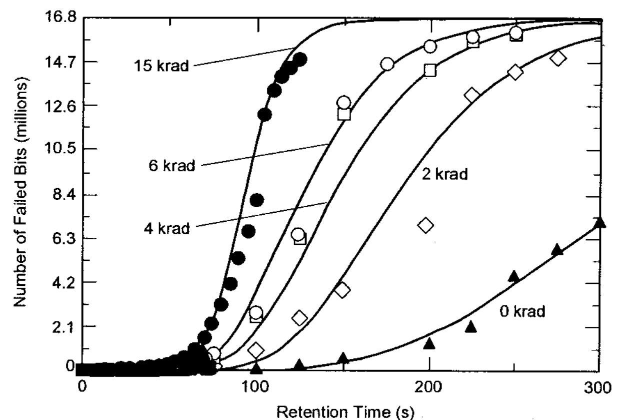

Figure 6. Change in retention time distribution for a DRAM caused by ionization damage. In this case all of the cells are irradiated, but the radiation has a much larger effect on marginal cells with low initial threshold voltage.

Retention time measurements after heavy ion irradiation also show that cells on the "tail" of the distribution are more sensitive to damage [10]. Thus, microdose damage from heavy ions can be investigated by examining threshold voltage distributions.

It is possible to measure threshold distributions on flash memories directly in an analogous manner to that of DRAMs. However, this usually requires special information from the manufacturer, using special probes to make tests on internal test points. Just as for the DRAMs, microscopic ionization damage will be apparent by a change in slope at the extremes of the threshold voltage distribution.

Microscopic ionization damage has been observed in multi-level flash devices after irradiation with heavy ions. The net effect was a shift of the internal state of some of the internal memory cells. This is shown schematically in Figure 7, where 18 cells with the highest internal storage level were shifted to the next level, 23 from the second highest to the third highest, and 2 from that level to the ground level. This is caused by ionization (microdose) that changes the storage level of the charge "packet" within the floating gate. Although this changes the stored information, it does not cause a permanent change in the device; rewriting the cell can be done to restore the information. These types of errors are expected to become more severe for future multi-level flash memories, particularly if larger numbers of bits are stored within each cell, because the internal margin for changes in threshold voltage is reduced.

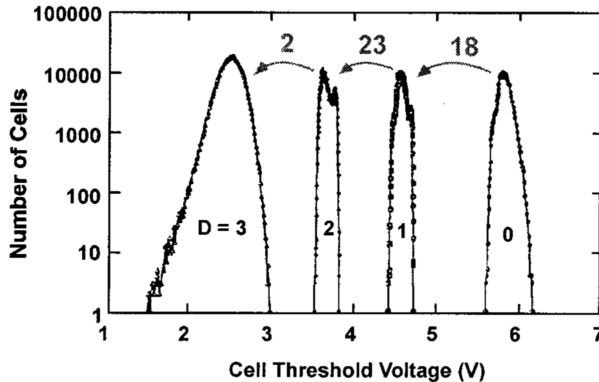

Figure 7. Change in higher-level storage locations in a multi-flash memory after irradiation with heavy ions.

VI. Permanent Errors Caused by Microscopic Damage

Permanent changes in thin oxide can occur due to the detailed interaction of the intense ionization track from a single heavy ion with the gate region, which produces localized damage in the structure of the gate [10]. The earlier work was done with 4-Mb DRAMs, and similar effects have been observed in 16 and 64-Mb DRAMs. This effect has been studied more recently in capacitor test structures [11], and can cause the leakage current to increase by several orders of magnitude. Figure 8 shows an example of this effect. Although the change in leakage current is small, it can affect the ability of the floating gate to store charge over long time periods. This is a permanent effect, and may limit the ability to use very advanced flash memories in space unless they are refreshed periodically. The magnitude of the leakage current depends on the thickness of the gate region as well as the quality of the oxide.

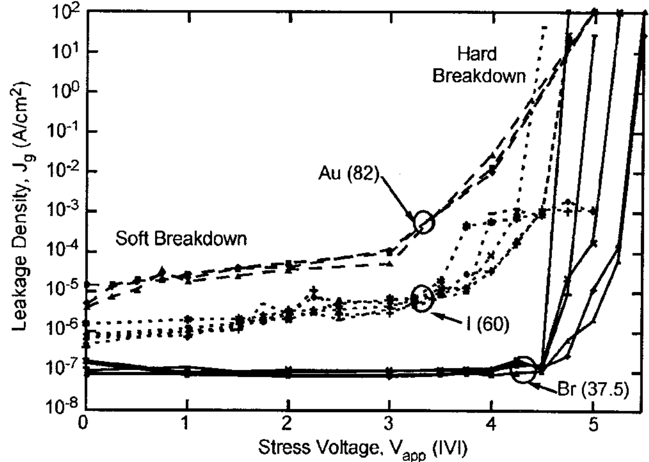

Figure 8. Increase in leakage current of a thin oxide after irradiation with heavy ions.

Although high electric fields are required in order to get large current changes (hard breakdown), soft breakdown can occur at very low electric fields and required only a single ion strike. It is possible to deal with this issue by rewriting the memory periodically (similar to refresh in a DRAM, but on a much longer time scale), but this failure mode is clearly an important issue for applying advanced flash memories in space. It may become more important for flash memories in the near future because of the constant requirement to decrease cell size and increase erase/write efficiency.

Other microscopic damage mechanisms may also be important for more highly scaled devices, including microscopic displacement damage from protons. More work is required in order to determine how small cell geometries and more elaborate memory architectures are affected by space radiation.

VII. Conclusions

Flash memories have unique design requirements that cause them to be more susceptible to radiation damage compared to more conventional microelectronic components. The high voltage required for the erase and write functions require that some of the internal transistors are designed with thicker gate oxides and more lightly doped channel regions compared to conventional digital logic transistors, making them far more susceptible to radiation damage. The charge pumps that are required to generate the high voltage for erasing and writing are usually the most sensitive circuit

functions, usually failing below 10 krad(Si). Some improvement can be realized by operating the flash memory devices without bias except during the time periods that they are required to operate, and that method has been proposed for possible implementation of advanced flash memories on the JPL Europa mission.

Single-event upset effects are far more difficult to deal with. The very complicated device architecture used in advanced flash devices causes their basic functionality to be affected by heavy ions and protons, and it is difficult to recognize and categorize these types of upsets because of the limited visibility about internal operating conditions. In some cases the device clearly does not function at all, but in others the errors may be difficult to detect -- such as errors in buffers or page address registers. Fortunately the overall error rate for those types of malfunctions is relatively small, allowing system mitigation with EDAC.

Permanent errors are a far more difficult problem for several reasons. First, tests of permanent errors are difficult and costly to perform. Second, some types of errors may occur even for devices that are not biased during the time that a heavy ion strike occurs. Error detection and correction may be a viable way to recognize this type of failure mechanism, but it is also necessary to understand how and why the errors are generated within the device, as well as whether internal errors in the memory controller will affect their operation in space.

REFERENCES

[1] H. R. Schwartz, D. K. Nichols and A. H. Johnston, "Single-Event Upset in Flash Memories," IEEE Trans. Nucl. Sci., **44**(6), 2315 (1997).

[2] D. N. Nguyen, et al., "Radiation Effects in Advanced Flash Memories," IEEE Trans. Nucl. Sci., **46**(6), 1744 (1999).

[3] D. R. Roth, et al., "SEU and TID Testing of the Samsung 128 Mbit and the Toshiba 256 Mbit Flash Memory," 2000 IEEE Radiation Effects Data Workshop, p. 96.

[4] S. Aritome, "Advanced Flash Memory Technology and Trends for File Storage Applications," 2000 IEDM Technical Digest, p. 763

[5] A. Fazio, "A High-Density High-Performance 180 nm Generation ETOX Flash Memory Technology," 1999 IEDM Technical Digest, p. 267.

[6] J-D. Coi, et al., "A 0.15 μm NAND Flash Technology with 0.11 μm^2 Cell Size for 1-Gbit Flash Memory," 2000 IEDM Technical Digest, p. 767.

[7] N. S. Saks, M. G. Ancona and J. A. Modolo, "Radiation Effects in MOS Capacitors with Very Thin Oxides at 80 K," IEEE Trans. Nucl. Sci., **31**(6), 1249 (1984).

[8] T. Oldham, et al., "Total Dose Failures in Advanced Electronics from Single Ions," IEEE Trans. Nucl. Sci., **40**(6), 1820 (1993).

[9] L. Z. Scheick, S. M. Guertin and G. M. Swift, "Analysis of Radiation Effects on Individual DRAM Cells," IEEE Trans. Nucl. Sci., **47**(6), 2534 (2000)

[10] G. M. Swift, D. J. Padgett and A. H. Johnston, "A New Class of Single-Event Hard Errors," IEEE Trans. Nucl. Sci., **41**(6), 2043 (1994).

[11] J. F. Conley, et al., ""Heavy Ion Induced Soft Breakdown of Thin Gate Oxides," presented at the 2001 IEEE Nuclear and Space Radiation Effects Conference, Vancouver, British Columbia, July 16-20, 2001; accepted for publication in the IEEE Trans. Nucl. Sci., December, 2001.