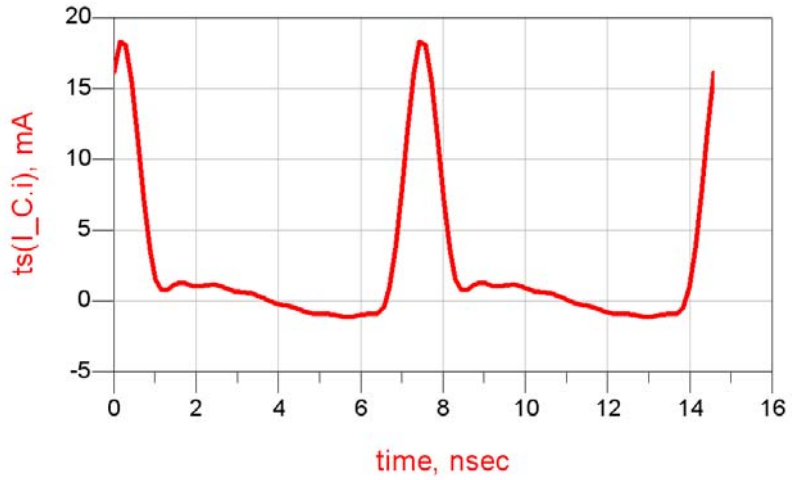
Amplitude prediction.

For some oscillator topologies, it is easy to predict the amplitude of the oscillator output. For example, the differential oscillator described in the first note set is biased by a current source, so the maximum current into the tank is known. If the R_P is also well controlled (not necessarily easy to do), then Vtank = I_C R_P.

Other topologies like the Colpitts are not so easy. In Lee's book, he presents a describing function method for predicting oscillator amplitude. It works for the common base/gate Colpitts pretty well, but seems to fail completely when trying to predict amplitude of even the common collector/drain version.

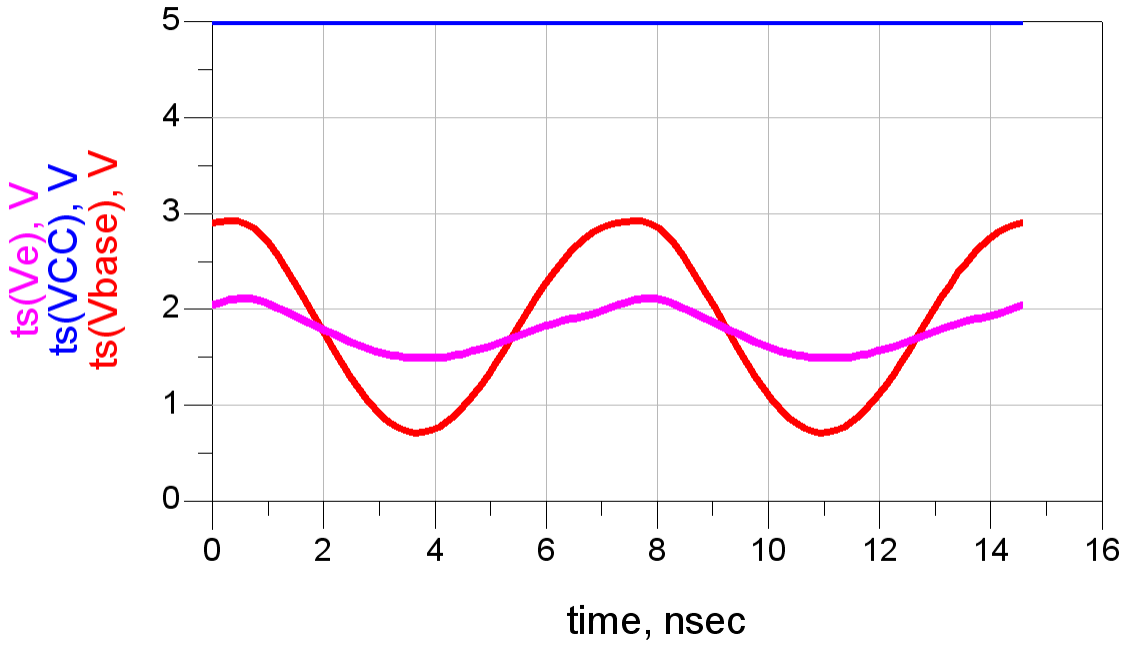
In general, simulation provides your best chance of getting an estimate of the limiting behavior and thereby the amplitude of your oscillator under consideration.

What we can glean from Lee's work, however, is that a well designed LC oscillator like the Colpitts must be current limited: that is, we allow the active device to go into cutoff for part of the period of oscillation. This reduces the effective g_m of the device, averaged over the period, and thus gives the needed gain compression. It also benefits phase noise as we will later see. The simulated drain current for a common collector Colpitts oscillator below illustrates that the device can be in cutoff for much of the period.



The opposite of current limiting is called voltage limiting. In that case, clipping limits the amplitude of oscillation. This is undesirable because it generates a lot of harmonic distortion plus the low impedance state when the device is driven into saturation or the ohmic region kills the tank Q for part of the cycle and is bad for FM or phase noise.

We can look at Vcb or Vdg to verify the limiting condition. In the case of the bipolar transistor, if Vcb = 0 or negative, the base collector junction is forward biased – a low impedance at the collector will be experienced.



The above simulated voltage plot confirms that the circuit is current limiting:

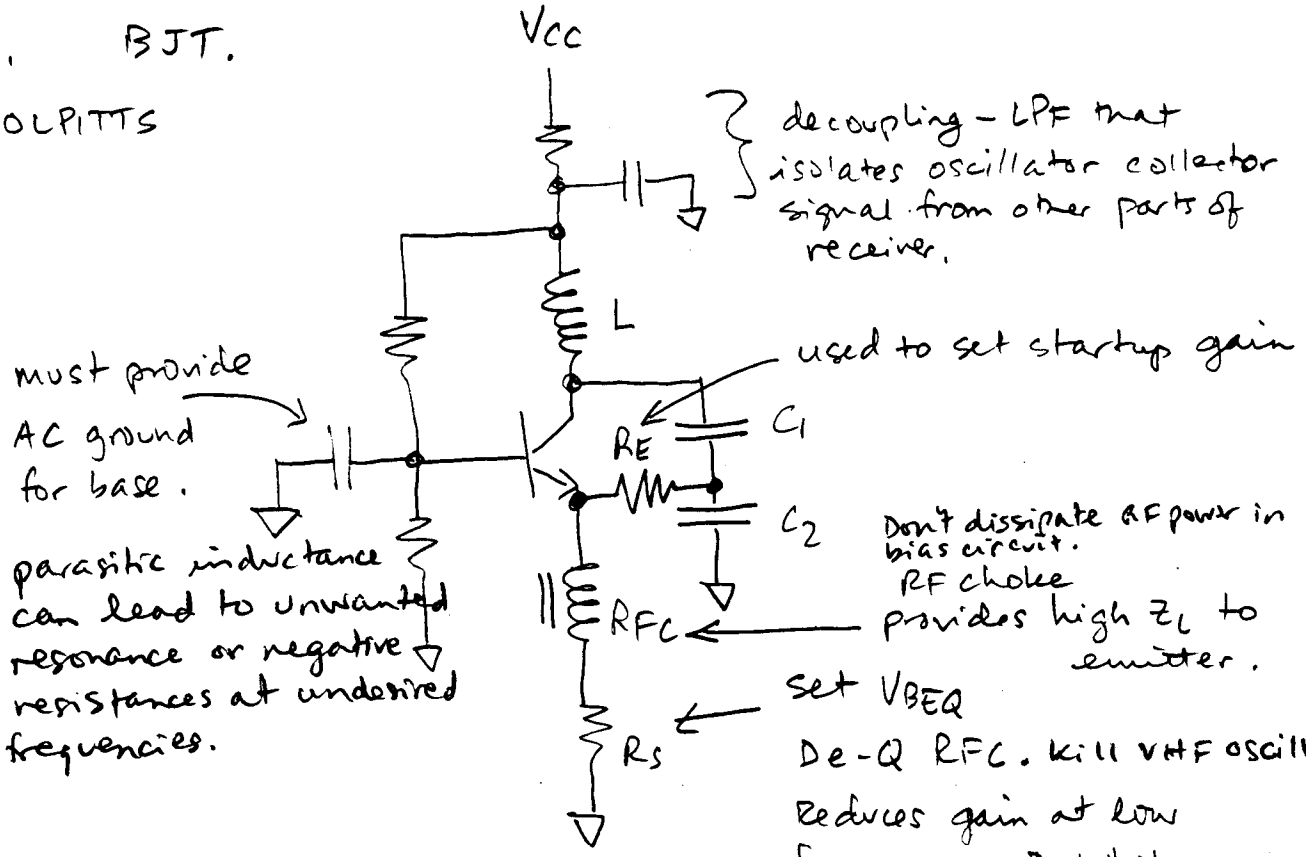
1. $V_{BE} < 0.7V$ for much of the period. Thus, the device is strongly in cutoff for much of the cycle.

2. $V_{CB} > 0$ for all of the period.

Bias Circuit Considerations

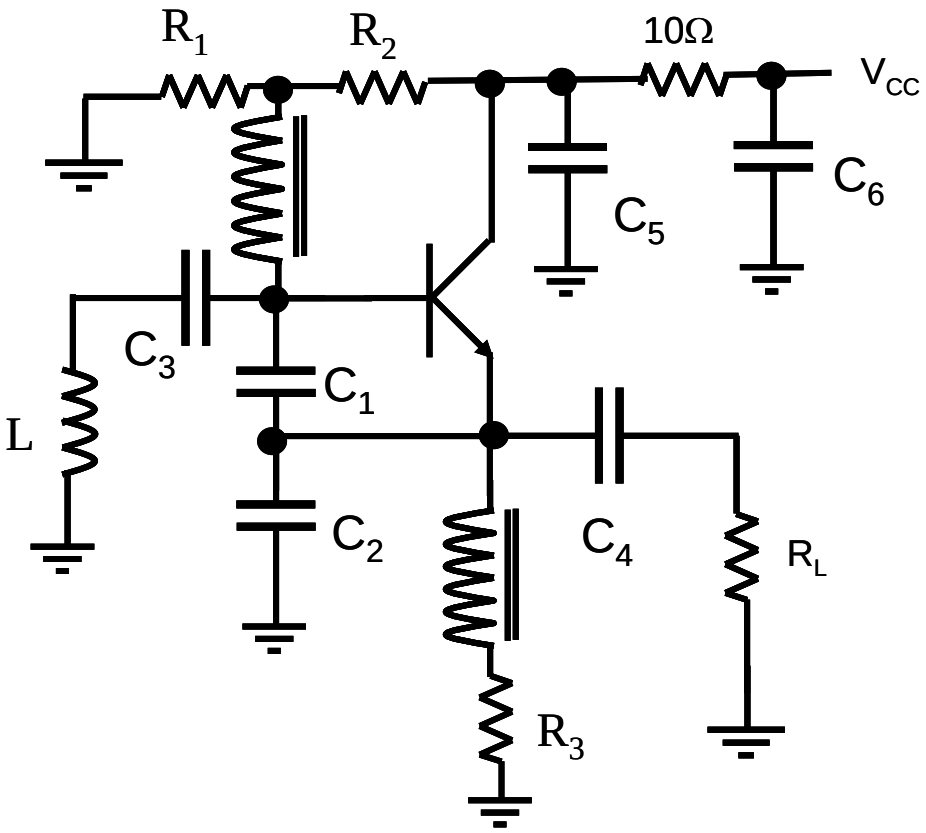
EX. BJT.

COLPITTS



Must select RFC carefully to avoid unwanted resonances. Use network analyzer!

Biasing option for Common Collector Colpitts Oscillator



Bias circuit design considerations

We have seen that the bias point chosen will affect many important characteristics of the oscillator.

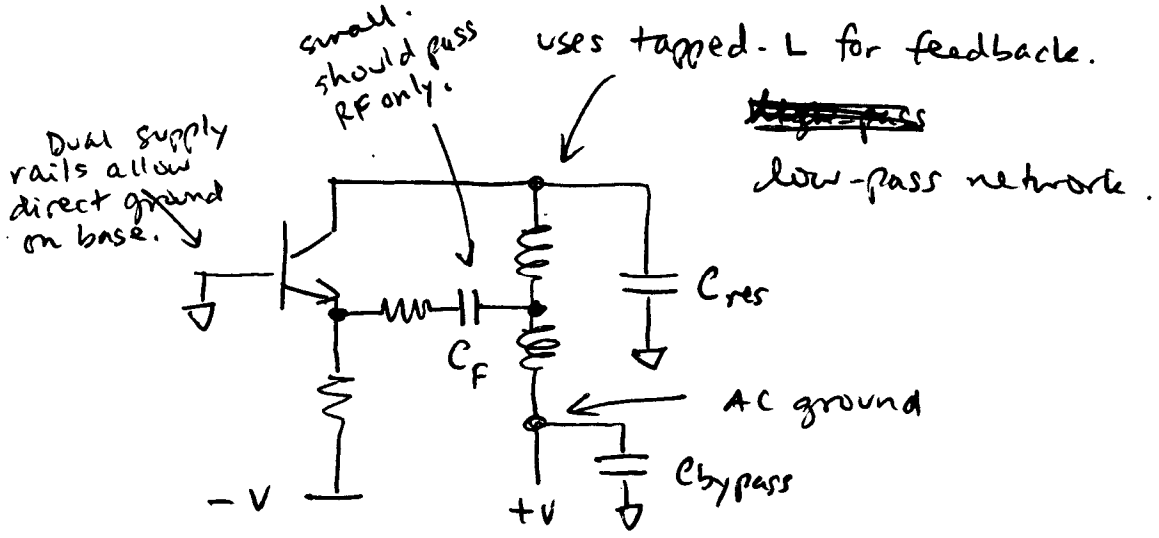
1. Startup. gain must be large enough to start oscillator from noise but not too large – too much $\Delta\phi$ or AM/PM conversion.

2. Limiting. Must have cutoff limiting of voltage swing. Saturation/ohm. region limiting will cause lots of harmonic distortion and noise. Loaded Q will die.

3. Temp. stability. As with all designs, amps. or oscillators, a temp-stable Q-point is necessary. Use DC feedback to accomplish.

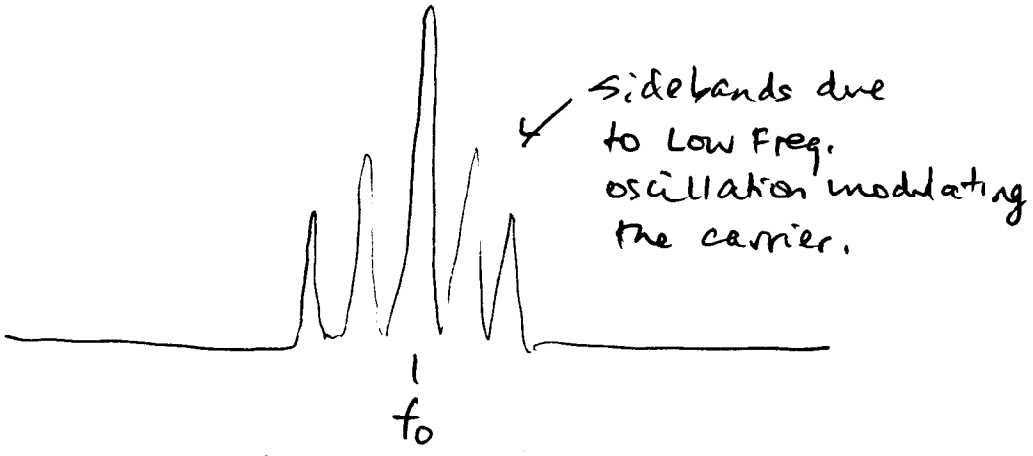
4. Bias circuit oscillation. You must be certain that the oscillator will not stop oscillating when it starts up. This can occur due to large-signal gain compression caused by the shift in bias point. Low frequency oscillations will occur.

Example: Hartley Oscillator



if C_F is too large, wide bandwidth of FB network will result in low frequency oscillations. This can be avoided with smaller C_F and lower gain at startup. Colpitts avoids the problem since FB network is high-pass.

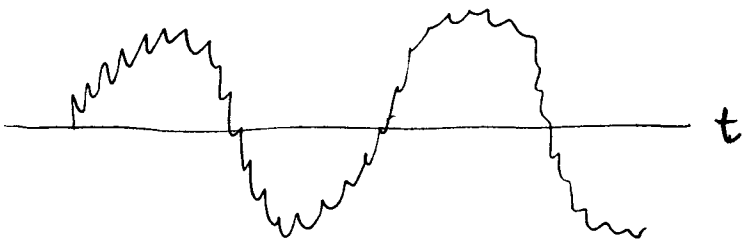
Signal will look like this:



As the low frequency oscillations build up in amplitude the bias point shifts and the oscillator can actually stop. Then, it must wait until the DC bias returns to a condition where $A\beta > 1$ before it will restart - a relaxation oscillator.

This condition is called "squeeging".

VHF/UHF oscillations can also occur if the circuit has parasitic resonances due to components (such as RF chokes). Also, if the circuit voltage limits instead of current limits, the resonator Q is reduced. Wide band high frequency feedback can cause VHF or UHF oscillations.



Output coupling

We have neglected to connect an output to the oscillator.

① Across resonator.

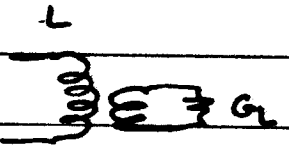
$$G_{LOAD} = G_p + \frac{g_m}{N^2}$$ (for max. power tra

Note that this reduces Q_L by 2x.

$$Q_L = \frac{\omega_0 C}{G_{TOTAL}}$$

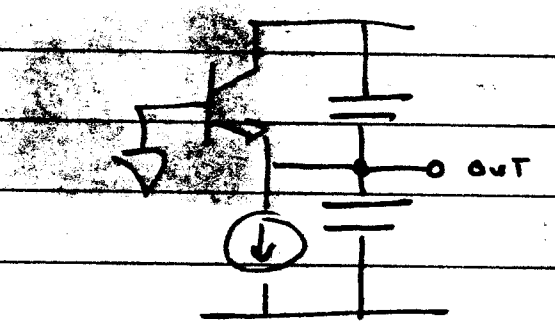
Low Noise requirements favor lighter coupling.

② Transformer



$$G'_{LOAD} = G_L/N^2$$

③ Take output off emitter if large G_L.

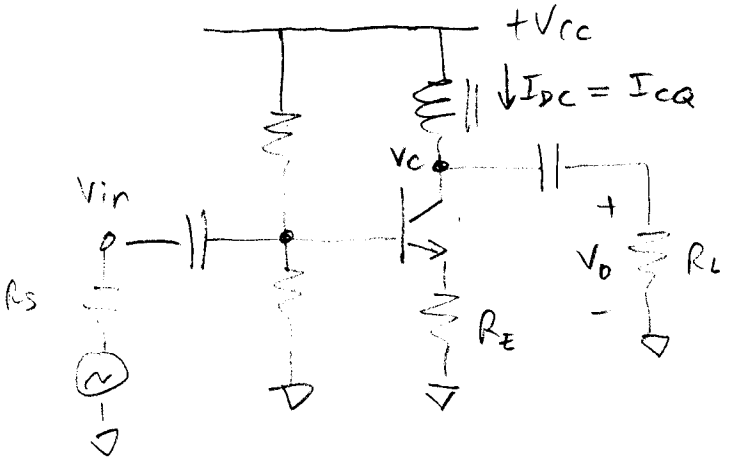


Now $G_L \| g_m$ must be considered in the design.

Buffer Amplifier Design

Both diode and FET ring mixers require large LO amplitude to switch rapidly and effectively. Sometimes a driver amplifier is used to increase the oscillator power. If the LO must tune over a wide bandwidth (>10%) we can't use tuned amp.

Class A amplifier with inductive load.



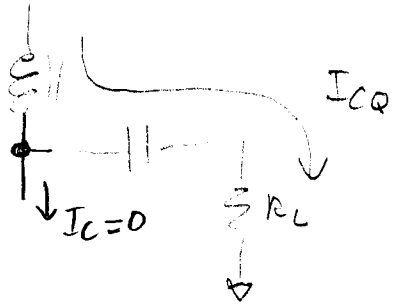
also, we know that $V_{c,avg} = V_{cc}$

1. What is the maximum V_o?

Device is driven into cutoff. $I_C = 0$

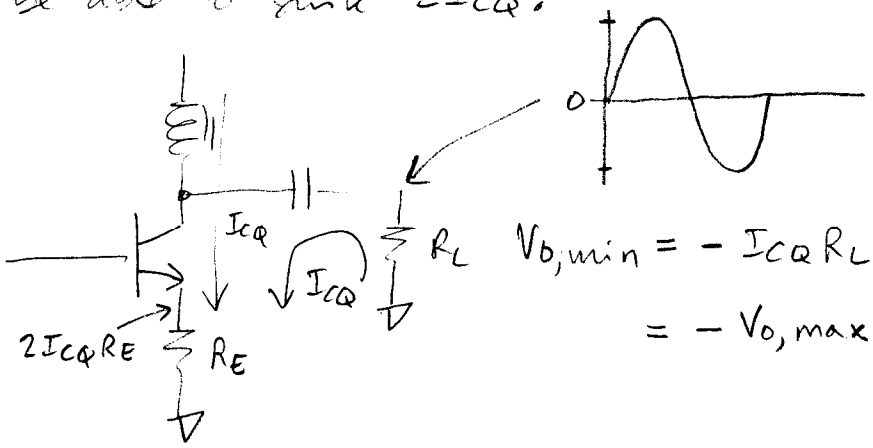
The RFC will try to keep $I_{DC} = I_{CQ}$, so

$V_{o,max} = I_{CQ} R_L$



to avoid clipping, make sure that cutoff is just reached or never reached.

2. To make sine wave symmetric, the device must be able to sink $2I_{CQ}$.



We must avoid clipping, so $I_{CQ}R_L < V_{CC} - V_{CE,sat} - 2I_{CQ}$

or, $V_{CC} > V_K + I_{CQ}(R_L + 2R_E)$

$V_K = V_{CE,sat}$ or "knee voltage"

Thus, $P_o = \dfrac{V_{o,max}^2}{2R_L} = \dfrac{1}{2} I_{CQ}^2 R_L$

3. Gain. $A_v \cong -\dfrac{R_L}{R_E}$

$$G_T = \frac{V_o^2/2R_L}{\hat{V}_{in}^2/2R_S}$$

Adjust R_E to set gain.

Note: The buffer amplifier is untuned. Thus, we need to avoid reduced conduction angle modes such as Class AB or Class B. There is no low impedance termination for even-order harmonic frequencies. Harmonic termination is needed to form the half sine wave current waveform for Class B. A push-pull design with appropriate transformer could be used if Class B is desired.

We must work within the limitations of the device chosen for the buffer.

$I_{C,max}$
$BV_{,CEO}$
Tmax

These can typically be found on the data sheet. A safe design does not run all the way to the limits of the device, so a reasonable margin needs to be provided. It may not be wise to exceed 75% of the recommended maximum values.

For the Class A buffer amplifier, the peak values of voltage and current are:

$$V_{CE,\,max} = V_{CC} + I_{CQ}\,R_L$$

$$I_{C,\,max} = 2\,I_{CQ}$$

Let's design a buffer.

Specs: 7 dBm output power (5 mW; 0.71V in 50 ohms); Source impedance = 100 ohms. Voltage output from oscillator = 0.5V.

The device has: $BV_{CEO} = 12V$; $I_{C,\,max} = 100$ mA

1. Determine I_{CQ}.

We start with $R_L = 50$ ohms.

$$Po = I_{CQ}^2\,R_L/2 = 0.005\ W \qquad I_{CQ} = 14.2\ mA.$$

This gives us a maximum current of 28.4 mA, well within the limits of the device.

2. Determine R_E.

This will be determined by the gain required.

$$A_v = 0.71/0.5 = 1.42 = -\tilde{g}_m R_L = \frac{-R_L}{r_e + R_E}$$

$g_m = 0.55$; $r_e = 1.8$ ohms. So, $R_E = (R_L/Av) - r_e = 33$ ohms.

Check the input resistance: $R_B||R_E (\beta+1) >> R_S$. Make sure the bias resistors (R_B) don't load down the oscillator or reduce the input amplitude significantly.

3. Determine $V_{CC,min}$, $V_{CC,max}$. This is the range of acceptable power supply voltages which avoid clipping and breakdown.

$$V_{CC,\,min} = V_{CE,sat} + I_{CQ}\,(R_L + 2R_E) = 2.1\ V$$

$$V_{CC,\,max} = 0.75\ BV_{,CEO} - I_{CQ}\,R_L = 8.3\ V$$

4. Check for temperature rise

Worst-case Power Dissipation = $P_D = V_{CC}\,I_{CQ}$ for Class A

Choose $V_{CC} = 5V$. $P_D = 71$ mW. (This will drop to approximately 66 mW at full output, but you must design for the worst case where the oscillator may fail to produce an output.)

$$Tmax = R_{TH}\,P_D + Tambient$$

where R_{TH} is the Thermal Resistance (degree C/Watt)

Maximum temperature is usually 150 C. If you exceed this, then you must reduce V_{CC} or I_{CQ}.

5. Stability. Finally, you must check for stability over a wide range of frequencies. Use the S parameter simulation mode in ADS and plot k and mag delta vs frequency. If there are potential instabilities, you must deal with them using techniques that were employed with the power amplifier designs last quarter.

How do you reduce power dissipation in a LO buffer amplifier?

The bias current of the amplifier is directly related to the output voltage swing and R_L. If the supply voltage is fixed, then you can reduce current to save power.

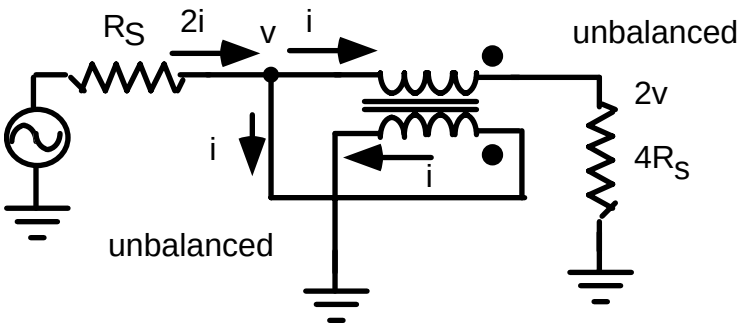
1. Increase R_L. This may be practical in situations where the frequency is relatively low and interconnection lengths short. This is quite practical for on-chip implementations.

But, if the oscillator and mixer are separated on different boards or distant from one another then a transmission line must be used to interconnect them. This requires Zo typically in the 50 to 75 ohm range.

2. Use a transformer to step up impedance at the drain or collector node. This is feasible if there is sufficient supply voltage to handle the extra voltage swing at the drain or collector and if the device is not close to breakdown.

Here is an example of a wideband transformer that is used from HF through VHF frequencies:

Ruthroff 4:1 un-un



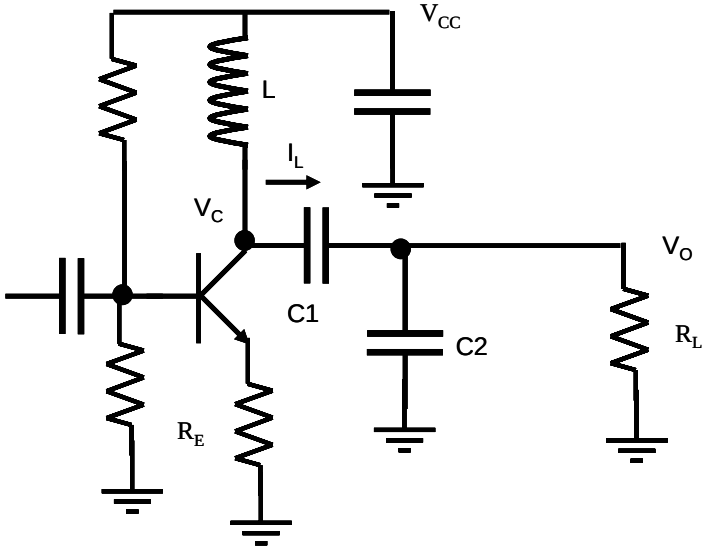
The circuit above provides a 4:1 transformation between two unbalanced impedances. It works by bootstrapping the voltage from v at the left to 2v at the right. The transformer windings are connected in series. The current at the input is 2i, split two ways. So the output current is just i. So, we get twice the voltage and half the current at the output. Of course, it can be used the other way to transform a lower R_L into $4R_L$ at the collector. The voltage at the high impedance end is twice that at the low impedance end, so if used at the drain of an amplifier, V_{CC} and breakdown voltage must be adequate.

The transformer is generally implemented using transmission lines, either coax or twisted wires. These are wrapped around a ferrite core to increase the common mode inductance and extend the bandwidth to lower frequencies.

For more information, see the note on RF transformer design on the course web pages.

3. Tapped capacitor tuned amplifier. If a narrowband buffer is adequate, then the tapped capacitor impedance transformer can be applied to the amplifier output. The

loaded Q of the resonator must be small enough to provide the required bandwidth for the application.



The ratio $n = \frac{C_1 + C_2}{C_1}$ applies to voltage and current and impedance as follows:

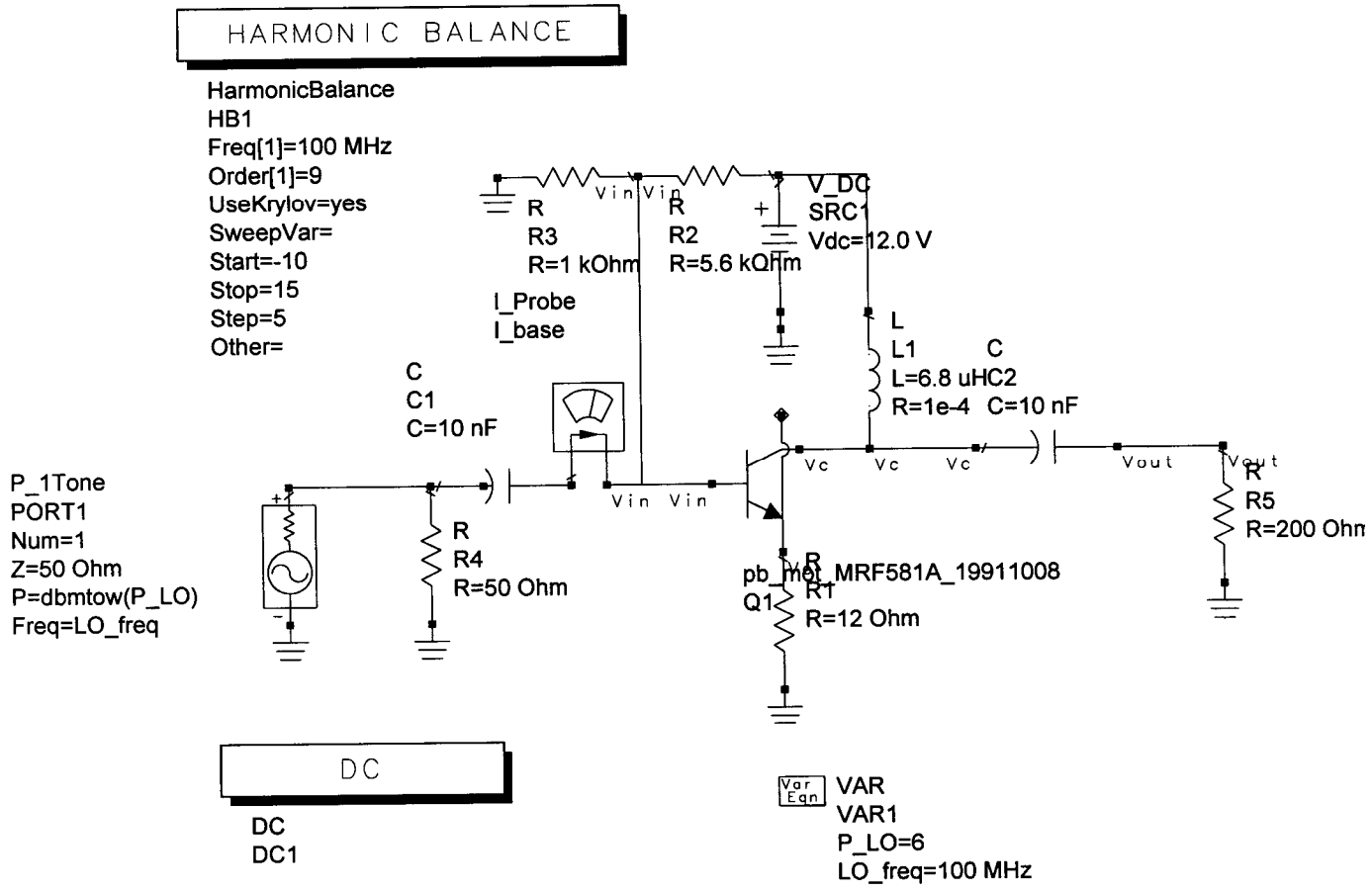
$$V_C = nV_O$$

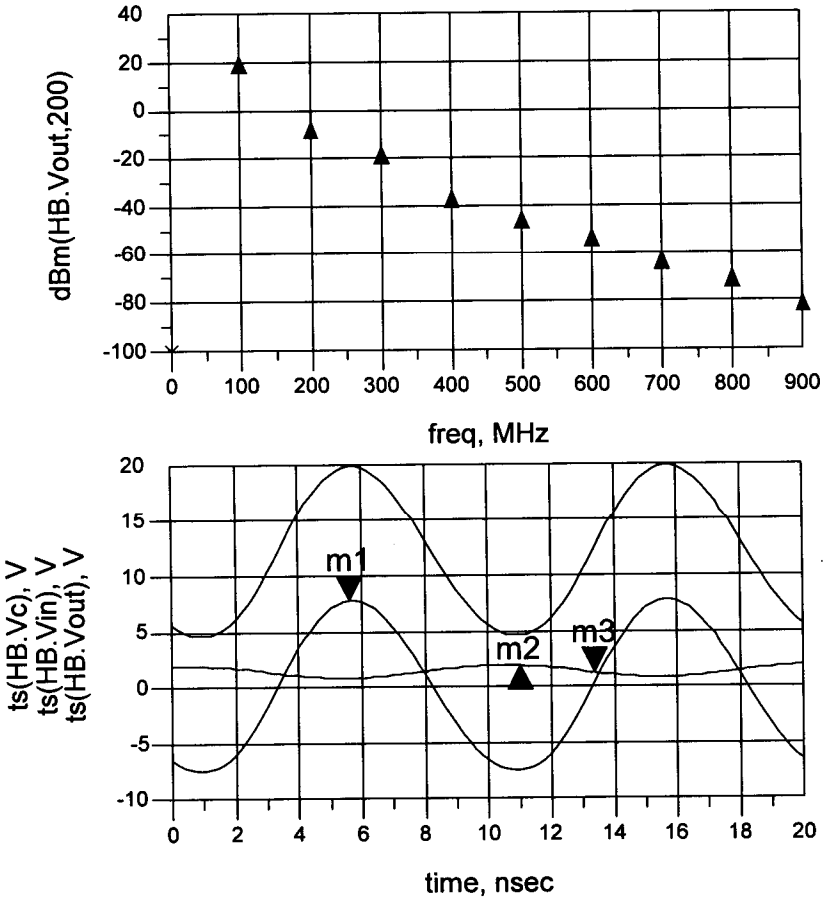
$$I_L = \frac{V_O}{nR_L}$$

$$Z_C = \frac{V_C}{I_L} = n^2 R_L$$

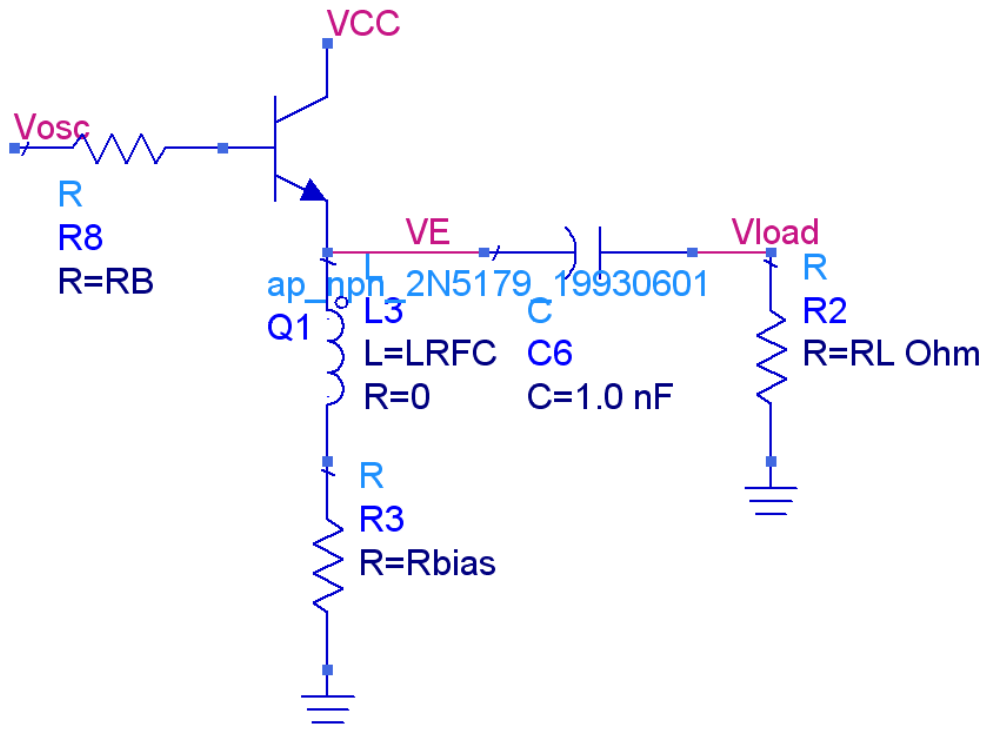
The collector voltage, V_C, will be scaled up by a factor of n, so one must have sufficient V_{CC} and breakdown voltage to scale by a large factor.

You can see though that bias current can be reduced by the factor 1/n when this is applied. If V_{CC} is fixed in the design, a net power savings is obtained.


HARMONIC BALANCE
HarmonicBalance
HB1
Freq[1]=100 MHz
Order[1]=9
UseKrylov=yes
SweepVar=
Start=-10
Stop=15
Step=5
Other=
R
R3
R=1 kOhm
Vin
Vin
R
R2
R=5.6 kOhm
V_DC
SRC1
Vdc=12.0 V
I_Probe
I_base
L
L1
L=6.8 uH
C
C2
R=1e-4
C=10 nF
C
C1
C=10 nF
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow(P_LO)
Freq=LO_freq
R
R4
R=50 Ohm
Vin
Vin
Vc
Vc
Vc
Vout
Vout
R
R5
R=200 Ohm
pb_mel_MRF581A_19911008
Q1
R
R1
R=12 Ohm
DC
DC
DC1
Var
Eqn
VAR
VAR1
P_LO=6
LO_freq=100 MHz


dBm(HB.Vout,200)
40
20
0
-20
-40
-60
-80
-100
0
100
200
300
400
500
600
700
800
900
freq, MHz
ts(HB.Vc), V
ts(HB.Vin), V
ts(HB.Vout), V
20
15
10
5
0
-5
-10
0
2
4
6
8
10
12
14
16
18
20
time, nsec
m1
m2
m3
m1
time=4.600nsec
ts(HB.Vout)=5.985 V
m2
time=-2.600E-9
ts(HB.Vin)=0.706
delta mode ON
m3
time=13.60nsec
ts(HB.Vin)=1.217 V

Emitter Follower Buffer Amplifier



- Simple design but less isolation than common emitter/source due to base-emitter capacitance.

- Bias current can be determined as with common emitter by the amplitude Vload and load resistance RL.

Varactor diodes – electronic tuning of resonator

$$C_j(V_R) = \frac{C_j(0)}{[1 + (V_R/\phi_B)]^m}$$

Abrupt Junction: $m = 0.5$

Linearly graded: 0.33

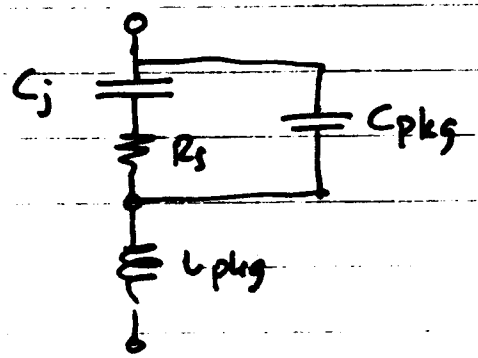
Hyper-abrupt: > 0.5

$C_j(0)$ = zero bias capaci

ϕ_B = built-in voltage

≈ 0.7 V typically fo

Silicon abrupt ju



Q is specified by series RC model:

$$Q = \frac{\text{reactance}}{R_s} = \frac{1}{\omega C_j R_s}$$

typically specified at 50 MHz and $V_R = -4$V

Silicon Tuning Diode

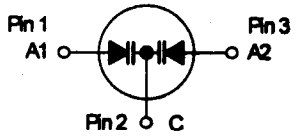
MV104

This device is designed for FM tuning, general frequency control and tuning, or any top–of–the–line application requiring back–to–back diode configurations for minimum signal distortion and detuning.

- High Figure of Merit — Q = 140 (Typ) @ V_R = 3.0 Vdc, f = 100 MHz
- Guaranteed Capacitance Range
  37–42 pF @ V_R = 3.0 Vdc (MV104)
- Dual Diodes – Save Space and Reduce Cost
- Monolithic Chip Provides Near Perfect Matching – Guaranteed ± 1.0% (Max) Over Specified Tuning Range

DUAL VOLTAGE VARIABLE CAPACITANCE DIODE

CASE 29–04, STYLE 15
TO–92 (TO–226AA)



MAXIMUM RATINGS (EACH DIODE)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	32	Vdc
Forward Current	I_F	200	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) **(EACH DIODE)**

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	32	—	—	Vdc
Reverse Voltage Leakage Current T_A = 25°C (V_R = 30 Vdc) T_A = 60°C	I_R	— —	— —	50 500	nAdc
Diode Capacitance Temperature Coefficient (V_R = 4.0 Vdc, f = 1.0 MHz)	TC_C	—	280	—	ppm/°C

	C_T, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF		Q, Figure of Merit V_R = 3.0 Vdc f = 100 MHz		C_R, Capacitance Ratio C_3/C_{30} f = 1.0 MHz	
Device	Min	Max	Min	Typ	Min	Max
MV104	37	42	100	140	2.5	2.8

TYPICAL CHARACTERISTICS (Each Diode)

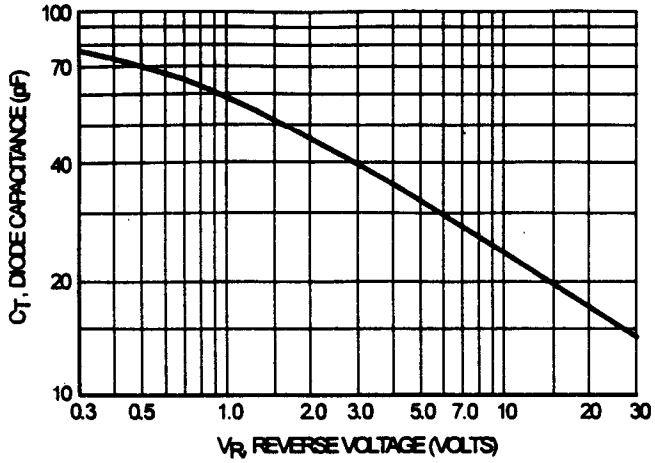


Figure 1. Diode Capacitance (Each Diode)

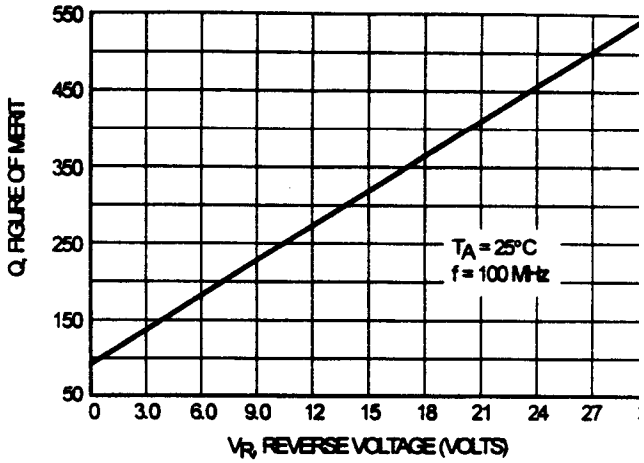


Figure 2. Figure of Merit versus Voltage

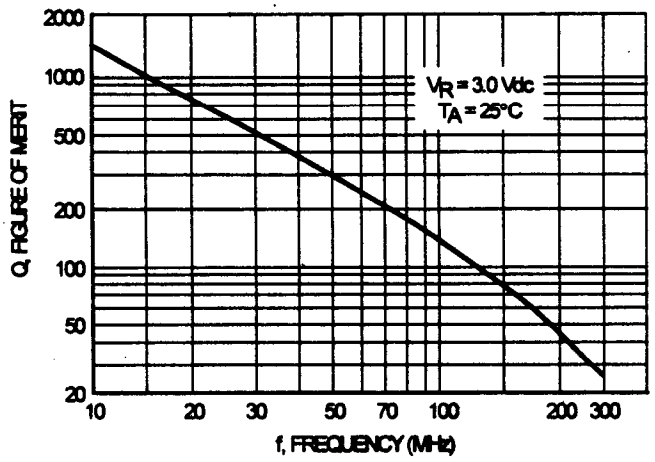


Figure 3. Figure of Merit versus Frequency

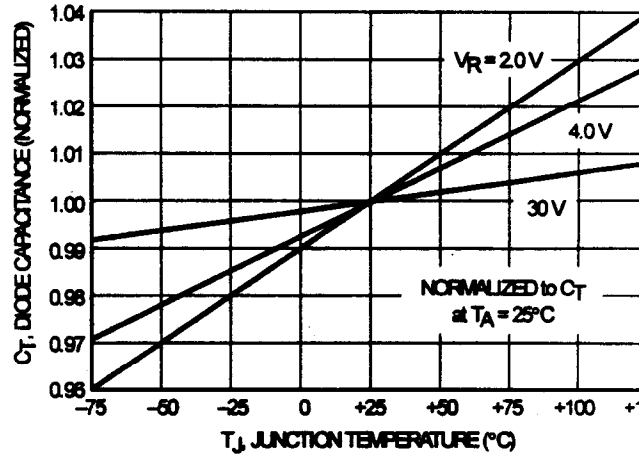


Figure 4. Diode Capacitance versus Temperatur

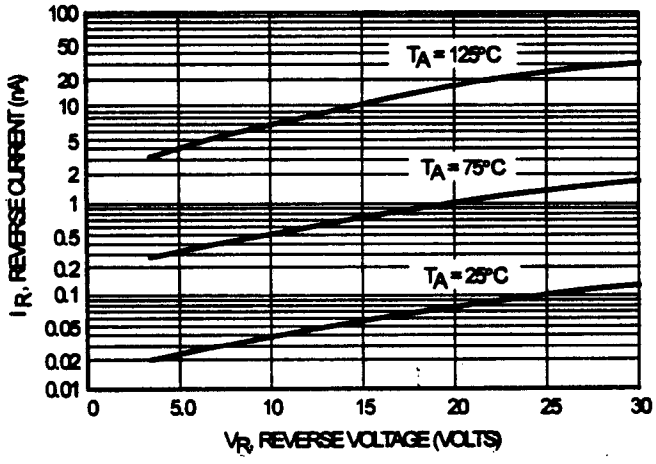
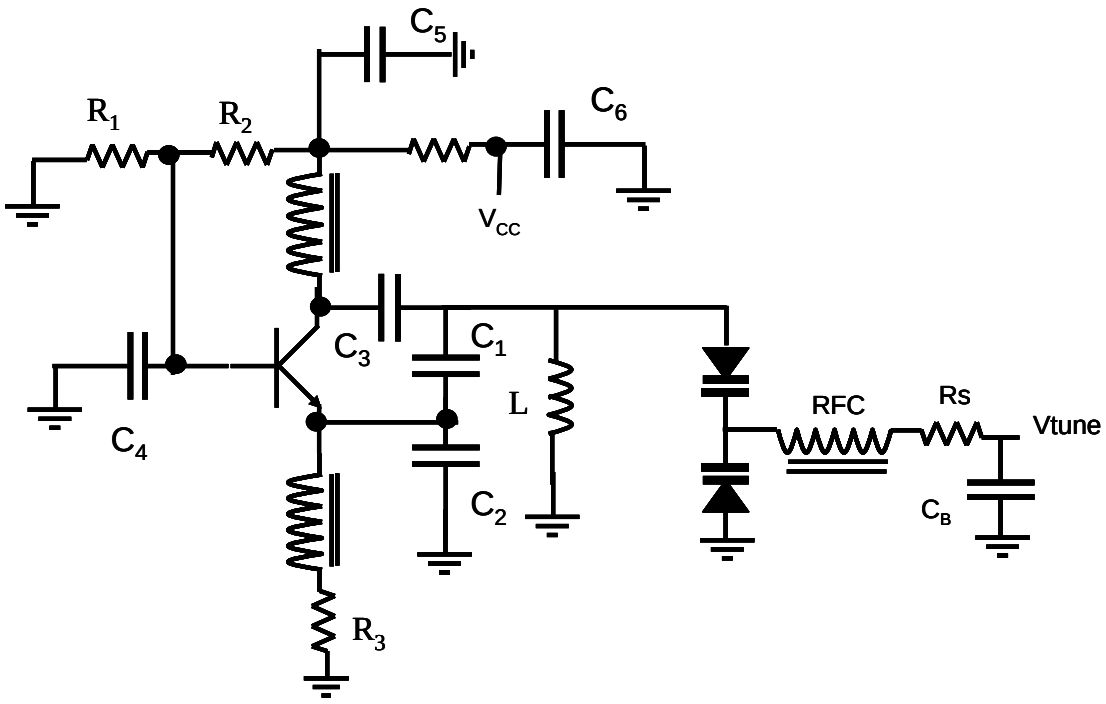


Figure 5. Reverse Current versus Reverse Voltage

Biasing the varactor diodes

Here is an example from a CB Colpitts oscillator:



- You must isolate the tuning port from the resonator. The RF choke is intended to present a high impedance to the node between the two back-to-back varactor diodes so that the oscillator signal does not leak out the tuning port.

- Rs is needed to de-Q the RFC in case it resonates with a diode.

- Two varactor diodes, back-to-back, are used to make the C – V characteristic symmetric and to avoid the possibility of forward bias.

- C_B is a bypass cap needed for isolation from outside. If the oscillator is used in a PLL, one must take care that the extra pole that C_B produces does not affect the loop phase margin.

- The tank inductor L keeps both ends of the varactor diode pair at ground DC potential so that each diode receives the same tuning voltage.

- The DC blocking capacitor C3 at the collector is needed to .

Tuning range of oscillator.

The minimum (Cmin) and maximum (Cmax) diode capacitance, L and the series combination of C1 and C2 will determine the tuning frequency range of the oscillator. Call the series capacitance C_T.

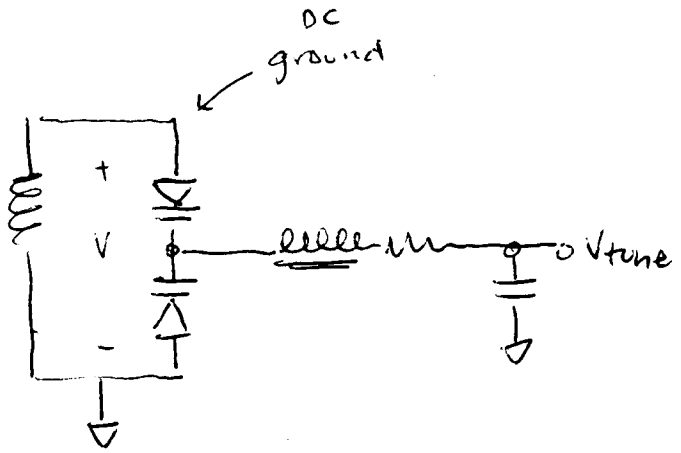
$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

Then

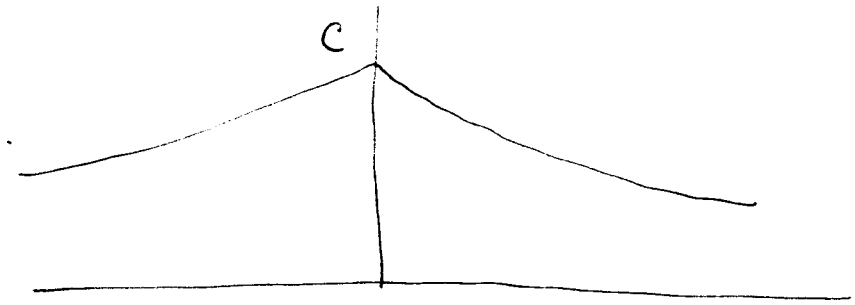
$$\omega_{\min} = \frac{1}{\sqrt{L\left(C_T + C_{\max}\right)}}$$

$$\omega_{\max} = \frac{1}{\sqrt{L\left(C_T + C_{\min}\right)}}$$

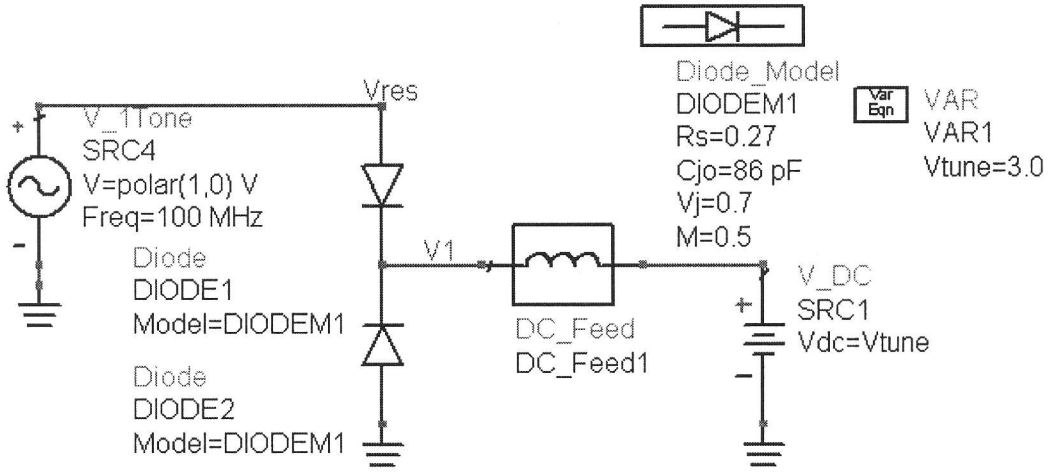
Two equations determine L and C_T for a given frequency range.

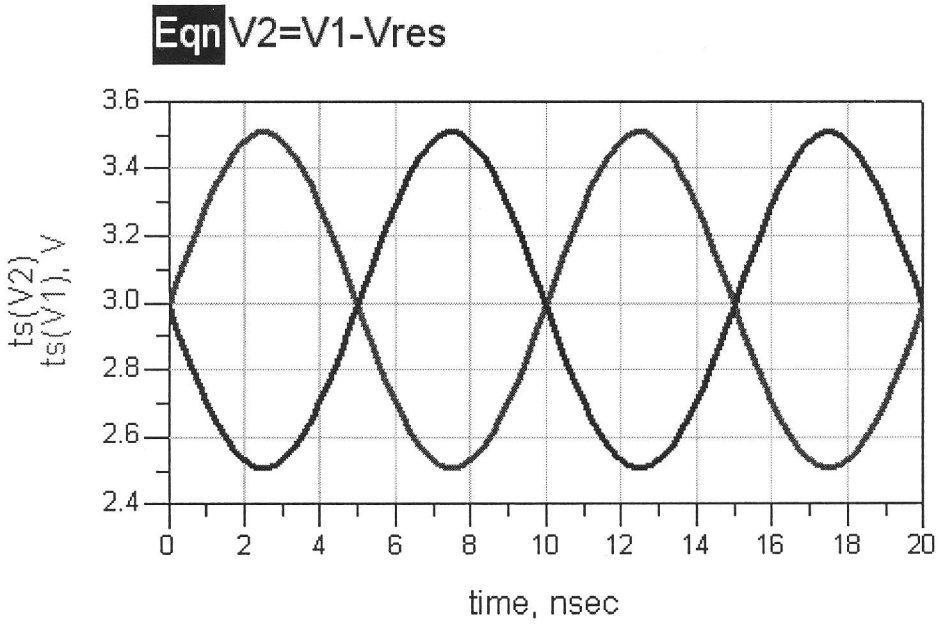


benefit: can't get into forward conduction



still nonlinear, but more symmetric.





Each diode has equal and opposite voltage swing.

Varactor Model Parameters

$$C_j(V_R) = \frac{C_j(0)}{[1 + V_R/\phi_B]^m}$$

Varactors are often specified by ratio of capacitance at two voltages.

ex. MV104: $\frac{C_j(3)}{C_j(30)} = 2.5 - 2.8$ (say 2.65 avg)

$$C_j(3) = 40\,pF$$

If we assume $\phi_B = 0.7V$,

$$\frac{C_j(3)}{C_j(30)} = \frac{[1 + 30/0.7]^m}{[1 + 3/0.7]^m}$$

$$\log_{10} \frac{C_j(3)}{C_j(30)} = m \log_{10} \frac{[43.9]}{[5.3]}$$

$$m = 0.46$$

$$C_j(0) = C_j(3)\underbrace{[1 + 3/0.7]^{0.46}}_{2.15} = 86\,pF$$

$$R_S = \frac{1}{\omega C_j(V_R) Q_u @ f}$$

Crystal Oscillator Design

The Pierce circuit below is a common one used when a quartz crystal oscillator is needed for an IC such as a PLL or microprocessor. A simple CMOS inverter, an inverting single transistor CE or CS amplifier can be used as the gain element needed for oscillation.

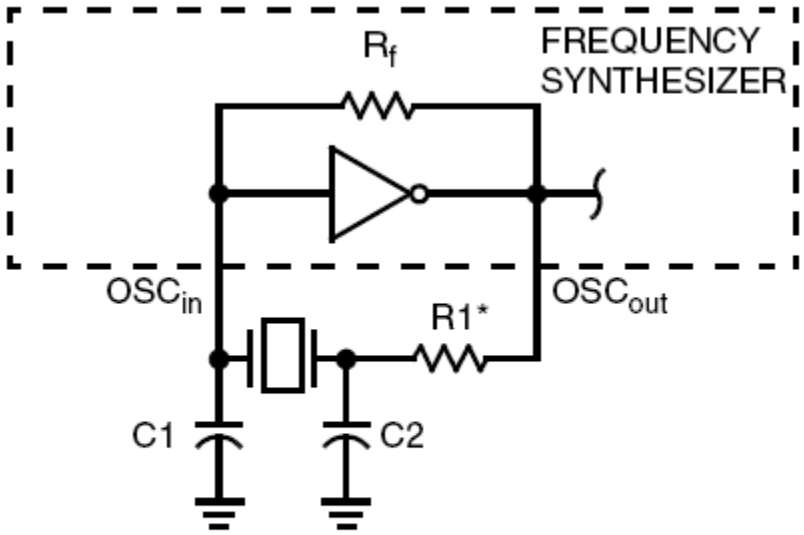


Figure 13. Pierce Crystal Oscillator Circuit *

(*From Freescale data sheet for MC145151-2 Frequency Synthesizer)

Rf is a feedback biasing resistor, often on-chip.

R1 is used to limit the current through the crystal to prevent heating and consequent frequency vs temperature drift.

C1 and C2 are external capacitors needed to obtain the correct oscillation frequency. All parallel resonant fundamental mode crystals are specified for a certain load capacitance CL.

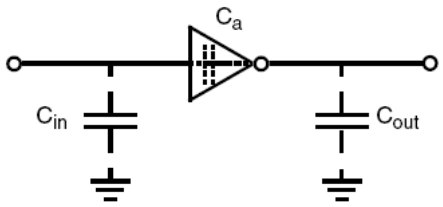
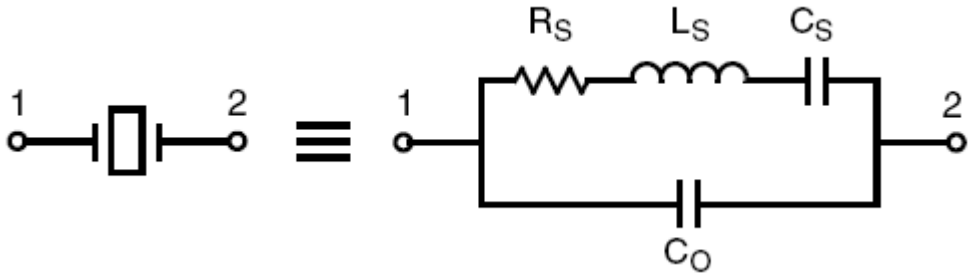


Figure 14. Parasitic Capacitances of the Amplifier *

Cin, Cout, Ca are parasitic capacitances of the amplifier (usually given on data sheet or can be calculated for a known discrete transistor amplifier). Cin and Cout may also include PC board capacitances.



*

C_S and L_S are the motional capacitance and inductance respectively and R_S is the internal series resistance. R_S is usually specified and can be used to calculate the power dissipation $P = I^2R_S/2$.

Co is the crystal holder capacitance – usually given by the vendor data sheet. Typically in the range of 2 to 10 pF.

To obtain the correct frequency:

$$C_L = \frac{C_1 C_2}{C_1 + C_2} + C_a + C_o + \frac{C_{in} C_{out}}{C_{in} + C_{out}}$$

C1 can be a variable capacitor so that the frequency can be adjusted if necessary.

The oscillation frequency varies inversely with thickness t.

At very high freq., t is small enough that it presents mechanical problems.

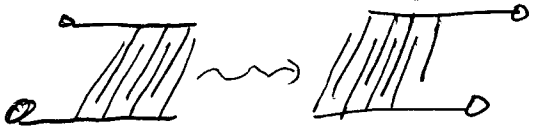
1 GHz → 1.7 μm

SAW Filters and Resonators

Surface Acoustic Wave

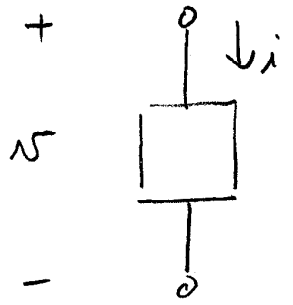
$LiNbO_3$

Thickness doesn't matter.



wavelength matches transducer spacing.

Positive Resistance



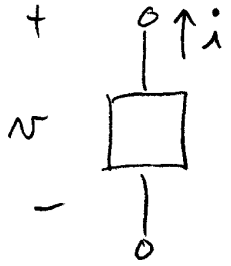
Passive sign convention

$vi = P > 0$

Power is dissipated

$\frac{v}{i} = R > 0$

Negative Resistance



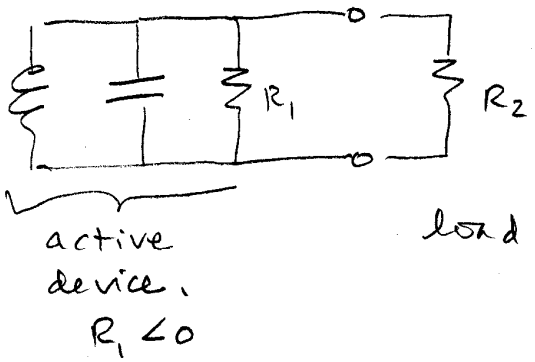
$\frac{v}{i} = R < 0$

$v \cdot i < 0$

Power is supplied or delivered

In RF circuits, we can generate a negative resistance using feedback.

Example. Parallel RLC oscillator



Question? should R_2 be > or < R_1 for oscillation?

Find admittance. Poles must be in right hand plane for oscillation.

$$Y = \frac{1}{sL} + sC + \frac{1}{R_1} + \frac{1}{R_2} = 0$$ characteristic equation

$$1 + s^2LC + sL\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = 0$$

$$\frac{1}{LC} + s^2 + \frac{s}{C}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = 0$$

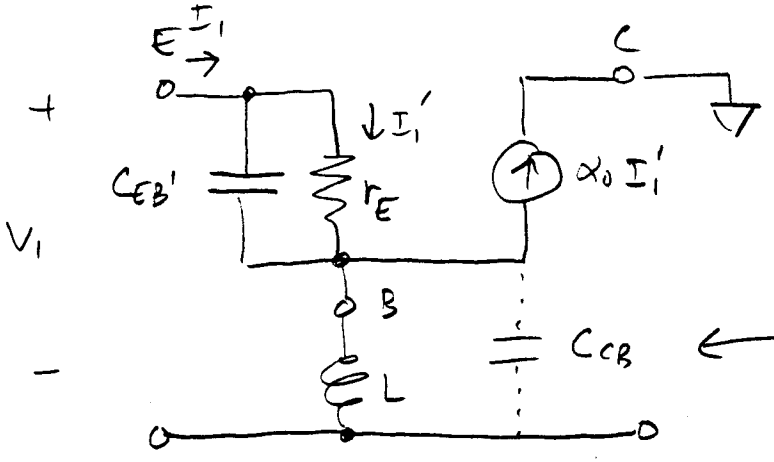
$$s = -\frac{1}{2C}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \pm \frac{1}{2}\sqrt{\frac{1}{C^2}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4}{LC}}$$

$R_2 > |R_1|$ for RHP poles.

Two terminal devices can be made to present one-port negative resistance through use of reactive feedback.

Ex. CB BJT with common base inductance

Find Z_{IN}



will limit upper freq. must remain inductive

$$\omega < \frac{1}{\sqrt{L C_{CB}}}$$

$$V_1 = I_1' r_E + j\omega (I_1 - \alpha_0 I_1')$$

$$I_1' = I_1 \frac{1/r_E}{j\omega C_{EB'} + 1/r_E} = I_1 \frac{1}{1 + j\omega/\omega_T} \qquad \text{(current divider)}$$

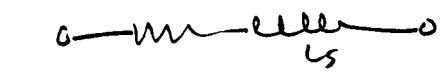
$$\text{So, } Z_{IN} = \frac{V_1}{I_1} = \frac{r_E}{1 + j\omega/\omega_T} + j\omega L - \frac{j\alpha_0 \omega L}{1 + j\omega/\omega_T}$$

rearranging:

$$Z_{IN} = \frac{r_E}{1 + (\omega/\omega_T)^2} \left(1 - \alpha_0 \omega^2 L C_{EB'}\right) + j\left[\omega L - \frac{\alpha_0 \omega L + r_E \omega/\omega_T}{1 + (\omega/\omega_T)}\right]$$

↑ negative real part when $\omega > \frac{1}{\sqrt{\quad}}$ and $\alpha_0 \cong 1$

Z_{IN} looks like $-R_S$ in series with inductance.



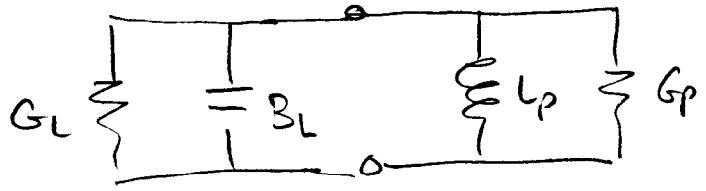
Now, we must provide resonator that

$$jB_D = -jB_L$$

and $$|G_D| \geq G_L$$

$$R_S = Re\{Z_{in}\}$$

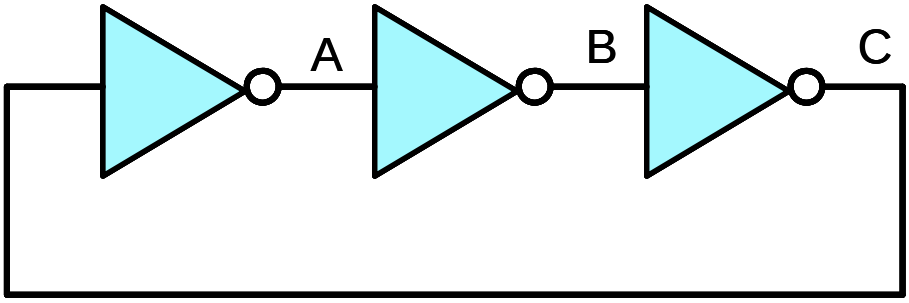
$$G_p = \frac{R_S}{R_S^2 + (\omega L_S)^2} \qquad L_p = \frac{(\omega L_S)^2 + R_S^2}{(\omega L_S)^2}$$

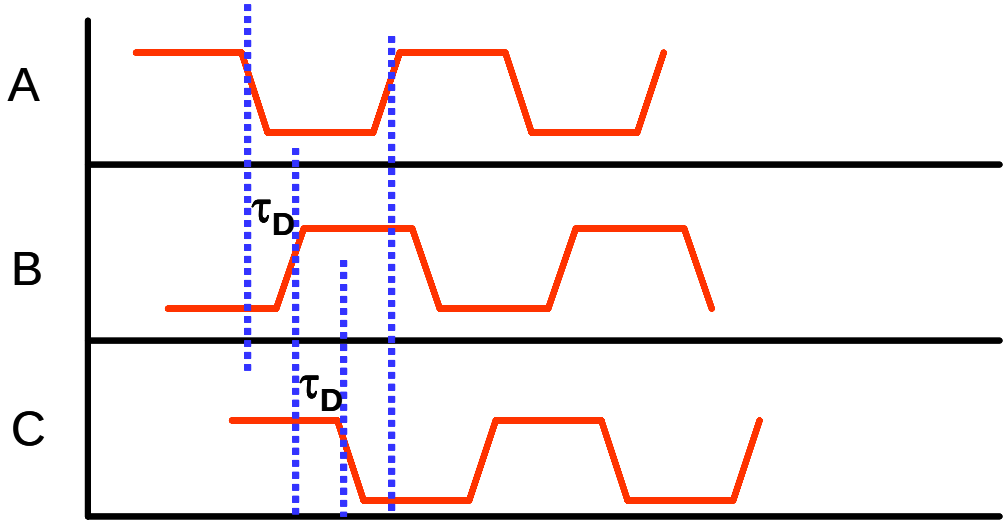


Ring Oscillators

An oscillator can be made by connecting an odd number of inverting gain stages in a ring. In order to start, the total loop gain must be greater than 1.

Ring Oscillator



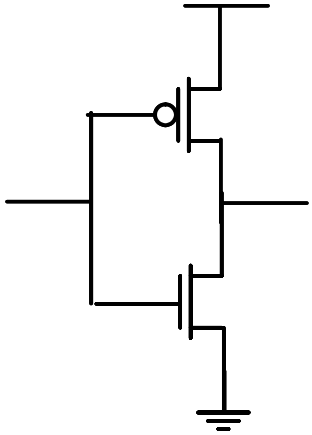


Period of oscillation: $$T = \frac{1}{n\tau_D}$$

Where n = number of stages

Implementation of Ring Oscillators:

CMOS Inverter

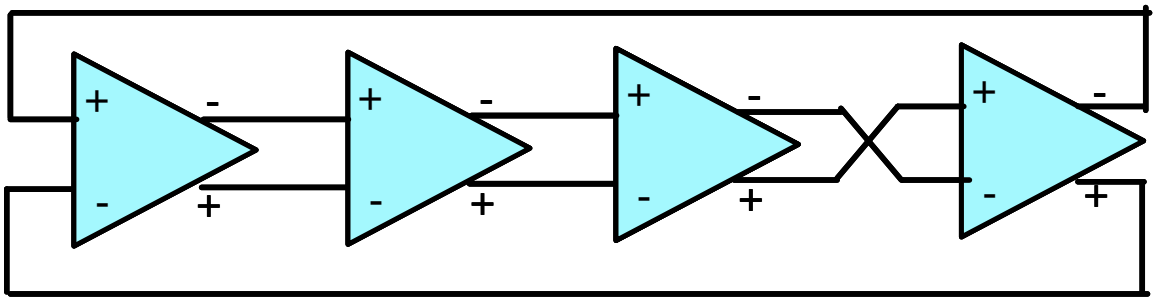


The CMOS inverter is a simple way of implementing a ring oscillator. We must have an odd number of stages. Otherwise, it forms a latch that hangs at either high or low.

Because ring oscillators are mainly used in mixed signal ICs where baseband digital and analog RF share the same die, a differential implementation is much more frequently utilized.

- Common mode rejection of substrate coupled noise
- Easy to control the delay
- Can use an odd or even number of stages

"Twisted Ring" Differential Ring Oscillator



Implementation of Differential Delay Cell:

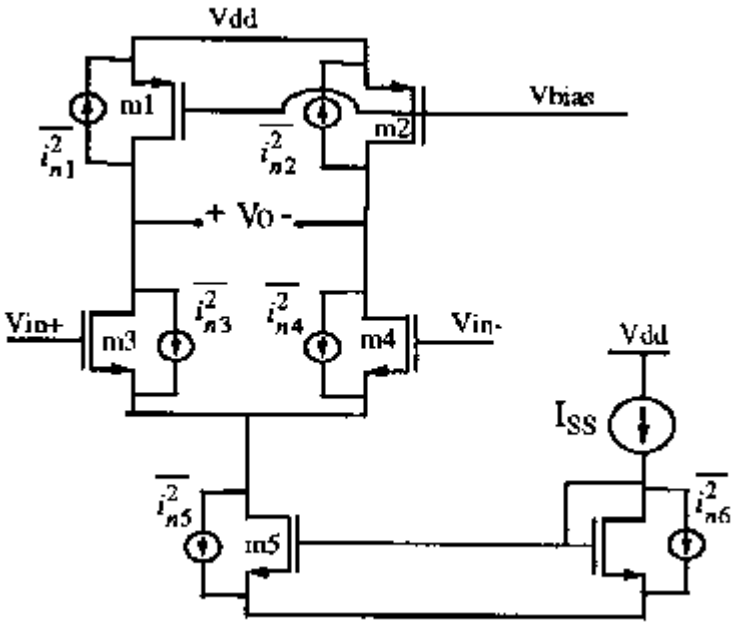


Figure 2. Differential delay cell with noise sources [1]

ISS is used to control the time delay through the cell. Noise sources are shown. The noise adds to the timing jitter produced by oscillator phase noise. The jitter occurs because of random phase variations that are converted to time delays at the crossover point as shown below.

[1] T. Weigandt, et al, Analysis of Timing Jitter in CMOS Ring Oscillators, IEEE Int. Symp. On Circuits and Systems, Paper 4.27, June 1994.

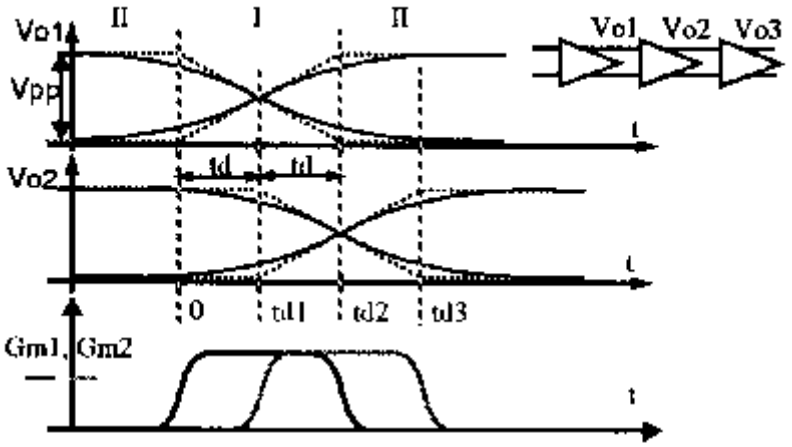
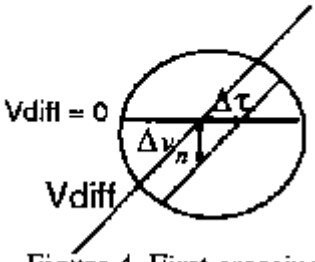


Figure 3. Output waveforms for CMOS inverter chain



$$\overline{\Delta\tau^2} = \frac{\overline{\Delta v_n^2}}{(\text{Slew Rate})^2}$$

Figure 4. First crossing approximation for timing jitter

When located in a phase locked loop, the oscillator frequency and phase are controlled by a filtered output from the phase detector. This output is proportional to the difference between the reference phase and the VCO phase and sets the delay of the oscillator loop.

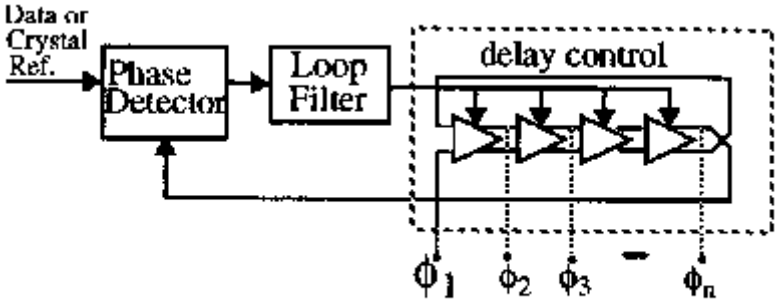


Figure 1. Ring-oscillator phase-locked-loop with multi-phase sampling