Hybrid Memory Cube
CONSORTIUM

Draft Specification Review Work Committee: Webinar Meeting

Introductions – Ground Rules

Participation:

- All lines will be muted except the speaker
- Please submit questions using the “Chat” field in the tool box
  - Questions will be captured for further response following the meeting
  - Select questions may be addressed during the call depending on time available
- HMCC Administration is available via chat and will respond as they are able

Introductions

Hybrid Memory Cube Officers:

- Chair: Mike Black, Micron Technology, Inc.
- Protocol Work Committee Chair: Jay Walstrum, Micron Technology, Inc.
- VSR Phy Work Committee Chair: Mike Li, Altera Corporation
- Secretary & Administration: Casey Kanen, VTM Group

Draft Specification Review Work Committee:

- Chair: Mike Black, Micron Technology, Inc.
- Secretary: Casey Kanen, VTM Group
- Protocol Speaker: Jay Walstrum, Micron Technology, Inc.
- Phy Speaker: Mike Li, Altera Corporation

HMCC Mission

HMCC Mission

To promote widespread adoption and acceptance of an industry standard serial interface and protocol for the Hybrid Memory Cube

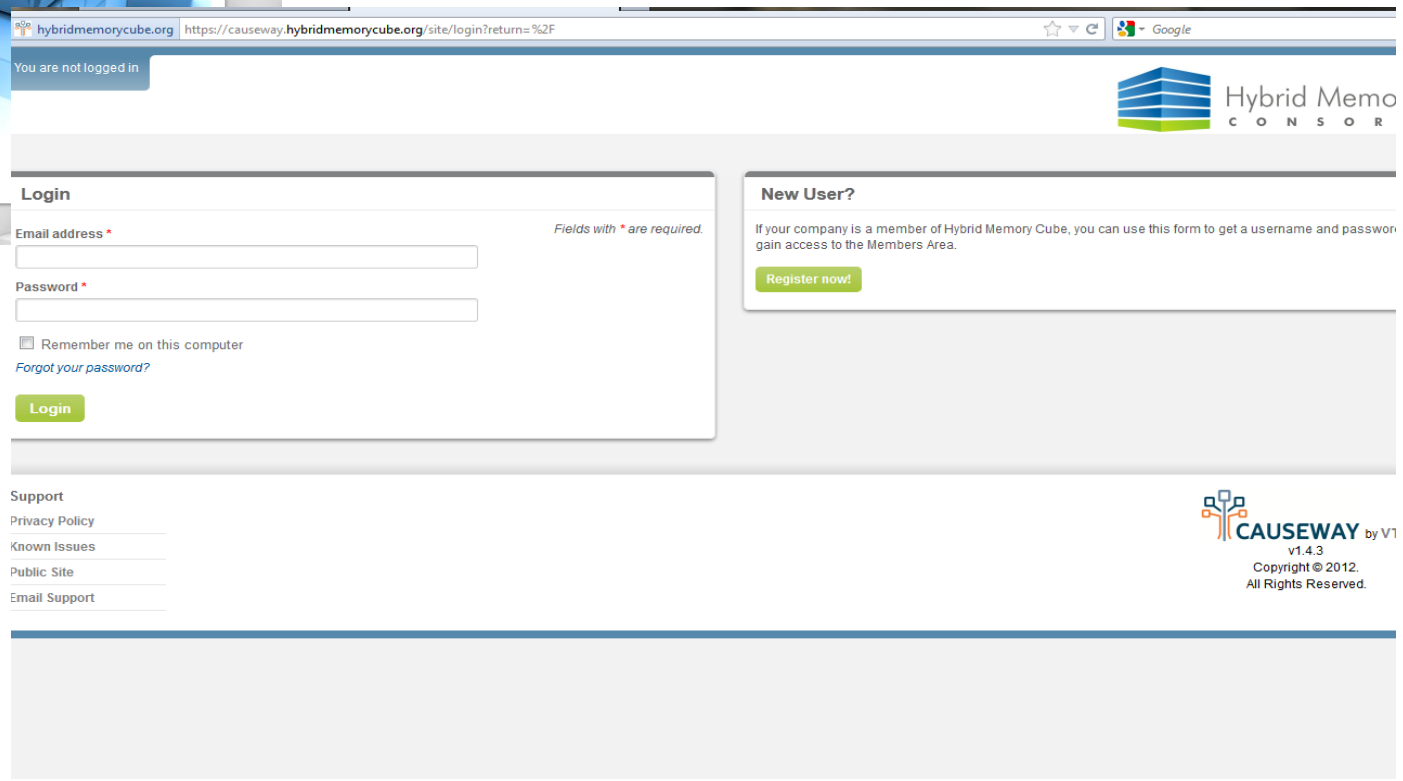
Log into hybridmemorycube.org to become an

Adopter and get into the game!

Causeway Tutorial: Log-In

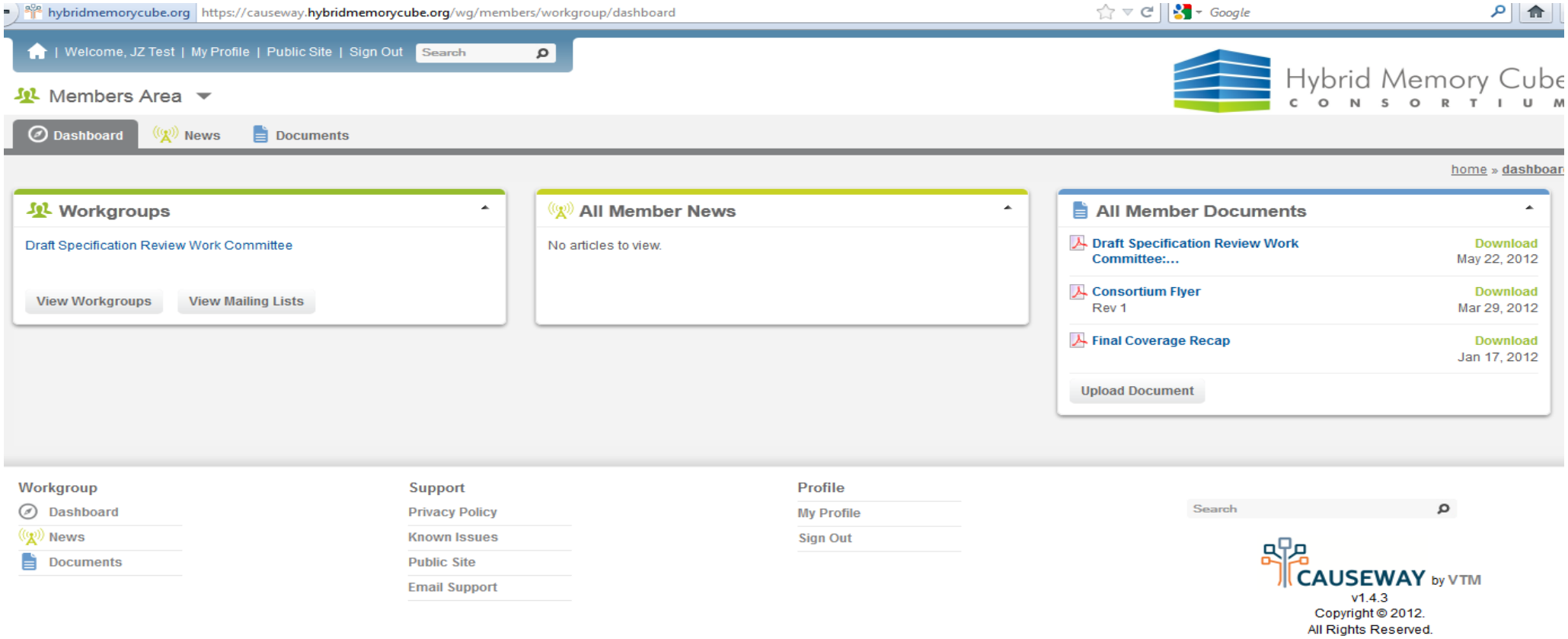
Visit: hybridmemorycube.org

Click on “Login” in the upper right



Enter credentials from HMCC Admin

Causeway Tutorial: Committee Access

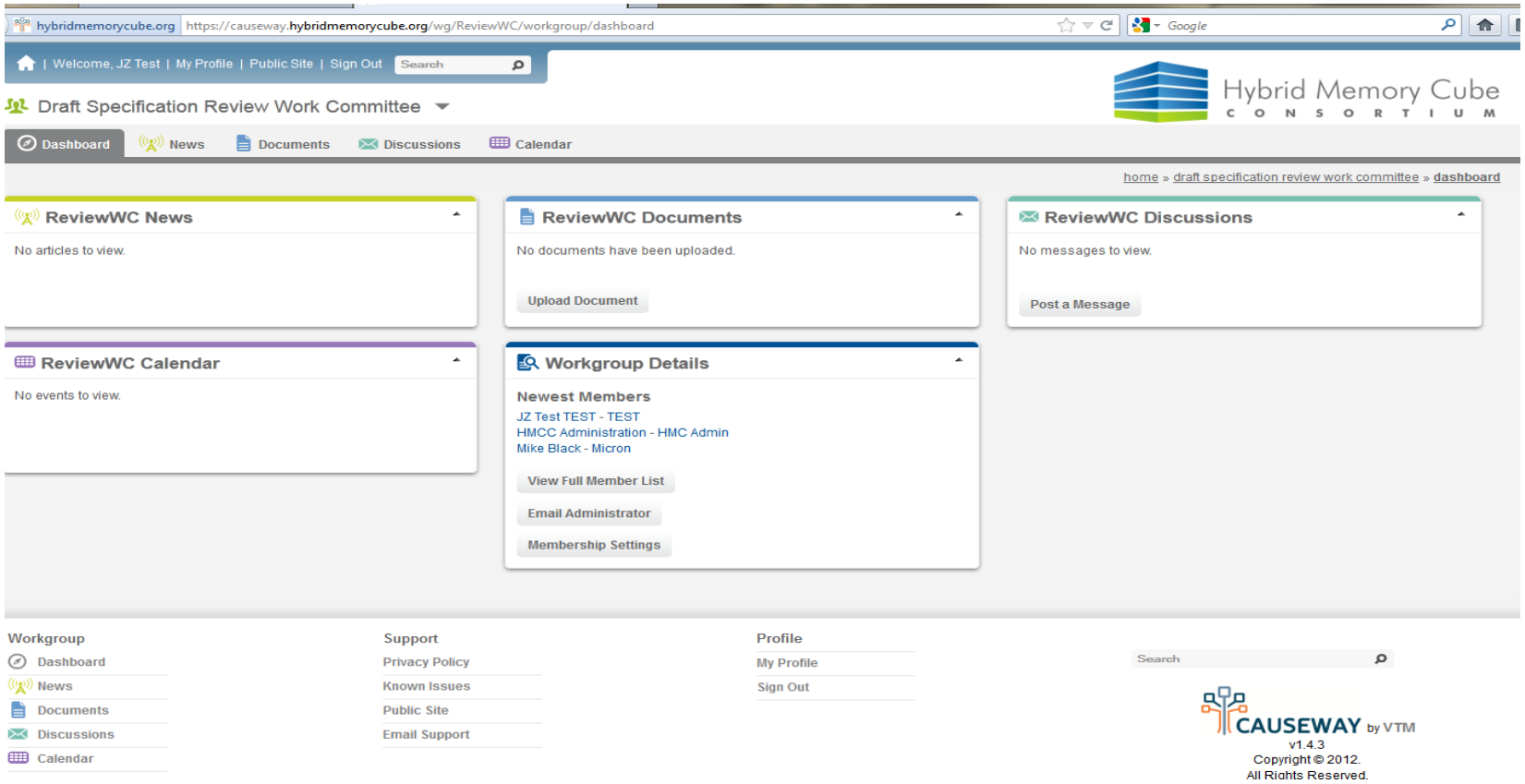


In the left select “Draft Specification Review Work Committee” OR

Click the Drop Down next to Members Area to Select the Committee

Note: If you do not see these options contact admin@hybridmemorycube.org

Causeway Tutorial: Modules



- News – Post articles to share
- Documents – Post markup or draft documents with version and check out controls
- Discussions – Archive and Online portal to Email the entire workgroup
- Calendar – Track upcoming meetings or event participation
- Details – Contact other engaged Adopters directly

HMCC Specifications

Analytics:

- Spec 2.0 was release mid-November, 2014
- Since then, the specification has been downloaded over 1,600 times
- Download version 2.0 today!
  - Visit http://www.hybridmemorycube.org/specification-v2-download-form/
  - Fill in your Name, Email, and Company Information to receive your copy

Spec 2.1

- Currently being revised now and will be available to the general public online once it has undergone its draft review by HMCC Adopters.
- Want to be first to personally review the draft? Become an HMCC Adopter today!

Questions?

Draft Specification Review: Protocol Committee

Jay Walstrum, Micron Technologies, Inc.

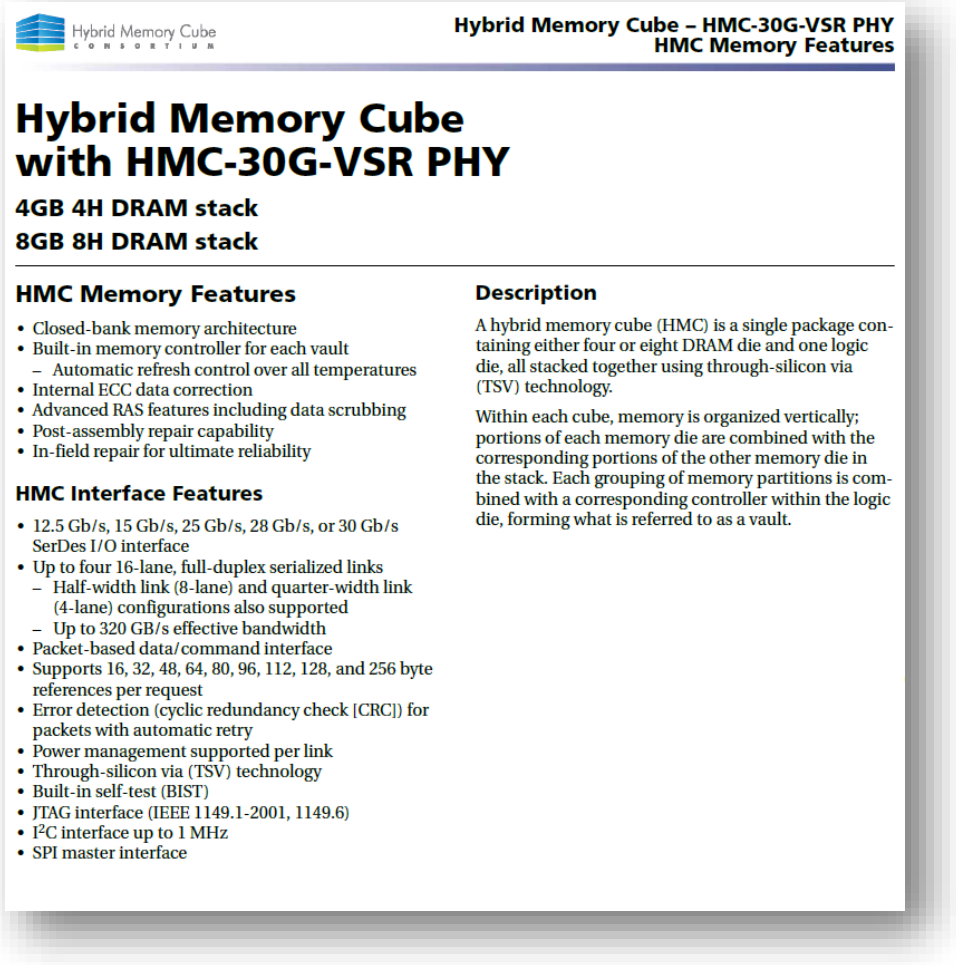
Agenda on Protocol

- Overview
- Architecture
- Power State Management
- Protocol Packet Format
- Memory Addressing
- Error Management and Health Monitor
- Package Options
- What's next!

HMCC 2.0 Specification

Double the bandwidth, Double the density

- Focus of Review today
  - Key differences with 1.1
  - FAQ's received
- HMCC Spec
  - Device Operation Guidelines
  - Vendor Implementation allows for flexibility



Hybrid Memory Cube CONSORTIUM

Hybrid Memory Cube – HMC-30G-VSR PHY
HMC Memory Features

Hybrid Memory Cube with HMC-30G-VSR PHY

4GB 4H DRAM stack
8GB 8H DRAM stack

HMC Memory Features

- Closed-bank memory architecture
- Built-in memory controller for each vault
  - Automatic refresh control over all temperatures
- Internal ECC data correction
- Advanced RAS features including data scrubbing
- Post-assembly repair capability
- In-field repair for ultimate reliability

HMC Interface Features

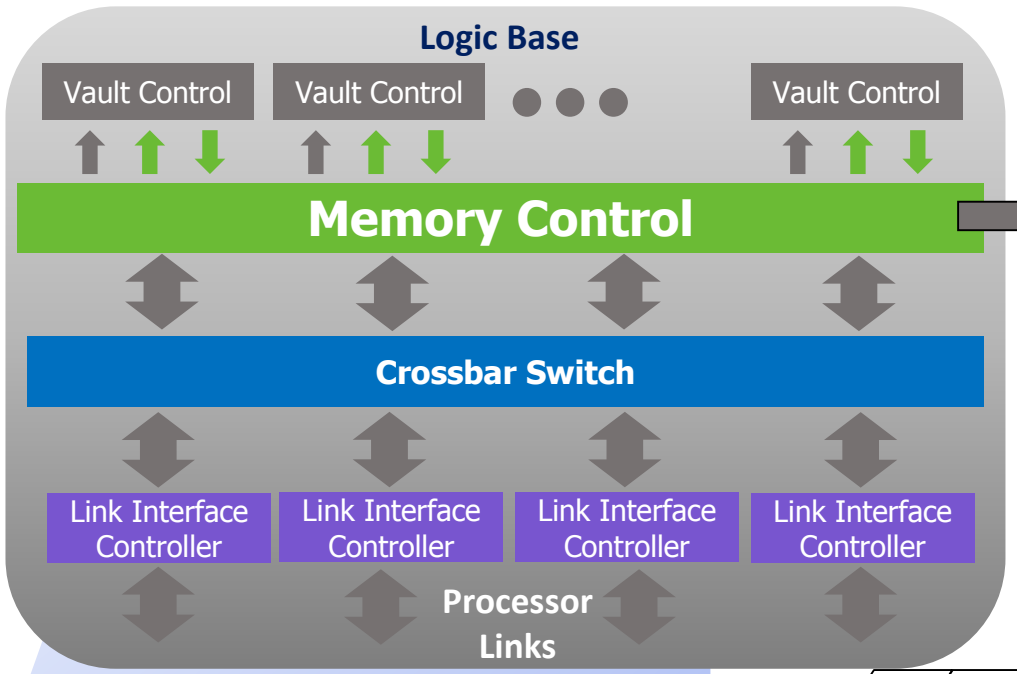
- 12.5 Gb/s, 15 Gb/s, 25 Gb/s, 28 Gb/s, or 30 Gb/s SerDes I/O interface
- Up to four 16-lane, full-duplex serialized links
  - Half-width link (8-lane) and quarter-width link (4-lane) configurations also supported
  - Up to 320 GB/s effective bandwidth
- Packet-based data/command interface
- Supports 16, 32, 48, 64, 80, 96, 112, 128, and 256 byte references per request
- Error detection (cyclic redundancy check [CRC]) for packets with automatic retry
- Power management supported per link
- Through-silicon via (TSV) technology
- Built-in self-test (BIST)
- JTAG interface (IEEE 1149.1-2001, 1149.6)
- I^2C interface up to 1 MHz
- SPI master interface

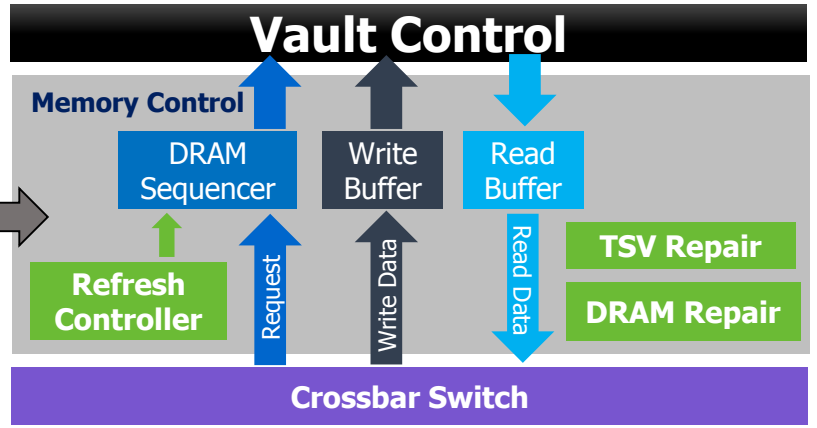
Description

A hybrid memory cube (HMC) is a single package containing either four or eight DRAM die and one logic die, all stacked together using through-silicon via (TSV) technology.

Within each cube, memory is organized vertically; portions of each memory die are combined with the corresponding portions of the other memory die in the stack. Each grouping of memory partitions is combined with a corresponding controller within the logic die, forming what is referred to as a vault.

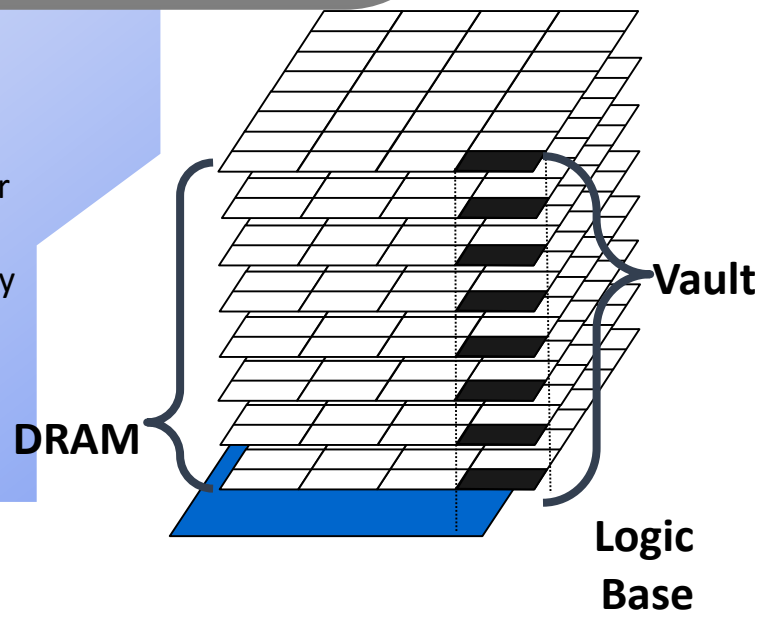
HMC Architecture





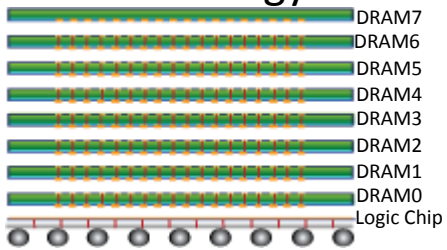
Logic Base

- Multiple high-speed local buses for data movement
- Advanced memory controller functions
- DRAM control at the memory rather than at distant host controller
- Reduced memory controller complexity and increased efficiency



Detail of Memory Interface

3DI & TSV Technology



Vaults are managed to maximize overall device availability -

- Optimized management of energy and refresh
- Self test, error detection, correction, and repair in the logic base layer

HMCC 2.0 Spec Configuration Options

HMC Configuration Options

Description	HMCC 2.0 Spec Configuration Options	HMCC 1.1 Spec Comparison
Max Line Rate/Phy Technology	**30Gb/s VSR (Very Short Reach)**	15Gb/s SR (Short Reach)
Number of links in package	**2, 4**	2, 4,
Link Lane Speed (Gbps)	**12.5, 15, 25, 28, 30**	10, 12.5, 15
Link Width	**Full, Half, Quarter**	Full, Half
Memory Density	**4GB, 8GB**	2GB, 4GB
Number of Vaults	**32**	16
Memory Banks	**4GB: 256 banks; 8GB: 512 banks**	2GB: 128 banks 4GB: 256 banks
Max Aggregate link bandwidth	**480GB/s (3.84Tb/s)**	240GB/s (1.92Tb/s)
Max DRAM Data bandwidth	**320GB/s (2.56Tb/s)**	160GB/s (1.28Tb/s)
Max Vault data Bandwidth	**10GB/s (80Gb/s)**	10GB/s (80Gb/s)

New Pins Descriptions

- Side band: I2C, JTAG
- New SPI
- New REFCLK
- Voltage Supplies

I²C Interface		
SCL	Bidirectional	I²C clock
SDA		

JTAG Interface		
TMS	Input	JTAG test mode select
TCK	Input	JTAG test mode clock
TDI	Input	JTAG test data-in
TDO	Output	JTAG test data-out
TRST_N	Input	JTAG test reset (active LOW)

SPI Master Interface		
SCK	Output	Serial clock
SDO	Output	Serial data output
SDI	Input	Serial data input
SS_N	Output	Chip select or slave select (active LOW)

REFCLK_BOOT[1:0]	Input	Bootstrapping pins that enable autonomous PLL configuration. Tie pins DC HIGH or DC LOW to match reference clock frequency being used. DC HIGH ≥ (V_{DDK} - 0.5V) and DC LOW ≤ (V_{SS} + 0.5V)

REFCLK_BOOT[1:0]	Reference Clock Frequency
00	125 MHz
01	156.25 MHz
10	[illegible]
11	312.50 MHz

REFCLK = 312.5Mhz

Supply Pins		
V_{DD}	Supply	Logic core supply: 0.9V ±0.027V
AV_{DD}	Supply	PHY core supply: 0.9V ±0.027V
V_{DDM}	Supply	DRAM supply: 1.1V ±0.03V
V_{PP}	Supply	DRAM wordline boost supply: 1.8V ±0.090V
V_{DDK}	Supply	GPIO, side-band control supply: 1.8V ±0.090V

“Link Retraining” mode

- New Power state mode to:
  - Fix link BER issues
  - Change link width, or line rate

Table 8: Link Power States and Conditions

Mode	Method of Entry	HMC Tx Lane Status	HMC Rx Lane Status	Link PLL Status
Active	Standard initialization	Enabled	Enabled	Enabled
Link retraining	LxRXPS asserted LOW while in active mode Held LOW for a minimum of <TBD> and released back to HIGH prior to 1ms	Pulled HIGH or LOW	Disabled	Enabled
Sleep	LxRXPS asserted LOW while in active mode Held LOW for a minimum of 1ms ($^{t}SREF^{3}$)	Pulled HIGH or LOW	Disabled	Enabled
Down	1) LxRXPS asserted LOW when P_RST_N transitions from LOW to HIGH; or 2) After the last link in active mode enters sleep mode (all other links already in sleep or down mode)	Pulled HIGH or LOW	Disabled	Disabled

new

1.1 to 2.0 spec Difference summary

Protocol Changes from 1.1 to 2.0 specification

Protocol Description	HMCC 2.0 Spec	HMCC 1.1 Spec
Duplicate Length (DLN)	-	4
Request Command (CMD)	**128 possible Requests (7 bits)**	64 possible requests (6 bits)
Request Tags (TAG)	**2048 tags (11 bits)**	512 Tags (9 bits)
Return Token Count (RTC)	**Encoded 3 bits**	5 bits – 32 absolute values
Forward Retry Pointer(FRP) Return Retry Pointer(RRP)	**512 Retry Buffer size (9 bits)**	256 Retry Buffer Size (8 bits)
Atomic Return Flag	**1 bit returned**	-
Data Packet Payload	**1.1 spec plus Added 256B**	16B Increments from 16B to 128B

Other Changes from 1.1 to 2.0 specification

Protocol Description	HMCC 2.0 Spec	HMCC 1.1 Spec
Scrambler	**PRBS31 (and PRBS15)**	PRBS15
Run Length Limit	**100 UI**	85 UI
Training Sequence (TS1)	**TS1 char every, every other, every 4th sequence**	TS1 char every sequence
Address Map mode	**Added 256 Max Byte Block size**	32, 64, 128 Max Byte Block Size
Atomics	**25**	6

Atomics

Boolean – Arithmetic – Comparisons – Bit operations

Spec 1.1 & 2.0

- Read-Modify-Write
  - No return data
  - No return flags

Read	•Go to request address •Read data value at the address
Modify	•Execute action specified by request
Write	•Write resulting value into DRAM

New in Spec 2.0

- Read-Modify-Write with Return
  - Return Original content
  - Return Flags

Read	• Go to request address • Read data value at the address
Modify	• Execute action specified by request
Write	• Write resulting value back into that location
Return	• Return Original DRAM Data to host

Atomic List

Arithmetic	BitWise	Boolean	Comparison
Dual 8-byte signed Add immediate*	16-byte Swap (Exchange)	16-byte AND (Read & Clear, Bitwise clear)	8-byte Compare & Swap if Equal
Dual 8-byte signed Add immediate with return	8-byte bit write*	16-byte NAND	16-byte Compare & Swap if Zero
Single 16-byte signed Add immediate*	8-byte bit write with return	16-byte NOR	Compare & Swap if Less Than (8-byte; 16-byte)
Single 16-byte signed Add immediate with return	-	16-byte OR (Bitwise set)	Compare & Swap if Greater Than (8-byte; 16-byte)
8-byte Increment	-	16-byte XOR (Bitwise toggle)	Compare if Equal (8-byte; 16-byte)

Address Map

Revision 1.1

Current 4GB memory map Protocol Revision 1.1

Request Address Bits	HMC-15G-SR REV1.0 Protocol 4GB 32-Byte Max Block Size	64-Byte Max Block Size	128-Byte Max Block Size
32			
31	DRAM[19]	DRAM[19]	DRAM[19]
30	DRAM[18]	DRAM[18]	DRAM[18]
29	DRAM[17]	DRAM[17]	DRAM[17]
28	DRAM[16]	DRAM[16]	DRAM[16]
27	DRAM[15]	DRAM[15]	DRAM[15]
26	DRAM[14]	DRAM[14]	DRAM[14]
25	DRAM[13]	DRAM[13]	DRAM[13]
24	DRAM[12]	DRAM[12]	DRAM[12]
23	DRAM[11]	DRAM[11]	DRAM[11]
22	DRAM[10]	DRAM[10]	DRAM[10]
21	DRAM[9]	DRAM[9]	DRAM[9]
20	DRAM[8]	DRAM[8]	DRAM[8]
19	DRAM[7]	DRAM[7]	DRAM[7]
18	DRAM[6]	DRAM[6]	DRAM[6]
17	DRAM[5]	DRAM[5]	DRAM[5]
16	DRAM[4]	DRAM[4]	DRAM[4]
15	DRAM[3]	DRAM[3]	DRAM[3]
14	DRAM[2]	DRAM[2]	Bank[3]
13	DRAM[1]	Bank[3]	Bank[2]
12	Bank[3]	Bank[2]	Bank[1]
11	Bank[2]	Bank[1]	Bank[0]
10	Bank[1]	Bank[0]	Vault[3]
9	Bank[0]	Vault[3]	Vault[2]
8	Vault[3]	Vault[2]	Vault[1]
7	Vault[2]	Vault[1]	Vault[0]
6	Vault[1]	Vault[0]	Byte[6]=DRMA[2]
5	Vault[0]	Byte[5]=DRMA[1]	Byte[5]=DRMA[1]
4	Byte[4]=DRMA[0]	Byte[4]=DRMA[0]	Byte[4]=DRMA[0]
3	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored
2	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored
1	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored
0	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored

4 bank bits

4 vault bits

- Intended to
  - Keep address bits in same location in request header
  - Keep default address map similar

Address Map

Current 4GB memory map Protocol Revision 1.1

New 4GB memory map Protocol Revision 2.0

	Revision 1.1			Revision 2.0			
	4GB			4GB			
Request Address Bits	32-Byte Max Block Size	64-Byte Max Block Size	128-Byte Max Block Size	32-Byte Max Block Size	64-Byte Max Block Size	128-Byte Max Block Size	256-Byte Max Block Size
32	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored
31	DRAM[19]	DRAM[19]	DRAM[19]	DRAM[19]	DRAM[19]	DRAM[19]	DRAM[19]
30	DRAM[18]	DRAM[18]	DRAM[18]	DRAM[18]	DRAM[18]	DRAM[18]	DRAM[18]
29	DRAM[17]	DRAM[17]	DRAM[17]	DRAM[17]	DRAM[17]	DRAM[17]	DRAM[17]
28	DRAM[16]	DRAM[16]	DRAM[16]	DRAM[16]	DRAM[16]	DRAM[16]	DRAM[16]
27	DRAM[15]	DRAM[15]	DRAM[15]	DRAM[15]	DRAM[15]	DRAM[15]	DRAM[15]
26	DRAM[14]	DRAM[14]	DRAM[14]	DRAM[14]	DRAM[14]	DRAM[14]	DRAM[14]
25	DRAM[13]	DRAM[13]	DRAM[13]	DRAM[13]	DRAM[13]	DRAM[13]	DRAM[13]
24	DRAM[12]	DRAM[12]	DRAM[12]	DRAM[12]	DRAM[12]	DRAM[12]	DRAM[12]
23	DRAM[11]	DRAM[11]	DRAM[11]	DRAM[11]	DRAM[11]	DRAM[11]	DRAM[11]
22	DRAM[10]	DRAM[10]	DRAM[10]	DRAM[10]	DRAM[10]	DRAM[10]	DRAM[10]
21	DRAM[9]	DRAM[9]	DRAM[9]	DRAM[9]	DRAM[9]	DRAM[9]	DRAM[9]
20	DRAM[8]	DRAM[8]	DRAM[8]	DRAM[8]	DRAM[8]	DRAM[8]	DRAM[8]
19	DRAM[7]	DRAM[7]	DRAM[7]	DRAM[7]	DRAM[7]	DRAM[7]	DRAM[7]
18	DRAM[6]	DRAM[6]	DRAM[6]	DRAM[6]	DRAM[6]	DRAM[6]	DRAM[6]
17	DRAM[5]	DRAM[5]	DRAM[5]	DRAM[5]	DRAM[5]	DRAM[5]	DRAM[5]
16	DRAM[4]	DRAM[4]	DRAM[4]	DRAM[4]	DRAM[4]	DRAM[4]	DRAM[4]
15	DRAM[3]	DRAM[3]	DRAM[3]	DRAM[3]	DRAM[3]	DRAM[3]	Bank[2]
14	DRAM[2]	DRAM[2]	Bank[3]	DRAM[2]	DRAM[2]	Bank[2]	Bank[1]
13	DRAM[1]	Bank[3]	Bank[2]	DRAM[1]	Bank[2]	Bank[1]	Bank[0]
12	Bank[3]	Bank[2]	Bank[1]	Bank[2]	Bank[1]	Bank[0]	Vault[4]
11	Bank[2]	Bank[1]	Bank[0]	Bank[1]	Bank[0]	Vault[4]	Vault[3]
10	Bank[1]	Bank[0]	Vault[3]	Bank[0]	Vault[4]	Vault[3]	Vault[2]
9	Bank[0]	Vault[3]	Vault[2]	Vault[4]	Vault[3]	Vault[2]	Vault[1]
8	Vault[3]	Vault[2]	Vault[1]	Vault[3]	Vault[2]	Vault[1]	Vault[0]
7	Vault[2]	Vault[1]	Vault[0]	Vault[2]	Vault[1]	Vault[0]	Byte[7]=DRAM[3]
6	Vault[1]	Vault[0]	Byte[6]=DRAM[2]	Vault[1]	Vault[0]	Byte[6]=DRAM[2]	Byte[6]=DRAM[2]
5	Vault[0]	Byte[5]=DRAM[1]	Byte[5]=DRAM[1]	Vault[0]	Byte[5]=DRAM[1]	Byte[5]=DRAM[1]	Byte[5]=DRAM[1]
4	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]
3	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored
2	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored
1	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored
0	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored

3 bank bits

4 bank bits

5 vault bits

4 vault bits

Address Map

Proposed Default Address map Protocol Revision 2.0 4GB & 8GB

Revision 2.0

4GB				8GB			
32-Byte Max Block Size	64-Byte Max Block Size	128-Byte Max Block Size	256-Byte Max Block Size	32-Byte Max Block Size	64-Byte Max Block Size	128-Byte Max Block Size	256-Byte Max Block Size
Ignored	Ignored	Ignored	Ignored	DRAM[19]	DRAM[19]	DRAM[19]	DRAM[19]
DRAM[19]	DRAM[19]	DRAM[19]	DRAM[19]	DRAM[18]	DRAM[18]	DRAM[18]	DRAM[18]
DRAM[18]	DRAM[18]	DRAM[18]	DRAM[18]	DRAM[17]	DRAM[17]	DRAM[17]	DRAM[17]
DRAM[17]	DRAM[17]	DRAM[17]	DRAM[17]	DRAM[16]	DRAM[16]	DRAM[16]	DRAM[16]
DRAM[16]	DRAM[16]	DRAM[16]	DRAM[16]	DRAM[15]	DRAM[15]	DRAM[15]	DRAM[15]
DRAM[15]	DRAM[15]	DRAM[15]	DRAM[15]	DRAM[14]	DRAM[14]	DRAM[14]	DRAM[14]
DRAM[14]	DRAM[14]	DRAM[14]	DRAM[14]	DRAM[13]	DRAM[13]	DRAM[13]	DRAM[13]
DRAM[13]	DRAM[13]	DRAM[13]	DRAM[13]	DRAM[12]	DRAM[12]	DRAM[12]	DRAM[12]
DRAM[12]	DRAM[12]	DRAM[12]	DRAM[12]	DRAM[11]	DRAM[11]	DRAM[11]	DRAM[11]
DRAM[11]	DRAM[11]	DRAM[11]	DRAM[11]	DRAM[10]	DRAM[10]	DRAM[10]	DRAM[10]
DRAM[10]	DRAM[10]	DRAM[10]	DRAM[10]	DRAM[9]	DRAM[9]	DRAM[9]	DRAM[9]
DRAM[9]	DRAM[9]	DRAM[9]	DRAM[9]	DRAM[8]	DRAM[8]	DRAM[8]	DRAM[8]
DRAM[8]	DRAM[8]	DRAM[8]	DRAM[8]	DRAM[7]	DRAM[7]	DRAM[7]	DRAM[7]
DRAM[7]	DRAM[7]	DRAM[7]	DRAM[7]	DRAM[6]	DRAM[6]	DRAM[6]	DRAM[6]
DRAM[6]	DRAM[6]	DRAM[6]	DRAM[6]	DRAM[5]	DRAM[5]	DRAM[5]	DRAM[5]
DRAM[5]	DRAM[5]	DRAM[5]	DRAM[5]	DRAM[4]	DRAM[4]	DRAM[4]	DRAM[4]
DRAM[4]	DRAM[4]	DRAM[4]	DRAM[4]	DRAM[3]	DRAM[3]	DRAM[3]	Bank[3]
DRAM[3]	DRAM[3]	DRAM[3]	Bank[2]	DRAM[2]	DRAM[2]	Bank[3]	Bank[2]
DRAM[2]	DRAM[2]	Bank[2]	Bank[1]	DRAM[1]	Bank[3]	Bank[2]	Bank[1]
DRAM[1]	Bank[2]	Bank[1]	Bank[0]	Bank[3]	Bank[2]	Bank[1]	Bank[0]
Bank[2]	Bank[1]	Bank[0]	Vault[4]	Bank[2]	Bank[1]	Bank[0]	Vault[4]
Bank[1]	Bank[0]	Vault[4]	Vault[3]	Bank[1]	Bank[0]	Vault[4]	Vault[3]
Bank[0]	Vault[4]	Vault[3]	Vault[2]	Bank[0]	Vault[4]	Vault[3]	Vault[2]
Vault[4]	Vault[3]	Vault[2]	Vault[1]	Vault[4]	Vault[3]	Vault[2]	Vault[1]
Vault[3]	Vault[2]	Vault[1]	Vault[0]	Vault[3]	Vault[2]	Vault[1]	Vault[0]
Vault[2]	Vault[1]	Vault[0]	Byte[7]=DRAM[3]	Vault[2]	Vault[1]	Vault[0]	Byte[7]=DRAM[3]
Vault[1]	Vault[0]	Byte[6]=DRAM[2]	Byte[6]=DRAM[2]	Vault[1]	Vault[0]	Byte[6]=DRAM[2]	Byte[6]=DRAM[2]
Vault[0]	Byte[5]=DRAM[1]	Byte[5]=DRAM[1]	Byte[5]=DRAM[1]	Vault[0]	Byte[5]=DRAM[1]	Byte[5]=DRAM[1]	Byte[5]=DRAM[1]
Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]	Byte[4]=DRAM[0]
Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored	Byte[3] = ignored
Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored	Byte[2] = ignored
Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored	Byte[1] = ignored
Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored	Byte[0] = ignored

System Health Monitor

- Integrity Checks on entire datapath: Host⇔DRAM⇔Host
  - Packet CRC from host through link to DRAM
  - CMD/ADRS parity checking
  - Retry on the bus to DRAM.
  - ECC on data to/from DRAM.
    - Detect/Correct SBE's
    - Detect/Correct failures on TSV (4 bit groups in 128 bit data)
    - Detect Multiple Uncorrectable Errors in DRAM and TSV

Error Reporting

Warnings, DRAM, Link, Protocol, Vault, Fatal

Table 17: ERRSTAT[6:0] Bit Definitions – No Errors

ERRSTAT Bit							Description	Response Packet Type
6	5	4	3	2	1	0		
0	0	0	0	0	0	0	No errors/conditions	

Table 18: ERRSTAT[6:0] Bit Definitions – Warnings

ERRSTAT Bit							Description	Response Packet Type
6	5	4	3	2	1	0		
0	0	0	0	0	0	1	Operational temperature threshold: The in-	Error response packet

Table 19: ERRSTAT[6:0] Bit Definitions – DRAM Errors

ERRSTAT Bit							Description	Response Packet Type	Notes
6	5	4	3	2	1	0			
0	0	1	0	0	0	0	SBE occurred (this status is normally disa-	Read or write response	1

Table 20: ERRSTAT[6:0] Bit Definitions – Link Errors

ERRSTAT Bit							Description	Response Packet Type
6	5	4	3	2	1	0		
0	1	0	0	0	0	0	Link 0 retry in progress: Link slave 0 has de-	Error response packet

Table 21: ERRSTAT[6:0] Bit Definitions – Protocol Errors

ERRSTAT Bit							Description	Response Packet Type	Notes
6	5	4	3	2	1	0			
0	1	1	0	0	0	0	Invalid command: An unsupported com-	Write response packet	

Table 22: ERRSTAT[6:0] Bit Definitions – Vault Critical Errors

ERRSTAT Bit							Description	Response Packet Type
6	5	4	3	2	1	0		
1	1	0	0	0	0	0	Vault 0 critical error: Command/Address	Error response packet

Table 23: ERRSTAT[6:0] Bit Definitions – Fatal Errors

ERRSTAT Bit							Description	Response Packet Type	Notes
6	5	4	3	2	1	0			
1	1	1	0	0	0	0	Link 0 retry failed and was unsuccessful after the retry limit was reached.	Error response packet (TAG = CUB number)	
1	1	1	0	0	0	1	Link 1 retry failed and was unsuccessful after the retry limit was reached.		
1	1	1	0	0	1	0	Link 2 retry failed and was unsuccessful		

Summary

- Double the Bandwidth, Double the density
- Leverage architecture and learning from 1.1
- Atomics – reduce Link traffic with more efficient commands
- Advanced Health Monitor and in field repair

2.1 Update coming soon

Questions?

HMC 30G-VSR Specification Overview

Mike Peng Li, Altera
Chair for 30G-VSR WC

Agenda

- Link
- TX
- RX
- Channel
- Reference clock

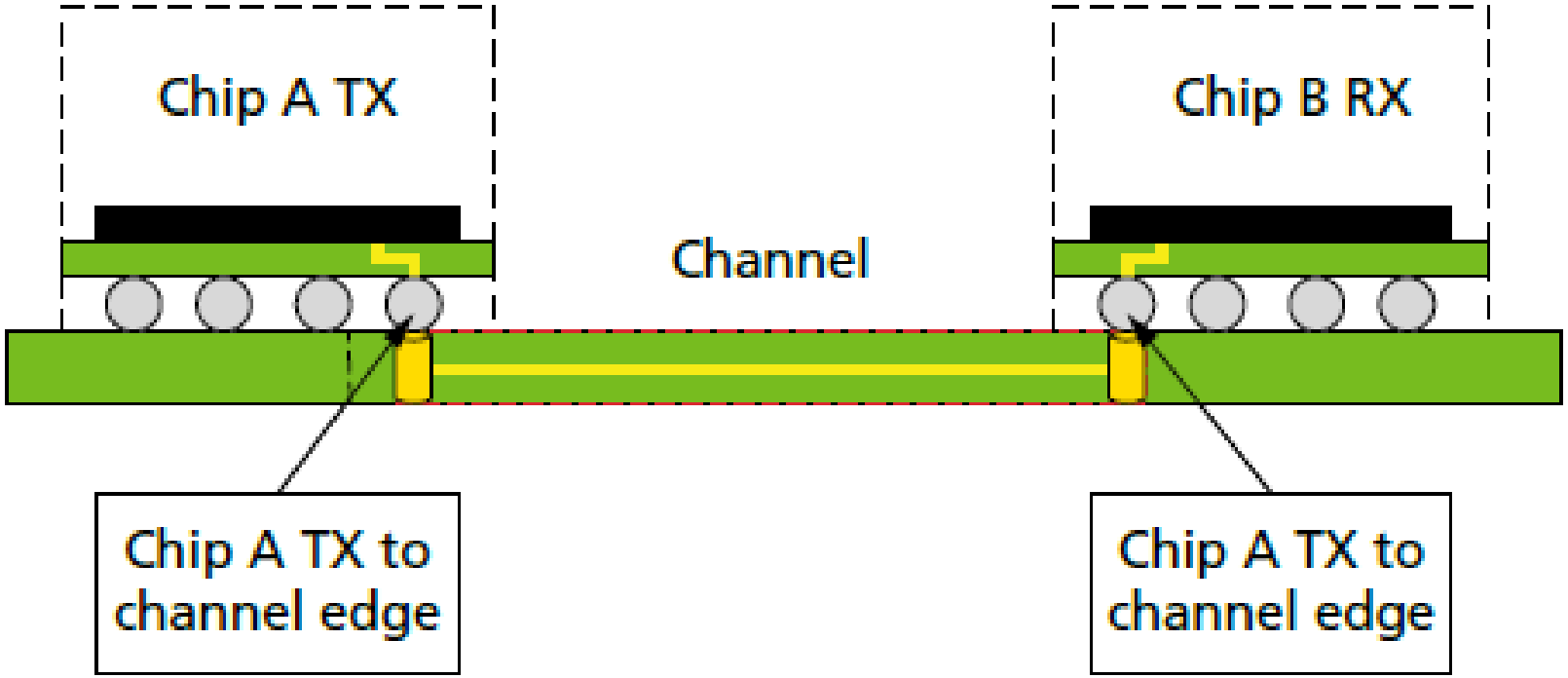
DC Electrical Characteristics

Table 105: DC Electrical Characteristics

Description	Parameter	Minimum (V)	Nominal (V)	Maximum (V)	Notes
Logic core supply	V_{DD}	0.873	0.9	0.927	1
Phy core supply	AV_{DD}	0.873	0.9	0.927	1, 2
DRAM supply	V_{DDM}	1.067	1.1	1.133	
DRAM wordline boost supply	V_{PP}	1.71	1.8	1.89	1, 2
GPIO, side-band control supply	V_{DDK}	1.71	1.8	1.89	
Analog Phy ground	AV_{SS}	–	0	–	
Ground	V_{SS}	–	0	–	

Notes:
1. See the vendor-specific HMC Design Users Guide for voltage supply regulation sharing restrictions.
2. Supplies may require filtering, refer to the vendor-specific HMC Design Users Guide for filtering information.
3. It is assumed that AV_{SS} and V_{SS} may be connected together at the board.

30G-VSR Link Topology



30G-VSR Link Configuration Examples

	2-Link	4-Link
Link Speed (Gbps)	15, 25, 30	15, 25, 30
Max Aggregated Link Bandwidth (Gbps)	120, 200, 240	240, 400, 480

Lane Rates Supported by 30G-VSR

Table 109: Synchronous Link Bit Rate Specifications

Notes 1–3 apply to the entire table

Parameter	Symbol	Value	Unit	Supported REFCLK (f_{REFCLK} = MHz)				Notes
				125	156.25	166.67	312.5	
Bit rate	BR12.5	12.5	Gb/s	Yes	Yes	Yes	Yes	
Bit rate	BR15	15.0	Gb/s	Yes	Yes	Yes	Yes	
Bit rate	BR25	25.0	Gb/s	Yes	Yes	Yes	Yes	
Bit rate	BR28	28.0	Gb/s	Yes	No	Yes	No	
Bit rate	BR30	30.0	Gb/s	Yes	Yes	Yes	Yes	

Notes:
1. Bit-rate tolerance is within ±100 ppm.
2. The link interface is synchronous, that is, the TX and RX run from the same reference clock.
3. Within a given link, all TX and Rx lanes can only run at one bit rate.

Link Coupling and Performance Parameters

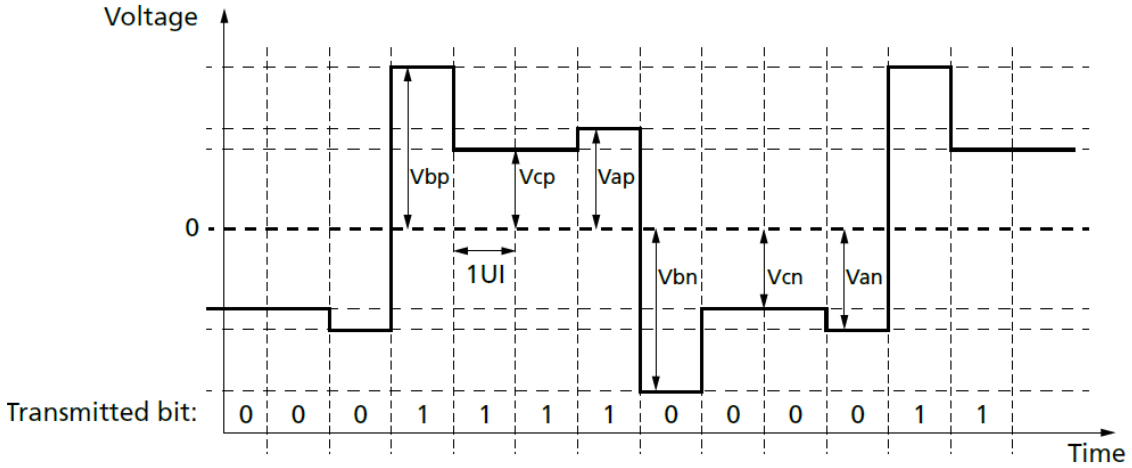
- Link Coupling
  - AC or DC
    - 0.1 μF is recommended for 30 Gbps
- Link Performance Parameters
  - Max Bit Rate
    - 30 Gbps
  - Bit Error Ratio (BER)
    - 1e-15

Link Equalization (I)

- TX
  - A 3-tap FFE equalizer

$$H(Z) = (C(-1)z^{+1} + C(0)z^{0} + C(+1)z^{-1})$$

  - Pre-tap, post-tap gains



$$TX_{pre\_gain} = 20\log10\left(\frac{V_{ap}-V_{an}}{V_{cp}-V_{cn}}\right) \quad (2)$$

$$TX_{post\_gain} = 20\log10\left(\frac{V_{bp}-V_{bn}}{V_{cp}-V_{cn}}\right) \quad (3)$$

  - Minimum pre-tap and post-tap gains
    - Pre: 2.5+-0.5 dB, 1.3 dB step
    - Post: 4.0+-0.5 dB, 1.6 dB step

Link Equalization (II)

- RX
  - A low-power CTLE
  - Recover the data at the BER target when worst TX (e.g., swing, jitter, noise, termination, FFE) and channel (e.g., IL, RL, and Xtalk) present

TX Specification (I)

Table 110: TX Signaling Parameters

Measurements are assumed to be at the package BGA ball; Parameters listed apply to HMC device only

Parameter	Symbol	Test Conditions/Comments	Min	Typical	Max	Unit	Notes
Link supply TX voltage	AV_{DD}	0.9V ±0.027V	0.873	0.9	0.927	V	1
Differential peak-to-peak output voltage	$V_{DIFF\_TX\ SWING}$	Measured with slow square wave (64 zeros followed by 64 ones) with ideal 100Ω differential termination	750 (with FFE off) 250 (with FFE on)	–	1025	mV	
Single-ended voltage (with respect to V_{SS}) on V_{TX_P}, V_{TX_N}	V_{TX_SE}	Active mode	0.2 × $AV_{DD,min}$	–	0.8 × $AV_{DD,max}$	V	
Down or sleep mode output voltage	V_{TX_PD}		AV_{SS}	–	AV_{DD}	mV	
DC common mode output voltage	V_{TX_CM}	V_{TX_CM} = DC of $\lvert V_{TX\_P} + V_{TX\_N} \rvert/2$	0.45 × $AV_{DD,min}$	$AV_{DD}/2$	0.55 × $AV_{DD,max}$	V	
AC common mode noise	$V_{TX\_CM\_NZ\ SQUARE\ WAVE}$	Measured with slow square wave output amplitude	–	–	50	mV_{PP}	
	$V_{TX\_CM\_NZ\ PRBS}$	Measured with PRBS15 data pattern	–	–	12	mV_{RMS}	
Short circuit current	I_{SHORT_TX}	Output pins shorted to GND or each other	–50	–	50	mA	3

TX Specification (II)

Measurements are assumed to be at the package BGA ball; Parameters listed apply to HMC device only

Parameter	Symbol	Test Conditions/Comments	Min	Typical	Max	Unit	Notes
Differential TX output rise/fall time	$^{t}TX\_RISE$, $^{t}TX\_FALL$	Measured from 20% to 80% into ideal 100Ω load	8	–	–	ps	
Differential transmitter resistance	R_{OD}		80	100	120	Ω	4
Single-ended transmitter resistance	R_{OSE}		40	50	60	Ω	4
Differential transmitter termination mismatch resistance	$R_{TX\_DELTA\_AC}$	AC-coupled; Measured within a differential pair	–	–	10	%	
	$R_{TX\_DELTA\_DC}$	DC-coupled ($V_{HRX} = AV_{DD}/2$ ±50mV); Measured within a differential pair	–	–	10	%	5
Output return loss - Relative to 100Ω differential system	$RL_{TX-DIFF}$	f0 - f1	–	–	–12	dB	6
		f1 - fb	–	–	–12 + 12 × log (f/f1)	dB	6
Common mode return loss – relative to ideal 25Ω impedance	RL_{TX-CM}	f0 - f2	–	–	–6	dB	6
		f2 - fb	–	–	–4		

TX Specification (III)

Measurements are assumed to be at the package BGA ball; Parameters listed apply to HMC device only

Parameter	Symbol	Test Conditions/Comments	Min	Typical	Max	Unit	Notes
Jitter generation up to 30 Gb/s	DJ_{TX}	Measured at output ball	–	–	0.15	UI	6, 7
	DCD_{TX}	Measured at output ball; Considered part of and included within DJTX	–	–	0.035	UI	8
	RJ_{TX}	BER = 1e-15 (peak-to-peak jitter)	–	–	0.15	UI	9, 10
	TJ_{TX}	BER = 1e-15		–	0.28	UI	10, 11
Output differential skew	^{t}TXSKEW_diff		–	–	0.12	UI	
Lane-to-lane output skew at TX	$L_{TX\text{-}SKEW}$	Full rate defined as 25 Gb/s up to 30 Gb/s	–	–	7	UI	11
		Half rate defined as lane rates 15 Gb/s and less			4.5		
TX drift	^{t}TX_DRIFT	Amount of one-way phase change that the HMC lanes can shift in time after initialization. Drift is referenced from the crossing of differential transmit data pairs to the crossing of the differential REFCLK signals. ^{t}TX_DRIFT is slow change (>100µs) in transmit data phase from changed REFCLK distribution delay within the HMC due to variation over specified temperature and voltage range	–	–	250	ps	

TX Specification (IV)

Notes:

1. Reference points are defined at the device package balls.
2. TX differential output may be pulled HIGH or LOW, or High-Z. Any given HMC device could operate in any one or more than one of these states during sleep. It is not required for every HMC device to support all mode capabilities. See vendor specific specification for operation supported.
3. Phy output must be shorted to ground to measure whether the actual short circuit current is characterized to be within the specified limits.
4. Refers to the resistive portion of the termination.
5. This behavior is not compensated for with impedance calibration.
6. f0 = 50 MHz, f1 = 0.1714 × fb, f2 = 10 GHz, and fb is the bit rate frequency.
7. DJ_{TX}, RJ_{TX}, and TJ_{TX} are measured with a reference clock recovery unit (CRU) whose jitter transfer function is defined by a "golden" PLL, namely 0dB when f ≥ BR/2578, 20 dB/dec when f< BR/2578.
8. DJ_{TX} is measured with PRBS15 (2^{15} - 1) pattern.
9. DCD_{TX} is measured with a clock pattern.
10. TJ_{TX} is measured with PRBS15 (2^{15} - 1) pattern.
11. RJ_{TX} is measured with PRBS15 (2^{15} - 1) pattern.
12. This parameter applies to HMC device only. It is measured at the crossing point of each differential pair.

RX Specification (I)

Table 111: RX Signaling Parameters

Parameters listed apply to HMC device only

Parameter	Symbol	Test Conditions/Comments	Min	Typical	Max	Unit	Notes
Link supply RX voltage	AV_{DD}	0.9V ±0.027V (±3%)	0.873	0.9	0.927	V	1
Differential peak-to-peak input voltage	V_{DIFF_RX}	$V_{DIFF\_RX} = 2 \times \lvert V_{RX\_P} - V_{RX\_N} \rvert$ Measured with reference load	200	–	1200	mV	2
Single-ended voltage (with respect to V_{SS}) on D+, D-	V_{RX_SE}		0	–	$AV_{DD,max}$ + 300	mV	
Common mode of the input voltage	V_{RX_CM}	V_{RX_CM} = DC of $\lvert V_{RX\_P} + V_{RX\_N} \rvert /2$	300	–	AV_{DD}	mV	
Short circuit current, RX off	$I_{SHORT\ RX\_OFF}$		–100	–	100	mA	3
Short circuit current, RX on	$I_{SHORT\ RX\_ON}$		–100	–	100	mA	3
Differential input resistance	R_{ID}		80	100	120	Ω	
	R_{ISE}		40	50	60	Ω	
Differential receiver termination mismatch resistance	R_{RX_DELTA}		–	–	10	%	
Differential input return loss – Relative to 100Ω differential system	$RL_{RX\text{-}DIFF}$	f0 - f1	12	–	–	dB	4
		f1 - fb	–12 + 12 × log (f/f1)	–	–	dB	4
Common mode return loss – relative to ideal 25Ω	$RL_{RX\text{-}CM}$	f0 - f2	–6	–	–	dB	4
		f2 - fb	–4	–	–	dB	

RX Specification (II)

Parameters listed apply to HMC device only

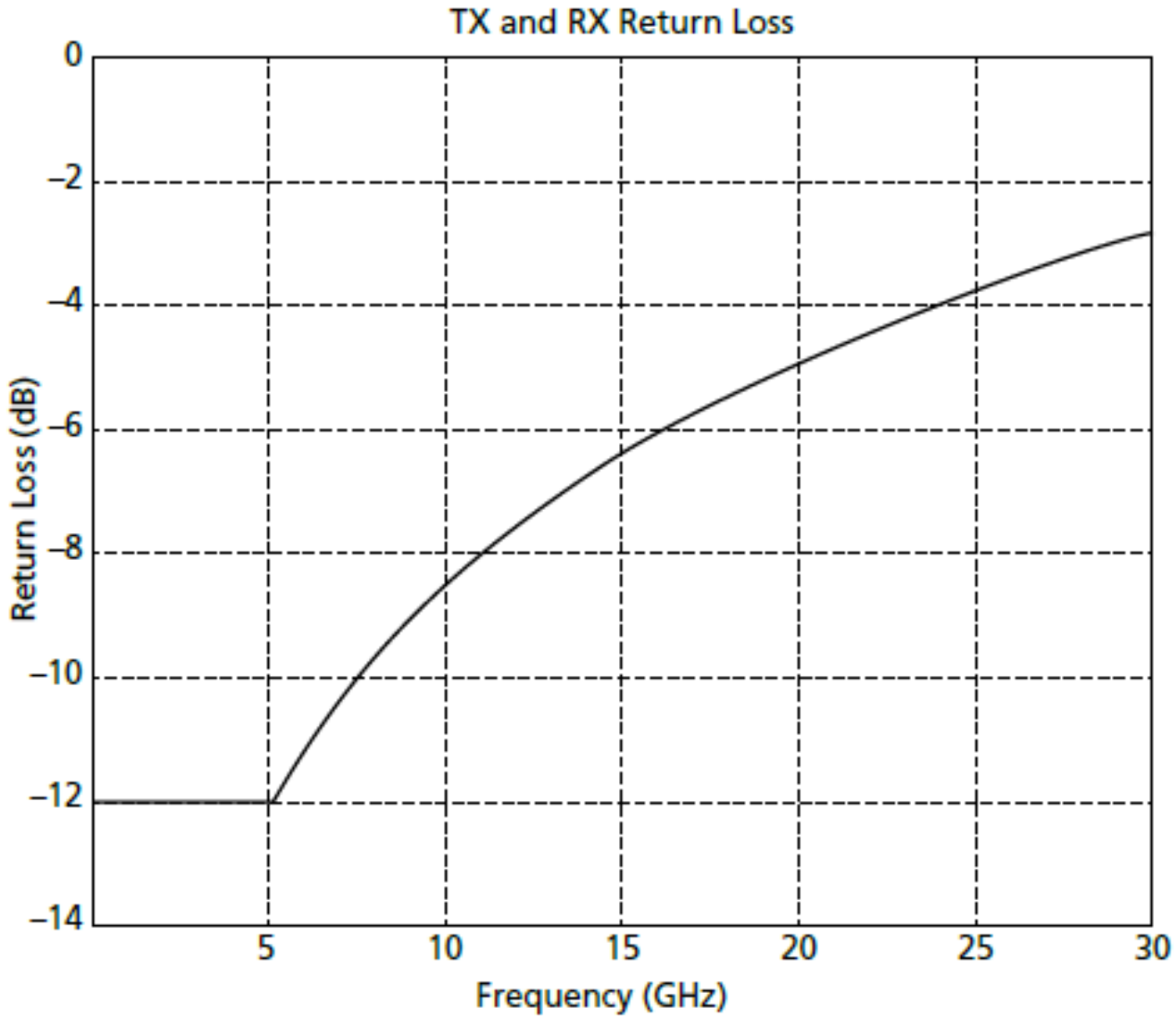
Parameter	Symbol	Test Conditions/Comments	Min	Typical	Max	Unit	Notes
Jitter tolerance	DJ_{RX}	Comprised of ISI, DCD, reflections, crosstalk, and SJ	–	–	1	UI	
	DDJ_{RX}	Composed of DCD and ISI	–	–	0.60	UI	5
	SJ_{RX}	Sinusoidal, high frequency when f2<f<fmax	0.05	–	–	UI	5, 6
		Sinusoidal, low frequency when fmin<f<f1	5	–	–		
	RJ_{RX}	Random jitter (rms)	–	–	7.5	UI	5
Input differential skew tolerance	R_{XSKEW_diff}		–	–	0.25	UI	
Lane-to-lane skew at RX	$L_{RX\text{-}SKEW}$	Lane-to-lane skew at a receiver that must be tolerated. RX INPUT skew is the difference between propogation delays of any two inputs of the same HMC LInk at identical transitions	–	–	32	UI	7

RX Specification (III)

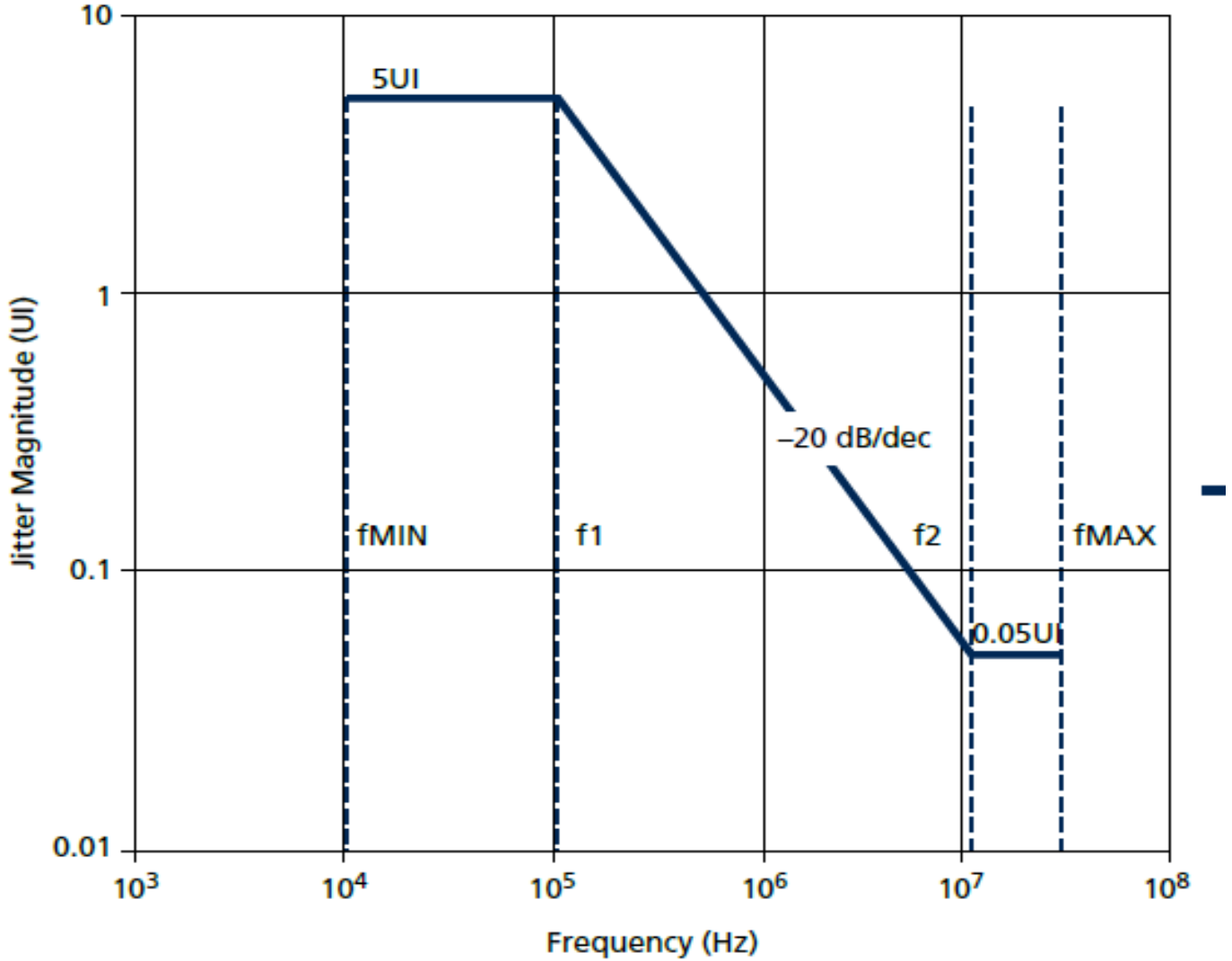
Notes:

1. Reference points are defined at the device package balls.
2. $V_{DIFF\_RX\_mIn}$ is an estimate that will be revised after the benefit of the RX equalization has been fully assessed. $V_{DIFF\_RX\_ax}$ value is based on a low frequency data pattern (64 ones followed by 64 zeros).
3. The receiver input absolute maximum voltage ratings in Absolute Maximum Ratings (page 101) cannot be exceeded for extended periods of time without affecting device reliability.
4. f0 = 50 MHz, f1 = 0.1714 × fb, f2 = 10 GHz, and fb is the bit rate frequency.
5. RX equalization can effectively open a "closed" eye signal at its input, to achieve a BER of 1E-15 or better. These jitter tolerance specifications correspond to the minimum equalization capability where RX DFE is not required. Assessment of RX equalization capabilities and BER for a given host TX and channel model can be performed using proven device model and simulation methods such as an IBIS-AMI receiver model, or other equivalent circuit or behavioral models.
6. See Figure 28 (page 111).
7. This parameter applies to HMC device only. Lane-to-lane skew contributes directly to memory latency, so minimizing skew between RX lanes is recommended. RX input skew is the difference between the propagation delays of any two inputs of the same link at identical transitions.

TX and RX Return Loss (RL)

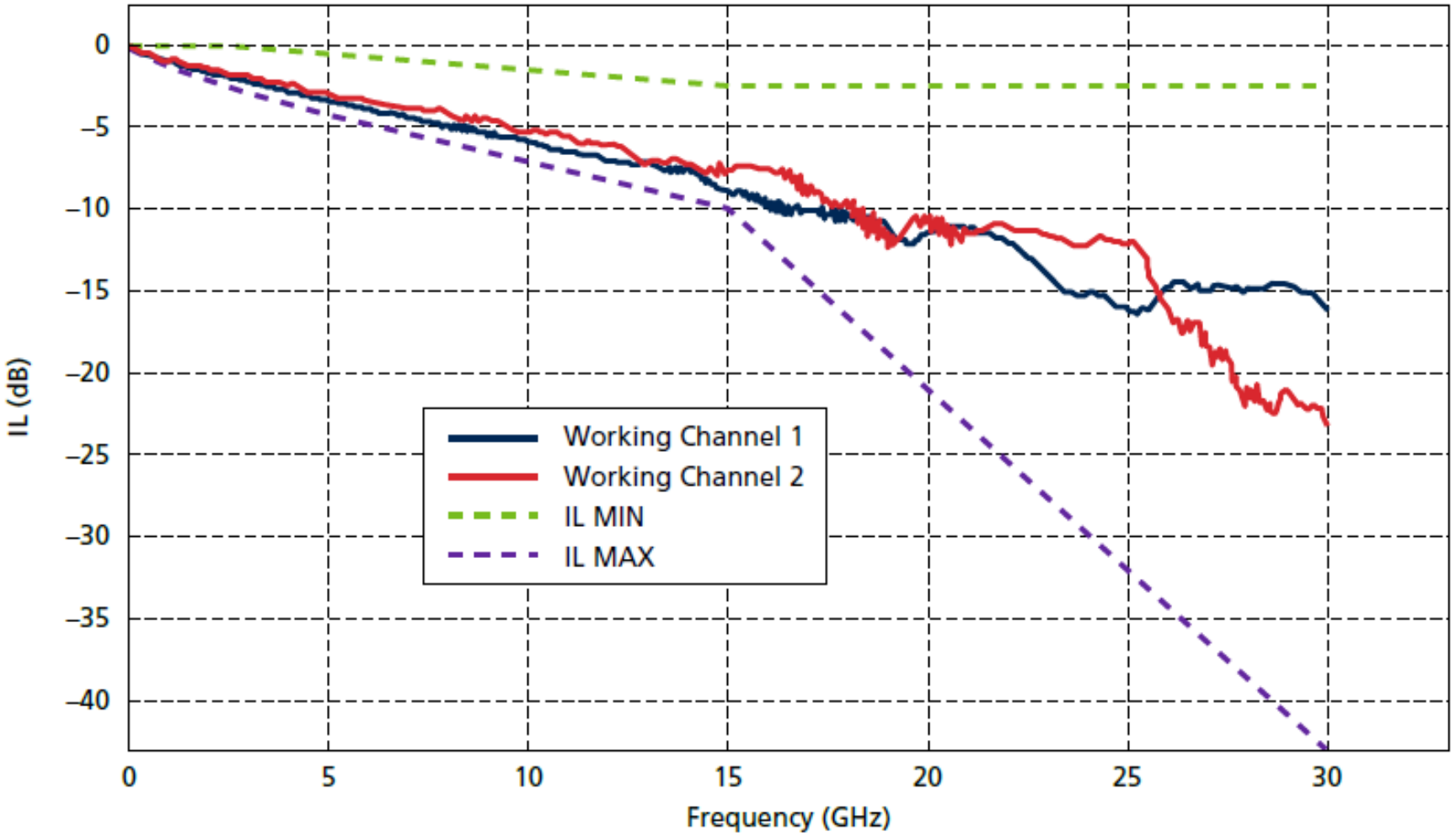


RX Sinusoidal Jitter Tolerance



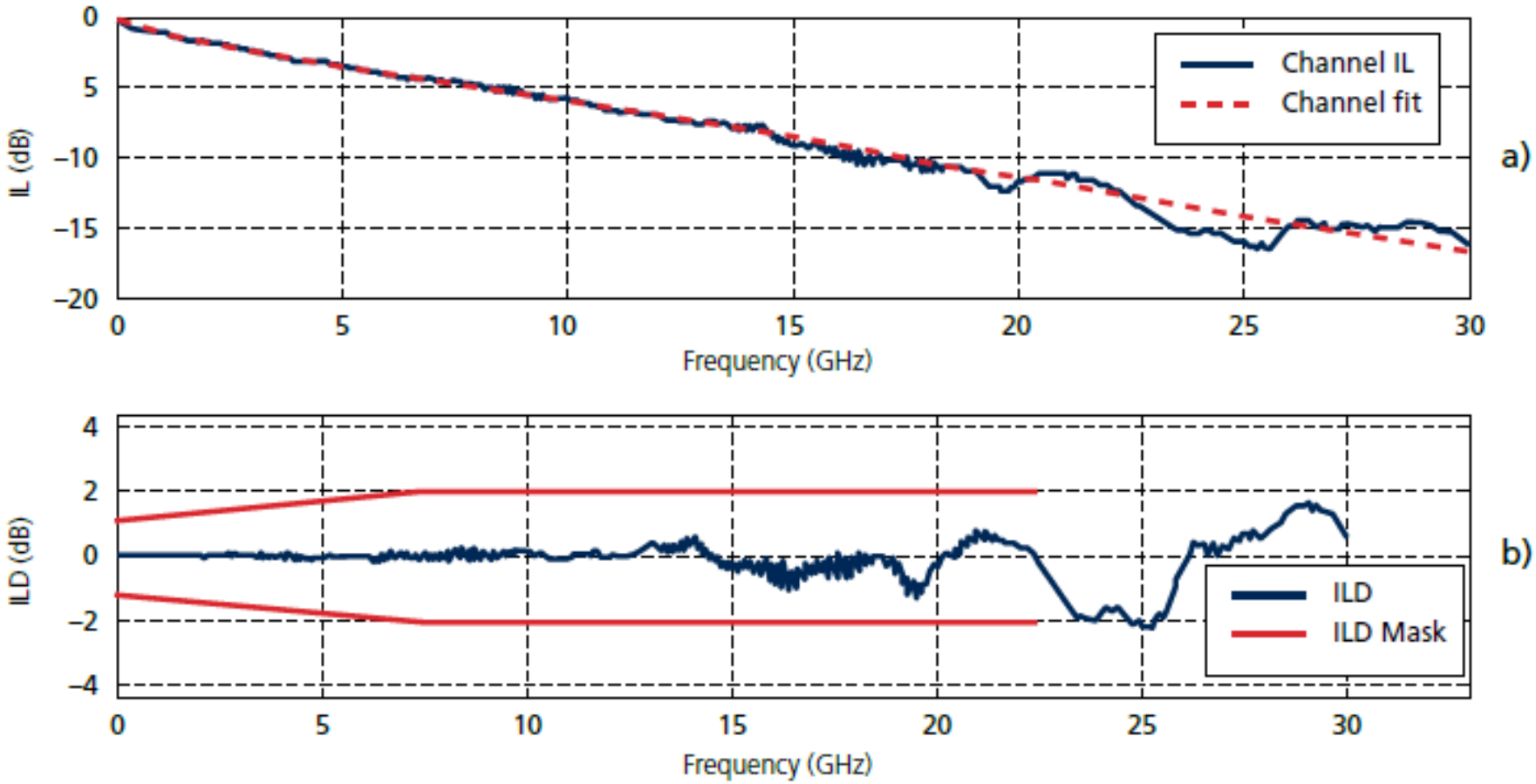
Where: f1 = fRX/257800, f2 = fRX/2578, fMIN = 10 KHz, and fMAX = 30 MHz.

Channel Insertion Loss Limits

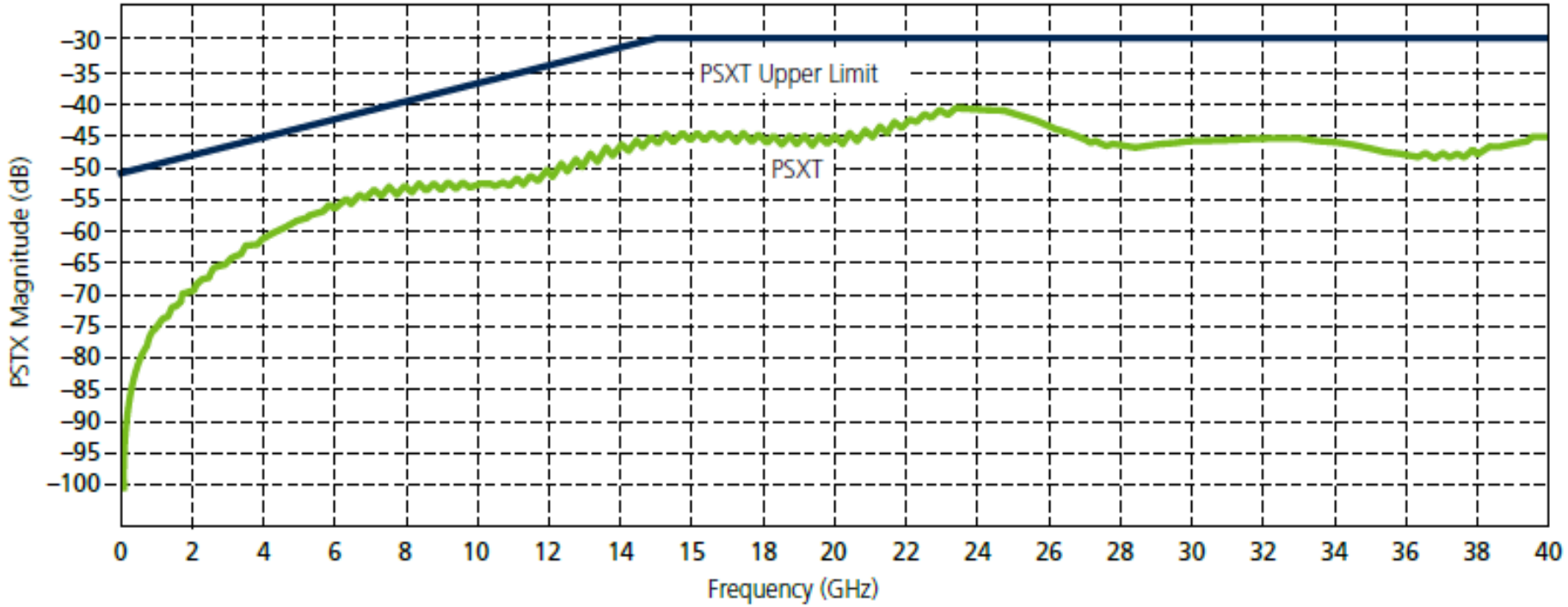


-10 dB at 15 GHz for 30 Gbps operation

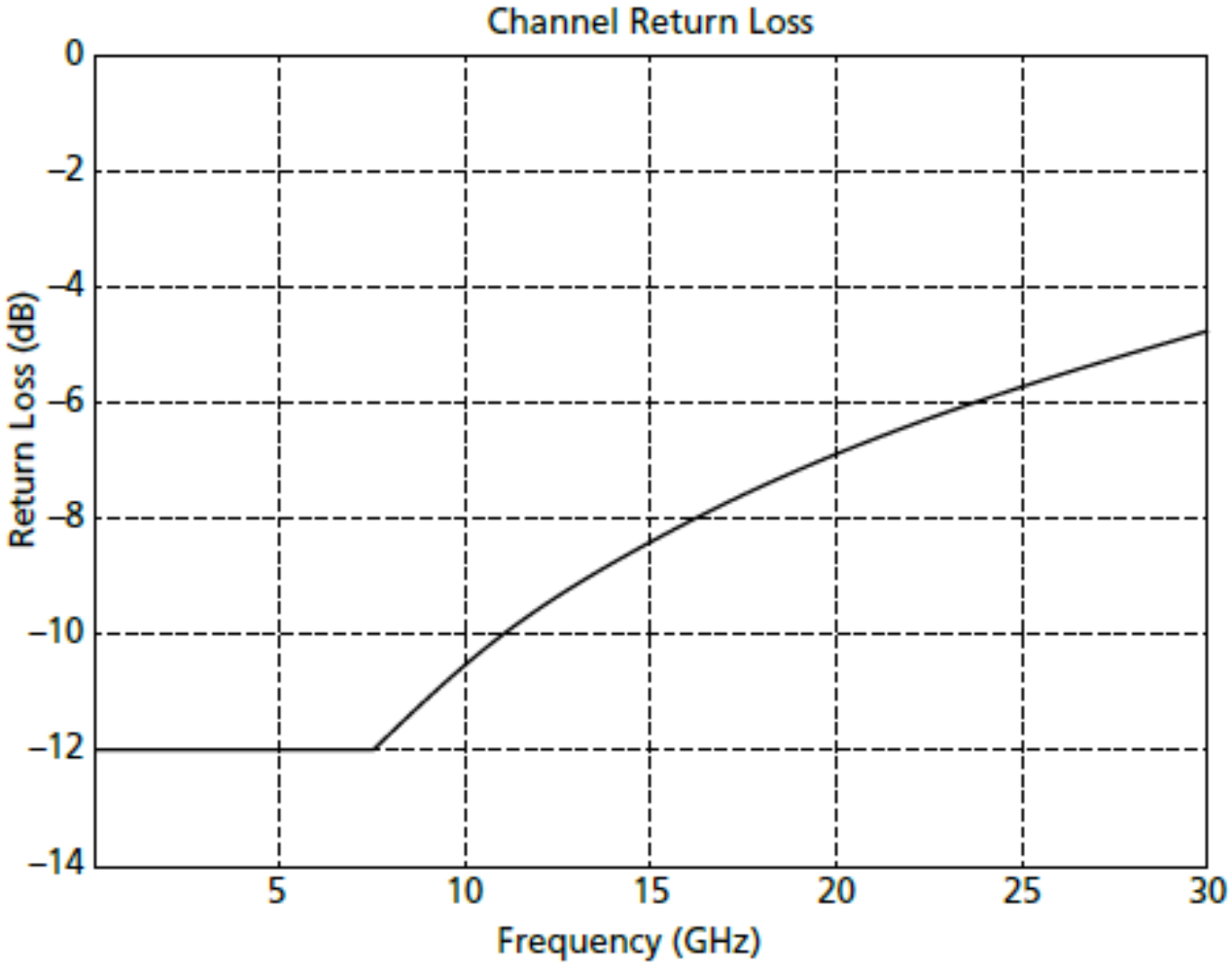
Channel Insertion Loss Deviation



Channel Xtalk Limit



Channel Return Loss Limit



Channel Parameter Summary (Informative)

Parameters	Min	Typ	Max	Notes
Differential insertion loss MIN: IL (dB)	–	–	≤0, fMIN < f < 1 GHz; <–(0.286(f - 1), 1 GHz ≤ f < fb/2; <-4, fb/2 ≤ f ≤ fb	fb: Baud rate, fMIN = 0.05 GHz
Differential insertion loss MAX: IL (dB)	–(0.073 + 0.9458 × sqrt (f × 30/fb) + 0.4176 × f × 30/fb), fMIN ≤ f < fb/2;(23 - 2.2 × f × 30/ fb), fb/2 ≤ f ≤ fb	–	–	
Differential input return loss: RLi (dB)	–	–	≥ –12, fMIN < f < 0.25fb; ≥–12 + 15log(4f/fb), 0.25fb < f < fb	
Differential output return loss: RLo (dB)	–	–	Same as RLi	
Power sum Xtalk: PSXT (dB)	–	–	<–30, 0.5fb ≤ f<fb ≤ 40 × (f/fb) - 50, fMIN ≤ f <0.5fb	
Insertion loss deviation peak (absolute): |ILD_pk| (dB)	–	–	1 + 4(f/fb)	fMIN < f < 0.25fb
	–	–	2	0.25fb < f < 0.75fb
Diff Impedance: Z_diff (Ω)	90	100	110	

Reference Clock Parameters

Parameter Description	Symbol	Min	Nom	Max	Unit	Notes
Reference clock input frequency	^{f}REFCLK	–	125, 156.25, 166.67, 312.50	–	MHz	
Reference clock frequency tolerance	^{f}TOL_REFCLK	–100	–	100	ppm	
Reference clock duty cycle tolerance	^{t}DCD_REFCLK	45	50	55	%	
Single-ended input voltage	V_{SE_REFCLK}	V_{SS} - 0.1	–	V_{DDK} - 0.1	V	
AC Coupled Inputs						
Differential input voltage	$V_{ID\_AC\_REFCLK}$	200	–	800	mV	1
Internal differential termination	$R_{ID\_AC\_REFCLK}$	90	100	110	Ω	2
AC coupling capacitance (external DC blocking capacitor)	$C_{DC\_BLOCK\_REFCLK}$	–	0.1	–	µF	
Reference Clock Phase Noise Requirements						
Clock phase noise offset from nominal input frequency	100Hz	–	–	–85	dBc/Hz	
	1 kHz	–	–	–97	dBc/Hz	
	10 kHz	–	–	–97	dBc/Hz	
	100 kHz	–	–	–114	dBc/Hz	
	1 MHz–1 GHz	–	–	–126	dBc/Hz	

Notes:
1. Using a 0.1µF AC coupling capacitor is recommended.
2. AC coupled input mode uses internal, calibrated differential termination.

Summary

- HMC 30G-VSR Electrical/Phy Specification reviewed
  - Link topology, lane rates, BER target
  - Link equalization: TX FFE and RX CTLE
  - TX (e.g., output swing, RL, jitter)
  - RX (e.g., input swing, RL, jitter tolerance)
  - Channel (e.g., IL, ILD, Xtalk)
  - Reference (e.g., input frequencies, tolerance, DCD, and phase noise)
- HMC 30G-VSR Specification is ready for HMC adopters

Questions?