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Metastability in CMOS Transmission Gate Base Interface Circuits

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Abstract: Our work proposed metastability measurement system in which asynchronous data input and sampling clock frequencies trigger metastability. , we demonstrate that dynamic memory cells present an anomalous behavior referred to as metastable operation with characteristics similar to those of static latches. During every cycle, the relative time of the two signals changes a bit, and eventually they switch sufficiently close to each other, leading to metastability. One common way to demonstrate metastability is to supply two clocks that differ very slightly in frequency to the data and clock inputs. Microwind simulations were performed in order to quantify the delay, power and metastability performance of several flip-flops base modules. A CMOS layout is also implemented in MICROWIND Layout editor to represnts the delay degradation due to metastability which affects the performance of circuits including timing simulation, power dissipation etc. The our work the flip-flop base module with both the master and slave stage protected with a excellent soft-error protection, significantly better than other flip-flops which only had protection on the slave stage. Moreover, we will show that flip-flop base module will have the best metastability performance.

Key Words - Transmission Gate D-Flip-Flop,Metastability.

I. Introduction

In digital systems, the term metastability refers to the anomalous behavior of devices with memory that may occur when input timing constraints are violated. When timing constraints cannot be guaranteed, metastability is unavoidable but the probability of its occurrence can be managed by the use of synchronizers. Metastability in digital systems occurs when two asynchronous signals combine in such a way that their resulting output goes to an indeterminate state. A common example is the case of data violating the setup and hold specifications of a latch or a flip-flop. In a synchronous system, the data always has a fixed relationship with respect to the clock. When that relationship obeys the setup and hold requirements for the device, the output goes to a valid state within its specified propagation delay time. However, in an asynchronous system, the relationship between data and clock is not fixed; therefore, occasional violations of setup and hold times can occur. When this happens, the output may go to an intermediate level between its two valid states and remain there for an indefinite amount of time before resolving itself or it may simply be delayed before making a normal transition. The our work the flip-flop base module with both the master and slave stage protected with a excellent soft-error protection, significantly better than other flip-flops which only had protection on the slave stage. Moreover, we will show that flip-flop base module will have the best metastability performance. Our work proposed metastability measurement system in which asynchronous data input and sampling clock frequencies trigger metastability. , we demonstrate that dynamic memory cells present an anomalous behavior referred to as metastable operation with characteristics similar to those of static latches

II. Metastability Theory:

Any flip-flop can easily be made metastable. Toggle its data input simultaneously with the sampling edge of the clock, and you get metastability. One common way to demonstrate metastability is to supply two clocks that differ very slightly in frequency to the data and clock inputs. During every cycle, the relative time of the two signals changes a bit, and eventually they switch sufficiently close to each other, leading to metastability. Synchronize any asynchronous input through one path that has at least one and preferably two flip-flops in series. The flip-flops should be running on the same edge of your system clock as the rest of the circuit. This will limit the area of potential problems to one path instead of several, and minimize the possibility of metastability entering the main part of the circuit. In the simplest case, designers can tolerate metastability by making sure the clock period is long enough to allow for the resolution of quasi-stable states and for the delay of whatever logic may be in the path to the next flip-flop. This approach, while simple, is rarely practical given the performance requirements of most modern designs. The most common way to tolerate metastability is to add one or more successive synchronizing flip-flops to the synchronizer. Ways of limiting metastability include using only one clock, using faster flipflops, decrease the asynchronous input frequency, and use synchronization hardware. These steps can easy be taken by designers to increase the reliability of a circuit

III. Transmission Gate D-Flipflop Bistability operation:

ACMOS D-latch (level sense), is used to store I bit of data. When CK is high and CKN is low, data Ddrives the latch, and node Q assumes the logic level of D, and QN the complement. The minimum time required to store the data is called the setup time. If the data transition occurs before the setup time, the value after the transition is stored in the latch. If the

transition occurs after the setup time, the value before the transition is stored The latter case results in a logic error. A SET FF can be configured to operate as master slave latch by cascading the sequential structure but it is incompetent as half of the clock edges are wasted, while the full implementation cost of the complete clock is endured. Next topology is Double Edge Triggered flip-flop DET, which can be triggered at the positive as well as the negative edges.

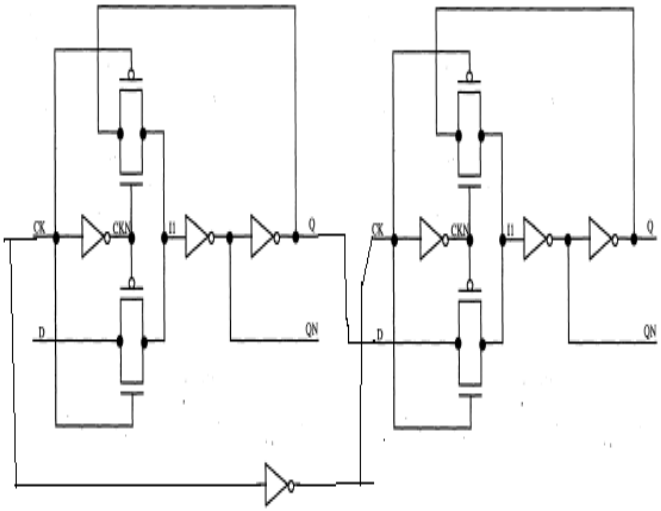

Fig 1 Transmission gate base D flipflop in Master Slave arrangement.

IV. Metastability Parameter Estimation:

The mean time between failures (MTBF) is used to represent the reliability of synchronizers. Normally, we obtain an input time and output time relationship first and then the corresponding MTBF can be computed. If the data signal transitions at a frequency of f_D with respect to a clock signal with a frequency of f_{CLK}, a common metric used to characterize metastability is the mean-time-between failures (MTBF), given

$$MTBF = \frac{1}{f_D f_{CLK} T_0 e^{-t_s/\tau}}$$

where T_0 is the width of the aperture window where a transition in the input data may result in metastability, and T is the resolution time constant that represents the inverse of the gain-bandwidth product of the feedback element in the flip-flop. Fig1 and Fig 2 shows the layout design for Transmission gate base D flipflop in Master Slave arrangement.

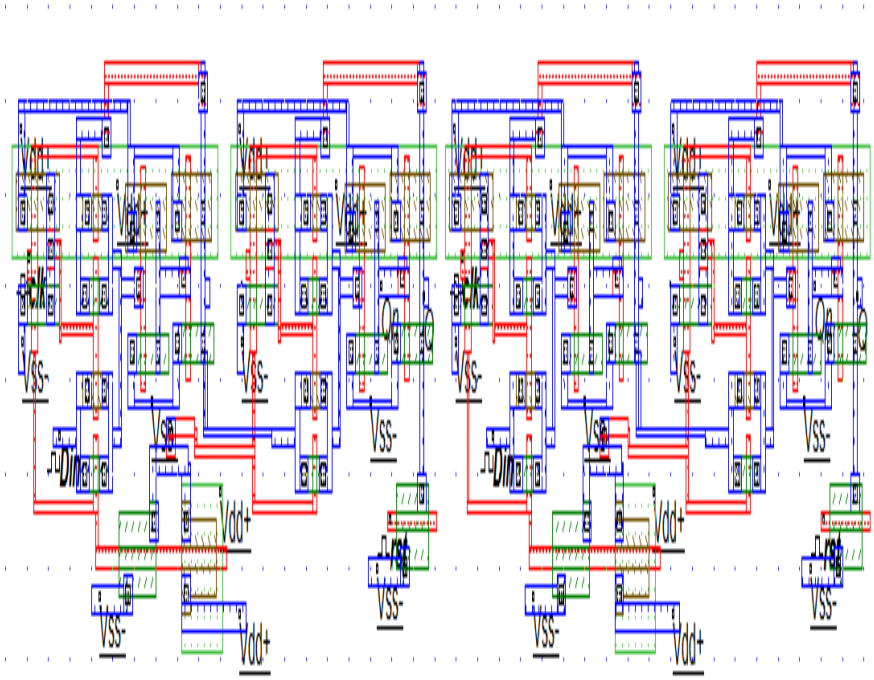

Fig2 Layout design for Transmission gate base D flipflop in Master Slave arrangement.

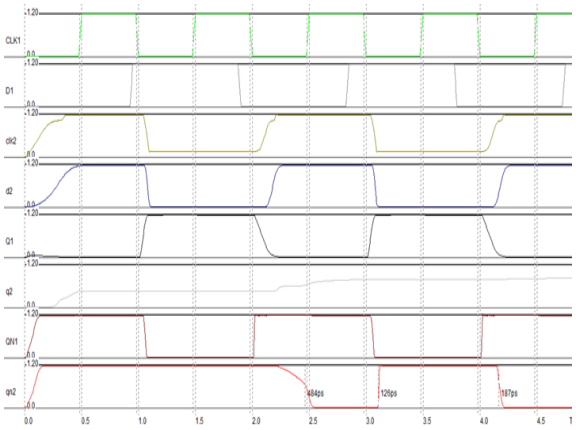

Fig 3 Metastable timing simulation for Transmission gate base D flipflop in Master Slave arrangement.

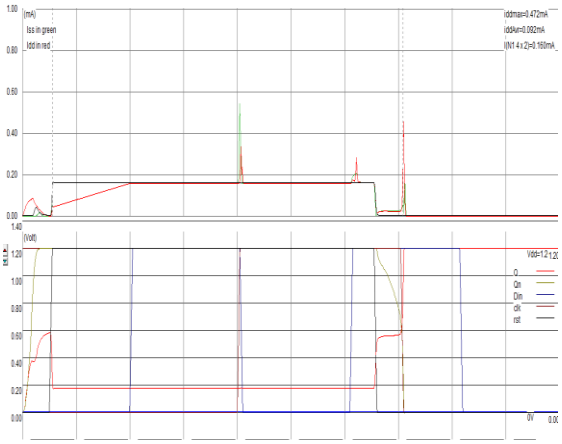

Fig 4 Current verses timing simulation for Transmission gate base D flipflop in Master Slave arrangement.

Many techniques have been devised to address the metastability problem and reduce the probability of synchronization failure to an acceptable level when interfacing between synchronous and asynchronous modules. The goal of each of these techniques is to increase the amount of time to resolve the metastability (i.e., increase ta). The simplest approach to achieve this is to use two (or more) latches in series to sample asynchronous signals arriving at a synchronous module. This increases the time allowed for a metastable condition to resolve. In other words, if n extra latches are added in series with an asynchronous input, the new value of ta is given by

$$t'_a = t_a + n(T - t_{pd})$$

where T is the clock period and tpd is the propagation delay through the added flip-flops. The cost, though, is an extra n cycles of delay when communicating data from an asynchronous module to a synchronous module, even when there is no metastability. Fig 3 and fig 4 shows Metastable timing simulations for Transmission gate base D flipflop in Master Slave arrangement.

In this table we have shown comparison between past and present result Analysis.

V. Parametric Analysis:

	Leaf cell	Max Current	Power dissipation	Switching delay	Clock freq.	Data freq
Our Work	Conventional NAND latch	0.865MA	21uW	In the range of ns	1GHz	0.59GHz
	Conventional NAND Flipflop	0.875mA	33uW	In the range of ns	1GHz	0.53GHz
	Metastable output flip-flop	1.461mA	270uW	0.473ns	1GHz	1GHz
	TG Latch	0.204mA	2uW	0.974ns	0.49GHz	0.23Ghz

	TG flip-flop	0.422mA	63uW	0.93ns	0.28GHz	0.49GHz
	TG Prapose Latch	0.42mA	1.2uW	In the range of ps	0.49GHz	1.82GHz
	TG Prapose flip-flop	0.860mA	0.187uW	0.272ns	0.49GHz	1.82GHz

Comparative Analysis:

	Power dissipation	Switching delay	Clock freq.	Number of transistor	Metasatable error calculates
Our work	0.187uW to 2uW	0.473ns to 0.974 ns	0.5GHz To 1GHz	12	15
Design in [1]	3.6 to 6.4uW	0.147 to 0.199ns	1GHz to 10GHz	14	11 to 49
Design in [2]	3.7uW to 7.21uW	1.46 to 4.36 ps	0.5GHz To 1GHz	48	NA

VI. Conclusion:

The data changes during the setup and hold time voilets the value of Q (Q_Metastable) may enter the metastable region resulting in a long time for Q to resolve to a stable value and therefor an unpredictable final value of Q. As clock speeds increase, synchronization issues are becoming increasingly important, so such a formal verification approach to the analysis of synchronization strategies is essential to produce reliable systems in the future. Flip flop is a high gain circuit, it will amplify the input voltage and output becomes at stable state. Due to the setup and hold time voilation the latch may have no initial voltage to amplify and thus the output of the flip-flop may become unpredictable and take an unbounded amount of time to settle to a stable level. The problem of metastability in analysis of latch and flip-flop designs was addressed.

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