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Design and Simulation of FPGAs Based Digital Discriminator

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Abstract— FPGAs (Field Programmable Gate Arrays) are especially popular for prototyping integrated circuits design. This paper presents a new reconfigurable high-performance approach for FPGAs based digital Discriminator. The principle of operation of designed digital Discriminator is based on measuring the height of pulses coming from detectors and comparing it with predefined set level. Complete circuit is designed by writing appropriate program in Very High Speed Integrated Circuit Hardware Description Language (VHDL) & ISE foundation 6.1i. We present our design, implementation, verification and simulation results with a Xilinx Spartan 3 XC3S400~4pq208. A maximum frequency of 358.423 MHz was reached with a minimum period of 2.790 ns. 11 slices out of 3584 were used.

Keywords— Pulse height analysis, VHDL, FPGA, Nuclear Spectroscopy, Digital circuits.

I. INTRODUCTION

In traditional nuclear spectroscopy system output signal from detector undergoes various steps. The structure of traditional spectroscopic system is showed in Fig.1.

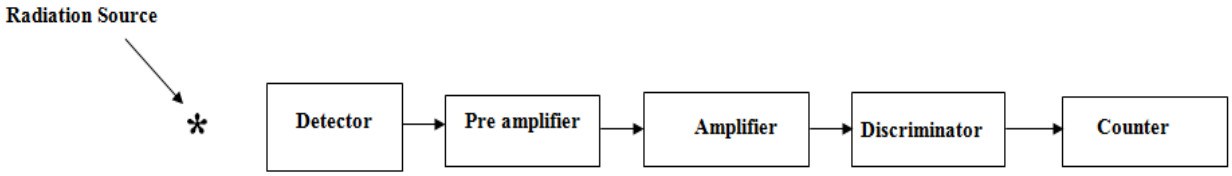

Fig.1 Traditional nuclear spectroscopy system

The theory of pulse height analysis is published in number of articles and textbooks. Nuclear particle interact with detector and produces a voltage pulse. The height of pulse is proportional to the energy deposited by nuclear particle in detector [1]. By measuring the height of pulse, energy of particle can be estimated. Various methods of measuring the pulse amplitude are there [2][3].Traditionally pulse height analysis process is realized by analog circuitry like integral Discriminator, Single Channel Analyzer etc. In analog circuitry hardware manipulation is necessary to adjust the measuring parameters which is either not possible all the time or difficult. A number of commercial available spectroscopy system now incorporate digital processing in place of traditional analog approach and they demonstrate significant advantage over analog system in some circumstances [4].

Emerging high level hardware description and synthesis technologies in conjunction with Field Programmable Gate Arrays (FPGAs) have significantly lowered the threshold for hardware development, opportunities exist to integrate these technologies into a tool for exploring and evaluating micro-architectural designs [5][6]. Embedded circuits can be designed using Very High Speed Integrated Circuit Hardware Description Language (VHDL) and can be implemented on FPGAs [7][8].

In this paper we present a detailed description of the designed digital Discriminator on reconfigurable platform FPGAs. It is assumed that preamplifier output signal is first acquired using high speed Analog to Digital Converter (ADC) and then it is processed and analyzed by FPGAs based digital discriminator. Section II briefly describes the theoretical description of analog Discriminator. Section III presents the digital FPGAs based Discriminator along with the associated Datapath unit and Control unit. The operations performed by the different section of both the units are described in detail. VHDL implementation and basic procedure utilized for verification is discussed in section IV. Section V presents the Schematics, simulation results, device utilization summary and Timing report of various units. In section VI result obtained from simulation are presented and section VII concludes the paper.

II. A INTEGRAL DISCRIMINATOR

Integral discriminator is the simplest unit that consists of a device that produces a logic output pulse only when the linear input pulse height exceeds a threshold, i.e. discriminator level [2].Amplitude discriminators are used for separating a useful signal from noise and for investigating random processes by means of amplitude analysis. In Fig. 2 a block diagram of Integral discriminator is shown below.

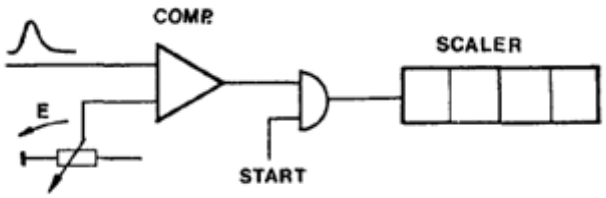

Fig. 2 Block diagram of Integral discriminator

In the circuit threshold level will be set every time and number of pulses which cross this level will be counted. This will continued by stepping down the threshold level. The SCALER is a recorder of pulses. For every pulse entering the SCALER, a count of 1 is added to the previous total. At the end of the counting period, the total number of pulses recorded is displayed. A Schmitt-trigger or an analog comparator can work as discriminator. Predefine or threshold level is adjustable and can vary over the whole range of Input signal.

III. FPGAs BASED DIGITAL DISCRIMINATOR

The detailed theory of analog Discriminator with suitable diagram is given in section II. In this section, we had manually designed the FPGAs based digital Discriminator for counting the pulses which fall above the predefined energy level. Our designed system has two main units: Datapath unit and Control unit.

A. Algorithm Description

A following mentioned sequence of operations is performed each time when a pulse is analyzed:

i. The Analog to digital converter (ADC) converts the analog pulse height into a digital number.
ii. This 8-bit number is compared with predefined threshold value and according to result, 0 or 1 will be generated.
iii. This result is further transfer to logic unit to produce logic pulses.
iv. Logic pulse is forwarded toward counter unit for the counting and display of final result.

B. Units required to implement digital Discriminator Circuit

After analyzing the algorithm presented in subsection III-*A*, we conclude that the following functional units are required for the designing of Datapath unit and Control unit.

i. An 8-bit comparator (U0)
ii. An 1-bit And gate (U1)
iii. An 1-bit latch (U2)
iv. An 4-bit counter (U3)
v. A Finite State Machine (FSM)

C. Datapath unit of digital Discriminator

Schematic of our designed dedicated Datapath unit for FPGAs based digital Discriminator is shown in Fig.3. It contains all the processing units required for implementation of algorithm mentioned in subsection III-*A*.

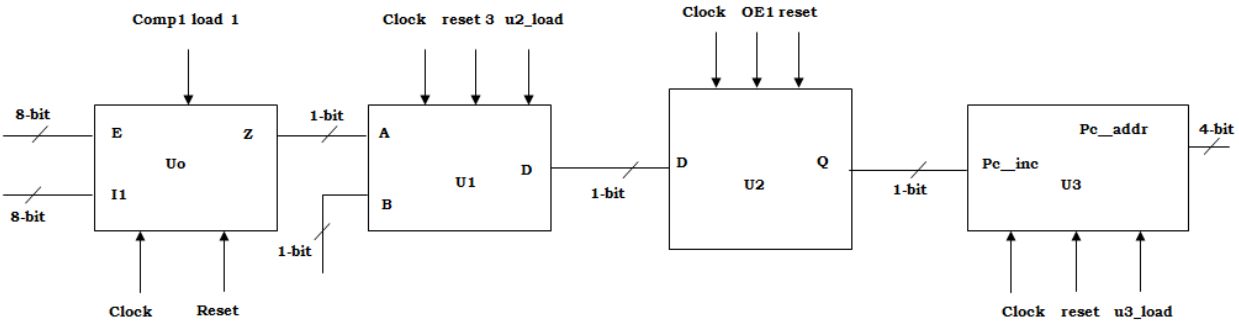

Fig.3 Schematic circuit of Datapath unit

Comparator unit (U0) has two 8-bit inputs E1 and I1. The input port is connected to the input E1 of the 8-bit comparator. By asserting comp1load1, the value at the input port is loaded into comparator, and compared for greater than or equal to predefined threshold value I1.Output of comparator is connected to input of logic unit. Logic unit (U1) has two 1-bit inputs A and B; one is connected to output of comparator and other from control unit. By asserting U2_ load the value of output of comparator and the value from control unit will be loaded in to logic unit and logical AND operation is performed. 1-bit tristate latch (U2) is connected between logic unit and counter unit. OE1 signal is used for enabling this latch. Finally the counter unit (U3) will count the logic ones generated by logic unit.

D. Control unit of digital Discriminator

The control unit inside the FPGAs based digital Discriminator unit is a Finite state machine (FSM). These control signals are the output signals from the output logic circuit that is inside the FSM. In every clock cycle, the control unit

will generate a different set of control signals for the Datapath unit to perform one predefined specific operation. The state diagram for the control unit of FPGAs based Discriminator unit has five states as shown in Fig.4.

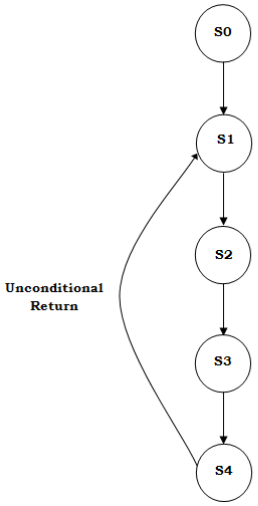

Fig. 4 State diagram for Control unit of digital Discriminator

- During State s0, initialization operation is performed. Signals reset and reset3 are asserted so that input data as well as output in every unit must be zero.
- During State s1, Comparator unit is activated by asserting comp1load signal. Two numbers are excepted and compared for less than, greater than or equal to.
- During State s2, Logic unit is activated by asserting u2_load signal.
- During State s3, Tristate buffer is activated by asserting signal OE1. It allows logic pulse from logic unit to reach Counter unit.
- During state s4, Counter unit is activated by asserting signal u3_load due to which counter count the logic pulse and gives running output.

After that control transfer from state s4 to state s1 unconditionally.

IV. VHDL IMPLEMENTATION OF FPGAS BASED DIGITAL DISCRIMINATOR UNIT

All the units related with Datapath unit and Control unit mentioned in section III are designed. These units are described in VHDL modules using ISE foundation 6.1i. Test benches have been written to test functionality of each module individually. The functionalities of each unit were verified by using Modelsim simulator. Finally Datapath and Control unit is combined by writing appropriate codes in VHDL to form complete the digital Discriminator Unit. Test benches have been written to test functionality of Discriminator unit. The designed system is simulated using Modelsim simulator. Final designed digital Discriminator is synthesized by using synthesis tools provided in the Xilinx Webpack 6.1i. Various aspects of designing parameter and timing are discussed with suitable schematic diagrams, waveform, circuit and time analysis reports in section V.

V. SIMULATION AND VERIFICATION

A. Datapath unit of FPGAs based discriminator

The detailed description of the Datapath unit is given in subsections III-*C*. Portion of synthesis report presented below shows all the synthesizing units, Device utilization summary and Timing report. Fig. 5 shows schematic of the component used to construct Datapath unit. It is generated by Synthesize-XST tool of Webpack 6.1i. Table 1 presents the device utilization report of Datapath unit. It gives the estimation of resources utilized during the designing process. Timing Summary report of Datapath unit is presented in Table 2. The maximum operational frequency of designed unit is 331.675 MHz.

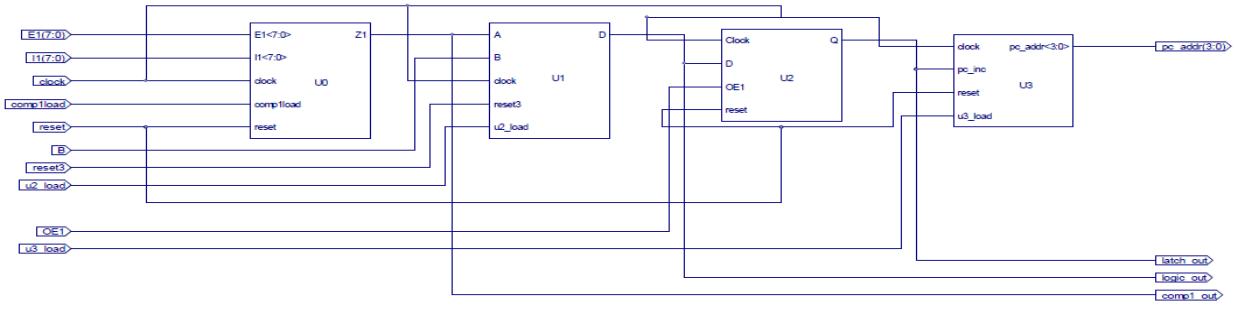

Fig. 5 Schematic of the component used in Datapath unit

TABLE 1
DEVICE UTILIZATION SUMMARY REPORT OF DATAPATH UNIT

==========

Selected Device: 3s400pq208-4

Number of Slices:	9	out of	3584	0%
Number of Slice Flip Flops:	8	out of	7168	0%
Number of 4 input LUTs:	15	out of	7168	0%
Number of bonded IOBs:	30	out of	141	21%
Number of GCLKs:	1	out of	8	12%

==========

TABLE 2
TIMING SUMMARY REPORT OF DATAPATH UNIT

==========

Speed Grade: -4

Minimum period: 3.015ns (Maximum Frequency: 331.675MHz)
Minimum input arrival time before clock: 5.416ns
Maximum output required time after clock: 6.689ns
Maximum combinational path delay: No path found

==========

B. Control unit of FPGAs based digital discriminator

The detailed description of the Control unit is given in subsections III-*D*. Fig.6 shows schematic of the component used to construct Control unit. It is generated by Synthesize-XST tool of Webpack 6.1i. Table 3 presents the device utilization report of Control unit. Timing report of Control unit is presented in Table 4. The maximum operational frequency of designed unit is 413.565 MHz.

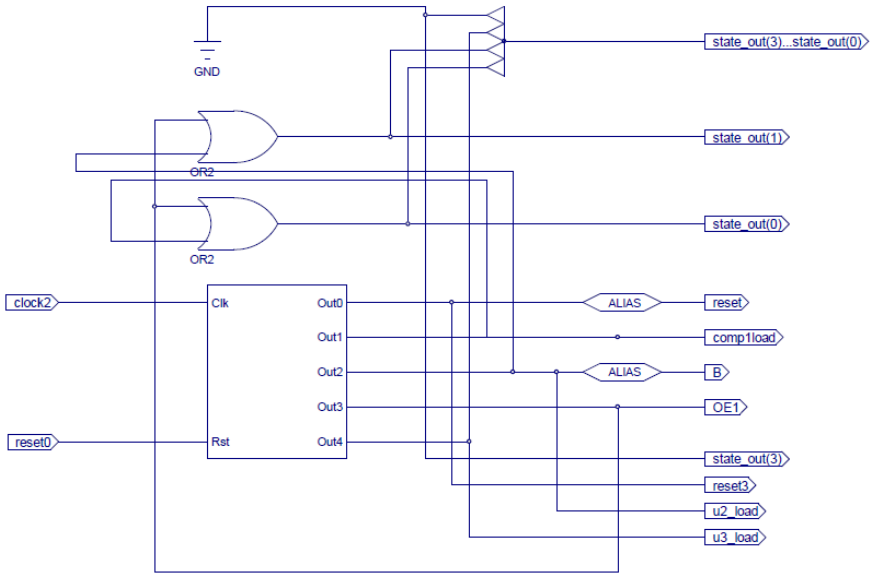

Fig. 6 Schematic of Control unit

TABLE 3
DEVICE UTILIZATION SUMMARY REPORT OF CONTROL UNIT

==========

Selected Device: 3s400pq208-4

Number of Slices:	4	out of	3584	0%
Number of Slice Flip Flops:	7	out of	7168	0%
Number of 4 input LUTs:	3	out of	7168	0%
Number of bonded IOBs:	12	out of	141	8%
Number of GCLKs:	1	out of	8	12%

==========

TABLE 4
TIMING SUMMARY REPORT OF CONTROL UNIT

```
=========================================================================
Speed Grade: -4

Minimum period: 2.418ns                (Maximum Frequency: 413.565MHz)
Minimum input arrival time before clock: No path found
Maximum output required time after clock: 7.620ns
Maximum combinational path delay: No path found
=========================================================================
```

C. FPGAs based digital Discriminator

The detailed description of the FPGAs based digital Discriminator model is given in section III of this paper. Fig. 7 shows schematic of the component used to design digital Discriminator unit. It is a combination of Datapath unit and Control unit. It is generated by Synthesize-XST tool of Webpack 6.1i. Fig.8 shows the waveforms generated by the FPGAs based digital Discriminator unit. From the waveform proper functioning of designed units are confirmed. Table 5 present the device utilization report of FPGAs based digital Discriminator unit. It gives the estimation of resources utilized during the designing process. Timing report of FPGAs based digital Discriminator unit is presented in Table 6. The maximum operational frequency of designed unit is 358.423 MHz.

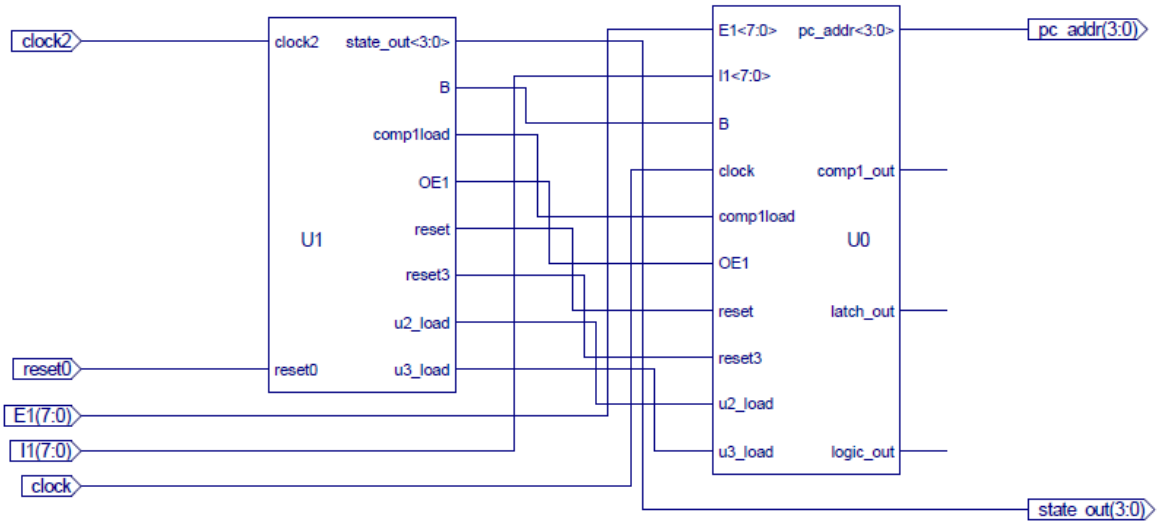

Fig.7 Schematic of FPGAs based digital Discriminator unit

U1 and U0 represent Control units and Datapath respectively.

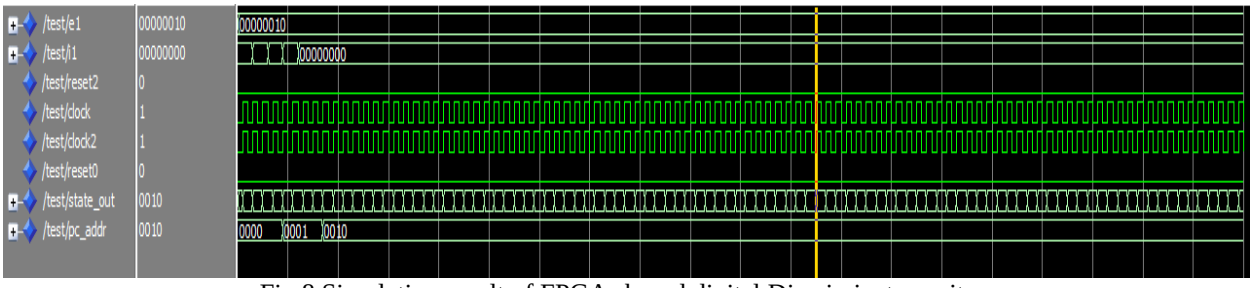

Fig.8 Simulation result of FPGAs based digital Discriminator unit

TABLE 5
DEVICE UTILIZATION SUMMARY REPORT OF FPGAS BASED DIGITAL DISCRIMINATOR UNIT

```
=========================================================================
Selected Device  : 3s400pq208-4

 Number of Slices:              11  out of   3584     0%
 Number of Slice Flip Flops:    12  out of   7168     0%
 Number of 4 input LUTs:        18  out of   7168     0%
 Number of bonded IOBs:         25  out of    141    17%
 Number of GCLKs:                2  out of      8    25%
=========================================================================
```


TABLE 6
TIMING SUMMARY REPORT OF FPGAS BASED DIGITAL DISCRIMINATOR UNIT

```
=========================================================================
    Speed Grade: -4
     Minimum period: 2.790ns                (Maximum Frequency: 358.423MHz)
     Minimum input arrival time before clock: 5.416ns
     Maximum output required time after clock: 7.620ns
     Maximum combinational path delay: No path found
=========================================================================
```

VI. RESULTS AND DISCUSSIONS

In this paper we described the principles, design, simulation and implementation of a fully reconfigurable FPGAs based digital Discriminator. Designed digital Discriminator is made of Control unit and Datapath unit. The complete digital Discriminator is programmed inside a Xilinx Spartan 3 XC3S400 FPGAs by using ISE foundation 6.1i. Complete circuit is designed using VHDL and verified by using Modelsim simulator. Datapath unit composed of 8-bit interface unit between ADC and Memory unit, 8-bit comparators, 1-bit logical Unit, 1-bit buffer, and 4-bit counter unit. Its maximum operational frequency is 331.675MHz. Control unit is composed of a finite state machine. It has 5 states. Its maximum operational frequency is 413.565MHz. Maximum operational frequency of designed FPGAs based digital Discriminator is 358.423MHz.

VII. CONCLUSIONS

The advantages of circuit designing in FPGAs have been widely recognized. This FPGAs based system can replace complex analog Discriminator circuitry. It is based on measuring the height of pulses coming from detectors, which is proportional to energy carried by the particles. All of the processing blocks used in this simulation system were translated into a hardware system using VHDL. Each processing block in the proposed system can be easily modified without any modification in the hardware of system. The pulse processing algorithm is easy to edit on such type of system, because changes are made through the software. System so developed is portable because most of the bulky analog electronics is eliminated.

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REFERENCES

[1] Tsoulfanidis, N., *Measurement and Detection of radiation*, Taylor & Francis Publishers, Third Edition, 1995.
[2] *SELECTED TOPICS IN NUCLEAR ELECTRONICS*, A technical document issued by the International Atomic Energy Agency, Vienna, 1986.
[3] Ahmed, S.N., *Physics and Engineering of Radiation Detection*, First edition, 2007.
[4] Knoll, G.F., *Radiation Detection and Measurement*, 3 rd edition, 2000.
[5] Ray J, Hoe J.C, "*High-level Modeling and FPGA prototyping of Microprocessors*", 11th ACM international symposium on Field Programmable Gate-Arrays, Feb 23-25, 2003.
[6] http://www.xilinx.com/.
[7] Hwang, E, *Digital Logic and Microprocessor Design with VHDL*, Indian Edition, 2007.
[8] Singh, Amitkumar., Dubey, S.K. and Bhatia, M.G. "Design and Simulation of FPGA based Digital System for Peak Detection and Counting" *International Journal of Advanced Research in Computer Science and Software Engineering*, vol. 3, pp. 804-807, Nov. 2013.

