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Design of Aging Aware Reliable Multiplier Using Mixed By-Passing Technique

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Abstract: ***Digital multipliers has many numbers of DSP applications. The overall performance leans on the output of the multiplier. When we apply a negative bias to the PMOS transistor, there occurs temperature instability. The minimum voltage at which the PMOS transistor is ON will be increased whereas it decreases the multiplier speed. Similarly, if we apply a positive bias to the NMOS transistor, temperature instability occurs.This degrades the transistors speed and the system fails because there is a violation in time. There exists an aging-aware multiplier with adaptive hold logic (AHL) circuit. This circuit provides higher throughput through the variable latency. In the existing method, Row or Column bypassing is done to reduce the aging effect. Our desired structure is that we are bypassing column and row together so that the throughput can be increased. We are implementing our advanced design in real time applications like FIR filters.***

Keywords: Adaptive Hold Logic (AHL), Temperature Instability, Mixed Bypassing Technique, Unreliable Latency.

I.INTRODUCTION

Differential multipliers are used in DSP applications, such as digital filtering, Fourier transform, and discrete cosine transform. If multipliers are slow, the circuit's execution will get reduced. When the Si molecule diffuses the boundary traps are left. The accumulated traps between the gate oxide and silicon interface result in increased threshold voltage which further reduces the circuit switching speed. After removing the bias voltage, the reverse reaction starts taking place which reduces the NBTI effect. All traps cannot be avoided by a reverse reaction which is generated during stress phase and Vth can be increased. Hence we are moving for reliable high-performance multipliers. A conventional method to decrease the effect of aging is overdesign, which includes things like guard-banding and increasing in size of the gate. But this approach makes area and power to get increased. Our advanced design makes area and power to be efficient by using AHL.

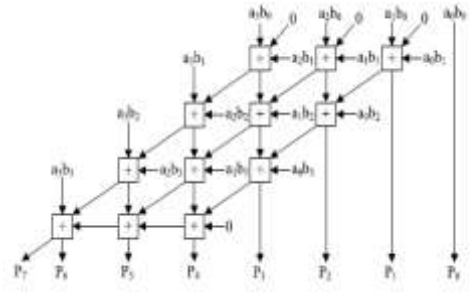

Fig.1. 4*4 Normal array multiplier

II. PRELIMINARIES

1) ARRAY MULTIPLIER

AM is a parallel multiplier. Each adder produces two outputs namely sum and carry. AM depends on add and shift algorithm. It utilizes more gates to increase the output by using the pipelining technique. Its diagram is given in Fig.1.

2) BYPASSING TECHNIQUE

Bypassing technique is performed in the multiplier for power optimization. Bypassing is done in either row or column of adders. Bypassing means turning off any rows or columns or else both in the array multiplier whenever some multiplier or multiplicand or both bits are zero.

Different types of bypassing are:

- Row-bypassing
- Column-bypassing
- Row and column-bypassing
-

ROW-BYPASSING MULTIPLIER

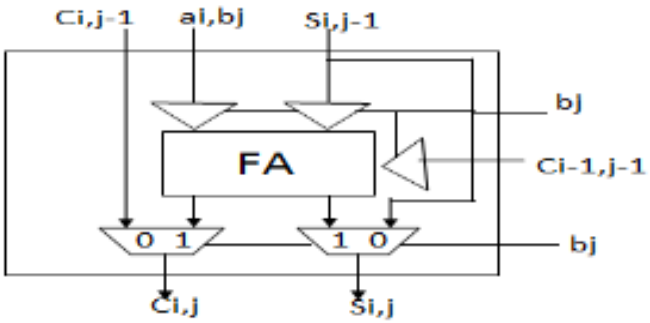

Fig .2. Structure of FA (row bypassing)

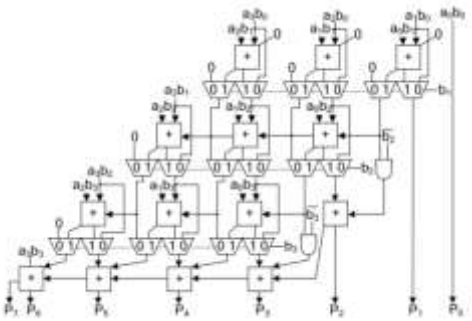

Fig.3. 4*4 row bypassing multiplier

It leans on the number of zeros present in the multiplier bits. During the operation, some rows of adders in the AM are disabled to save the power and also it reduces the usage of clock cycles. The working of low-power row-bypassing multiplier and low-power column-bypassing multiplier are same, but selector of MUX and the tri-state gates use the multiplier bit.
A full adder is added to the 3 triple-state buffers to halt the input. Two 2:1 MUX are attached at the output of sum and carry for switching in between the normal path and bypassed path. The disadvantage is that it requires additional correcting security.

COLUMN BYPASSING MULTIPLIER

It leans on the number of zeros present in the multiplicand bit. During the operation, some column of the adders in AM are disabled to save the power. Here each full adder is added with two tri- state buffers. At the carry input side, the tri-state buffer is not required. Two 2:1 MUX are connected at the output of sum for switching between the normal path and bypassed path. The advantage of column bypassing is that extra correcting circuit is eliminated. And it uses the simple full adder.

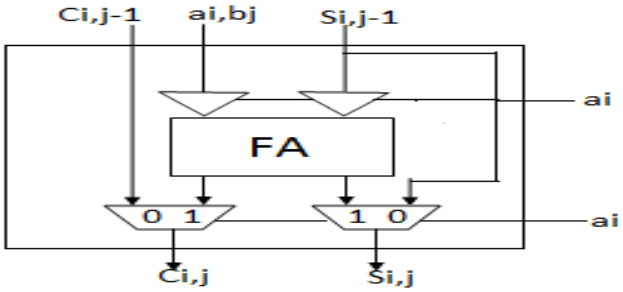

Fig .4. Structure of FA (column bypassing)

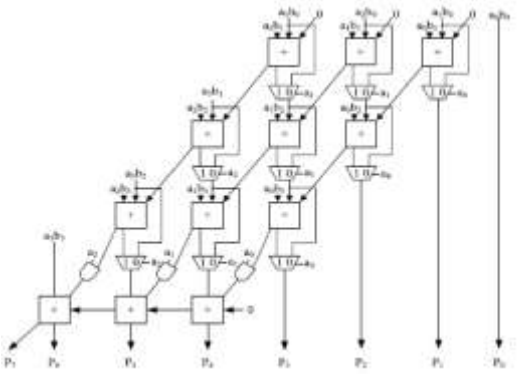

Fig.5. 4*4 column bypassing multiplier

3) VARIABLE LATENCY DESIGN

It is used to depreciate the timing waste which occurs in conventional circuits which use the crucial cycle as an execution cycle. It divides the cycle into two paths. They are a precise path and deeper path. Precise path executes in a single cycle and deeper paths execute in two cycles. To enhance the accuracy of the hold logic and to optimize performance, a short path activation function algorithm was proposed.

4) AGING EFFECT

When PMOS or NMOS transistor is given a voltage of negative or positive bias respectively, results in V_{th} drift. After removing the bias voltage, the recovery process will occur to depreciate the V_{th} drift. If the constant stress is applied to NMOS (PMOS) transistor, it is called as static PBTI (NBTI). When the characteristic nature of stress along with the recovery phases is called as dynamic NBTI (PBTI). The drift in threshold voltage of the classification of MOS transistors which is due to static effect is depicted by dc reaction-diffusion (RD). The model transition occurs when the transistor is under alternative phases, which in turn causes to change from dc RD model to a RD model.

III. PROPOSED ARCHITECTURE

1) RAZOR FLIP-FLOP

It is used to check whether one cycle is enough to complete the operation. Otherwise, it exhibits two cycles to carry out re-execution. It contains the operation of a digital flip flops like D, shadow latch, XOR gate and MUX. Razor flip-flop is used

to for finding the instant violations. As a result, the main flip-flop fetches the operation result.

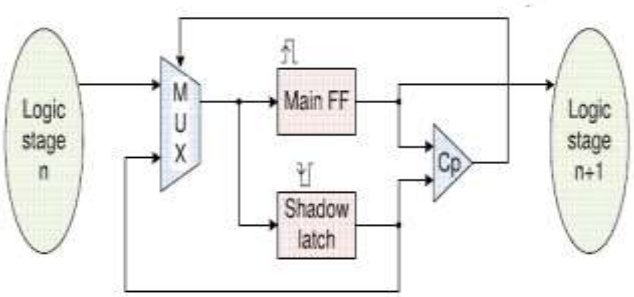

Fig.6. Razor flip-flops

The shadow latch catches the result using a delayed clock signal. If the resulting bit of flip-flop differs from shadow latch, then timing transgression will exist. The comparator obtains the error signal and this error from razor flip-flop is advised to AHL. Therefore the error is corrected within a few cycles.

2) ADAPTIVE HOLD LOGIC

The working principle of AHL is variable latency technique. It will check for the number of execution cycle needed to perform the operation. It will also give the minimum performance degradation after considering the aging effects. Fig.7 Adaptive Hold Logic circuit. Let the input bit for AHL circuit be 'm'.

AHL contains the following block.

- Aging indicator
- Judging blocks
- D flip flop
- One multiplexer

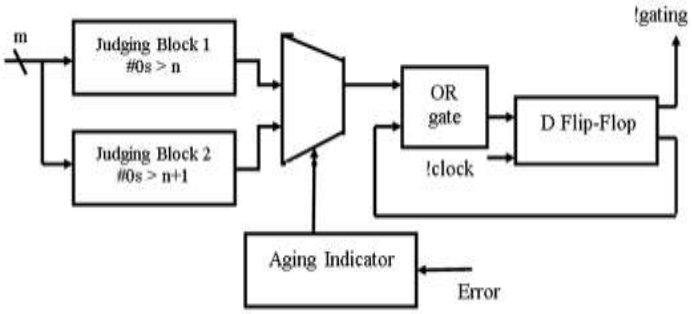

Fig.7 Adaptive hold logic circuit

AGING INDICATOR

It is used to check the performance degradation caused because of aging effect. Initially, the indicator shows a null value i.e. the output is 0. It is incorporated in the unit called counter which is used for counting the errors as a whole. At the outset of the operation, aging indicator output is set to zero.

JUDGING BLOCKS

AHL contains two judging blocks. The first block output is one, if the count of zeros present in the input sequence is more than n, provided that the n value is decided by the user. The corresponding block output is 1 if the zero count in the input sequence is higher than n+1. Initially, the depreciation effect is not significant. Hence first judging block is used. If it becomes significant after some period of time, the second judging block is used.

OPERATION OF AHL CIRCUIT

The judging blocks decide the execution cycles required for completing the operation when the input sequence arrives. Now the result will rely on both the output from the judging blocks which is passed to the multiplexer. It will select the result, according to the outcome of aging indicator. The result of the multiplexer and the complement of Q signal from D flip-flop are given to OR gate.

Then the result of OR operation is given to D flip flop.

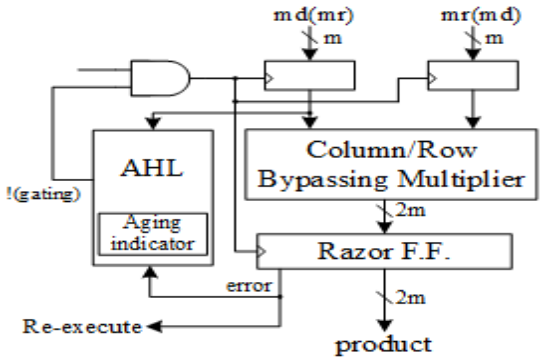

Fig.8. Proposed architecture model

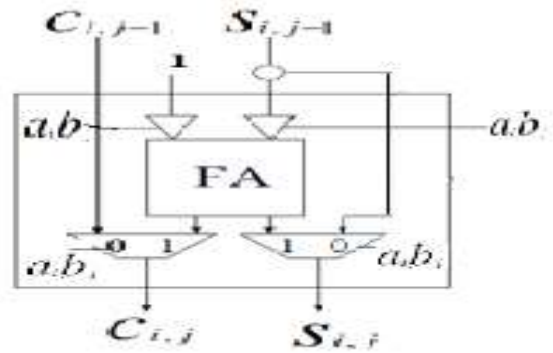

Fig.9. Structure of FA (Mixed bypassing)

The output of MUX is 1 when the input series requires 1 cycle. The value of!(gating) the signal is one and the new data will be latched by flip-flops in next cycle. The result of MUX is 0 when the input sequence needs 2 cycles for completing the operations. Now the result of OR gate is 0. As the result, it neglects the clock signal for next cycle. Now the!(gating) signal value is 0.

3) MULTIPLIER WITH AHL ARCHITECTURE

It contains the inputs of two m-bit and output of 2m-bit, a row or column by-passing multiplier, razor flip flops and AHL circuit. The row or column by-passing multiplier and AHL circuit start working simultaneously after the start of the input pattern. AHL circuit determines the count of the execution cycle. AHL output is 1 for conventional operations and it will be zero to disable triggering signal of D flip-flop when input requires two cycles for its completion.

For row multiplier, the signal fed to AHL is multiplication. On the other hand, the column becomes the multiplicand. The outcome of row or column by-passing multiplier is given to razor flip-flops. The path delay timing violation is checked by razor flip-flops. If timing violations exist, the multiplier will give an incorrect result. Now the operation is again executed with two cycles which cause the latency. Our proposed AHL multiplier predicts the count of execution cycles. When this AHL circuit predicts incorrectly, few of the input pattern causes the timing variation.

4) MIXED BY-PASSING TECHNIQUE

The carry from the previous row is considered to get correct carry propagation. The advantage of this mixed technique is low power consumption. The triple-state buffers are placed at the input. Two 2:1 MUX is used at the sum and carry side for switching between the normal path and by-passed path. Disable signal transformation in adder are by-passed when the buffer state is 1 and the incoming sum bit is by-passed downwards.

AND gate is used as signal gating element in modified FA. If the column is by-passed, (Ai=0), AND gate does not permit signal at other input of AND gate and carries out is equal to zero. When a row is bypassed (B_j=0), C_i is given as input of carrying MUX. The selection of the line for the multiplexer is B.

In the mixed by-passing technique, the area, power, and delay are reduced. It will further reduce the cost of the multiplier.

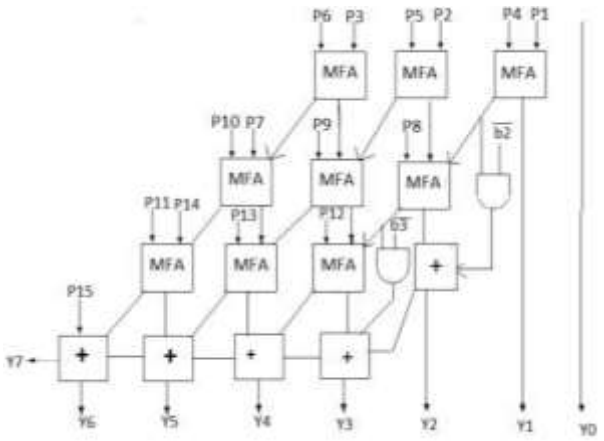

Fig.10 Row and Column bypassing multiplier

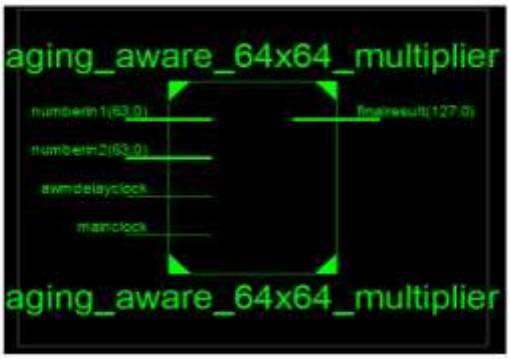

Fig.11 Block diagram of aging-aware 64*64 multiplier

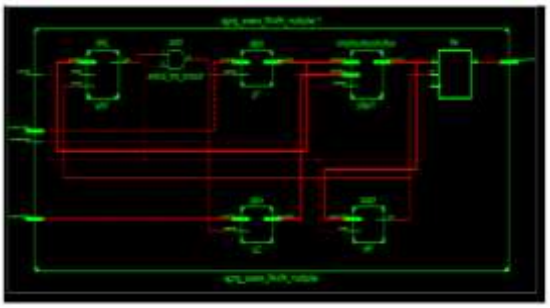

Fig.12. RTL schematic of 64*64 aging-aware multiplier

IV.SIMULATION RESULT

The experiment is done in Xilinx ISE software where VHDL code is used for design implementation. The throughput of the multiplier is compared with various bypassing techniques. Row by-passing multiplier needs extra correction circuit and

Fig.13. Simulation output waveform of array multiplier.

Measuring Quantity	Types of Multipliers			
Power(mW)	Array multiplier	Row multiplier	Column multiplier	R&C multiplier
	123	113	95	108
Delay(ns)	21.131	20.0621	17.423	19.311
Area (No.of slices)	18	27	17	25
Power delay product	2599.113	2267.0173	1655.185	2085.588
Area delay product	380.358	541.6767	296.191	482.775

Fig.14. Comparison table

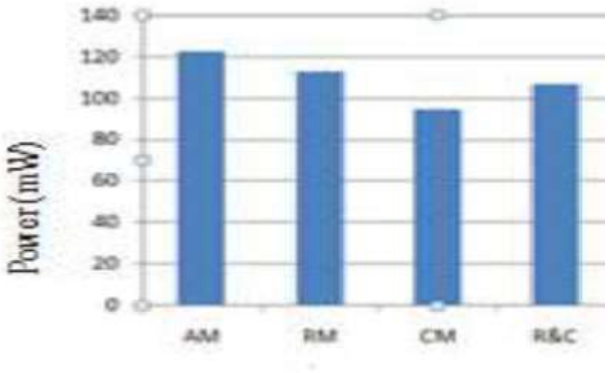

Fig.15. comparison graph

The structure of Full adder is difficult. Power utilization is low but Area is high. In column by-passing power usage is less, but the area is high. In mixed by- passing area, power and delay are reduced.

CONCLUSION

This paper proposed a reliable aging-aware multiplier with mixed by-passing technique. Our method uses variable latency design to have low-performance degradation. Reduction in power is the main aim of VLSI system design. Total power usage is get reduced by decreasing the dynamic power.

By reducing power, area and delay the circuit performance is enhanced. Therefore the mixed by-passed multiplier is efficient in DSP application of VLSI design.

FUTURE WORK

The length of the device can be increased in future. It can be done for unsigned multiplier too. It can also be implemented in real time applications.

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