BROOKSPEAK

Ground Bounce Part 1:

By Douglas Brooks, President
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As signal rise times continue to increase, a phenomenon called "ground bounce" begins to be an issue. But many people don't know what it is or don't know much about it. Here are some things it isn't. It isn't what happens when Ken Griffy Jr. hits a ground ball. It's not what happens when your checkbook gets really low. And its not what happens in an earthquake. It IS a source of circuit noise and signal distortion that occurs inside an IC package, and therefore is not well understood by some people outside the semiconductor industry.

Should you be concerned? Well, since it happens inside a package, there isn't much a designer can do about it. But a very similar phenomenon occurs outside the package on the board. There, the designer CAN (and in fact should) do something about it. Therefore, it is useful to understand this and related phenomena.

This month's column will explain ground bounce. Next month's column will extend the discussion to related issues and what the circuit and board designers need to do about it.

A very simplified schematic of an output circuit is shown in **Figure 1**. The output goes high when Q2 turns off and Q1 turns on. Similarly, the output goes low when Q1 turns off and Q2 turns on. When the signal transitions from high to low, Q2 provides a path for current to flow from the output to ground. How much current flows depends on, among other things, how many devices (loads) are connected to the output. The loads tend to be capacitive, so the initial current spike is not negligible. The output voltage (Vout) is measured between the output pin of the device and Ref B, which is at ground. Similarly, when the output goes high, Q2 turns off and Q1 turns on. Vout rises to Vcc (Ref A) less the voltage drop across Q1.

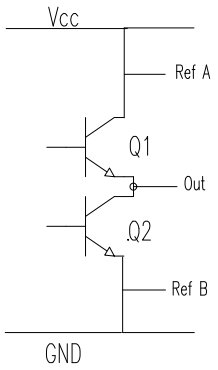

Figure 1
Typical Output Circuit

Actually, Ref A is not at Vcc and Ref B is NOT at ground. Ref A is the positive voltage point on the chip and Ref B is the ground on the chip. **Figure 2** illustrates that there is some inductance in the very small lead wires between the chip itself and the lead carrier of the package. This inductance is very small, but it is not necessarily trivial.

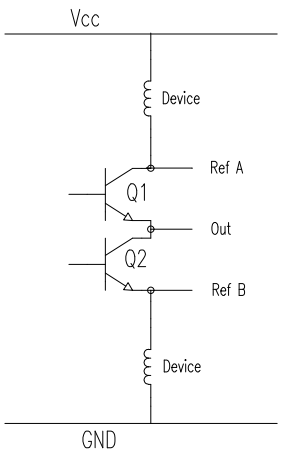

Figure 2
Effects of internal lead inductance

Consider what happens the moment Q2 turns on and Q1 turns off. A spike of current flows from the output through Q2 to ground. This current flows through the inductance in the lead. The voltage across this inductance (V Ref B) is directly related to the change in current ($V = L * dI/dt$). And dI/dt? That's related to rise (and/or fall) time of the device. The faster the rise and fall times, the smaller is dt, the greater is dI/dt (the change in current per unit time) and the higher is the voltage drop across any inductance.
Now, as Q2 turns on and the output voltage starts to fall, the voltage between the output and Ref B falls just as before. But the voltage at Ref B, relative to ground rises because of the current spike through the lead inductance. Thus, Vout does not fall all the way, but "bounces" above ground because of this inductive drop. This is called ground bounce.

Now, a device down stream has an input that is referenced to ground. It is looking for a signal from Q2 that is a certain level (spec'd at the level between the output and Ref B.) What it sees is that voltage plus the ground bounce --- i.e. a signal that doesn't immediately fall all the way to the spec'd logical low. That's why ground bounce is bad!

Now, let's switch the circuit the other way, Q2 turns off and Q1 turns on. Current flows from Vcc through Q1 to the output. How much depends on the loads. The current flowing through Q2 and the inductor at Ref B stops, and there is a negative dI/dt voltage drop across the inductor at Ref B. Thus the real Vout tries to rise to the spec'd value above ground, put it is pulled down by the negative voltage spike at Ref B and perhaps by some of the voltage drop across Ref A. The device downstream is looking for a spec'd logical high voltage value above ground, but sees a voltage which is that less the inductive drop at Ref B and at least some influence from the inductive drop at Ref A. This is also called ground bounce.

All voltages return to their spec'd values relative to Vcc and ground after the currents stop changing and reach

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their steady state values (i.e. when dI/dt goes to zero.)

Obviously, the integrated circuit is designed to be able to operate dependably in this environment. The chip input circuit recognizes a logical high that is some level below the maximum spec'd value, and recognizes a logical low that is higher than the minimum spec'd value. This ability is called the noise margin of the device. As long as the "noise" level contributed by the lead frame inductance is within this noise margin, it is not a concern.

So, should you, as a designer, be concerned about these inductances? The answer is no. They are not large enough to cause problems in a normal environment (at least if the device manufacturer has been truthful in his specs and careful in his manufacturing processes.) And, there is nothing about it you can control, anyway. What you DO need to be concerned about is the ADDITIONAL inductances you are going to insert between Ground (or Vcc) and the device which are going to add noise to the circuit that looks exactly like ground bounce, which WILL increase the noise, which MAY cause the noise to exceed the noise margins, and which you CAN do something about.

That's for next month.

BROOKSPEAK

Ground Bounce Part 2:

By Douglas Brooks, President
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Last month I described a phenomenon called "Ground Bounce." To quickly review that column: The output voltage of an IC is referenced to the ground on the chip (Ref B in **Figure 1**), but we see it in our system referenced to the ground pin of the package. The tiny wire connection between the chip and the lead frame of the package contributes a small amount of inductance in the circuit. When Vout goes low, a spike of current flows through this inductance and creates a voltage spike at Ref B. A device connected to the output of our circuit sees a logical low that is the spec'd low for the device PLUS the voltage spike across the inductance of the lead frames. This is called ground bounce.

But the situation gets worse (isn't that always the way?) The Vcc and ground pins of the package are not at Vcc and ground. Vcc and ground are established and regulated at the power supply. When Q2 turns on and current flows to "ground", it must not only flow to the ground pin of the package, but then across the ground plane to the true reference ground at the power supply.

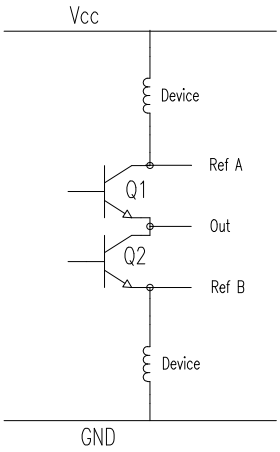

Figure 1
Typical Output Circuit

The plane has both a resistive component and an inductive component between the package pin and the power supply ground. So a better representation of the situation is **Figure 2**. Now, if Q2 turns on and the output goes low, the dI/dt current flow passes through both the inductance of the lead wire in the chip and also the inductance of the ground plane. Vout becomes the spec'd Vout (referenced to the chip ground) PLUS the voltage across the inductance of the lead wire Plus the voltage across the inductance of the plane. Now we are talking about a "bounce" that can be destructive.

So what do you, the designer, do? You use heavy copper planes. You make them as full as possible with as few cuts and holes as possible. But, in fact, this inductance in many high speed circuits is just too large to tolerate. So you use bypass caps.

The purpose of bypass caps is to provide something that looks like a regulated Vcc and ground right at the package for a short time until the inductance of the planes can be overcome. **Figure 3** illustrates this. With well designed and placed bypass caps, the transient currents when the logic device changes state don't have to flow to and from the power supply somewhere on the board, they simply flow to and from the cap.

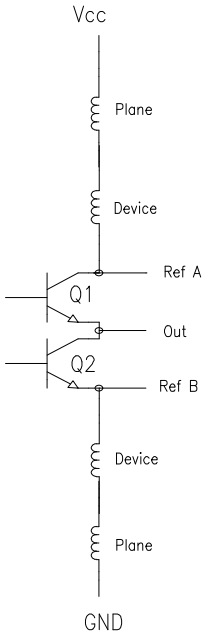

Figure 2
Planes Add Additional Inductance

Now, there is one more gotcha (isn't that always the way?) The leads and traces associated with the bypass caps have inductances associated with them (**Figure 4**). By-

pass caps improve the noise problem contributed by the planes dramatically, but they introduce their own noise source. Now, if Q2 turns on, Vout will be the spec'd value referenced to the chip ground, plus the voltage "bounces" associated with the chip lead wire plus the inductance of the bypass cap lead.

This is why we place bypass caps as close as possible to the device we are protecting and use wide traces, etc., to minimize this added inductance.

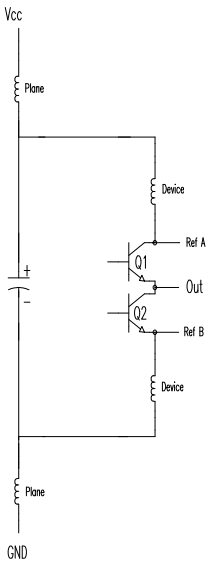

Figure 3
By Pass Caps Provide Local Charge Storage

There is some confusion in the industry about one aspect of the placement. (a) The bypass cap can be placed close to the ground pin of the package, which minimizes the inductance in the ground path but increases it in the Vcc path. Or (b), the bypass cap can be placed close to the Vcc pin, which minimizes the inductance in the Vcc path but increases it in the ground path. Or (c), we can place the bypass cap half way between and equalize the inductance in the two paths.

Most engineers instinctively think (a) is correct. The Motorola FACT book, and at least one speaker at a PCB Design Conference states that (b) is the correct answer. I posted this question on the IPC's DesignerCouncil e-mail forum (which I encourage all of you to join*). The best answer I got back was "I've been wondering the same thing. When you find the answer let me know!" I called an applications engineer at Motorola and read him the paragraph from their own FACT book. His response? "Gee, I'm not sure I agree with that!" If any one has a definitive answer to this question, let me know and I'll print it in this column. Until then, here is the TRUTH (as interpreted by Brookspeak!)

The bias toward (b) goes back to the days of radio tubes, when signal outputs were extremely sensitive to voltage changes at the plate of the tube! The answer about placement depends on where the signal is referenced. In typical TTL, GTL and ECL circuits, signals are referenced to ground. They are affected more by noise on ground than they are by noise on Vcc. So you want to keep ground as clean as possible and locate bypass caps as close as possible to the ground terminal of the device.

In some circuits, such as MOS and CMOS, the devices switch between the two power supply rails and are affected equally by Vcc and ground bounce. A case can be made to locate the bypass cap equally between the Vcc and ground pins of the package in these cases.

And the best design practice is to tie the bypass cap leads to the planes, and run traces (off the planes) from the device pins to the cap (of course, making the traces as short and as wide as possible to minimize inductance.). Keeping these traces off the plane will isolate them from any other noise that might exist on the plane from other parts of the circuit.

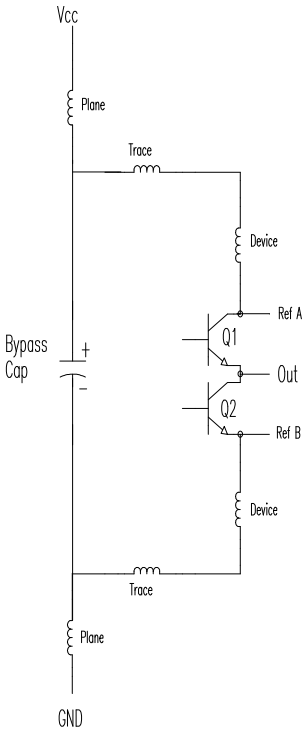

Figure 4
By Pass Caps Add Lead and Trace Inductance

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