Recent Trends in CMOS Low Noise Amplifiers

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***Abstract* - This paper presents an overview and comparison of CMOS low noise amplifier (LNA) architectures. A brief review of noise figure and linearity is presented to give the reader some background into typical performance measures of LNAs. A traditional radio frequency (RF) receiver architecture is presented and LNA performance is related to overall receiver performance. Recent CMOS LNA performance comparisons are made and a representative LNA architecture is reviewed. The two highest performance CMOS LNAs to date (introduced at ISSCC 2001) in terms of noise figure and linearity are reviewed. Finally, a predicted low-voltage CMOS architecture based on an innovative bipolar architecture is presented.**

I. INTRODUCTION

Low Noise Amplifiers (LNA) are the backbone of radio frequency (RF) communications receivers. Their specifications define the overall noise performance and can have deleterious effects on the linearity of the RF receiver. However, consumer demands to increase the frequencies at which RF systems operate are straining the capabilities of existing architectures.

CMOS LNAs are recently drawing intense attention because users want a cheaper, fully integrated solution. Bipolar solutions generally offer higher performance, but cannot be fully integrated with the receiver's baseband digital signal processing which is inherently realized in CMOS technology.

This paper gives an introduction to the fundamental concepts of LNAs and their relevance to modern wireless communications receivers. Section II introduces two fundamental concepts in LNA performance measure, noise figure and linearity. Section III will show how these two performance measures affect the overall specifications of a RF receiver. From there, some traditional CMOS architectures are described in Section IV. The two highest performance CMOS LNAs to date (reported at ISSCC 2001) are described in Section V. Finally, a prediction of a future CMOS LNA design is presented in Section VI.

II. TWO FUNDAMENTAL PERFORMANCE MEASURES OF LOW NOISE AMPLIFIERS

Noise Factor and Noise Figure

The noise factor (F) of a two port stage is simply defined as:

$$F = \frac{SNR_{IN}}{SNR_{OUT}} \tag{1}$$

where SNR_{IN} and SNR_{OUT} are defined as the signal-to-noise ratios at the input and the output of the stage, respectively. Thus the noise figure is a measure of the degradation of the SNR through a stage. A stage with better noise performance has a lower noise factor (the minimum being 1).

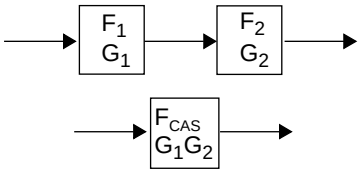


Figure 1: Noise factor of a cascaded system

For a cascaded system of two stages as shown in Fig. 1,

$$F_{CAS} = F_1 + \frac{1}{G_1}(F_2 + 1) \tag{2}$$

where G_1 is the gain of the first stage and F_1, F_2, F_{CAS} are the noise factors of the first stage, second stage and the cascade of the two stages, respectively. Hence, the noise factor of the entire cascaded system depends only on the noise figure of the first stage, given that the gain G_1 of the first stage is large enough to make the second term of equation (2) negligible. *Because LNAs are the first gain stage in a RF receiver, they are required to have moderate gains and low noise factors.*

Finally, the noise figure (NF) of a system is simply the noise factor (F) measured in Decibels:

$$NF = 10\log(F) \quad in\ dB \tag{3}$$

Noise figure is used instead of noise factor to characterize LNAs in literature and will be used through the remainder of this paper.

Linearity - Third-order intercept point (IP3)

The IP3 of stage is a measure of its linearity. While many analog and RF circuits are approximated with a linear model to obtain their response to small signals, non-linearities often lead to harmful phenomena. For this discussion, we assume that an input of *x(t)* to a system leads to the linear and nonlinear output:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \qquad (4)$$

We find that if *x(t)* consists of sinusoids of two frequencies ω_1 and ω_2, then output contains terms at the frequencies $n\omega_1$ +/- $m\omega_2$. These terms are called intermodulation (IM) products are present due to the nonlinearity of the system described in (4). The *order* of an intermodulation product is *(n+m)*.

Of particular interest are the third-order IM products at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$, illustrated in Fig. 2. If the difference between ω_1 and ω_2 is small, the components at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ will appear very close to the original signals. These unwanted signals may cause errors in the detection of the wanted signals.

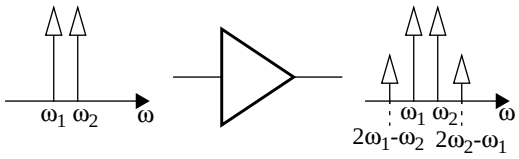


Figure 2 Third-order intermodulation in a nonlinear system

A measure the relative strength of the unwanted signals at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ is the third-order intercept point (IP3). Two equal power tones at frequencies ω_1 and ω_2 are applied to a system and the power of the third-order IM products are measured. A typical plot of output vs. input power in dBm [= 10log(x/0.001)] is shown in Fig. 3.

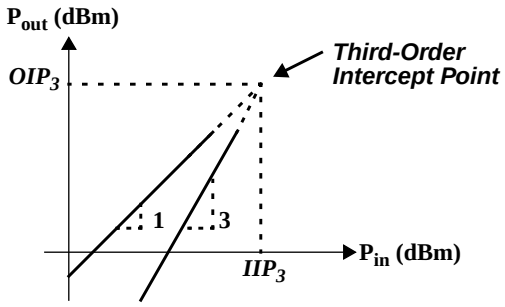


Figure 3 Growth of Output Components in an intermodulation test

The top line is a plot of the power of the linear term of equation (4) and the bottom line is a plot of the power of the third-order IM products. It can be shown that the power of the third order IM products increases with a slope of three relative to the slope of the linear gain line. The IP3 is the point at which the two lines intersect. A standard measure in RF circuits is the IP3 referred to the input power called the input-referred IIP3 (or IIP3). As inferred from Fig. 3, higher values of IIP3 mean lower third-order IM products for a given input power. *Thus, the higher the IIP3 of LNA, the better its linearity.*

III. A MODERN COMMUNICATION RECEIVER

In this section, a typical communication receiver architecture is presented. The performance measure of the entire receiver is also related to the performance of the LNA.

Fig. 4 shows the basic architecture used in many RF receivers. The RF signal is detected by the antenna and put through a band pre-select filter with unity nominal gain in the band of interest. The band pre-select filter usually has low selectivity (wide passband) because its passband is centered at such high frequencies. The LNA is the first gain stage of the receiver, and may or may not be tuned to a specific passband. Image reject filtering may be in the signal path before a mixer brings down the RF signal to the intermediate frequency (IF) for further signal processing.

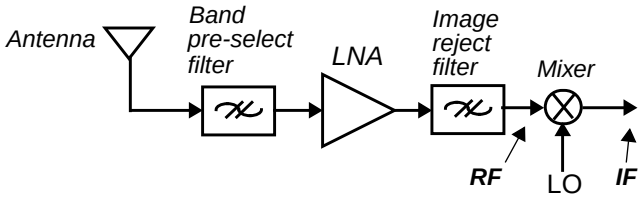


Figure 4 A Typical Wireless Receiver

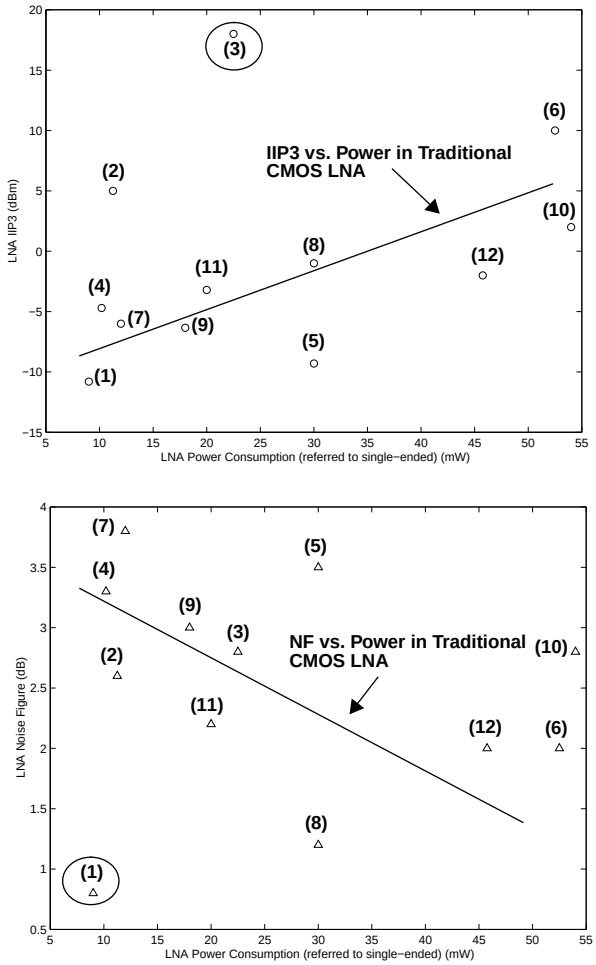
From equation (2), it is seen that the LNA is responsible for providing the first gain in the receiver while itself contributing as little noise as possible. Although the mixer tends to define the linearity of a given receiver, an exceptional IIP3 in the LNA allows the linearity of the mixer to be relaxed considerably. This can be greatly advantageous in some architectures.

The LNA impedances should be matched closely to 50 Ω at both its input and output for maximum power transfer at radio frequencies. LNA input and output matching is also essential because RF filter responses are heavily dependent on matching conditions. Finally, the LNA must have good reverse isolation (signal path from its output to input) so that the LO signal at the output is not permitted to traverse backwards through the LNA into the antenna (a phenomenon known as LO leakage).

IV. TRADITIONAL CMOS LNAS

The term ‘traditional’ is a misnomer when it comes to CMOS LNAs. As late as 1996, only four published papers on CMOS LNAs existed in literature [4]. In fact, CMOS LNA architectures have not changed drastically since the first published CMOS LNA because most advancements were accomplished during the bipolar age of RF circuits.

However, some interesting design styles that optimized noise figure and/or linearity at moderate power consumptions have dominated over the last five years. A plot of recent trends in CMOS LNA achievements is shown in Fig. 5. The solid line in each graph shows the IIP3/power and NF/power trade-off. In general, power can be exchanged for lower NF and higher IIP3.



(1) Leroux 2001, CMOS @ 1.23GHz [1]
(2) Ding 2001, 0.35um CMOS @ 900MHz [2]
(3) Ding 2001, 0.35um CMOS @ 900MHz [2]
(4) Janssens 1998, 0.5um CMOS @ 900MHz [3]
(5) Shaeffer 1997, 0.6um CMOS @ 1.5GHz [4]
(6) Rodgers 1999, UTSi CMOS @ 2.0GHz [5]
(7) Shahani 1997, 0.35um CMOS @ 1.6GHz [6]
(8) Floyd 1999, 0.8um CMOS @ 900MHz [7]
(9) Zhou 1998, 0.6um CMOS @ 900MHz [8]
(10) Kim 1998, 0.8um CMOS @ 1.9GHz [9]
(11) Karanicolas 1996, 0.5um CMOS @ 900MHz [10]
(12) Huang 1999, 0.25um CMOS @ 900MHz [11]

Figure 5 Trends in Noise figure and IIP3 in recent CMOS LNAs

Designs 1 and 3 are state-of-the-art representatives of optimum noise figure and linearity, respectively. These designs will be discussed in the next section. Design 11 (Karanicolas [10]) is a representative high performance design, reporting the lowest noise figure and highest IIP3 per unit power until this year. Other designs (12, 8, 6) give better performance but with at least 50% more power consumption.

The basic problem with using CMOS for LNAs is its inherently low transconductance and hence small gain. A typical CMOS LNA suffers from not providing enough single stage gain to make the second term in equation (2) negligible. Thus, CMOS LNAs usually trade power for noise figure by increasing bias currents.

Karanicolas, however, uses an intelligent current-reuse technique to effectively double the

transconductance of a single stage without increasing the bias current. Fig. 6 shows a simplified schematic of design 11. Transistors M_1 and M_2 are essentially a digital inverter biased for large gain by the negative feedback loop. The key to this design is that given the same bias current, the effective transconductance of this LNA is $g_{m1} + g_{m2}$ versus simply g_{m1} in the case that transistor M_2 were omitted.

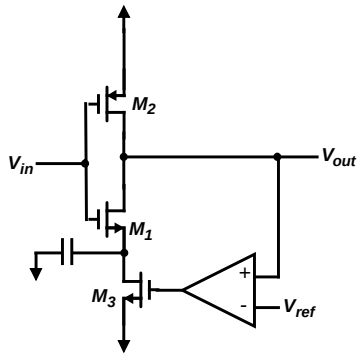


Figure 6 Simplified current-reuse LNA schematic [10]

The design was optimized for linearity (maximum IIP3) by choosing V_{ref} so that the output obtains the maximum swing without clipping. The actual design uses two of these identical stages in cascade for better reverse isolation (to block signals from the output from leaking back to the input). A major drawback of this design is its inherently high input and output impedances, requiring it to have external matching networks. This obstacle precludes the use of this design in fully integrated applications.

V. STATE-OF-THE-ART CMOS LNAS

Lowest noise figure to date

Design 1 in Fig. 5 has the lowest reported noise figure to date. Leroux's design has achieved this while also consuming a fraction of the power compared with other designs. It achieves input and output matching on-chip and includes the effects of ESD protection diodes, making it fully integratable.

Fig. 7 shows the simplified schematic of the design [1]. To maximize gain and reverse isolation while conserving power, a cascode topology is used. Furthermore, degradation of linearity is prevented because only a single stage is employed. The cascode configuration minimizes the Miller effect, significantly lowering the input capacitance seen at the gate of M_1 and enhancing stability. The use of a load inductor L_2 permits large gains with no DC voltage drop, a necessity for low-voltage design (1.5V). The input of LNA is protected from ESD by two reverse-biased diodes D_1 and D_2.

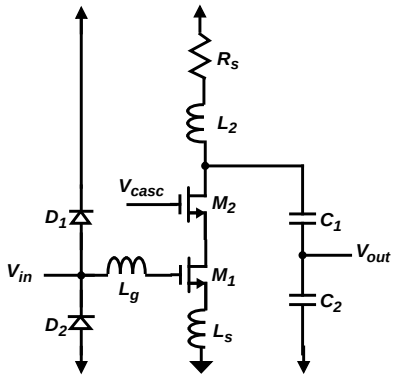


Figure 7 Simplified LNA schematic with ESD protection

The input and output impedances are matched to 50 Ω by using on-chip impedence transformations [12]. The input matching (to 50 Ω) is accomplished with on-chip inductors L_g, L_s and transistor M_1. The input impedence at high frequencies is:

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs1}} + \left(\frac{g_{m1}}{C_{gs1}}\right)L_s \tag{5}$$

which can be set to a real impedance of 50 Ω at resonance (@1.23 GHz for this application) with proper component selection. The output impedence match is achieved by the capacitive divider of C_1 and C_2 and the load inductor L_2. At resonance, the impedence seen at V_{out} is 50 Ω, while the impedence seen at the drain of M_2 is 500 Ω. Thus, a high gain is attained even under matched conditions.

The noise figure of this design is minimized by careful device sizing and layout. The large gain of the single stage minimizes the last term in equation (2). As shown in [1],[13], intricate

second order noise effects which are beyond the scope of this paper are taken into account to minimize the noise figure. This design is highly attractive because it is fully integrated and is the first published design (to the author's knowledge) to incorporate ESD protection making it immediately viable for commercial use.

Highest IIP3 to date

Design 3 reports the highest linearity in a LNA to date. Ding [2] achieves IIP3 maximization by introducing an architectural innovation. The placement of two LNAs in parallel allows the third-order IM products to be effectively cancelled. The drawback of this design is a doubling of power consumption due to the dual-LNA architecture.

The basic innovation in this LNA is the cancellation of the third-order harmonics. Omitting the second term (because the second-order harmonics usually fall out band) of equation (4) gives:

$$y(x) = Ax\left(1 + \alpha_2 x^2\right) \tag{6}$$

If an auxiliary signal path with β times the signal gain is also passed through an identical system, then the third harmonic is cancelled by subtracting $1/\beta^3$ times the auxiliary output from the primary output [2]. The procedure is shown below:

$$y_{main}(x) = Ax\left(1 + \alpha_2 x^2\right)$$

$$y_{aux}(\beta x) = A\beta x\left(1 + \alpha_2 \beta^2 x^2\right)$$

$$y(x) = y_{main}(x) - \left(\frac{1}{\beta^3}\right) y_{aux}(\beta x)$$

$$= A\left[1 - \left(\frac{1}{\beta^2}\right)\right] x \tag{7}$$

The third harmonic caused by the third-order term is completely cancelled theoretically. However, nonlinearity cancellation is limited in practice by device mismatches which are on the order

of 1%. The auxiliary LNA consumes additional power and decreases the gain of the main LNA by $1/\beta^2$ as shown by equation (7).

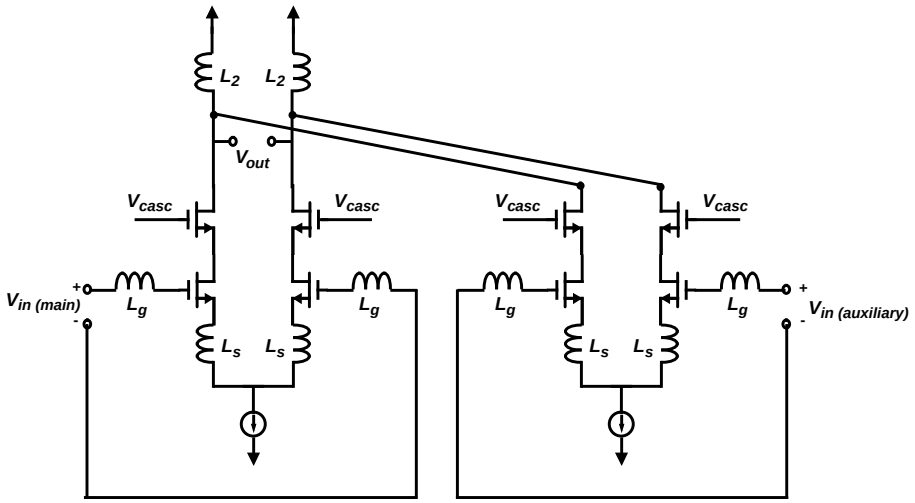


Figure 8 Simplified high linearity LNA schematic

Fig. 8 shows a simplified schematic of the design [2]. Each LNA is implemented differentially with a telescopic cascode inductor-degenerated architecture. This type of CMOS LNA has become the most popular design choice in recent years ([1], [6], [7], [11]) because it achieves high-gain and low noise in a single low-power stage with internal input and output matching. Input matching is achieved with inductors L_g and L_s.

A β of 2 (see equation 7) is chosen for this implementation which means that the auxiliary LNA requires $1/8^{th}$ of the gain of the main LNA. To achieve better matching, the sizes and drain currents through the two LNAs are identical, but only $1/8^{th}$ of the auxiliary output current is subtracted from the main LNA output. Thus, this implementation consumes twice the power.

Since the auxiliary LNA contributes only $1/8^{th}$ more output noise, its addition increases the overall noise figure of the circuit by less than 0.2dB. One major drawback of the given implementation is that the reported power gain (<5dB) of the full LNA is much less than its voltage gain (23.8dB), implying that the output impedance is extremely large and not matched to 50 Ω. This obstacle prevents this LNA from interfacing with external filters (see Fig. 4) at its output and results in extremely poor power transfer.

VI. PREDICTED LNA RESEARCH

As shown in Fig. 5, CMOS LNAs are already capable of achieving high performance with moderate power consumption. However, due to increasing demand for low-power portable devices, future LNA research will be directed at sustaining performance while decreasing power.

As evidenced by the highest performance designs of late ([1], [2], [6], [7], [11]), cascoding of MOS devices has become almost a standard in CMOS LNAs. However, as supply voltages decrease, new architectures for CMOS LNAs must be defined.

An extremely innovative low-power bipolar design (Long, [14]) has yet to be reported in CMOS technology. Fig. 9 shows the simplified schematic. This design can operate at supplies well under 1V because the only required DC voltage drop is across M_1 (about V_{eff}). The input matching is achieved with network L_g and C_1.

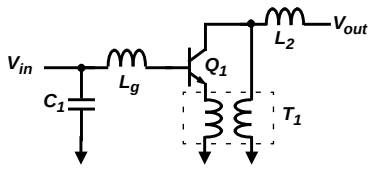


Figure 9 Bipolar LNA incorporating transformer feedback

The integrated transformer T_1 has two purposes. The negative feedback it employs improves the linearity of the circuit. More importantly, the transformer feedback tunes out the Miller capacitor C_{gd}, which is the main reason non-cascoded common-source MOS stages are so unattractive. The normally present feedback path through this capacitor causes poor isolation from the output to the input. This lack of reverse isolation causes instability in the LNA and makes input and output matching extremely difficult (because they are then inter-dependent).

Other forms of feedback which attempt to accomplish this either largely increase the noise figure (feedback resistor from gate to drain) or must be accomplished off-chip with high quality components (inductor and capacitor from gate to drain). This interesting method of transformer feedback permits the design of fully-integratable, stable and extremely low-voltage CMOS LNAs.

VII. CONCLUSION

This paper presented a comparison of recent CMOS LNA architectures in terms of noise figure and linearity. A brief overview of noise figure and linearity (IP3) was presented to give the reader some background into typical LNA perfomance measures. A typical RF receiver architecture was presented and LNA specifications were related to overall receiver specifications. Recent CMOS LNA performance comparisons were made and a traditional LNA architecture was reviewed. Two of the highest performance CMOS LNAs to date in terms of noise figure and linearity were reviewed. Finally, a predicted CMOS architecture based on an extremely low-voltage bipolar architecture was presented.

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