ECE 1371 - Term Paper

MODELING OF SILICON-COMPATIBLE ON-CHIP INDUCTORS

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I. INTRODUCTION

The rapid growth of the wireless communication market has fueled a large demand for low cost, portable products. Traditionally, radio systems are implemented on the board level making use of a large number of discrete components. However, advancements in silicon-compatible (CMOS/Bipolar) IC technology has provided device performance suitable for analog operation up to several giga-hertz thus making it possible to integrate radios on a chip to meet market demands [1]. In addition, inductors are a crucial part of any RF circuit which has prompted a great deal of effort towards the use of on-chip inductors in the quest for higher levels of system integration. On-chip inductances of up to 20 nH [2] are realizable on silicon-compatible IC's using planar spiral geometries. Figure 1 illustrates the layout of a square on-chip inductor. Even though circular geometries have been known to provide a somewhat higher Q, 90° segments have been used since non-Manhattan geometries are not permitted by many technologies. An underpass is used to access the inner spiral.

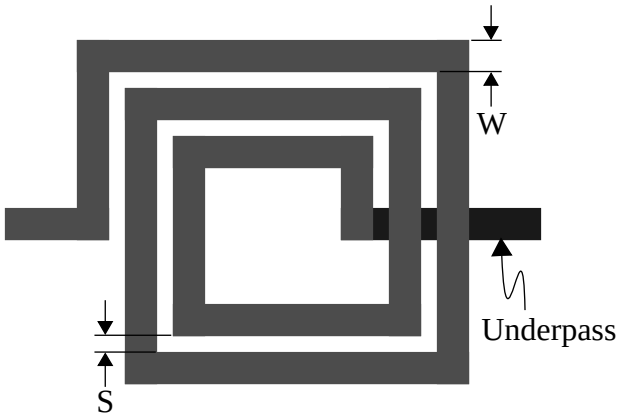


Figure 1 *- Layout of an on-chip inductor (2.5 turns).*

The successful use of on-chip inductors in silicon IC's was first reported by Nguyen and Meyer in 1990 [3]. However, the performance of these inductors suffer from the presence of a low resistivity substrate which is typically in the range of 1 - 100 Ω-cm for modern very large scale integration (VLSI) [2]. Therefore, a good understanding of the factors that effect the performance of on-chip inductors is needed to design these elements for a given application. Section II will clearly define the measure of merit which is used for energy storage elements such as inductors, referred to as the Q factor or the quality factor. The definition of Q factor is somewhat general which can cause some confusion. However, the aim of this section is to clarify any confusions regarding Q. In section III, a summary of common on-chip inductor modeling techniques used is given and a closed form expression for Q is calculated. Section IV summarizes some techniques used to enhance the Q of on-chip inductors and end with a design guideline for implementing close to optimum inductors. Finally, section V gives some conclusions.

II. Quality of Energy Storage Elements

A. Ideal Energy Storage Elements

There are two circuit elements which allow the storage of energy. They are inductors and capacitors. Inductors allow the storage of magnetic energy, while capacitors allow the storage of electric energy. It can easily be shown that the energy stored in an inductor is given by,

$$E_L = \frac{1}{2} L i_L^2 \tag{1}$$

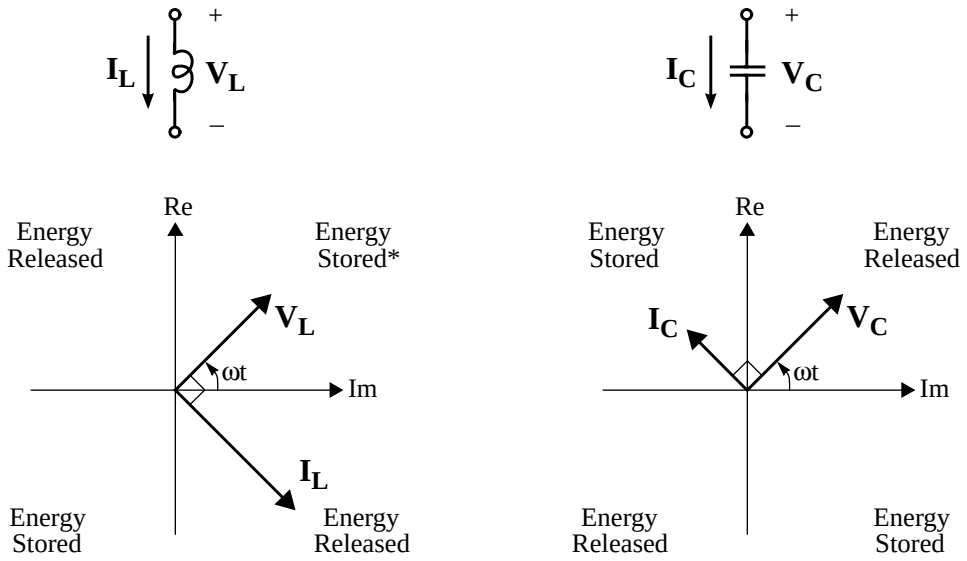
and the energy stored in a capacitor is given by,

$$E_C = \frac{1}{2} C v_C^2 \tag{2}$$

where i_L is the instantaneous current through the inductor and v_C is the instantaneous voltage across the capacitor.

Of interest is the sinusoidal steady state characteristic of storage elements. The sinusoidal steady state current-voltage phasor relationship of an ideal inductor and an ideal capacitor is shown in figure 2. Note that phasor quantities are represented by bold capital letters which will be

the convection used throughout this paper. The current and voltage phasors in these elements rotate at angular velocity of ω radians per second while keeping a constant relative phase ±90°. It is seen from figure 2 that these storage elements store and release energy twice every period. This can also be seen from equations (1) and (2) by noting that under sinusoidal steady state, i_L^2 and v_C^2 increase and decrease twice every period.



* The storage and release of energy in each quadrant is given with reference to the location of the voltage phasor.

Figure 2 *- Sinusoidal steady state current-voltage phasor relationship for inductors and capacitors.*

From equation (1) and the voltage current phasor relationship of an inductor, the peak magnetic energy stored in an inductor in sinusoidal steady state is given by,

$$E_{\text{peak inductor}} = \frac{1}{2}L\left|\mathbf{I_L}\right|^2 = \frac{\left|\mathbf{V_L}\right|^2}{2\omega^2 L} \tag{3}$$

where $|\mathbf{I_L}|$ and $|\mathbf{V_L}|$ correspond to the peak current through and the peak voltage across the inductor. In a similar manner, using equation (2), the peak electric energy stored in a capacitor in sinusoidal steady state is given by,

$$E_{\text{peak capacitor}} = \frac{1}{2}C\left|\mathbf{V_C}\right|^2 = \frac{\left|\mathbf{I_C}\right|^2}{2\omega^2 C} \tag{4}$$

where $|\mathbf{V_C}|$ and $|\mathbf{I_C}|$ correspond to the peak voltage across and the peak current through the capacitor. The above two formulas are very important and will be used again and again to determine the quality of real storage elements.

B. Definition of Quality Factor

The quality factor, or simply the Q of an inductor or a capacitor is a measure of the performance of these elements defined for a sinusoidal excitation and is given by,

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy lost per cycle}} = \omega \cdot \frac{\text{energy stored}}{\text{average power loss}} \tag{5}$$

The above definition is quite general which causes some confusion. However, in the case of an inductor, energy stored refers to the net peak magnetic energy, and in the case of a capacitor, energy stored refers to the net peak electric energy. More will be said on this later.

To illustrate the determination of Q, lets look at some pure lossy inductors and capacitors. Consider first an ideal inductor in series with a resistor (see figure 3). This case models an induc-

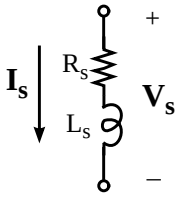


Figure 3 *- Inductor having a series resistance.*

tor with resistance in the winding. Since the current in both elements is equal, we use the equation for the peak magnetic energy in terms of current given in (3) to write,

$$Q = 2\pi \cdot \frac{\text{peak magnetic energy stored}}{\text{energy lost per cycle}}$$

$$= 2\pi \cdot \frac{\frac{1}{2}L_s|\mathbf{I_s}|^2}{\frac{1}{2}R_s|\mathbf{I_s}|^2 \cdot T}$$

$$= \frac{\omega L_s}{R_s} \tag{6}$$

where T is the period of the sinusoidal excitation. Note that the quality factor of an inductor with a lossy winding increases with frequency. This makes intuitive sense since as frequency

increases, the series combination becomes more and more reactive and the phase difference between $\mathbf{V_s}$ and $\mathbf{I_s}$ approaches 90°. Also note that as the resistance in the inductor decreases, the quality of the inductor increases, and in the limit Q becomes infinite since there is no loss. Using the above procedure, the quality factor of other pure lossy inductors and capacitors can be determined. The results are summarized in figure 4. An interesting result worth noting is that of the fourth case in figure 4 which models a capacitor having a finite resistance dielectric. It will be seen later in section III that this models the finite resistance substrate in a silicon-compatible technology. It is seen that Q in this case decreases as the conductivity of the dielectric increases.

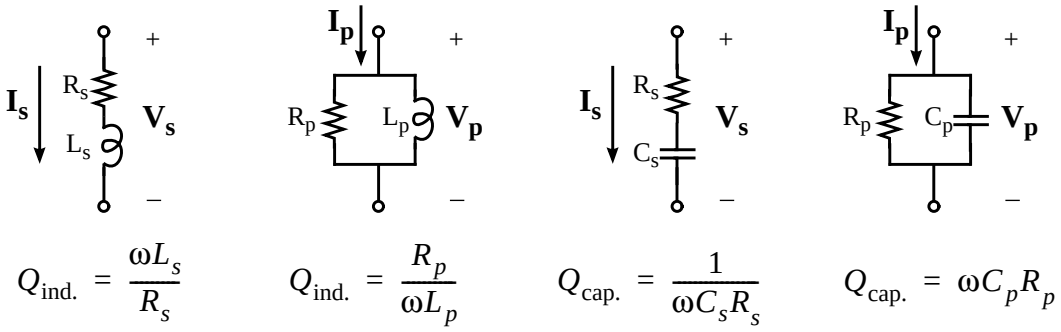


Figure 4 *- Quality factor of pure lossy inductors and capacitors.*

C. Q of Real Inductors and Capacitors

The definition of quality factor was given in the previous subsection. Interestingly, this also defines the Q of an LC tank. As previously mentioned, this definition is general in the sense that it does not specify what stores or dissipates the energy. The subtle distinction between an inductor or capacitor Q and an LC tank Q lies in the intended form of energy storage. I an inductor for example, only the magnetic energy stored is of interest and any energy stored in the inductors electric field because of some inevitable parasitic capacitance in a real inductor is counterproductive. Therefore, the Q of an inductor is proportional to the net magnetic energy stored and is given by,

$$Q_{\text{ind.}} = 2\pi \cdot \frac{\text{net magnetic energy stored}}{\text{energy lost per cycle}}$$

$$= 2\pi \cdot \frac{\text{peak magnetic energy - peak electric energy}}{\text{energy lost per cycle}} \qquad (7)$$

For a capacitor the exact opposite is true and we have,

$$
\begin{aligned}
Q_{cap.} &= 2\pi \cdot \frac{\text{net electric energy stored}}{\text{energy lost per cycle}} \\
&= 2\pi \cdot \frac{\text{peak electric energy - peak magnetic energy}}{\text{energy lost per cycle}} \\
&= -Q_{\text{ind.}}
\end{aligned}
\tag{8}
$$

An inductor or a capacitor is said to be self resonant when the peak magnetic and electric energies are equal. Therefore, Q of an inductor or capacitor vanishes to zero at the self-resonant frequency. At frequencies above the self-resonant frequency, no net magnetic (electric) energy is available from an inductor (capacitor) to any external circuit. In contrast, for an LC tank, the Q is defined at the resonant frequency ω_0, and the energy stored term in the expression for Q given by (5) is the sum of the average magnetic and electric energy. Since at resonance the average magnetic and electric energies are equal we have,

$$
\begin{aligned}
Q_{\text{tank}} &= 2\pi \cdot \left.\frac{\text{average magnetic energy + average electric energy}}{\text{energy lost per cycle}}\right|_{\omega = \omega_0} \\
&= 2\pi \cdot \left.\frac{\text{peak magnetic energy}}{\text{energy lost per cycle}}\right|_{\omega = \omega_0} \\
&= 2\pi \cdot \left.\frac{\text{peak electric energy}}{\text{energy lost per cycle}}\right|_{\omega = \omega_0}
\end{aligned}
\tag{9}
$$

The last two equalities are due to the fact that from equations (1) and (2), the average magnetic or electric energies at resonance for a sinusoidal excitation is $\frac{1}{4}L|\mathbf{I_L}|^2 = \frac{1}{4}C|\mathbf{V_C}|^2$ which are half the peak magnetic and electric energies given by (3) and (4).

To clarify the above discussion, lets look at the parallel RLC circuit of figure 5 and determine its inductor Q and its tank Q. We calculate the quality of the inductor as follows,

$$
\begin{aligned}
Q_{\text{ind.}} &= 2\pi \cdot \frac{\text{peak magnetic energy - peak electric energy}}{\text{energy lost per cycle}} \\
&= 2\pi \cdot \frac{\dfrac{|\mathbf{V_p}|^2}{2\omega^2 L_p} - \dfrac{1}{2}C_p|\mathbf{V_p}|^2}{\dfrac{1}{2}\dfrac{|\mathbf{V_p}|^2}{R_s} \cdot T}
\end{aligned}
$$

$$= \frac{\frac{1}{\omega L_p} - \omega C_p}{\frac{1}{R_p}}$$

$$= \frac{R_p}{\omega L_p} \cdot \left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right] \tag{10}$$

where the resonant frequency $\omega_0 = \frac{1}{\sqrt{L_p C_p}}$. Here $\frac{R_p}{\omega L_p}$ accounts for the magnetic energy stored and the ohmic loss in the parallel resistance (see figure 4). The second term in (10) is the self-resonance factor describing the reduction in Q due to the increase in the peak electric energy with frequency and the vanishing of Q at the self-resonant frequency. Some intuitive understanding of what is actually happening can be obtained by looking at figure 2. In the parallel RLC case $\mathbf{V_L} = \mathbf{V_C} = \mathbf{V_p}$ which is depicted in the figure 2. Note that in each quarter cycle, when energy is being

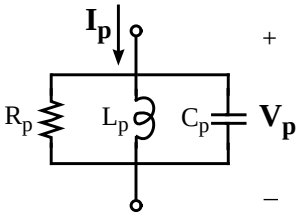


Figure 5 *- Parallel RLC circuit.*

stored in the inductor, it is being released from the capacitor and vice versa. As ω increases the magnitude of $\mathbf{I_L}$ decreases while the magnitude of $\mathbf{I_C}$ increase until they become equal at the resonant-frequency ω_0, so that an equal amount of energy is being transferred back and forth between the inductor and the capacitor. At this frequency $Q_{ind.}$ is zero (see equation (10)). As ω increases above ω_0 the magnitude of $\mathbf{I_L}$ becomes increasingly less than the magnitude of $\mathbf{I_C}$, and the net magnetic energy stored becomes increasingly more negative. That is, at frequencies above ω_0, no net magnetic energy is available from an inductor to any external circuit. The inductor is capacitive in nature, and $Q_{ind.}$ given by equation (10) is negative. Now using (9) to calculate the tank Q we have,

$$Q_{\text{tank}} = 2\pi \cdot \left.\frac{\text{peak electric energy}}{\text{energy lost per cycle}}\right|_{\omega = \omega_0}$$

$$= 2\pi \cdot \left. \frac{\frac{1}{2} C_p |\mathbf{V_p}|^2}{\frac{1}{2} \frac{|\mathbf{V_p}|^2}{R_s} \cdot T} \right|_{\omega = \frac{1}{\sqrt{L_p C_p}}}$$

$$= \frac{R_p}{\sqrt{L_p / C_p}} \tag{11}$$

Note that the tank Q is not zero unlike the inductor Q which is zero at resonance. Also, note that the same result can be derived using a more well-know relationship: The ratio of the resonant-frequency to the -3-dB bandwidth. For a series RLC circuit, the capacitor Q (the series RLC circuit is capacitive at low frequencies) and the tank Q can be determined using the same procedure as above. The final results are summarized in figure 6.

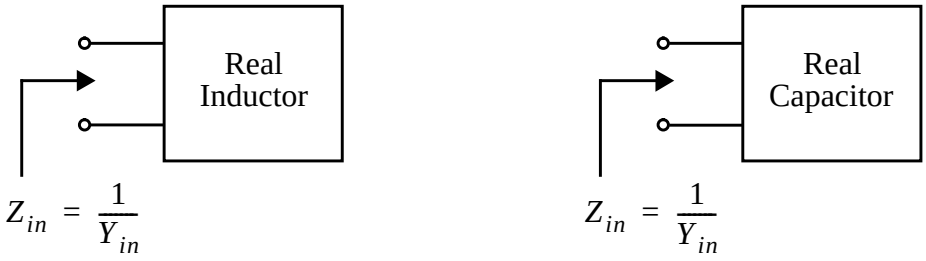
$$Q_{\text{ind.}} = \frac{\frac{1}{\omega L_p} - \omega C_p}{\frac{1}{R_p}} = \frac{R_p}{\omega L_p} \cdot \left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right] \qquad Q_{\text{cap.}} = \frac{\frac{1}{\omega C_s} - \omega L_s}{R_s} = \frac{1}{\omega C_s R_s} \cdot \left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right]$$

$$Q_{\text{tank}} = \frac{R_p}{\sqrt{L_p / C_p}}, \quad \omega_0 = \frac{1}{\sqrt{L_p C_p}} \qquad Q_{\text{tank}} = \frac{\sqrt{L_s / C_s}}{R_s}, \quad \omega_0 = \frac{1}{\sqrt{L_s C_s}}$$

Figure 6 *- Quality factors of RLC circuits.*

Both Q definitions discussed above are important, and their applications are determined by the intended function in a circuit. When evaluating the quality of on-chip inductors as a single element, the definition of inductor quality given by (7) is more appropriate and will be used in this paper. However, if the inductor is being used in a tank, the definition given by (9) is more appropriate. Finally, note that in figure 6 the inductor quality factor of a parallel RLC circuit is given by the negative of the ratio of the imaginary part to the real part of the input admittance. Similarly, note that the capacitor quality factor of a series RLC circuit is given by the negative of the ratio of

the imaginary part to the real part of the input impedance. Since, any circuit has an equivalent admittance and impedance, inductor and capacitor Q factors can be easily determined using the above facts. The above statements are summarized in figure 7. The method of figure 7 is appropriate for determining the Q of inductors or capacitors from simulation or measurement results.



$$Z_{in} = \frac{1}{Y_{in}} \qquad Z_{in} = \frac{1}{Y_{in}}$$

$$Q_{\text{ind.}} = \frac{Im\{Z_{in}\}}{Re\{Z_{in}\}} = -\frac{Im\{Y_{in}\}}{Re\{Y_{in}\}} \qquad Q_{\text{cap.}} = -\frac{Im\{Z_{in}\}}{Re\{Z_{in}\}} = \frac{Im\{Y_{in}\}}{Re\{Y_{in}\}}$$

Figure 7 *- Alternative method for determining the Q in real inductors or capacitors.*

III. On-Chip Inductor Modeling

A. Lumped Circuit Model of On-Chip Inductors

The goal of on-chip inductor modeling is to represent this device which is rich in electromagnetic phenomenon with an accurate lumped element model that can easily be understood for design purposes and can also be entered in a circuit simulator. Since the geometrical dimensions of these devices are small compared to the wavelength, it is possible to model them by a lumped-element circuit. The simplest model that has been proposed and has proven to accurately predict the behaviour of on-chip inductors is shown in figure 8 [4]-[6]. In this model, L represents the

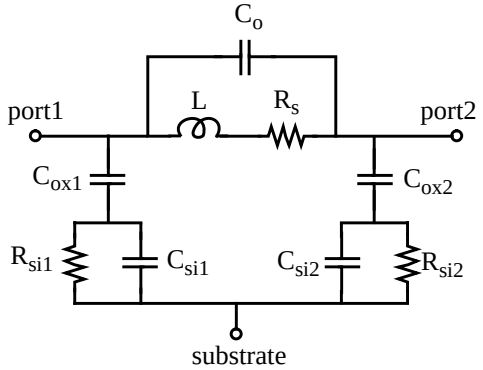


Figure 8 *- Lumped circuit model of an on-chip inductor.*

spiral inductance. Numerous closed form expressions have been developed to estimate the spiral inductance [7]-[9]. However, Greenhouse's method [10] is the one most widely used because of its accuracy and its ease of implementing in a computer program. R_s is the series resistance of the spiral and varies with frequency in a complicated manner. There are four factors that effect the resistance of a microstrip line in a silicon technology: 1)DC, 2)Edge effect, 3)Proximity effect, and 4)Skin effect [11]. A more accurate expression for R_s can be found in [12]. However, R_s can be estimated by[13],

$$R_s \approx \frac{\rho \cdot l}{W \cdot \delta \cdot (1 - e^{-t/\delta})} \tag{12}$$

where ρ is the resistivity of the metal spiral, l is the total length of the spiral, W is the width of the metal segments (see figure 1), t is the thickness of the metal, and δ is the skin depth given by,

$$\delta \approx \sqrt{\frac{\rho}{\pi \mu_0 f}} \tag{13}$$

where f is the frequency of operation. C_o is mainly due to the overlap between the spiral and the underpass (see figure 1) [14] and can be approximated by a simple parallel plate capacitance equation,

$$C_o \approx \frac{A_{ov} \varepsilon_{ox}}{d_{ov}} \tag{14}$$

where A_{ov} and d_{ov} are the overlap area and the distance between the spiral and the underpass respectively, and ε_{ox} is the permitivity of the oxide layer between the two metal layers. The effect of interturn fringing capacitance is usually small because the adjacent turns are almost equipotential and therefore neglected in the model. Even though the spiral of figure 1 is not symmetric, we can assume it is and approximate $C_{ox}=C_{ox1}=C_{ox2}$ which account for the capacitive coupling between the spiral and the lossy substrate to be given by

$$C_{ox} \approx \frac{A_{\text{ind.}} \varepsilon_{ox}}{2 d_{ox}} \tag{15}$$

Here $A_{ind.}$ is the area of the inductor, and d_{ox} is the distance between the spiral and the substrate. Fortunately, the error introduced by the symmetric assumption is negligible in most instances. Also, its is possible to implement a symmetric on-chip inductors which have been found to have a better Q under symmetric excitation [15]. In a similar manner we can assume that $R_{si1}=R_{si2}=R_{si}$

and $C_{si1}=C_{si2}=C_{si}$ in an asymmetric spiral. The value of these substrate parameters are approximately given by,

$$R_{si} \approx \frac{2}{W \cdot l \cdot G_{sub}} \tag{16}$$

$$C_{si} \approx \frac{W \cdot l \cdot C_{sub}}{2} \tag{17}$$

where G_{sub} and C_{sub} are fitting parameters that are constant for a given substrate and a given distance between the spiral and the substrate [8]. G_{sub} has a typical value of about 10^{-7} S/μm^2 and a typical range for C_{sub} is between 10^{-3} and 10^{-2} fF/μm^2.

It is also worth mentioning that other modeling techniques have been proposed. One example is shown in figure 9 [16]. The model presented above only takes into account the electric coupling between the spiral and the substrate through C_{ox}. However, the magnetic coupling between the spiral and the substrate which causes eddy currents to flow in the substrate is not

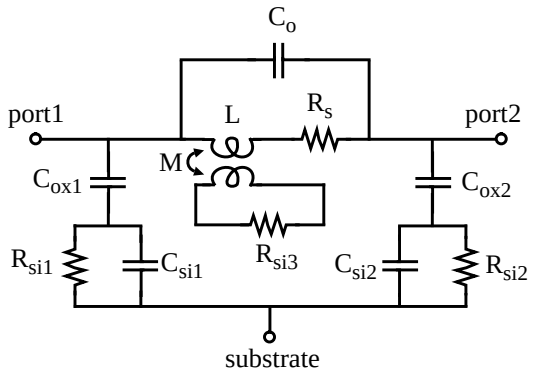


Figure 9 *- Lumped model including magnetic coupling between the spiral and the substrate.*

accounted for. These currents flow in a direction opposite to that of the spiral current and have the effect of decreasing the inductance and introducing extra loss which are accounted for in the model of figure 9. A similar effect occurs when a ground shield is used to decouple the spiral from the substrate in order to increase the isolation and Q of the inductor. More will be said on this is section IV. Another technique which takes into account the distributed nature of the on-chip inductor, models each segment of the spiral separately [2],[17]-[19]. The model of each segment is given is figure 10 which takes into account self and mutual inductances as well as capacitances between each section.

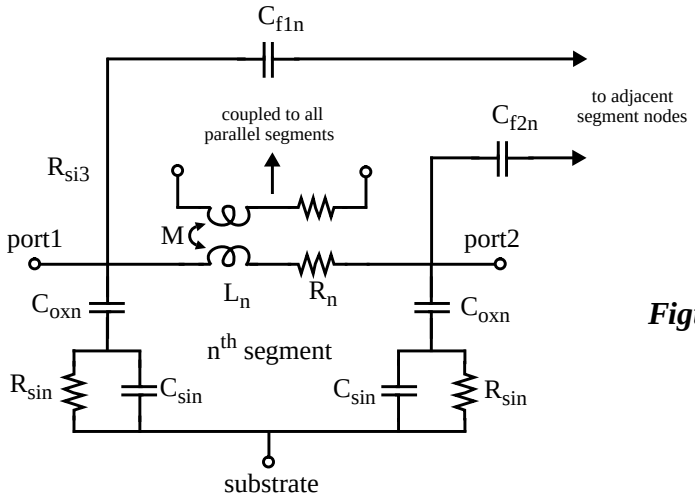


Figure 10 *- Lumped model for one segment of spiral inductor.*

B. Q of On-Chip Inductors

We will now determine the Q of on-chip inductors using the lumped model in figure 8. In order to determine Q, we use the one-port connection shown on the left side of figure 11, which is obtained by grounding the substrate and one port of the inductor. The use of a one port connection in our calculation unnecessary complexity in the analysis while preserving the inductor char-

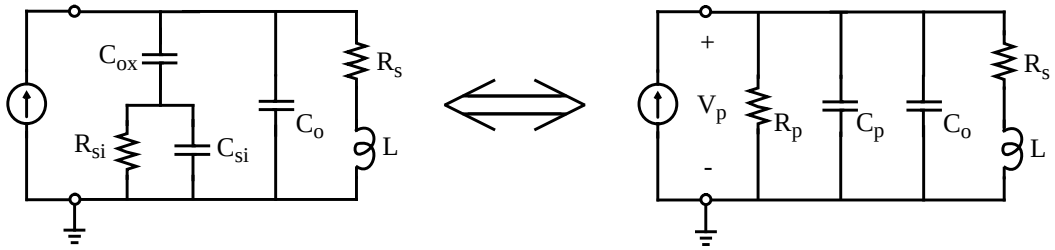


Figure 11 *- Lumped one-port on-chip inductor model and its equivalent circuit.*

acteristics. To facilitate our analysis, the effect of the oxide and the substrate given by Cox, Csi, and Rsi are replaced by an equivalent frequency dependent shunt resistance R_p and capacitance C_p (see right side of figure 11). R_p and C_p are given by the following expressions,

$$R_p = \frac{1}{\omega C_{ox}^2 R_{si}} + \frac{R_{si}(C_{ox} + C_{si})^2}{C_{ox}^2} \tag{18}$$

$$C_p = C_{ox} \cdot \frac{1 + \omega^2 R_{si}^2 C_{si}(C_{ox} + C_{si})}{1 + \omega^2 R_{si}^2 (C_{ox} + C_{si})^2} \tag{19}$$

From the equivalent circuit of figure 11, the peak energies and the energy lost per cycle can easily be calculated to give,

$$\text{Peak magnetic energy} = \frac{|\mathbf{V_p}|^2 L}{2[R_s^2 + (\omega L)^2]} \tag{20}$$

$$\text{Peak electric energy} = \frac{|\mathbf{V_p}|^2 (C_o + C_p)}{2} \tag{21}$$

$$\text{Energy loss per cycle} = \frac{2\pi}{\omega} \cdot \frac{|\mathbf{V_p}|^2}{2} \cdot \left[\frac{1}{R_p} + \frac{R_s}{R_s^2 + (\omega L)^2} \right] \tag{22}$$

Now by substituting (20)-(22) into (7) or by using the method of figure 7, after some tedious manipulation, we obtain the following expression for the Q of an on-chip inductor modeled by figure 11,

$$Q_{\text{on-chip}} = \frac{\omega L}{R_s} \cdot \frac{R_p}{R_p + R_s\left[1 + \left(\frac{\omega L}{R_s}\right)^2\right]} \cdot \left[1 - (C_o + C_p)\left(\frac{R_s^2}{L} + \omega^2 L\right)\right] \tag{23}$$

Here, $\omega L/R_s$ accounts for the magnetic energy stored and the series loss in the spiral (6). The second term in (23) is the substrate loss factor representing the energy dissipated in the semiconducting silicon substrate. The last term is the self-resonant factor representing the reduction in Q due to the increase in the peak electric energy with increasing frequency. The self-resonant frequency ω_0 can be solved by setting the self-resonant factor equal to zero which gives,

$$\omega_0 = \sqrt{\frac{1}{L(C_o + C_p)}\left[1 - \frac{R_s^2}{L}(C_o + C_p)\right]} \tag{24}$$

With the use of equation (23) and (24) and the knowledge of how geometric parameters of the spiral inductor effect the values of the components in the lumped circuit model of figure 8, described in the previous subsection, it is possible to do a rough on-chip inductor design and maximize Q for a given application. One can then confirm that the design meets the requirements using electromagnetic simulators such as Momentum or Sonet. Figure 12 shows a typical net inductance

curve $\frac{Im\{Z_{in}\}}{2\pi f}$ (dotted line) and a typical Q curve $\frac{Im\{Z_{in}\}}{Re\{Z_{in}\}}$ (solid line) for an on-chip inductor.

These curves were obtained for a 3.5-turn spiral in a 0.18-micron CMOS process using Momentum EM simulator. Q reaches a peak of about 6.5 before going back to zero at a resonant-frequency of about 17 GHz. Above this frequency, the inductor becomes capacitive and no net magnetic energy is available from the inductor. Note that the simulation was done to demonstrate the behaviour of an on-chip inductor and is not by any means an optimum design.

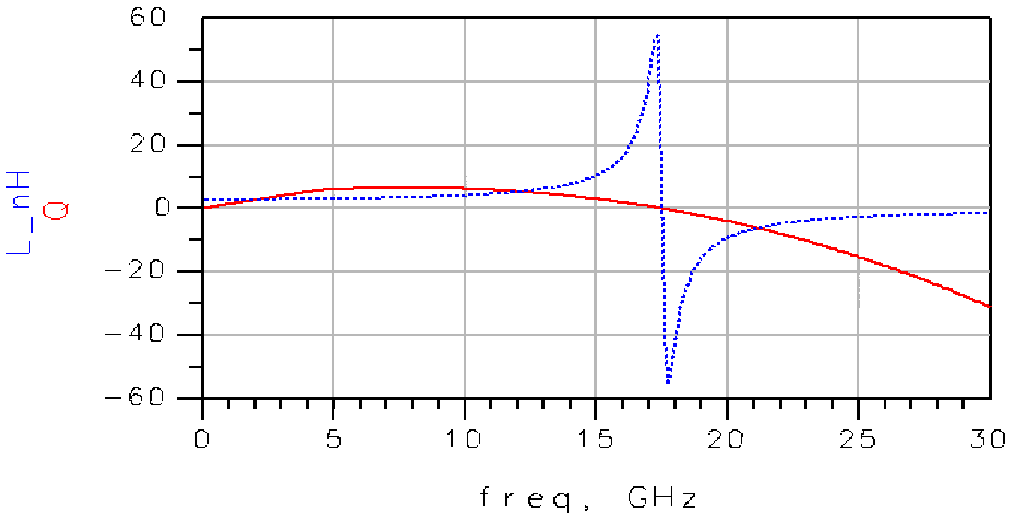


Figure 12 *- Net inductance (dotted line), and Q (solid line) for a 3.5-turn spiral in 0.18-micron CMOS.*

IV. Q Enhancement Techniques

With the metal layers provided by modern process technologies, metal strips can be stacked by using vias in order the decrease the spiral resistance R_s. This has the effect of increasing the peak Q (refer to (23)). Peak Q increases of 50% have been reported by shunting three metal layers [20]. However, this technique increases C_{ox} due to the decreased spacing between the spiral and the substrate leading to a decrease in the resonance frequency (refer to (24)).

The finite resistivity of the substrate in silicon technologies contribute greatly to the degradation of Q at high frequencies. Looking at the lumped element model of figure 11, it is seen that

as frequency increases, the energy dissipation in the substrate becomes more severe since the voltage drop across R_{si} increases. From (18) and (23), it can be shown that as R_{si} goes to zero or infinity, the substrate loss factor in the Q equation goes to unity. Therefore, by making the substrate a short or an open we can eliminate energy dissipation in the substrate and isolate the inductor. Using a high resistivity silicon [21] or etching away the silicon [22],[23] is equivalent to making the substrate an open. However, these methods are not compatible with standard silicon technologies and require extra processing steps that can hinder the mechanical integrity and reliability of the inductor. A better solution witch does not suffer from these disadvantages is the use of a ground shield between the spiral and the substrate in order to short the substrate to ground [6],[24],[25]. According to Lenz's law, image currents or eddy currents will be induce in a solid ground shield by the magnetic field of the spiral inductor. The induced current will flow in a direction opposite to that of the spiral current. This results in a negative mutual coupling between the currents, reducing the magnetic field and thus the overall inductance.

One can model this phenomenon using a transformer where the primary and secondary circuits represent the inductor and the ground shield respectively [6] (See left side of figure 13). The induced current flowing in the secondary will impose a counter electromotive force on the primary. This effect can be accounted for by adding a reflected impedance Z_r in series with the primary circuit [26] (See right side of figure (13). This impedance is given by,

$$Z_r = \frac{(\omega M)^2}{R_2^2 + (\omega L_2)^2}[R_2 - j\omega L_2] \tag{25}$$

Note that the imaginary part of Z_r is negative, signifying the reduction in the overall inductance. Also note the increase in overall resistance due to the real part of Z_r, denoting the additional energy loss due to the ground shield. It is seen from (25) that the negative effects of a solid ground shield diminishes as R_2 approaches infinity. This can be achieved by inserting features in the ground shield to oppose the flow of the image current. Specifically, slots orthogonal to the spiral are created in the solid ground shield, which are sufficiently narrow to prevent the vertical electric fields from leaking through the shield to the substrate. Such a shield is referred to as a patterned ground shield and is shown in figure 14. It has been found that the use of a pattered ground shield has very little effect of the inductance and increases the peak Q by about 33% [6].

However, it should be mentioned that the use of a patterned ground shield reduces the resonant-frequency of the inductor due to a faster roll-off of Q at frequencies above the peak-Q frequency. This can be seen from (24) and (19) mainly due to the increase in C_p, as well as C_{ox} since the ground shield is closer to the spiral than the substrate is.

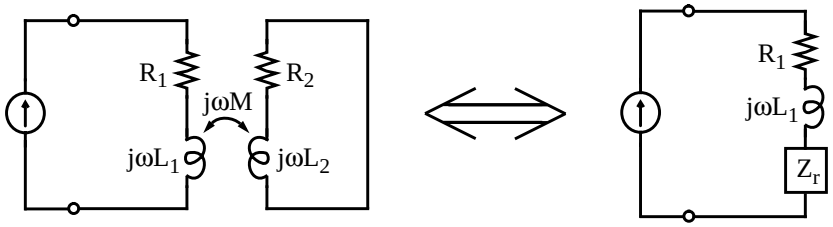


Figure 13 *- AC model for the effect of a solid ground shied on an inductor.*

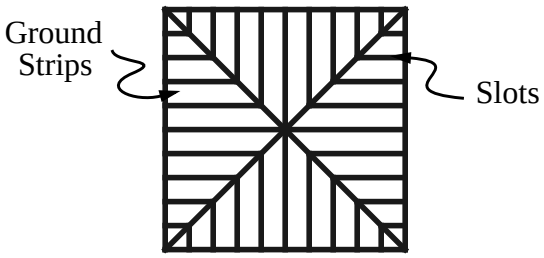


Figure 14 *- Patterned ground shield.*

Finally we end this section by suggesting some design guidelines for realizing close to optimum square on-chip inductors [2],[12],[27]. 1) The space between the outer spiral turn and any other surrounding metal structures must be at least 5W (refer to figure 1) to avoid any unwanted coupling. 2) Tight magnetic coupling, using the minimal allowable spacing for S, not only maximizes Q but also reduces total chip area. 3) A 10 to 15 μm strip width W is close to optimum for the Q-factor when frequency of operation is in the 1-3 GHz range. 4) Opposing sets of coupled lines must be separated by at least 5W to allow enough magnetic flux to pass through the hollow part of the spiral. 5) The oxide layer should be as thick as possible to reduce the substrate parasitic capacitance, thus increasing the inductor self-resonant frequency. In other words, use the highest metal layer to implement the spiral inductor. 6) The metal thickness and resistivity are fixed by the fabrication technology; however, multilevel metal processes allow for the parallel connection of metals or metal stacking to reduce the ohmic losses (increase Q) at the expense of decreasing the oxide thickness (lower resonant-frequency).

V. CONCLUSIONS

As stated earlier, the use of on-chip inductors is crucial in an effort to meet market demands for low cost, portable radio systems. From the point of view of radio frequency (RF) circuits, the lack of good inductors is by far the most conspicuous shortcoming of standard silicon IC processes. Although active circuits can sometimes synthesize the equivalent of an inductor, they always have higher noise, distortion, and power consumption than "real" inductors. Q of on-chip inductors implemented in standard silicon processes are in the neighborhood of 5. However, with good modeling and design techniques on-chip inductor Q's of 10 have been achieved [2]. It is likely that with improved modeling techniques accompanied by improvements in silicon processes (e.g. copper interconnects, increased number of metal layers) Q values exceeding 10 can easily be achieve in a standard silicon technology in the near future. Also, developments in silicon-compatible suspended structures may be used in the future to realize on-chip inductor Q's above 36 [28]. And last but certainly not the end of all the possibilities is the use of varying line widths in each turn to optimize Q [29].

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