

Oscillator Phase Noise and Jitter

Oscillators are an integral part of many systems today. In both RF and synchronous digital systems, accurate clock sources are required for correct operation. Oscillator uncertainty in these system has many affects, such as increasing the required channel separation in RF systems, and reducing timing margins in digital systems. This paper, tutorial in nature, covers the nature of oscillator phase noise and jitter, the sources of noise, and architectures and design approaches that result in low noise systems.

I. What is phase noise

Phase noise and timing jitter are both measures of uncertainty in the output of an oscillator. Phase noise defines the frequency domain uncertainty of an oscillator. If the output of an oscillator is given as $V(t) = V_o \cos[\omega_o t + \phi(t)]$, then $\phi(t)$ is defined as the phase noise. This expression of noise is useful for analog designers in situations such as RF design when the spectral content of $\phi(t)$ is of importance in determining the interference of out of band signals. In cases of small noise sources (a valid assumption in any usable system), a narrowband modulation approximation can be used to express the oscillator output as:

$$\begin{aligned} V(t) &= V_o \cos[\omega_o t + \phi(t)] \\ &= V_o [\cos(\omega_o t) \cos[\phi(t)] - \sin(\omega_o t) \sin[\phi(t)]] \\ &= V_o [\cos(\omega_o t) - \sin(\omega_o t) \phi(t)] \end{aligned} \tag{1}$$

This shows that phase noise will be mixed with the carrier to produce sidebands around the carrier, giving a direct connection between phase noise and the spectral output of the oscillator.

The noise spectral power density of an oscillator is defined units of decibels below the carrier per Hertz (dBc/Hz) and is defined as $L_{total}\{\Delta\omega\} = 10 \log_{10} \left[\frac{P_{sideband}(\omega_o + \Delta\omega, 1Hz)}{P_{carrier}} \right] = 10 \log_{10} [S_\phi(f)]$.

Timing jitter is a measure of oscillator uncertainty in the time domain. Timing jitter is a more

useful parameter for digital designers who must, for example, determine if a synchronous system meets flip-flop setup and hold times when timing jitter is taken into account. Timing jitter is specified as a statistical parameter, σ_t , the standard deviation of the absolute timing error. This parameter measures the time difference between a point in $V(t) = V_o \cos[\omega_o t]$ and the equivalent point in $V(t) = V_o \cos[\omega_o t + \phi(t)]$. In oscillators in an open loop system, σ_t grows without bound, as the timing variance of each cycle adds to that of the previous cycle. In an oscillator in a closed loop system, such as a VCO in a PLL, σ_t (hopefully) becomes a finite quantity due to the feedback from the phase detector. Other useful jitter expressions are the cycle jitter σ_C , defined as the variance of the difference between the period of a cycle and its average, and cycle to cycle jitter σ_{CTC} , defined as the variance of the difference in period between two consecutive clock cycles.

II. Noise sources

There are two main categories of oscillator noise sources, thermal/shot noise, and supply/substrate noise. Although typically dominated by the supply and substrate noise, thermal noise can be explicitly determined for an oscillator during design and sets a lower limit on what is achievable in the design, while supply/substrate noise is environment dependent.

Although other types of oscillators, such as LC and relaxation, are commonly used, this work will focus on ring oscillators due to the ease of integration that has made them so prevalent.

Thermal Noise

Classical Approach

Thermal noise in oscillators has been traditionally modeled using an linear time invariant approach [3]. While this approach has been shown to be flawed [2], oscillators are not time

invariant systems, it is still instructive to understand this view.

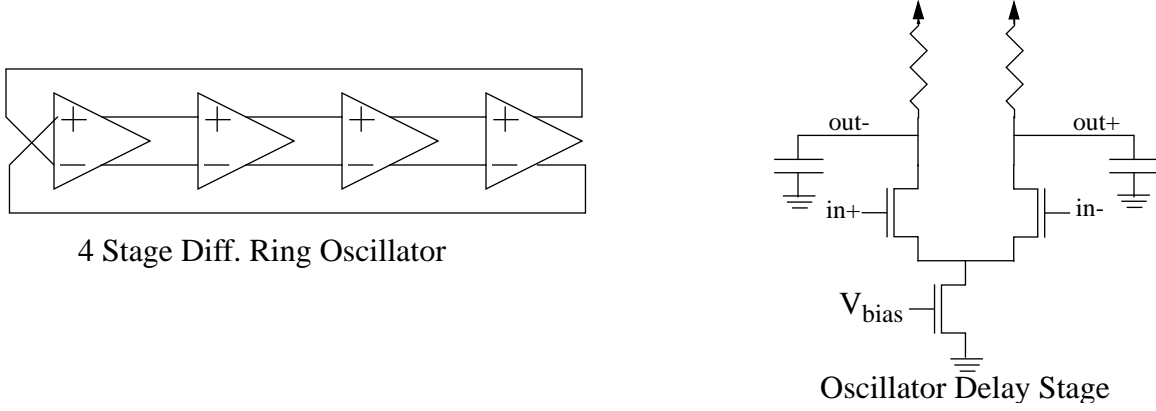


Figure 1. Ring Oscillator System and Delay Stage

The link between thermal noise and phase jitter can be illustrated by observing a stage in a differential ring oscillator of Figure 1 [1]. If jitter is measured at the zero crossings, then a noise source superimposed on the input signal as in Figure 2 will cause a change in the timing equal to the noise voltage multiplied by the slope of the waveform at that point, or $\Delta T = \frac{dV}{dt} \Delta V$. If we make the simplification that the single stage shown in Figure 1 switches instantaneously, we can model the output transition as $V_{out}(t) = R_L I_{DD} (1 - 2e^{-t/\tau})$, where $\tau = R_L C_L$. The delay of this inverter stage can be shown to be $t_{inv} = R_L C_L \ln 2$. The slope at the zero-crossing point is $\left. \frac{dV_{out}}{dt} \right|_{V=0} = \frac{I_{DD}}{C_L}$. The

timing jitter component can now be given as $\overline{\Delta t_{inv}^2} = \frac{\Delta V}{dV/dt} = \overline{V_{noise}^2} \frac{C_L^2}{I_{DD}^2}$. A more useful expression is

the jitter relative to the stage delay, which is $\frac{\overline{\Delta t_{inv}^2}}{t_{inv}^2} = \overline{V_{noise}^2} \frac{C_L^2}{I_{DD}^2} \frac{1}{(R_L C_L \ln 2)^2}$.

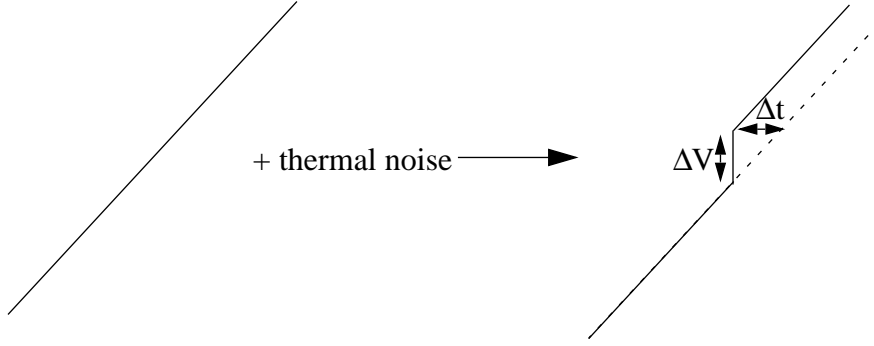


Figure 2. Voltage Noise to Phase Noise Conversion in Oscillator Waveform

The thermal noise imposed on the delay stage in Figure 1 derives from two sources, the load resistor and the MOS input transistor. The noise due to the load resistor is $V_{n-R}^2(f) = 4kTR_L$, and the noise due to the MOS (long channel) transistor is

$V_{n-Q}^2(f) = I_{n-Q}^2(f)R_L^2 = \left(\frac{2}{3}4kTg_m\right)R_L^2 = \frac{2}{3}4kTR_LA_v$, where A_v is the inverter gain g_mR_L . By multiplying

the spectral power density of the noise by the noise bandwidth, $BW = \frac{1}{4R_LC_L}$, we find the mean-

squared noise $\overline{V_{noise}^2} = \frac{2kT}{C_L}\left(1 + \frac{2}{3}A_v\right)$. This allows us to express the relative jitter as

$$\frac{\overline{\Delta t_{inv}^2}}{t_{inv}^2} = \frac{2kT}{C_L}\left(1 + \frac{2}{3}A_v\right)\frac{C_L^2}{I_{DD}^2(R_LC_L\ln 2)^2} = \frac{2}{\ln 2}\frac{kT}{t_{inv}I_{DD}V_L}\left(1 + \frac{2}{3}A_v\right), \text{ where } V_L = I_{DD}R_L. \text{ This is only one stage}$$

in the oscillator, to get the relative jitter for the entire oscillator we have:

$$\frac{\overline{\Delta T_{osc}^2}}{T_{osc}^2} = \frac{2N}{(2N)^2}\frac{\overline{\Delta t_{inv}^2}}{t_{inv}^2} = \frac{2}{\ln 2}kT\frac{f_{osc}}{I_{DD}V_L}\left(1 + \frac{2}{3}A_v\right) \quad (2)$$

Note that the only designer adjustable parameters are the power per stage, $I_{DD}V_L$, and the stage gain, A_v . The gain variable should be minimized to reduce noise, but should be at least 2 to ensure continued oscillation.

The phase noise can be related to the relative jitter [4] for white noise sources by:

$$S_{\phi}(\Delta f) = \frac{f_{osc} \Delta T_{osc}^2}{\Delta f^2 T_{osc}^2} = \frac{2}{\ln 2} \frac{kT}{I_{DD} V_L} \left(1 + \frac{2}{3} A_V\right) \frac{f_{osc}^2}{\Delta f^2} \quad (3)$$

In practice, measurements show a region with a $1/\Delta f_{osc}^2$ dependence similar to (3), but always larger in magnitude. In addition, a region with $1/\Delta f_{osc}^3$ dependence at small frequency offsets is also found. The traditional approach to modeling was to use fudge factors to make the model fit reality, but these had to be determined from circuit measurements, and could not be predicted beforehand.

Time Variant Approach

The linear time invariant approach just presented, while giving some insight into noise sources, is incorrect due to the assumption of the system being time invariant. A simple example demonstrates the time variant nature of an oscillator.

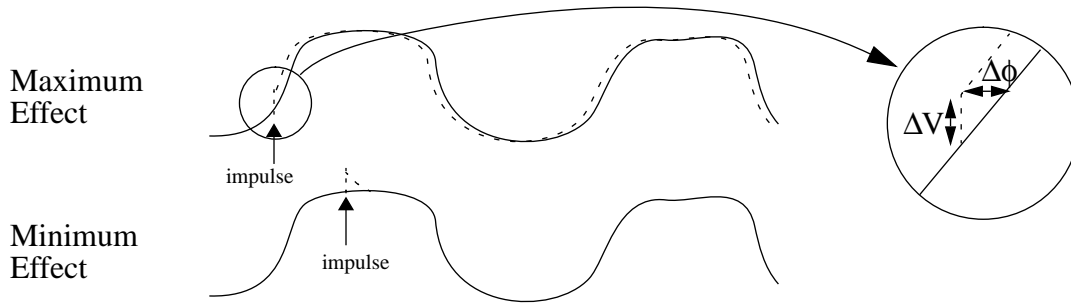


Figure 3. Waveform Impulse Sensitivity

It can be seen from Figure 3 that the system is clearly time variant. Noise applied near the zero crossing has maximum effect on the phase error, while noise applied at the extremes of the cycle have minimum effect due to amplitude limiting in the inverter stage. The time dependent noise sensitivity of the system can be described by the function $\Gamma(\omega_0\tau)$, called the impulse sensitivity function, or ISF, a unitless and periodic function that describes how much phase shift results from applying a unit impulse at any point in time, such that $\Delta\phi = \Gamma(\omega_0\tau) \frac{\Delta q}{q_{max}}$ where $q_{max} = C_{node} V_{swing}$.

This function will resemble the derivative of the output waveform, but will differ due to effects

such as voltage dependent diffusion capacitors on the output node and cyclostationary modulation of the MOS noise sources. In order to determine the ISF of a design, hspice simulation should be performed, applying impulses at various phases of the period, and recording the resulting offset. Because the effect of any noise introduced persists indefinitely, we can describe the impulse response of the system to a unit impulse of charge as $h_\phi(t, \tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau)$, where $u(t)$ is the unit step. The total excess phase due to a noise current $i(t)$ can therefore be described by the expression

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t, \tau)i(\tau)d\tau = \int_{-\infty}^t \frac{\Gamma(\omega_0\tau)}{q_{max}}i(\tau)d\tau \quad (4)$$

Because the ISF is periodic, it can be expressed as the fourier series

$$\Gamma(\omega_0\tau) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \phi_n), \text{ where } \phi_n \text{ is the phase of the } n^{\text{th}} \text{ harmonic, and can be ignored for}$$

random input noise sources. This series expansion allows us to rewrite (4) as

$$\phi(t) = \frac{1}{q_{max}} \left[c_0 \int_{-\infty}^t i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega_0\tau) d\tau \right] \quad (5)$$

This expression is the key to understanding the effects of noise, thermal and otherwise, in an oscillator. A useful interpretation of (5) is to view the phase as the summation of a series of copies of $i(t)$ modulated around harmonics of the carrier. The low pass property of the integration causes only noise close to the harmonics of the carrier to translated in frequency to become close-in noise sidebands to the carrier. The ISF coefficient c_0 represents the DC content of the ISF and can be minimized by design, primarily by ensuring symmetry of the oscillator waveform. This has some important design implications in minimizing the impact of the $1/f$ MOS device noise. The $1/f$ noise from MOS devices has a significant impact on the close-in phase noise that can be quite problematic for RF designers trying to maintain channel separation.

To demonstrate the effect of a interfering signal $i(t) = I_n \cos[(n\omega_0 + \Delta\omega)t]$ on the oscillator, we

evaluate (5) which results in $\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega t)}{2q_{max}\Delta\omega}$ which will result in two equal sidebands at $\pm\Delta\omega$ around the oscillator frequency in $S_\phi(\omega)$. This frequency modulation of noise sources could not be explained in previous models, and was attributed to unspecified non-linearities that were never quantified.

We can now find the phase noise due to a random white noise process with power spectral density $i_n^2/\Delta\omega$. The spectral power density of the phase noise becomes:

$$S_\phi(\omega) = \frac{i_n^2/\Delta\omega}{4q_{max}^2\Delta\omega^2} \sum_{n=0}^{\infty} c_n = \Gamma_{rms}^2 \frac{i_n^2/\Delta\omega}{2q_{max}^2\Delta\omega^2} \quad (6)$$

A flicker, or 1/f, noise source $i_n^2 \frac{\omega_{1/f}}{\Delta\omega}$ will similarly become $S_\phi(\omega) = c_0 \frac{i_n^2/\Delta\omega}{4q_{max}^2\Delta\omega^2} \frac{\omega_{1/f}}{\Delta\omega}$. This is the sources of the $\frac{1}{f^3}$ noise observed, but not predicted by the time invariant models.

An analysis in [2] shows that using a number of simplifying assumptions in ring oscillators, we can express $\Gamma_{rms} = \sqrt{\frac{2\pi^2}{3\eta^3} \frac{1}{N^{1.5}}}$ where $t_d = \frac{\eta}{dV/dt|_{max}}$.

The spectral power density of the phase noise due to a random white noise process can be evaluated for the differential ring oscillator in Figure 1. For the differential ring oscillator, we first note that $P = NI_{tail}V_{DD}$ and $f_{osc} = \frac{1}{2Nt_d} \approx \frac{I_{tail}}{2\eta Nq_{max}}$. The thermal noise due to the MOSFET and load resistor is $\frac{i_n^2}{\Delta f} = \frac{4kT}{R_L} \left(1 + \frac{2}{3}A_v\right)$. Inserting into (6), multiplying by $2N$ noise sources and rearranging gives:

$$S_\phi(\omega) = \frac{8}{3\eta} N \frac{kT}{P} \left(1 + \frac{2}{3}A_v\right) \frac{V_{DD}}{V_{swing}} \frac{\omega_{osc}^2}{\Delta\omega^2} \quad (7)$$

which has the same form as the spectral power density of the linear time invariant analysis (3),

but offset by some fixed gain.

The single ended ring oscillator can be analyzed in a similar manner, noting that

$$P = 2NV_{DD}q_{max}f_{osc}, \quad f_{osc} = \frac{1}{2Nt_D} = \frac{I_{tail}}{4\eta Nq_{max}} \quad \text{and} \quad \frac{i_n^2}{\Delta f} = \frac{2}{3}4kT(g_{m-n} + g_{m-p}).$$

Substituting into (6), multiplying by N noise sources and again rearranging gives:

$$S_\phi(\omega) = \frac{16kT}{9\eta} \frac{V_{DD}}{P} \frac{\omega_{osc}^2}{V_{eff} \Delta \omega^2} \quad (8)$$

It is worth noting that the phase noise for the differential ring oscillator is a function of N, the number of stages, while the single ended ring oscillator is not.

The time variant analysis of oscillator noise matches closely the observed noise in physical oscillators. This new model explains the upconversion of 1/f noise, which the time invariant model couldn't, and provides a way to analyze designs prior to fabrication to determine their noise properties. If we assume an ISF with $c_1 = 1$ and $c_{n \neq 1} = 0$, this approach simplifies to the time-invariant analysis.

Supply and Substrate Noise

Differential ring oscillators are inherently far more insensitive to supply and substrate noise than single-ended ring oscillators. While both types of oscillators will see most of the supply noise coupled directly onto their outputs, in the differential case, much of the coupled noise will be common mode, and will not effect the next stage.

The same analysis using the ISF can be applied to supply and substrate noise. While thermal noise is generally only analyzed for the delay stage input nodes, supply and substrate noise also requires the analysis of the tail current node in common source, differential pair stages. ISF functions need to be generated for all the sensitive nodes in the circuit. The primary difference between analyzing the two types of noise is that supply and substrate noise in all the ring

oscillator delay stages is correlated, while thermal noise is not. Because the ring oscillator delay stages and their ISFs are staggered evenly in phase by $2\pi/N$, where N is the number of delay stages, all the ISF coefficients c_n that aren't integer multiples of N times the carrier frequency cancel out when the ISFs of all the stages are summed together. In addition, the ISF of the tail current node of the differential ring oscillator has only even coefficients since the tail current ISF is periodic with twice the frequency of the carrier (it doesn't know its left from its right signal swing).

It is also instructive to examine how supply and substrate noise is coupled into an oscillator stage [6]. This coupling primarily takes place through the voltage dependent diffusion capacitors in the differential delay stage. A change in supply voltage will alter the capacitance on the output nodes and hence change the frequency.

III. Non-Linearities

Although not a true source of phase noise, non-linearities creates spectral content other than the oscillator frequency, and is of interest to RF designers. Due to device non-linearities, and stage saturation, we can express the output waveform in terms of its (partial) Taylor series expansion $V_{out} = \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3$. In a fully differential system, the even terms cancel out.

In a 3 stage ring oscillator, the stages operate in their linear region for most of the cycle. As the number of stages increases however, the stages have time to saturate and introduce non-linearities into the waveform. Another way of viewing this is that fewer stages give sinusoidal-like output, while using more stages results in a more digital-like, square wave.

IV. Low Noise Architectures

The goal in analyzing oscillator noise processes is to be able to gain some insight into designing oscillators that exhibit low noise. We will now look at a few techniques to minimize the various noise sources.

There are a number of approaches that can be used to minimize the effects of thermal noise. Both the time variant and invariant analysis show that the two main parameters influencing thermal noise are power per stage, and stage gain for the differential ring oscillator. The stage gain, as mentioned in a previous section, should be approximately 2. The power must be sufficient such that the thermal noise due to (7) does not exceed the system specification. If the design does not operate in a noisy environment, the single ended ring oscillator is preferred, as it is inherently quieter than the differential version by a factor f approximately $N\left(1 + \frac{2}{3}A_v\right)$.

The thermal $1/f$ noise is primarily of interest to RF designers and can be minimized by designing for zero DC content in the ISF. The use of symmetric loads [5] and equal rise and fall times are a good first cut, but simulation is required to explicitly determine the ISF, and then adjust circuit parameters to eliminate the DC content. In [2] it is shown that, surprisingly, for a single-ended CMOS inverter type oscillator, the PMOS to NMOS width ratio that minimizes c_0 is 1.25, not the 2.5-3 used in conventional designs.

Supply and substrate noise benefit from being correlated noise sources due to the cancellation of ISF coefficients c_n where n is not an integer multiple of N , the number of stages. In order to maximize this benefit, the design should attempt to maximize the noise correlation by expending effort on making sure the layout is regular, interleaved, equally loaded etc. By increasing the number of stages we also cancel out more terms of the ISF, but layout matching issues will soon cancel any benefit. An interesting fact to note is that only ISF coefficients of N times the carrier

survive, and the tail current node has only even coefficients. Hence, while a four stage ring oscillator will be sensitive to tail current node ISF terms $c_0, c_4, c_8 \dots$, a five stage will only be sensitive to $c_0, c_{10}, c_{20} \dots$. It appears beneficial therefor, to use an oscillator with an odd number of stages if the design allows it.

Similar to thermal noise, correlated noise sources also benefit from minimizing the DC content in their ISF. The ISF functions differ though, and the goal of minimizing c_0 for supply and substrate noise may conflict with the goal of minimizing c_0 for thermal/shot noise. The designer will have to evaluate the environment the oscillator is to be used in to determine which noise source is dominant and should be minimized.

It was indicated in the previous section that supply noise tends to couple into differential delay stages through the voltage dependent diffusion capacitors. This implies that it is beneficial to make the capacitance of the output nodes as supply voltage independent as possible. This can be achieved through the addition of poly-poly capacitors to the output nodes. This would entail minimizing the number of delay stages in order to create a high frequency ring oscillator that can then be slowed to the desired speed with the additional capacitors. Also, by minimizing the width of the input differential pair transistors, the diffusion capacitance is minimized, and can be replaced with poly capacitors. Happily, this technique coincides with the goal of minimizing the stage gain to reduce thermal noise. This technique is limited though, as the stage gain must be at least 2 for the oscillator to function. Channel length can be reduced in addition to width, but short channel effects will increase the thermal noise. If supply noise dominates, this may be acceptable.

In addition to decreasing the oscillator sensitivity to power supply noise, some designs employ a local voltage regulator to provide a clean supply just for the oscillator.

It was shown in the previous section that single ended ring oscillators produce lower phase

noise due to thermal jitter for the same power as their differential counterparts. Differential ring oscillators are often preferred, however, due to their lower sensitivity to supply and substrate noise. Figure 4 shows a ring oscillator structure that consists of two single-ended ring oscillators coupled together by weak inverters that keep the two structures 180 degrees out of phase. This structure somewhat reduces the sensitivity to supply and substrate noise, while enjoying some of the benefits of differential oscillators, and may be preferable in less noisy environments.

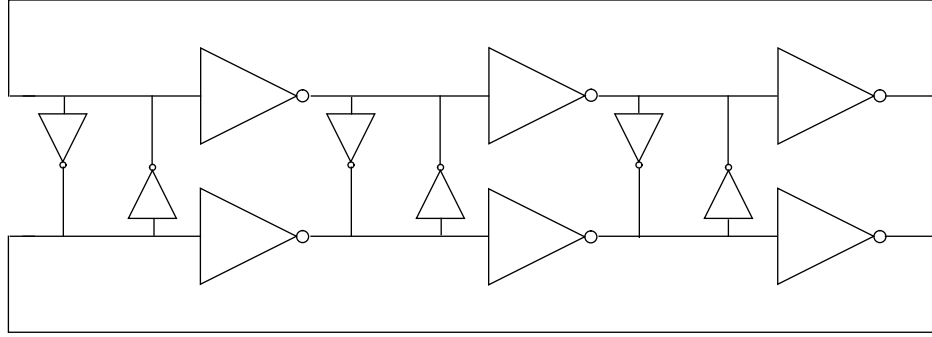


Figure 4. Coupled Single-ended Ring Oscillator

V. VCOs inside PLLs

PLLs are an important building block in many systems. There are a number of potential noise sources within a PLL, but the VCO noise is typically the dominant source. Other sources of noise in a PLL system consist of dead zones in the phase detector, pulses in the charge pump, and noise in buffers that distribute the signal. When VCOs are embedded inside a PLL, the loop dynamics will modify the noise characteristic. Phase noise below the PLLs loop bandwidth will be significantly attenuated. It is desirable to have the loop bandwidth as large as possible to attenuate noise, but for stability reasons, the loop bandwidth shouldn't exceed 1/10 of the VCO frequency.

To determine the timing jitter at the output of the PLL the timing variance over the settling period,

given in oscillator periods, n , typically 10-100, is summed to give $\frac{\overline{\Delta T_{pll}^2}}{T_{pll}^2} = n \frac{\overline{\Delta T_{osc}^2}}{T_{osc}^2}$. To find the

timing variance from the phase noise spectral power density derived in this paper, we repeat (3)

for convenience, $S_{\phi}(\Delta f) = \frac{f_{osc} \Delta T_{osc}^2}{\Delta f^2 T_{osc}^2}$.

VI. Conclusions

Oscillator noise can be well predicted and minimized during design. Thermal noise can be minimized with increased power and shot noise can be minimized through careful design that eliminates c_0 . Supply and substrate noise can be minimized through careful layout that ensures maximum correlation between noise sources for each delay stage.

References

- [1] Ken Martin, "Phase-Locked Loops", class notes 2000
- [2] Ali Hajimiri and Thomas Lee, "The design of Low Noise Oscillators", Kluwer 1999
- [3] Behzad Razavi, "A Study of Phase Noise in CMOS Oscillators", IEEE JSSC Vol. 31, No. 3, March 1996
- [4] Weignandt, Kim and Gray, "Analysis of Timing Jitter in CMOS Ring Oscillators", ISCAS, 1994
- [5] J.G. Maneatis et al., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques" IEEE JSSC, Vol. 31, No 11, Nov 1996, pp. 1723-1732
- [6] Frank Herzel and Behzad Razavi, "A Study of Oscillator Jitter Due to Supply and Substrate Noise", IEEE TCAS II, Vol. 46, No. 1, Jan. 1999, pp. 56-62