Department of Electrical and Computer Engineering
University of Toronto

Final Term Report : A Study of Low-Voltage, CMOS Op Amps

Prepared by:	Tony Pialis Student# 951 087 060
Class Instructor	Prof. Khoman Phang
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1 Abstract

Currently, there is an ever-growing demand for low-power mixed signal integrated circuits for such applications as mobile or wired communications and other portable systems. In these applications, the supply voltage is being scaled down to reduce overall power consumption. As for the fabrication process, digital CMOS is always the preferred technology due to its efficient economic costs. As a result, contemporary analog circuits must not only operate with low supply voltages, but should also be realizable in typical digital CMOS processes. However, this concession leads to significant performance degradation of the analog circuits. Since op amps are the most critical building blocks in all analog systems, the objective of this report is to study the theory and design of low voltage op amps for digital CMOS processes.

Two categories of low voltage op amps have been identified as being suitable for low voltage applications [1]. The first category operates with 2-3V power supplies. The distinct features of this class of op amps are that they utilize N-P complementary, input pairs and the gain stages use active gain enhancement to boost the gain of the overall op amp. However, N-P input complementary pairs typically suffer from reduced Common-Mode Rejection Ratios (CMRR), so several auxiliary circuit techniques will be introduced that attempt to improve the performance of the wide-swing input stage [2]. Furthermore, the active gain enhancement technique is found to cause instability problems, so a procedure developed in [1] and [11] for stabilizing these amplifiers will also be demonstrated.

The second class of op amps can operate below 1.5V power supplies and must depend on multistage cascading for high gain. As a result of the multiple, cascaded structure, some special compensation techniques must be incorporated into the design to ensure the overall stability of the cascaded system. This paper will introduce three similar compensation methods used to ensure the stability of cascaded, low-voltage op amps: Nested Miller Capacitor Compensation (NMCC), Multi-Path Nested Miller Compensation (MNMC) and Nested Gm-Capacitor Compensation (NGCC). Furthermore, it will be shown that the NGCC technique has several design advantages over both MNMC and NMCC, in terms of enhanced performance and simplicity of design, as discussed in [3].

In summary, this report will briefly outline some of the significant contributions that have been made over the last decade to improve the performance of operational amplifiers operating at supply voltages below 3.3V.

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2 Introduction

The present packing densities for CMOS technologies allow for complete systems to be integrated on a single chip. A wide range of applications require the integration of analog and digital subsystems, which poses several significant challenges to the design of analog circuits in a typical digital CMOS environment. The fast-paced trend to lower the supply voltage, which is mainly driven by the power consumption of the digital circuits, places further challenges on the analog designer. The main reason for the difficulty in designing CMOS analog circuits is the fact that the threshold voltage is not scaling down proportional to the supply voltage.

One of the most crucial building blocks in analog systems is the operational amplifier. Significant research has been devoted over the past 20 years for the development and enhancement of the op amp structure. Yet most historical topologies fell short of providing satisfactory performance below 3V power supplies. Historical structures typically consisted of an input stage and one or two intermediate gain stages. These gain stages had to provide high DC gain which could be achieved by using cascoding (vertical gain enhancement). Such topologies have little headroom in sub-1.5V supply environments, and are therefore unsuitable for that regime of supply voltage. This can be seen by comparing the driving capability of the cascoded structure, shown in Figure 2.1(a), with the simple gain stage, shown in Figure 2.1(b). For this analysis, it is assumed that the output transistors M_c and M_s in both circuits carry the same current I_L and that V_T=0.8V with an overdrive voltage V_{gs}-V_T is equal to 0.2V. Since the voltage swing of the cascode gain stage is smaller than the simple gain stage, the size of M_c is expected to be larger than M_s, and this size difference will increase as the supply voltage is further scaled down. Figure 2.2 shows the normalized size of M_c and M_s (normalized to the size of M_s at 3V) as a function of the supply voltage, V_{supply}[1]. The cascode stage will result in unreasonable increase in size for M_c for supply voltage below 1.6V. Therefore, this implies that cascoding is not the proper topology for sub-1.5V applications.

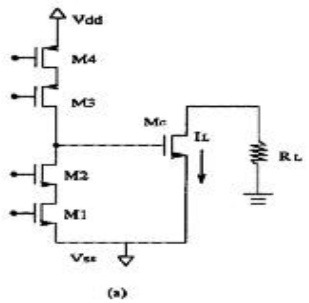

Figure 2.1(a): A Cascode Gain stage Plus Output Stage

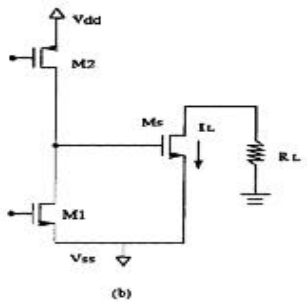

Figure 2.1(b): A Simple Gain Stage Plus Output Stage

Rather, a new topology which is more suitable for sub-1.5V applications should use horizontal gain enhancement rather than vertical enhancement. By cascading several simple (non-cascoded) low gain stages, high DC gain can be achieved. Such simple amplifier stages provide small DC gain (~20dB), but can easily operate at a sub-1.5V supply and 0.15um process. The main challenge in designing such a multistage amplifier, is in ensuring the overall stability of the op amp. As a result, special compensation techniques have been developed to achieve stability for op amps implemented with cascaded gain stages.

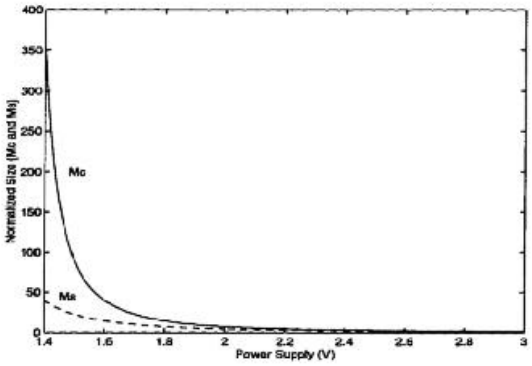

Figure 2.2: Normalized Transistor Size As a Function of Power Supply

2.1 Objectives

The objective of this paper is to introduce the most promising low voltage op amp design techniques that have been published to date. There are two main challenges in the design of low voltage op amps that all circuit topologies must confront: the first is to develop a stable multistage amplifier topology to achieve high DC gain. The second is to develop the basic building blocks to facilitate the realization of the proposed topologies.

Two main classes of op amps can be identified: one operating around 2-3V, and the other operating at sub-1.5V. The two classes are distinct in their structures and will be introduced separately.

The first class of op amps, which operate at 2-3V typically, use N-P complementary input pair to achieve rail-to-rail swings. This class of op amps will typically use active gain enhancement to achieve high DC gain. For this topology, tremendous research has been performed to further enhance the performance of the op amp. However, there are severe common-mode gm variation and CMRR degradation problems associated with the input stage using N-P complementary pairs. Several techniques have been published that address this problem [2]; as a result, some of the most popular and effective rail-to-rail, input stage topologies will be briefly introduced in this report. Another problem exists with the 2-3V class of op amps that degrades their stability due to the use of active gain enhancement. A common design procedure that compensates for this stability will be outlined in this report, accordingly.

The sub-1.5V class of op amps rely on horizontal cascading to achieve high-gain. In this report, three compensation methods for this cascaded topology will be demonstrated. The Nested Gm-Capacitor Compensation (NGCC) technique will be shown to have a larger gain bandwidth that the more traditional Nested Miller Capacitor

Compensation (NMCC) and the Multi-Path Nested Miller Compensation (MNMC) techniques.

Subsequently, this paper has been divided into the following sections:

- Section 3: describes the theory, and circuit level implementation of the 2-3V class of op amps. The fundamental transistor-level topology for an op amp with rail-to-rail complementary N-P input pair will be introduced. Auxiliary circuits for the rail-to-rail opamp, such as a constant-gm biasing circuit for the complementary input pair, and active gain enhancement techniques will also be reviewed.
- Section 4: outlines the work related to the second category of op amps that operate with sub-1.5V power supplies. The NMCC, MNMC and the NGCC compensation topologies will be introduced. Also, systematic design procedures will be demonstrated that allows for a simple design procedure for each of the three topologies.
- Section 5: concludes the report with a summary of both categories of low voltage op amps and outlines the advantages and limitations associated with each class of op amp.

3 2-3V Class of Op Amp With Rail-to-Rail Input Stage and Active Gain Enhancement

This chapter will focus on the basic design aspects of the two fundamental components for a low-voltage op-amp: a rail-to-rail, constant-gm, complementary input stage and an active gain-enhanced output stage. The discussion will begin with a rail-to-rail, constant-gm, input stage.

3.1 Introduction to Rail-to-Rail, Complementary Input Stages

For the usual differential pair used as an input stage of an opamp with a 1V V_T and a 3V power supply, the input common mode range is less than 2V. This is a significant limitation, especially if the op amp is intended for use as a general purpose one, e.g. used as a unity-gain buffer. As a result, there has been much research focused on the area of op-amps with linear regions of operation that extend from rail-to-rail, for low-voltage applications. In these op amps, an n-channel differential pair and a p-channel differential pair are connected in parallel as shown in Figure 3.1. This technique allows the input stage to operate rail-to-rail. For this input stage, there are basically three operation regions; when the common mode voltage, V_{CM}, is near the negative power supply V_{SS}, only the p-channel input pair are operational. In contrast, for V_{CM} near the positive power supply, V_{DD}, only the n-channel input pair operational. For V_{CM} around mid-rail, both differential pairs operate. As a result, at least one of the two differential pairs will operate for any V_{CM} between both power supply rails.

It is desirable to maintain the nominal performance of the circuit for the entire common mode input range. One of the most important circuit parameters is the transconductance, g_{mT}, of the input stage. The total transconductance of the input stage shown in Figure 3.1 is the sum of the transconductance of the n- and p-channel differential pairs g_{mn} and g_{mp}, as demonstrated in Equation 3.1.

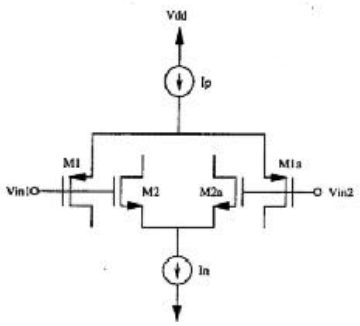

Figure 3.1: Rail-to-Rail, Complementary Input Stage

$$g_{mT} = g_{mN} + g_{mP}$$
$$g_{mT} = \sqrt{2K_N I_N} + \sqrt{2K_P I_P} \qquad (3.1)$$

If I_N and I_P are provided by constant current sources, then the variation in g_{mT} as a function of common-mode voltage can vary as much as 100%. This change is not desirable because it complicates the frequency compensation of the op amp and also results in harmonic distortion as described in [2][4]. As a result, it is desirable that g_{mT} be made constant, irrespective of the input, common-mode voltage.

Consequently, the following two subsections will briefly describe several alternative circuit techniques used to design active-mode, constant-gm, complementary input stages.

3.2 Wide-Swing, Constant-Gm Input Stage, Assuming $K_N=K_P$

Since the transconductance of a MOS device is proportional to the square-root of the drain current, and also the type of transistor used, i.e., n- or p-channel, a solution for stabilizing the total transconductance, g_{mT}, of the input stage was proposed in [5-8], under the assumption that an n-channel MOSFET can be matched to a p-channel MOSFET. Under this assumption, i.e. $K_N=K_P=K$, then Equation 3.1 can be rewritten as follows:

$$g_{mT} = \sqrt{2K}(\sqrt{I_N} + \sqrt{I_P} \qquad (3.2)$$

Then, the sum of the square roots of I_N and I_P must be kept constant to obtain a constant-gm input stage. Circuits that achieve this relationship based on the assumption that $K_N=K_P$ have been discussed in several papers, see [5] and [6]. Figure 3.2 presents a square-root, biasing circuit for a complementary, rail-to-rail input stage, as presented in [6].

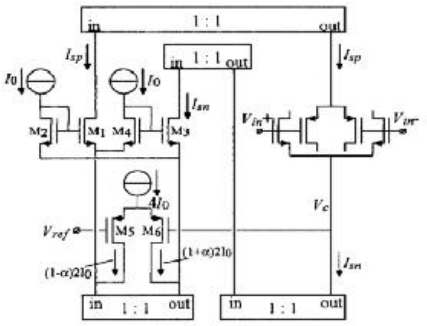

Figure 3.2: Constant-Gm, Input Stage

The circuit shown in Figure 3.2 forces the relation described in Equation 3.3, through the use of transistors M1-M4 which are connected in a MOS translinear loop [9]. As a result, the relation between the drain currents can be derived as described in Equation 3.4. The actual value of I_{SN} and I_{SP} are defined by a second condition, see Equation 3.3, which is forced by the differential pair M5/M6 and a current mirror. The factor α is dependent on the differential input voltage of M5/M6 and thus, on the common-mode voltage of the op amp.

$$\sqrt{I_{SN}} + \sqrt{I_{SP}} = \sqrt{I_O} + \sqrt{I_O} \qquad (3.3)$$

$$I_{SN} + I_{SP} = 4a\,I_O \;\; with \;\; -1 \le a \le 1 \qquad (3.4)$$

One major drawback with this type of constant-gm implementation, is that it is assumed that there is a fixed rato of electron-to-hole mobilities μ_N/μ_p, such that a fixed ratio of NMOS to PMOS dimensions $(W/L)_N/(W/L)_P$ can result in $K_N=K_P$. However, in general, different processes will have different μ_N/μ_p ratios, and furthermore, μ_N/μ_p variations can even occur within the same process. The variation of μ_N/μ_p can vary as much as 30% for a particular process, such that if the design was carried out using the median value of the ratio, the final value may have a +/-15% variation[2]. As a result, the

next section will describe a constant-gm input stage that does not rely on K_N matching K_P.

3.3 Wide-Swing, Constant-Gm Input Stage, Assuming $K_N \neq K_P$

Since earlier designs of rail-to-rail, complementary input stages were based on the assumption that $K_N=K_P$, [2] and [4] introduced several, revised comstant-gm input stages that improved upon the previous designs because they did not require for matching of n-channel transistors with p-channel transistors. Rather, the architecture proposed in [2] and [4] used negative feedback to maintain a constant transconductance for the rail-to-rail input stage. The rail-to-rail input stage with negative feedback operated as follows: a bias current $I_{n,max}$ was supplied to the bias circuit which served to keep $g_{mn} + g_{mp}$ constant. The constant-gm bias circuit produced a current I_P that was subsequently fed into the p-channel differential pair. The actual value of I_P being used by the differential pair was monitored by a separate circuit and any error currents were fed back into the bias circuit as the common-mode voltage was varied. This information was then used to vary I_n, which was the current that biased the n-channel differential pair, and thus maintained g_{mT} constant.

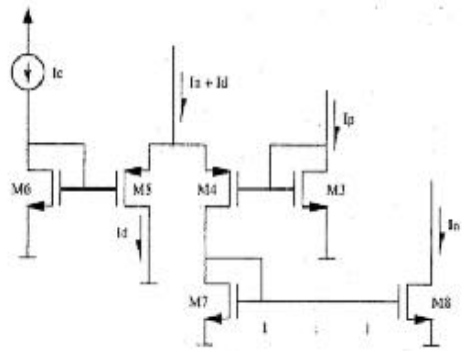

Figure 3.3: Revised, Constant-Gm Bias Circuit as Described in [2]

$$v_{SG6} + v_{GS6} = v_{SG4} + v_{GS3} \quad (3.5)$$

$$\sqrt{2I_C K_P} + \sqrt{2I_d K_n} = \sqrt{2I_n K_n} + \sqrt{2I_p K_p} \quad (3.6)$$

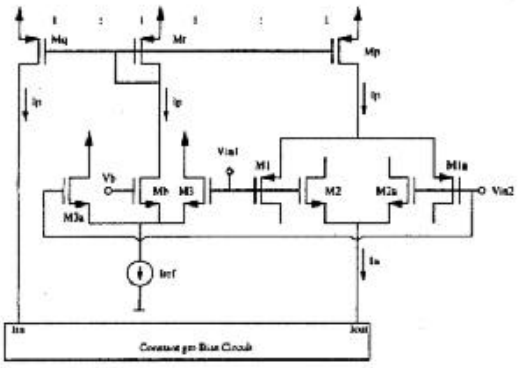

Figure 3.4: Implementation of Current Monitor as Described [2]

Figure 3.3 displays a low-voltage, constant-gm bias circuit for the wide-swing input stage[2][4]. The drain currents I_c and I_d are fixed bias currents, while I_n and I_p are the biasing currents for n- and p-channel input stages, respectively. In this circuit it is assumed that the input to the circuit is a copy of the common-mode current used by the p-channel differential pair and the output of the bias circuit is the bias current for the n-channel differential pair. By summing the gate-to-source voltages of transistors M3-M6, the relations expressed in Equations 3.5 and 3.6 can be found to be true. As a result, this circuit ensures that the total transconductance of the input stage is held constant.

Next, a monitor circuit, which was used to monitor the current level of I_P and feed it back to the constant-gm bias circuit, is displayed in Figure 3.4. In this circuit, the p-channel differential pair biasing current, I_P, is actively biased through transistor M_P. The

gate terminal of transistor M_b is biased with a constant fixed voltage, v_b. As V_{in1} and V_{in2} are increased, M3 and M3a consume a larger portion of Iref. Then the drain current in M_b decreases and I_p accordingly decreases with increasing V_{cm}.

However, rail-to-rail, complementary input stages suffer from one significant disadvantage which results from the fact that the complementary input pairs degrade the Common-Mode Rejection Ratio (CMRR) of the amplifier. This occurs in the range where the tail current switches between the P and N-channel input pairs. A CMRR as low as 40-55dB has been reported in [10]. Interested readers should refer to [1] for a detailed analysis of the CMRR degradation of rail-to-rail complementary input stages. In [1], the systematic and the process dependent CMRR factors are derived for several rail-to-rail input stages using various constant-gm biasing topologies.

3.4 Active Gain Enhancement

The first part of Section 3 introduced several, rail-to-rail complementary input stage topologies that can be used in the design of op amps with minimum power supplies of between 2-3V. The remaining portion of this chapter will introduce an active gain enhancement technique using auxiliary amplifiers to boost the output resistance of moderately low-voltage op amps.

The gain of analog circuits in a sub-micron technology is usually small due to short-channel effects. For the folded cascode op amp, the DC gain is approximately g_m^2/g_o^2, which is on the order of 40-60dB. However, for high-accuracy circuits, op amps with very high open loop gains and high unity-gain frequencies are required in order to meet both accuracy and fast settling requirements. As a result, active gain enhancement has been shown in [11-12] to be an effective method of meeting these design challenges in low-voltage applications, where further transistor cascoding is not possible. A variety of amplifiers can be used to implement the gain-boosting auxiliary amplifier, for instance, a simple inverting stage [12], or a fully differential amplifier [11-12]. Bult and Geelen have reported an op amp with 90dB gain and 116MHz unity gain bandwidth. The advantage of the active gain enhancement is that the DC gain of the op amp is enhanced by a factor of A_{aux}, which is the gain of the auxiliary amplifier, without sacrificing the unity gain bandwidth of the op amp.

An amplifier using active active-gain enhancement is prone to instability. The output settling time response (node 3 in Figure 3.5) typically exhibits high frequency oscillations of small magnitude. This is a direct consequence of the poor design of the feedback loop involving the auxiliary amplifier. This potential instability, which results from the feedback loop, can be observed through the large amplitude oscillations at the output of the auxiliary amplifier (node 2 in Figure 3.5). Bult and Geelen [11] have identified the potential instability in gain-enhanced amplifiers and have introduced criteria to stabilize circuits of this type.

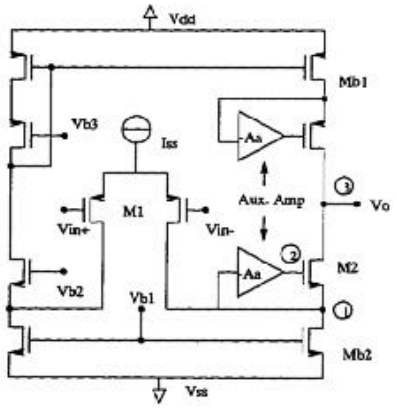

Figure 3.5: Gain-Enhanced Folded-Cascode Op Amp

$$A_{V,DC} = g_{m1}g_{m2}r_{o2}r_{b1}(A_{aux}+1) \quad (3.7)$$

$$F_{ORIG-3dB} < F_{T-AUX} < F_{ORIG-T} \quad (3.8)$$

$$b \cdot F_{ORIG-3dB} < F_{T-AUX} < F_{ORIG-T} \quad (3.9)$$

In [11] it was revealed that the unity-gain frequency of the auxiliary amplifier stage should be made smaller than the non-dominant pole frequency of the main amplifier, which is located at the source of M2 in Figure 3.5. The reason being, that the closed-loop gain enhancement may become unstable if the auxiliary amplifier is too fast. As a result, the auxiliary stage can be designed as a cascoded gain stage, with smaller width and non-minimal length transistors at lower current levels. [11] showed that a safe frequency range for the location of the unity-gain frequency $F_{T\text{-}AUX}$ is given by Equation 3.8, where $F_{ORIG\text{-}3dB}$ and $F_{ORIG\text{-}T}$ are the F-3dB and unity gain frequencies of the op-amp without active-gain enhancement, respectively.

However, the settling behaviour of the gain-enhanced cascoded amplifier stage should also exhibit a simple, first-order roll-off in the frequency domain response of the closed-loop output stage. Unfortunately, because of the presence of a closely spaced pole and zero (doublet) as described in [11], the auxiliary amplifier requires a higher unity-gain frequency than described in Equation 3.8. It is well known in control theory that a doublet can seriously degrade the settling behaviour of an op amp due to a slow settling component [14].

The approach taken in [11] was to make the "slow" settling component fast enough to meet the circuit requirements. If the time constant of the doublet $1/\omega_{PZ}$ is made smaller than the dominant time constant of the closed loop amplifier, $1/\beta\omega_{ORIG\text{-}T}$, with feedback factor β, the settling time will not be increased by the doublet. This occurs when the unity-gain frequency of the auxiliary amplifier is higher than –3dB frequency of the main circuit. However, for stability reasons, the unity-gain frequency of the auxiliary amp must also be lower than the second-pole frequency of the main amplifier. This results in a limited "safe" frequency range for the unity-gain frequency of the auxiliary stage, as described in Equation 3.9. This range is smaller than that described in Equation 3.8, due to the consideration of the settling-time of the op amp in closed-loop configuration. A satisfactory implementation, however, is still not difficult to achieve because the load capacitor of the additional stage, which determines $F_{T\text{-}AUX}$, is typically much smaller than the load capacitor of the main op amp.

As a result, the active-gain enhancement technique is a valuable gain boosting method for moderately low supply voltages in the regime of 2-3V. Very high gain amplifiers, of between 70-90dB, can be realized with this technique without compromising the unity-gain frequency, nor the output swing of the overall amplifier.

4 Op Amps For Sub-1.5V Power Supplies

As the power supply voltage continues to scale below 2V, designing analog circuits for digital processes becomes a significant challenge. The reason being that as the power supplies continue to scale down, the MOS threshold voltages V_T, do not scale proportionally because of the excessive leakage currents from digital CMOS circuits. As a result, typical op amp topologies are no longer suitable at sub-1.5V power supplies.

Operational amplifiers designed with power supplies over 2V can use such traditional gain stages as cascoding, current mirroring and active gain enhancement to achieve considerably high DC gains. At 2-3V power supplies, there is typically no need for more than 2-stages of gain for most common-purpose integrated amplifiers. As a result, compensating a 2-stage amplifier involved a relatively straightforward design procedure using Miller compensation, as described in [15]. Furthermore, adequate gain could also be achieved using single, cascoded gain stages, that were suitable for these supply voltages when biased with wide-swing, cascoded current-sources. As a result, for moderate supply voltages, there existed several op amp topologies that were satisfactory for a wide-range of applications, with none of them requiring complex compensation techniques, as needed for integrated op amps in the sub-1.5V power supply regime.

At extremely low power supplies, vertical gain enhancement techniques are no longer suitable because there is not enough voltage headroom to implement neither cascoded current-mirrors nor active-gain enhancement. As a result, horizontal gain-enhancement techniques, or cascading, of three to four simple gain stages must be used to achieve amplifiers with 70dB to 90dB of gain that are required in high precision analog circuitry. Such cascaded topologies are difficult to design with ensured stability because of the increased complexity of the closed-loop system. Single, and two-stage op-amps have at the most, one non-dominant pole that must be compensated for, while a three-to-four stage cascaded amplifier, can have up to three closely spaced, non-dominant poles, which significantly increase the complexity of the op amp compensation.

As a result, several compensation techniques have been developed to simplify the compensation procedure, and also to ensure the unity-gain frequency of the op amp is maximized with the inclusion of the compensation network. The following three subsections will briefly describe the three dominant compensation techniques developed over the last decade for cascaded, op amp topologies: Nested Miller Compensation [16], Multi-Path Nest Miller Compensation [17] and Nested Gm-C Compensation [1][3]. The first compensation technique to be introduced will be the Nested Miller Compensation structure, which was the first technique to be introduced in literature.

4.1 Nested Miller Capacitor Compensation Technique (NMCC)

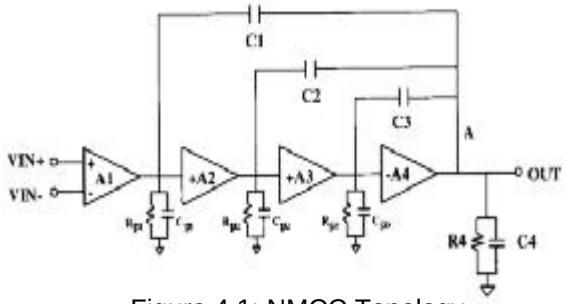

Figure 4.1: NMCC Topology

The block diagram of a multiple nested Miller compensated amplifier is shown in Figure 4.1. The case of a single-ended structure with four stages of gain is represented. The first stage is a differential input stage, the second and third ones are intermediate, non-inverting gain stages, and the last one is the inverting output stage delivering the power to the load represented by resistor R_4 and capacitor C_4. If a completely differential structure were used it would not be mandatory to use non-inverting intermediate gain stages, but in this case a crossing of the intermediate compensation capacitors would be necessary to obtain a stable structure.

$$f_i = \frac{1}{2pR_{Pi}C_{pi}}, i = 1,2,3 \quad (4.1)$$

$$f_4 = \frac{1}{2pR_4C_4} \quad (4.2)$$

A bode plot for the amplifier is presented in Figure 4.2. The poles of the open-loop frequency response without compensation capacitors are at the frequencies stated in Equations 4.1 and 4.2, where R_{Pi} and C_{pi} are the output resistences and capacitances, respectively, of the i-th stage, while R_4 and C_4 represent the external loads. Consider now the movement of the poles when the compensation loops are closed. The insertion of the compensation capacitors C_i produce a pole-splitting effect similar to that occurring in a simple Miller compensated structure. In this case, the pole at the output of the first stage, f_{im}, is pushed to a very low frequency while all other poles, including the one at the output, are pushed to high frequencies. The position of the dominant pole, f_{im}, is given by the Equation 4.3 which shows that f_{1m} is moved down to a frequency by a factor equal to the product of the gains of all the following stages. In order to obtain good phase margin, this pole must be at a very low frequency while the other non-dominant poles $f_{2m}…f_{Nm}$ must be at frequencies higher than the unity-gain frequency f_t of the amplifier. The exact position of the non-dominant poles can be quite complex to calculate. In fact, if

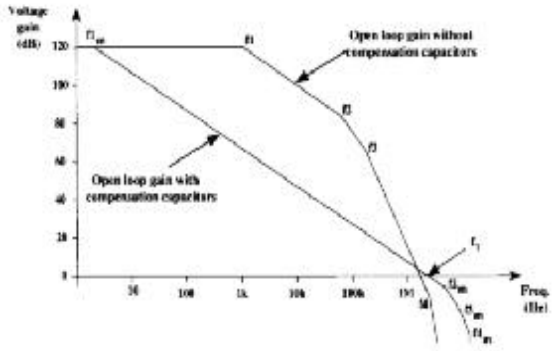

Figure 4.2: Bode Plot of an Amplifier With Double Nested Miller Compensation

$$f_{1m} = \frac{1}{2pG_{m2}R_{p2}G_{m3}R_{p3}G_{m4}R_4R_{P1}C_1} \quad (4.3)$$

no special precaution is taken, these poles tend to interact with each other giving rise to complex pairs. This produces bumps in the frequency response, which is an indication of a critical design from the point of view of stability.

A stable and robust design and a simple expression for the non-dominant poles can, however, be obtained if the rules in Equations 4.4 and 4.5 are followed, as described in [18], where G_{mi} is the transconductance of the i-th stage.

$$\frac{G_{mi}}{C_i} \leq \frac{1}{2} \cdot \frac{G_{mi+1}}{C_{i+1}} \quad (4.4)$$

$$G_{mN} >> G_{mi}, i = 1, N-1 \quad (4.5)$$

$$f_{im} \approx \frac{G_{mi}}{2pC_i} i = 2..4 \quad (4.6)$$

$$f_t \approx \frac{G_{m1}}{2pC_1} \quad (4.7)$$

When the above rules are satisfied, the approximate position of the non-dominant poles is given by Equation 4.6, while the unity-gain frequency of the amplifier is given by Equation 4.7

The first stability condition (Equation 4.4) requires each non-dominant pole to be positioned at a frequency, which is at least twice as high as the previous one. When this condition is satisfied, all of the poles are sufficiently separated so as not to interact with each other and as a result, all of them will be located on the real axis. In this case, each one of them can be associated with the output of each amplifying stage when computing the amplifier open-loop transfer function. The output of the first stage is associated with the dominant pole and the outputs of the following *n-1* stages with the non-dominant ones. Equation 4.4 is a stringent limitation that considerably limits the overall bandwidth of the amplifier as the number of stages is increased. It was made possible to overcome the bandwidth reduction effect using another compensation method entitled the Multi-Path Nested Miller Compensation (MNMC) technique, which was originally published in [16] and [17]. As a result of this significant performance improvement, the MNMC topology will be discussed in the following section.

4.2 Multi-Path Nested Miller Compensation

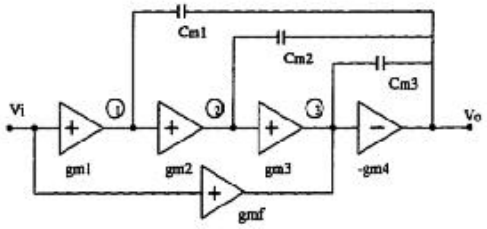

Figure 4.3: MNMC Technique Topology

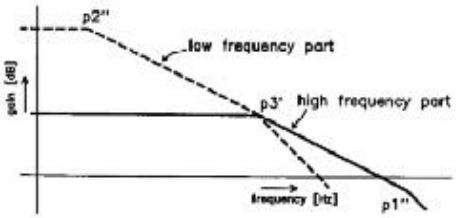

Figure 4.4: Bode Plot of the MNMC Structure

Multi-path Nested Miller Compensation (MNMC) adds an independent parallel input stage to transform the NMCC structure to the MNMC structure, as demonstrated in Figure 4.3. In Figure 4.4, the bode plot of the MNMC amplifier is shown. Drawn as a dashed line is the high-gain, low frequency part established by the three-stage NMCC amplifier. The solid line represents the high-frequency part created by the parallel input stage, with

transconductance g_{mf}, the output stage, with transconductance $-g_{m4}$, and Miller capacitor C_{m1}. Since this HF part is solely determined by a two-stage amplifier with simple Miller compensation, no bandwidth reduction takes place.

It is important to note that the multi-path input stage adds a zero to the transfer function, although the poles do not change compared to the NMCC structure. This makes evident, that the pole positioning of the MNMC structure should be different than the NMCC structure, otherwise the second pole will remain in its place and no bandwidth improvement would occur. The position of the second lowest pole p_2", with respect to its original position p_2' before closing the second Miller loop is given by Equation 4.8. From Equation 4.8, it can be seen that the greater ratio g_{m2}/C_{m1} compared to the limiting pole frequency p_2', can lower the bandwidth of the circuit. Setting g_{m2} to zero leads to $p_2''=p_2'$. In this case, there is no bandwidth reduction, since only two stages are active, so a better choice is $g_{m2}/C_{m1} \approx 0.1p_2'$. With this ratio, the bandwidth reduction is only about 10% and still three stages contribute to the low-frequency gain.

$$p_2'' = \frac{p_2'}{2} + \frac{p_2'}{2}\sqrt{1 - \frac{4g_{m2}}{p_2' \cdot C_{m1}}} \quad (4.8)$$

$$\frac{g_{m3}}{C_{m2}} = \frac{g_{m4}}{C_{m1}} \; if \; \frac{g_{m2}}{C_{m1}} << p_2' \quad (4.9)$$

$$w_{pz} = \frac{g_{m2}}{C_{m1}} \approx 0.1p_2' \approx 0.2w_0 \quad (4.10)$$

Putting the multi-path zero on top of the third pole p_3 requires the conditions expressed in Equation 4.9. As Equation 4.9 reveals, the matching of the pole and the zero only depends on the matching of transconductances and capacitors. The position of the new pole-zero doublet is expressed in Equation 4.10. In contrast to the NMCC structure, closing the outer-most Miller loop in the MNMC structure only moves the poles a fraction because of the low value of g_{m2}/C_{m1} and also the multi-path zero eliminates the detrimental effects of the pole p3, thus increasing the overall bandwidth of the amplifier. The final compensation technique that will be presented in this report is the Nested Gm-C Compensation Technique (NGCC), which extends the idea of MNMC by adding more feed-forward transconductance stages to bypass the gain drop of each amplifier stage at high frequencies. As a result, this method extends even further the bandwidth of the overall amplifier than both the NMCC and the MNMC techniques.

4.3 Nested Gm-C Compensation

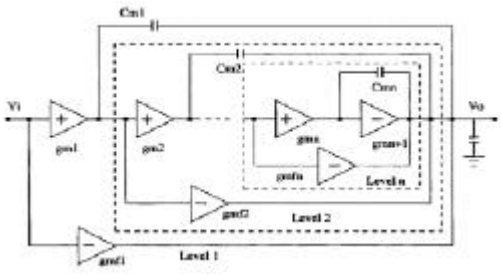

Figure 4.4: Cascaded Amplifier With NGCC Topology

Consider a three-stage NGCC amplifier as shown in Figure 4.4. It was shown in [1] that a three-stage amplifier has a transfer function shown in Equation 4.11, with some negligible second order terms omitted for simplicity. It can be seen from Equation 4.11, that the forward path transconductances g_{mf1}, and g_{mf2} affect the location of the poles and zeros of the transfer

function. Furthermore, if the forward path transconductances are set to be: $g_{mf1}=g_{m1}$ and $g_{mf2}=g_{m2}$, Equation 4.11 reduces to Equation 4.12, which now has all of the RHP zeros cancelled. This is due to Multi-Path Zero cancellation as described previously in Section 4.2.

Consequently, based upon the derivation obtained in [1][3], Equation 4.12 can now be re-cast generally into the form shown in Equation 4.13 for an n-th stage cascaded NGCC amplifier. This relation was subsequently used in [1][3] for the stability and the settling time analysis of any general, n-th order NGCC op amp.

$$\frac{Vo(s)}{Vi(s)} = -\frac{g_{m1}g_{m2}g_{m3} + sg_{m1}(g_{mf2}-g_{m2})C_{m2} + s^2(g_{mf1}-g_{m1})C_{m1}C_{m2}}{g_{o1}g_{o2}g_{o3} + sg_{m2}g_{m3}C_{m1} + s^2(g_{m3}+g_{mf2}-g_{m2})C_{m1}C_{m2} + s^3C_LC_{m1}C_{m2}} \quad (4.11)$$

$$H(s) = \frac{Vo(s)}{Vi(s)} = \frac{-g_{m1}g_{m2}g_{m3}}{g_{o1}g_{o2}g_{o3} + sg_{m2}g_{m3}C_{m1} + s^2g_{m3}C_{m1}C_{m2} + s^3C_LC_{m1}C_{m2}} \quad (4.12)$$

$$\frac{Vo(s)}{Vi(s)} = \frac{-\prod_{j=1}^{N} g_{mj}/g_{oj}}{\left(1+\frac{-\prod_{j=1}^{N} g_{mj}}{f_1}\right)\bullet\left(1+\frac{s}{f_2}+\frac{s^2}{f_2f_3}+\ldots+\frac{s^{n-1}}{\prod_{i=2}^{N} f_i}\right)} \quad (4.13)$$

$$f_4 > f_2 \quad (4.14) \qquad \text{and} \qquad f_4 > f_2 \bullet \frac{1}{(1-f_1/f_3)} \quad (4.15)$$

Next, [1][3] examined the transfer function for a 3-stage NGCC amplifier, and demonstrated that only two simple conditions had to be met in the design of the compensation network to ensure the stability of the closed-loop system. These straightforward design constraints are now repeated in Equations 4.14 and 4.15, respectively. A comparison of these design criteria with the NMCC technique was subsequently performed in [1][3]. There, it was shown that the corresponding stability criteria of an NMCC amplifier are extremely complex. Consequently, the two simple criteria for a NGCC structure make it much easier to design in practice than both its NMCC and MNMC counterparts. Furthermore, it was also shown in [1][3] that if two amplifiers were designed for identical power consumption, the first amplifier implemented using the NMCC topology, and the second using the NGCC structure, then the NGCC amplifier would have the greater gain-bandwidth product than the corresponding NMCC structure.

Structurally, the only difference between the NGCC and the NMCC topologies are the extra Gm feed-forward stages. However, when these extra Gm feed-forward stages are typically implemented on a circuit level, they consume almost no significant area or power overhead when compared to its equivalent NMCC structure.

Figure 4.5(b) depicts the transistor level implementation of the basic cell for a NGCC amplifier as obtained from [1][3]. The G_{M1} block is realized using the non-inverting amplifier created by M_{11}-M_{14}, such that the transconductance of M_{11} must be set equal to the transconductance of G_{M1}. The second stage G_{m2} is implemented using the inverting stage M_{21} and M_{22} and once again, the transconductance of M_{22} must be set equal to that of G_{M2}. The simplest way to realize the feed-forward stage G_{Mf1} is to use a single MOSFET (M_{f1}), which is driven by the input and connected to the output node. To ensure that $G_{m1}=G_{mf1}$, the transistor M_{f1} is sized identically as M_{11}. Since M_{22} is typically larger than M_{f1}, such that $g_{m22}>g_{mf1}$, then M_{21} is necessary to provide the DC current required by M_{22}. Finally, this implementation ensures that both silicon area and power consumption of the NGCC amplifier are conserved, when compared to a NMCC amplifier.

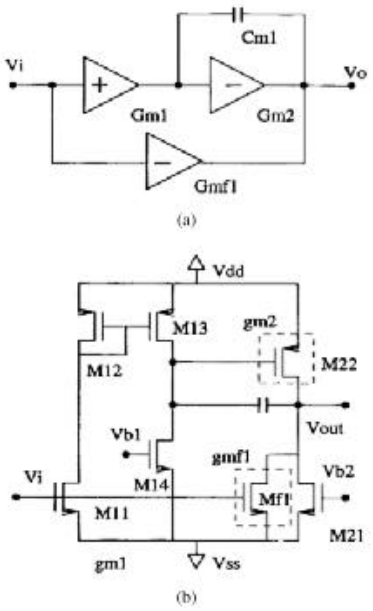

Figure 4.5: (a) The basic NGCC Module; (b) Its Transistor Level Implementation

The same approach depicted in Figure 4.5(b) can be extended to realize multi-stage amplifiers, as shown in [1] and [3]. In these implementations, a differential input stage and an extra feed-forward stage have been added (g_{mf1}). All gain stages, other than the differential stage, can operate with a supply voltage of $V_T+2V_{DS(SAT)} \approx$ (1.2V for V_T=0.8V). The differential stage, which requires $V_T+3V_{DS(SAT)} \approx$ (1.4V for V_T=0.8V), determines the minimum allowable power supply voltage for the amplifier. If low V_T devices were used for the input pair to increase the common-mode range, then the minimum possible power supply would be around 1.2V for a 0.4um process.

As a result, the bandwidth advantage and ease of implementation offered by the NGCC topology will increase its prominence in high accuracy, mixed-signal circuits as supply voltages continue to scale below 1.5V for CMOS VLSI's.

5 Conclusions

This report has investigated the theory and implementation of low voltage amplifiers. This work was motivated by the technology trend towards lowering the supply voltages from 3.3V down to 1.5V and lower. Consequently, two main categories of op amps have evolved over time, one operating between 2-3V and the other operating at 1.5V and below. As a result, the two categories have different structural features, which were determined by their corresponding power supply voltages.

Significant effort and research has been devoted to the enhancement of amplifier topologies operating with 2-3V power supplies. One of the most important building blocks for such op amps is the N-P complementary input differential pair, which is used to achieve a rail-to-rail input swing. This circuit has several drawbacks, in particular, the severe dependence of the total input stage transconductance, g_{mT}, on the input common-mode voltage. As a result, this report presented several alternative methods of stabilizing the input transconductance, which significantly eased the design of optimal compensation networks for these op amps. Another important circuit technique for 2-3V op amps is active gain enhancement, which allows for a significant increase in DC gain, although, the misuse of this technique may lead to instability or prolonged settling time. However, the instability resulting from the inclusion of the auxiliary amplifier in a gain stage can be compensated, as described in [11]. As a result, this report outlined a design technique for active gain enhanced, gain stages that ensured the stability and suitable settling time for high-precision op amps.

The second major part of this research was dedicated to addressing the need for op amps operating at sub-1.5V power supplies. It was found that op amps with 1.5V or lower supply voltages could not rely on cascoding techniques to realize high DC gain; instead multi-stage, cascaded amplifiers must be used in these environments. As a result, multiple Miller compensated compensation loops must be used to stabilize the multi-stage amplifiers, however, as shown it is quite difficult to design these compensation networks in practice. In this research, three different types of compensation schemes were introduced, along with design constraints for each compensation structure. It was also shown, that the NGCC topology provided maximum op amp bandwidth and the simplest stabilization when compared to the NMCC and MNMC structures, respectively.

In summary, the design of op amps in low voltage environments is critical to the successful integration of front-end analog circuits in sub-1.8V CMOS ICs. Furthermore, op amps are an invaluable tool to analog designers, but in order for this tool to be viable, designers of the future must learn the new techniques that allow traditional amplifiers to operate successfully in deep sub-micron VLSI's.

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