MOSFET DEVICE MODELING FOR ANALOG CIRCUITS DESIGN

Student name: Truong, Long Giang

Student #: 970304580

Course: ECE1352F

1. INTRODUCTION

The technological trend towards deep sub-micrometer dimensions, low voltage and low power design have set a new stage for today's device modeling for analog work. It becomes necessary to address the behavior of shrinking geometry MOS transistors. The appearance of different physical effects contributes to short-channel characteristics of MOS transistors [1]. This outlines new requirements for current MOSFET models. MOSFET models have to include physical parameters, have simple descriptions and be applicable to any advanced technology.

However, most of current advanced MOSFET models tend to be descriptive and lack of physical parameters. As a result, those models have a loss of inaccuracy in circuit simulation when moving into the deep sub-micrometer domain. Therefore, it is essential to develop a physically correct modeling so that we have accurate MOS transistors in simulating circuit operations.

The report starts with examination of deficiencies of current MOSFET models arise when moving analog circuits design toward deep sub-micrometer regime. Then, it discusses a surface-potential-based model that provides precision expressions satisfying the outlined requirements.

2. DEFICIENCIES OF CURRENT ADVANCED MOSFET MODELS

This section starts with a brief discussion of three regions of channel inversion with respect to gate source voltage. Next, it describes the poor modeling of the moderate operating region of current MOSFET models, poor modeling of the drain small signal conductance in saturation and poor modeling of intrinsic capacitances.

2.1 Three regions of channel inversion [2]

As gate source voltage V_{GS} is greater than threshold voltage V_T , an inverted channel is formed under the gate. However, the channel does not invert suddenly as V_{GS} is increasing but rather gradually. Therefore, we define three regions of channel inversion with respect to V_{GS}. The first region is weak inversion that occurs when V_{GS} is much below V_T. When the channel is strongly inverted, we have a strong inversion region. Moderate inversion is the region in between weak and strong inversion. Figure 2.1 illustrates a basic MOS structure and clearly shows the inverted channel formed under the gate as V_{GS} is increased.

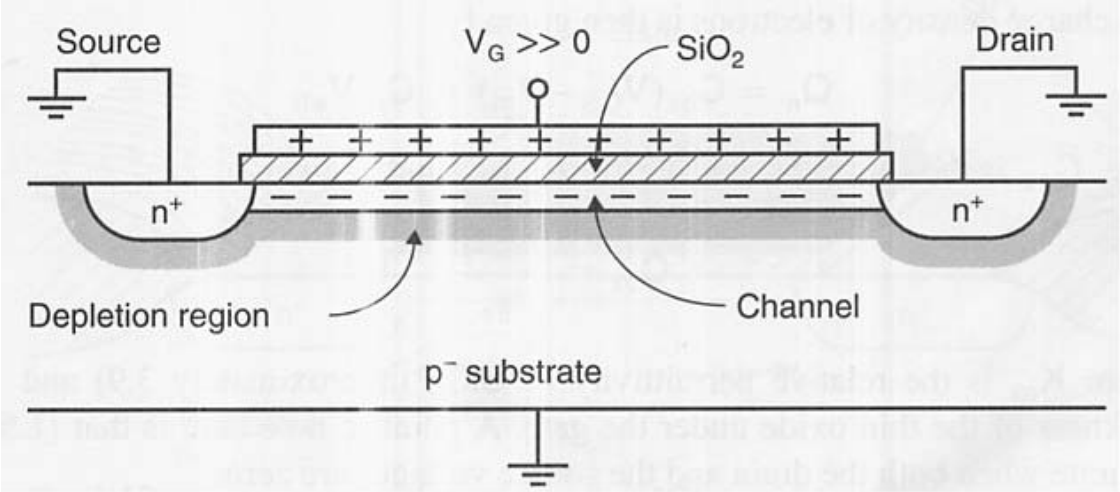

Figure 2.1: Basis MOSFET structure [2].

2.2 Poor modeling of the moderate region [3]

As design trend is moving toward low voltage and low power operation, the accurate modeling of moderate region is essential. However, most common advanced MOSFET models have assumed the moderate inversion region to be the bottom of the strong inversion region. As a result, strong inversion region expressions are used to simulate

analog circuit operations that result in large errors. The reason is that square law of strong inversion region vanishes since deeper sub-micrometer devices have mobility reduction and velocity saturation effects in moderately inverted channel. Hence, square law is becoming linear in short channel limit i.e. the drain current $I_{DS} \alpha (V_{GS} - V_T)$. In order to examine the moderate inversion region behavior, the I_D- V_{GS} relationship is plotted with very small V_{DS}. Figure 2.2 clearly shows that there exists a region where $I_D(V_{GS})$ is neither exponential (weak inversion region) or a polynomial (strong inversion region). Therefore, the computation of g_m in this region uses weak or strong inversion expressions will be incorrect. The error is magnified when we are considering low voltage and low power circuits. Hence, a correct modeling of the moderate inversion region is important.

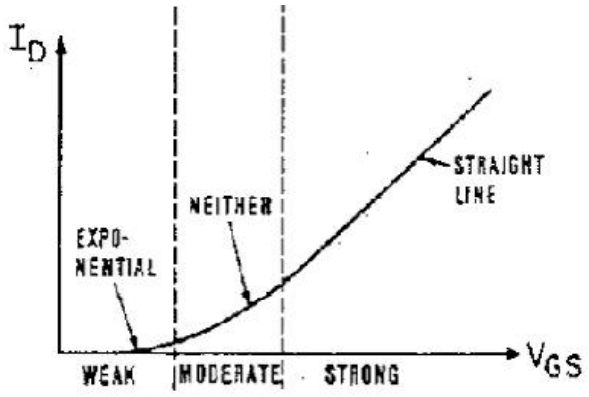

Figure 2.2: I_D- V_{GS} relationship in three regions of channel inversion [3].

2.3 Poor modeling of drain small signal conductance

Some advanced MOSFET models show the discontinuities in the derivatives of the drain current I_D at the boundary between linear and saturation region and between weak and

strong inversion conditions. The popular MOSFET model, BSIM3v3, is used in the following simulation [4]

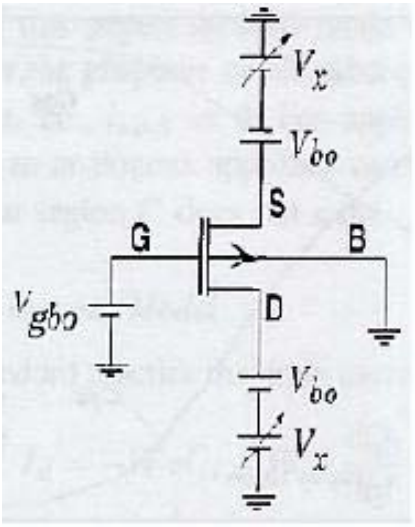

Figure 2.3.1: schematic drawing of the simulated circuit [4]

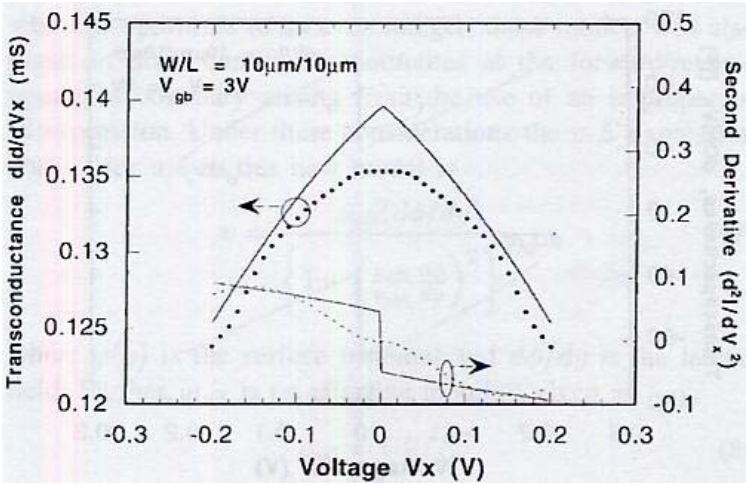

Figure 2.3.2: dI_D / dVx versus Vx [4]

Figure 2.3.1 includes the fixed gate substrate bias voltage V_{gb0}. Source substrate bias voltage is ($V_{b0} - Vx$). Drain substrate bias is ($V_{b0} + Vx$). V_{b0} is nonzero and Vx is an independent voltage. $V_{DS} = 2Vx$. In theory, I_D and all its higher derivatives with respect to

the terminal voltages are continuous. This implies that second derivative of I_D in the simulated circuit should be continuous at Vx = 0.

Figure 2.3.2 has clearly shown a discontinuity at Vx = 0 for second derivative of I_D while measured data is smoothed at the transition point. In order to illustrate a seriousness of this problem, we examine a CMOS inverter and its drain conductance g_d versus V_{DS} in the following example [3]

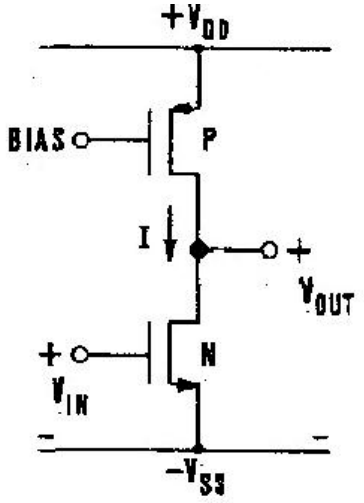

Figure 2.3.3: a CMOS inverter [3]

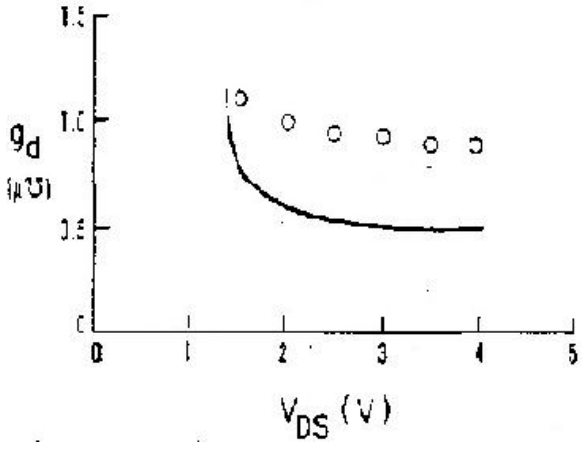

Figure 2.3.4: g_d versus V_{DS} with 40% error between measured and simulated data [3]

The small signal gain of the inverter is $g_{mN}/ (g_{dN} + g_{dP})$. An error of 40% is obtained from Figure 2.3.4. The gain is therefore overestimated to be 1/(1-0.4) = 1.67 times what the real value is. For a 2-stage CMOS amplifier with two cascaded inverters, we will obtain a small signal gain of 1.67x1.67= 2.8 times what the actual value is. This results in 180% error in calculating small signal gain.

2.4 Poor Small Signal intrinsic capacitance modeling

In addition to drain current behavior, poor modeling of terminal charges is also a major problem for most current MOSFET models. The same circuit in Figure 2.3.1 is used to simulate gate, source, drain and bulk charges of BSIM3v3. Figure 2.4.1 shows the discontinuity at Vx = 0 for trancapacitance dQ_G/dVx.

From the physical point of view, it is expected that capacitances Cgd ($=dQ_G/dV_D$) and Cgs ($= dQ_G/dV_S$) are equal when $V_{DS} = 0$. However, simulated results show that the two capacitances are nonidentical at $V_{DS} = 0$ as observed from Figure 2.4.2.

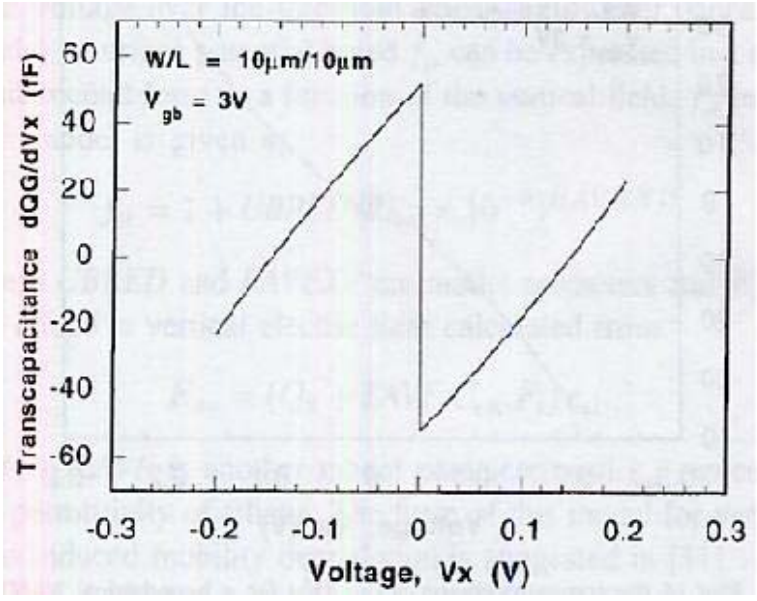

Figure 2.4.1: plot of trancapacitance dQ_G/dVx [4]

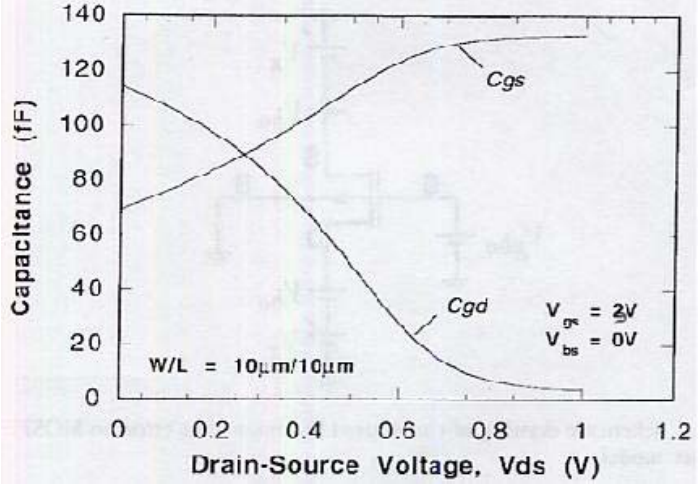

Figure 2.4.2: plot of Cgd and Cgs versus V_{DS} [4]

Design trend also moves to high-speed applications, the accurate modeling of capacitive characteristics of MOSFET is essential for small AC and transient simulation.

3. DESCRIPTION OF A PHYSICALLY CORRECT MODEL FOR DEEP SUB-MICROMETER REGIME

This section starts with a brief discussion of a modified model BSIM4 that is intended to correct the deficiencies in most popular and advanced MOSFET models discussed in section 2. However, it still doesn't satisfy the outlined requirements of the deep sub-micrometer technology trend. Next, the section describes the continuous surface potential based modeling which takes into account physical aspects, provides simple and easy description and is highly accurate.

3.1 Piece-wise approach modeling of BSIM4 [5]

BSIM4 has attempted to acknowledge the existence of moderate inversion region and discontinuities occur at transition boundary between linear and saturation, and

weak/strong inversion region. The model provides different expressions for different operating regions. It also tries to solve the discontinuity issue by smoothing numerically at transition point. For instance, an effective drain source voltage is defined to remove discontinuity at transition between linear and saturation region in the following equation

$$V_{DS\_eff} = V_{DS,SAT} - 0.5\ \{V_{DS,SAT} - V_{DS} - \delta + [(V_{DS,SAT} - V_{DS} - \delta)^2 + 4\delta V_{DS,SAT}]^{0.5}\ \}$$

Where $V_{DS,SAT}$ is the saturation voltage and δ is a fitting parameter. The obvious drawback is the complexity of mathematical expression that includes additional parameters introduced for smoothing. Hence, it will affect the simulation convergence time and complicate the model description. Moreover, the "artificial" modeling also lead to un-physical behavior that is more problematic in deep sub-micrometer design where process variations play a dominant role in ensuring the accuracy of circuit simulation.

3.2 Continuous surface potential based approach modeling [5]

This modeling approach is using the drift-diffusion approximation to describe drain current I_{DS}. As a result, it provides only one expression for all regions of operation.

$$I_{ds} = \frac{W_{eff}}{L_{eff}}\frac{\mu}{\beta}\left\{C_{ox}(\beta V_G' + 1)(\phi_{SL} - \phi_{S0}) - \frac{\beta}{2}C_{ox}(\phi_{SL}^2 - \phi_{S0}^2)\right.$$
$$- \frac{2}{3}(qN_{sub}L_D\sqrt{2})\left[\{\beta(\phi_{SL} - V_{bs}) - 1\}^{\frac{3}{2}} - \{\beta(\phi_{S0} - V_{bs}) - 1\}^{\frac{3}{2}}\right]$$
$$\left. + (qN_{sub}L_D\sqrt{2})\left[\{\beta(\phi_{SL} - V_{bs}) - 1\}^{\frac{1}{2}} - \{\beta(\phi_{S0} - V_{bs}) - 1\}^{\frac{1}{2}}\right]\right\}$$

Where N_{sub} = impurity concentration of substrate

L_D = extrinsic Debye length

β = inverse of thermal voltage

φ_{S0} = surface potential at source

φ_{SL}= surface potential at drain

V_{bs} = bulk charge

V'_G = gate voltage minus flat band voltage

The key quantities in this model expression are surface potentials at source and drain. Those physical quantities are computed iteratively using Poisson equation as a function of applied voltages. It is shown that the average iteration count is small; hence this iterative process won't slow down the simulation time.

This modeling expression is continuous in all bias conditions without the loss of physical meaning of MOSFET devices. All discontinuities are eliminated without introducing smoothing parameters. Therefore, the model is simple and comprehensible. Higher derivatives are smoothed at transition points. That is an important requirement for precision modeling of analog and RF circuits.

The first model using this approach is HiSIM developed by Hiroshima University and Semiconductor Technology Academic Research Center. Some important phenomena are observed after simulation as illustrated from Figure 3.2.1 and Figure 3.2.2. Figure 3.2.1 shows that the measured data have matched the simulated results. Figure 3.2.2 demonstrates 2 important intrinsic capacitances Cgg and Cgs as a function of V_{GS}

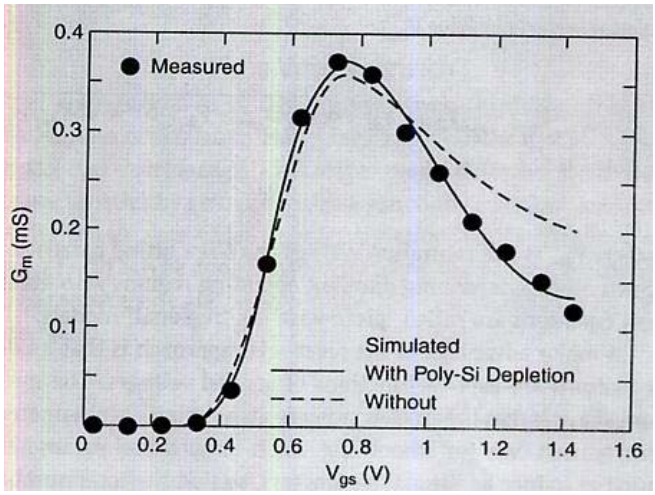

Figure 3.2.1 shows the agreement of the measured and simulated gm [5]

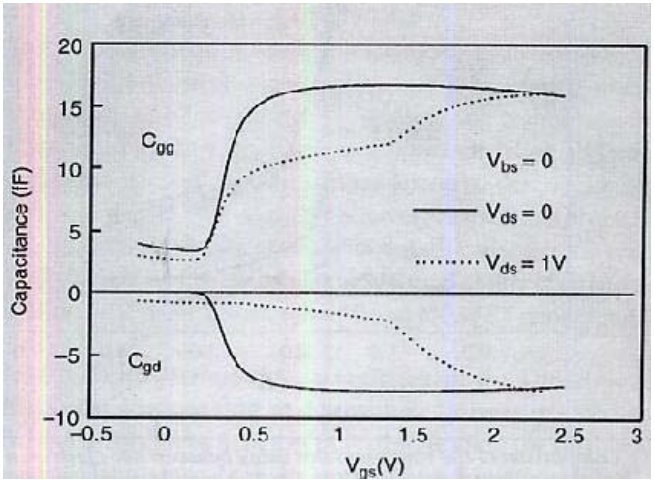

Figure 3.2.2 shows intrinsic capacitances [5]

HiSIM model has described all terminal charges with surface potentials hence basic device characteristics such as capacitances have preserved original physics.

A surface-potential based approach modeling has satisfied the outlined requirements of the new technological trend in deep sub-micrometer domain. This modeling has provided simple and highly accurate expression, improved convergence and simulation speed, and preserved original physics of MOS transistor.

4. CONCLUSIONS

This report has reviewed the deficiencies of current popular MOSFET models when technological trend moving towards 100nm design and low voltage/ low power operations. It outlined the new requirements for MOSFET modeling in the deep sub-micrometer regime. A great deal of emphasis is placed on obtaining physical-based, simple and highly accurate models. A comprehensible description of the surface potential description based on the drift diffusion approximation is practical and able to satisfy the foreseeable future of MOSFET models.

5. REFERENCES

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