ECE1352F Term Paper
Decision Feedback Equalizers and their Application to Magnetic Storage Read Channels

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Abstract

Intersymbol interference (ISI) can be a major speed-limiting factor in high-speed communications links, and must be mitigated to achieve an acceptable bit-error rate (BER). One efficient method of ISI mitigation is channel equalization using a decision-feedback equalizer (DFE) [1]. One system in which DFEs have been implemented extensively to combat severe ISI is the magnetic storage read channel. Many DFE architectures for this application have been proposed and implemented ([1],[2],[3]) .

This paper describes the motivation for the development of DFEs for use in high-speed communications systems, and in particular, the magnetic storage read channel. The operation and architecture of the DFE is described and several recent mixed-signal and analog implementations of DFEs are presented and compared. In particular, the Look-Ahead DFE (LADFE) and Random Access Memory DFE (RAM-DFE) are shown to provide substantial performance improvements over other architectures.

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1 Introduction

To satisfy the need for increased data capacity, the data rates of today's communications links are pushed increasingly higher. At such high speeds channel impairments lead to pulse smearing or ISI. To allow communication at high speed while maintaining an acceptable BER, systems must perform ISI mitigation [4]. Mitigation of ISI has many possible implementations, including transmit-side pre-emphasis [5] and maximum-likelihood sequence estimation (MLSE) [6]. Another common method is receive-side equalization, which can be performed in either the analog (continuous or discrete-time) or digital domains. A forward equalizer (FE) generates a signal to cancel ISI based on a combination of past samples of the received signal. Alternatively, a DFE can be used. The DFE generates a signal to cancel the ISI based on a combination of past output decisions. The use of a DFE in conjunction with an FE can result in improved ISI cancellation and as a result this solution is employed in many high-speed systems [1].

One system in which the DFE is commonly used is the magnetic storage read channel. To allow the development of affordable storage media with greater capacity, the data density of these devices is becoming extremely high [7]. With this increase in density comes an increase in ISI. While partial response maximum likelihood (PRML) detection is an alternative solution for these applications, in many cases the DFE has been identified as the optimal method for ISI cancellation [4]. As a result, much research gone into the development of high-performance DFEs for these systems. Also, there has been recent interest in the development of analog and mixed-signal DFEs that have similar performance to digital DFEs while providing a significant reduction in power consumption ([3],[8]).

This paper describes the state of the art in analog and mixed-signal decision-feedback equalization. While the basic concepts apply to all systems, the paper will present DFE implementations

for the magnetic storage read channel only, to maintain a reasonable scope and to allow direct comparison between competing architectures. In Section 2, the motivation for decision feedback equalization in magnetic storage channels will be further developed. In Section 3, the basic operation of the DFE is explained. In Section 4, the architecture of the DFE is described, with specific examples from the literature. In Section 5, recent architectural innovations of DFEs are presented and compared.

2 Motivation for Decision Feedback Equalization in Magnetic Storage Channels

As described in Section 1, the ISI in magnetic storage read channels is increasing as data densities are increased for greater storage capacity. Data is represented by a magnetization pattern on the storage device. When the read head passes over this pattern, it generates alternating positive and negative pulses for every transition (1-0 or 0-1) in the recorded data. The impulse response due to an isolatied transition is modelled by the Lorentzian function [9]:

$$L(t) = \frac{1}{1 + (\frac{2t}{PW_{50}})^2} \tag{1}$$

PW_{50} represents the pulse width at half-amplitude, and this quantity increases with recording density. A plot of this impulse response for a PW_{50}=2.5T (corresponding to a typical recording density) is given in Figure 1. T represents one bit period. From the plot it is obvious that there is significant signal power outside of the symbol period, and that ISI would present a serious problem for the detection of symbols sent over such a channel [9].

It is apparent that for operation at high data densities with low BER, this ISI must be cancelled. For disk-drives, the most common methods of ISI cancellation are PRML detection and decision-feedback equalization. PRML involves the use of the Viterbi algorithm to estimate the most likely

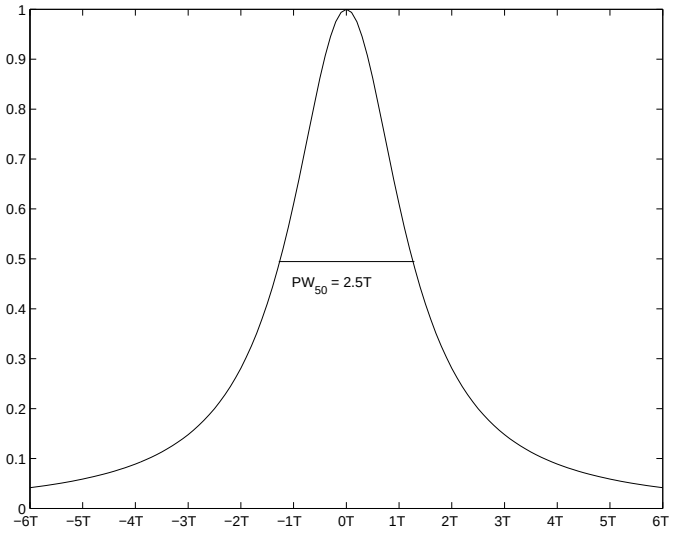

Figure 1: *Impulse response for the magnetic storage channel with PW_{50}=2.5T.*

data sequence based on samples of the input signal [1]. The DFE solution provides a simpler CMOS implementation than PRML detection [4], and in many channels it has been shown to have better performance [10].

2.1 Motivation for Analog and Mixed-Signal DFEs

DFEs can be implemented using digital, mixed-signal or analog circuitry. For disk-drive channels digital implementation involves a high-speed flash analog-digital converter (ADC) with medium (6 bits) resolution preceding the DFE circuitry. The power needed for the 63 comparators in this ADC as well as the power and area required for the digital multiplication in the equalizer filter is relatively high [2]. Analog equalizers can be smaller than digital equalizers [3] and the addition and multiplication functions can be performed efficiently in the analog domain, without the need for a high-speed ADC [1]. Coefficient adaptation may still be performed in the digital domain in a mixed-signal circuit, allowing for simple initialization and control of the coefficients [2]. In general,

for applications which do not require the precision and robustness that the digital implementation provides, or for portable systems, the power and die area savings provided by an analog or mixed signal implementation are attractive [4].

3 DFE Operation

A block diagram of the DFE is given in Figure 2. The term DFE is used interchangeably to represent the setup shown in Figure 2, including the FE, feedback equalizer (FBE) and slicer, as well as just the FBE and slicer components. In this paper, for completeness, the FE will be considered as part of the DFE.

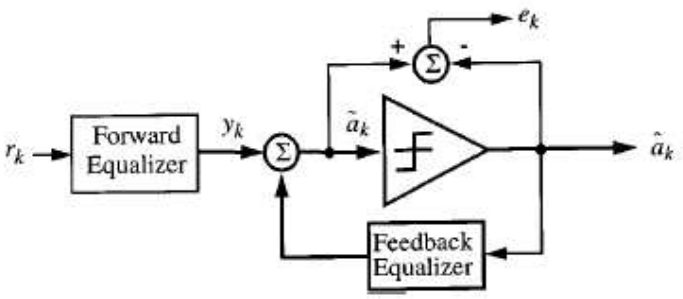

Figure 2: *Block Diagram of DFE. [11]*

If we define the peak of the Lorentzian impulse response given in Equation 1 and illustrated in Figure 1 as the cursor, then we can consider the non-zero values of the impulse response occurring before the cursor as contributing to precursor ISI. Likewise, the non-zero values occurring after the cursor contribute to postcursor ISI. The function of the forward FE in Figure 2 is to cancel the precursor ISI, while the FBE is responsible for cancelling the postcursor ISI. The input to the slicer is sampled at discrete time instants, with a period equal to the bit period. Therefore, the ISI must only be cancelled at those time instants. Consider the sampled impulse response in Figure 3(a).

After equalization by the FE the ideal output would be given by Figure 3(b), with all precursor ISI removed. After subsequent equalization by the FBE, the ideal output would be simply an impulse, shown in Figure 3(c), such that all ISI has been cancelled [2].

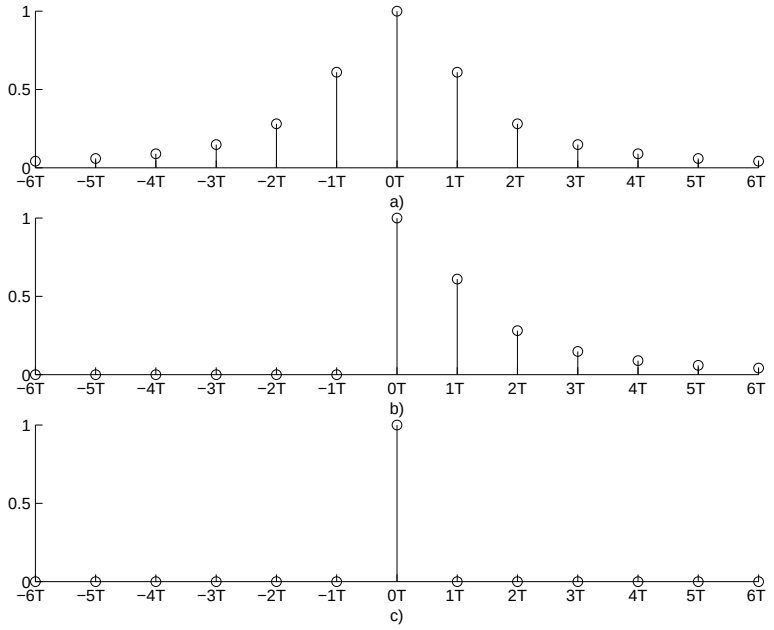

Figure 3: *Sampled Impulse Response. (a) Before equalization. (b) After forward equalization to remove precursor ISI. (c) After forward and feedback equalization to remove pre- and postcursor ISI. [2]*

The FE performs equalization based on samples of the received signal, r_k. The FBE, however, performs equalization based on the past output decisions, a_k. Using past output decisions provides some advantages. First, multiplication by the coefficients is trivial, since the input signal to the equalizer is binary. Also, the input signal to the equalizer is free from noise, so the equalizer does not enhance noise in the system. This is not true for the FE, which provides a high-frequency noise boost [1]. One drawback to this equalizer structure is that only postcursor ISI can be mitigated. This is not a problem for the system that we are studying, since precursor ISI is handled by the FE. This is also why the FE is often considered a part of the DFE architecture. Another drawback

is that if the slicer makes an error, the FBE can potentially make the situation worse since the cancellation signal it generates will be incorrect and the error may be allowed to propagate. This can result in burst errors and results in a degradation in the DFE performance [1].

Most communications channels require adaptive equalization to account for changing channel conditions over time. Magnetic storage channels are no different, as different sectors of the drive can have different densities and thus the read channel can vary [8]. Both equalizers are typically adapted such that the error signal e_k, between the output $\hat{a}_k$ and input $\tilde{a}_k$ to the slicer is minimized.

4 DFE Architecture

The basic architecture of the DFE was given in Figure 2. At the highest level, the DFE consists of an FE, an FBE and a decision circuit. Other blocks may be required depending on the particular implementation. In this section, each of these components is discussed independently, and recent implementations of each block are reported.

4.1 Forward Equalizer (FE)

The FE is a typically an FIR filter with adaptive coefficients. Realization of a discrete-time FIR filter requires a tapped delay line, sample and hold circuitry, and analog multiplication and addition (adaptation circuitry is discussed in Section 4.3). Since the output of the filter is the sum of the multiplied signals, multipliers with current outputs are generally desirable, to make the addition at the output trivial [12].

In [13], the input to the FE is sampled into a 5-tap delay line. The delay line is a cascade of 8 open-loop track and hold circuits. The waveform is sampled onto the gate capacitance of a pMOS differential amplifier through a FET switch in series with a charge-cancelling dummy transistor.

Feedback is used to set the common mode level of the amplifier and to set its voltage gain to exactly one, to maintain linearity. A schematic of this delay line is given in Figure 4. Tunable transconductors are used to multiply these analog signals with their tap weights and allow current addition or subtraction at the output of the filter.

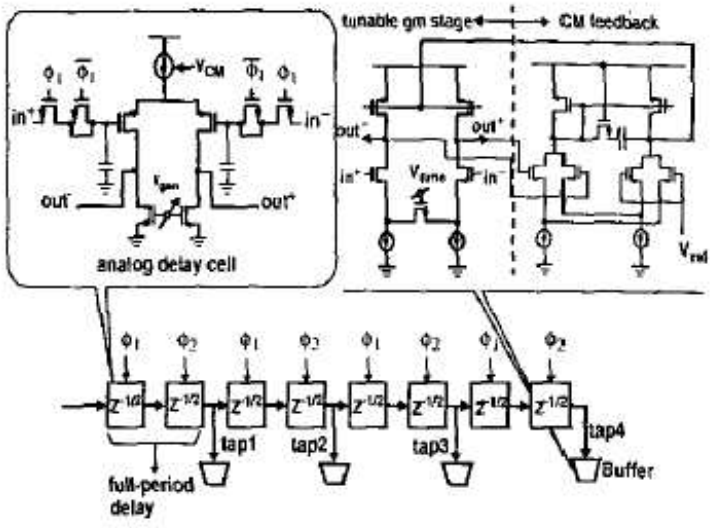

Figure 4: *Discrete-time Analog Delay Line Implemented using Track and Hold Amplifiers. [13]*

Alternatively, the FE can be implemented as a continuous-time filter. In [8], a five-tap FIR filter is implemented which makes use of programmable delay cells. These delay cells are Bessel allpass filters which have a delay which is tunable from 4ns to 14ns to allow accurate matching with the symbol period. The filters are implemented as MOSFET-C networks. A schematic of the delay cell is given in Figure 5. This FE also makes use of analog tap multipliers.

In [12], two third-order continuous-time allpass equalizers are described. The intent of these equalizers is to provide a lower-power alternative to FIR implementations for lower end disk-drives where a decrease in performance is acceptable. The filters were implemented as Gm-C current-mode structures. The response of these devices was shown to closely match the desired third-order

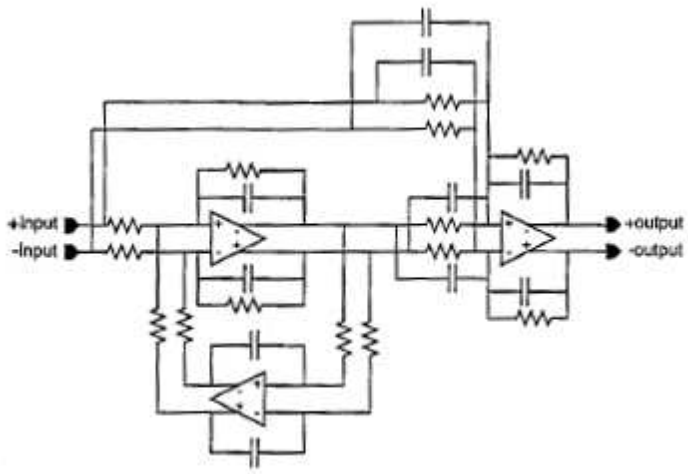

Figure 5: *Continuous-time Analog Delay Cell Implemented as Allpass Bessel Filter MOSFET-C Networks. [8]*

response and provide equivalent performance when compared to conventional FIR digital equalizers with power reduction by a factor of 10-100.

Finally, in [7], a one-zero continuous-time analog FE is used in a DFE system. This equalizer provides an ISI cancellation term which is a linear combination of the input signal $x(t)$ and its derivative $x'(t)$. The derivative signal is in this case available from a low-pass filter which precedes the FE in this system, so it is obtained for free. The products $\alpha_0 x(t)$ and $\alpha_1 x'(t)$ are provided by Gilbert cell multipliers that produce current outputs. The one-zero equalizer is shown to perform better than a five-tap FIR filter for channels with $PW_{50} < 2.2T$.

4.2 Feedback Equalizer (FBE)

Typically, the FBE is also an FIR filter, but it differs from the FE in that the input to the filter is a binary waveform. For a mixed-signal implementation, the coefficients are typically binary also, but the multiplication is performed using analog circuitry because the binary input makes it simple. Thus, the coefficient weights must be converted to an analog signal, using current-mode digital-

analog converters (DACs). Also, the delay line is simpler than in the FE case, since it can be made up of flip-flops in a shift register configuration.

In [4], a low-power BFE making use of current-steering techniques is described. The structure of this equalizer is illustrated in Figure 6. The magnitude of the cancellation terms are generated by scaling the tail currents of NMOS differential pairs based on the coefficient values. Addition and subtraction of the cancellation terms can be performed based on the polarity of the input to the amplifiers. The multiplication with the binary signal is performed by inserting NMOS current switches controlled by the binary input between the cancellation term generators and the output. When the input is low, the tail current is steered to V_{DD}. Since the tail current is not altered for a change in the binary signal, this circuit has a fast response time and is able to operate at high speeds.

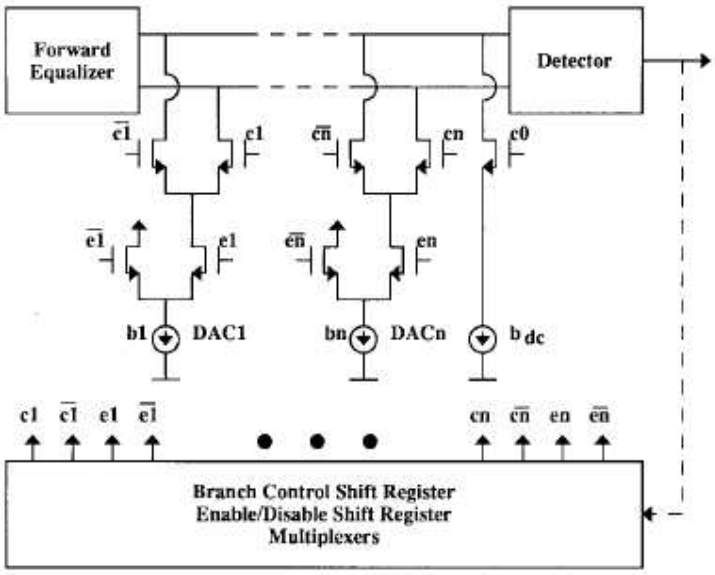

Figure 6: *FBE Circuit making use of Current-Steering Techniques. [4]*

Another implementation of the BFE differs from the past example in that it involves a RAM lookup-table. This type of BFE is described in [7], and illustrated in Figure 7. In this implemen-

tation, the BFE has a 4-tap delay line. The values in this delay line are past output decisions, $\hat{a}_k$, and are used as the address for the lookup-table. The output of the lookup table is the ISI cancellation value based on the past four output decisions. This approach is very powerful because the ISI cancellation that it performs is not limited to linear functions of the past decisions, so it is able to cancel ISI more effectively. While its appeal fades for larger numbers of taps (because the RAM scales exponentially with tap number), it provides good performance for channels with $PW_{50} < 2.5T$.

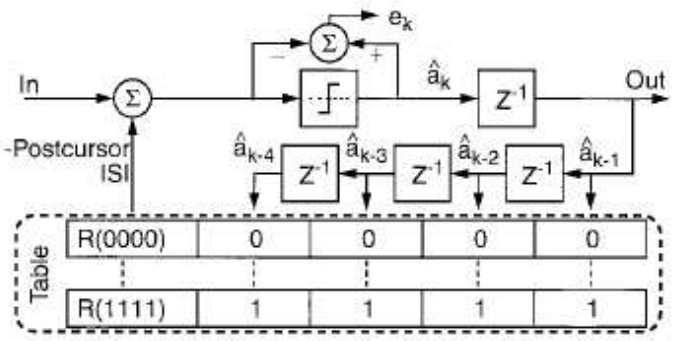

Figure 7: *FBE Circuit making use of RAM Lookup-Table. [7]*

In [8], an FBE implementation is described which makes use of a combination of linear and nonlinear ISI cancellation. An 8-tap delay line is formed by the concatenation of 3- and 5-bit shift registers. The bits in the 3-bit shift register are used as the address into an analog RAM to generate a nonlinear cancellation signal. The bits in the 5-bit register are used to generate a linear cancellation signal. Thus, the total cancellation is nonlinear in the three most recent decisions, and linear in the five oldest decisions.

4.3 Coefficient Adaptation

Coefficient adaptation is extremely important and has been omitted from the discussion of the equalizers until this point. The equalizers described in Sections 4.1 and 4.2 must continuously adapt to changes in the channel to maintain an acceptable level of ISI correction. The most common method of coefficient adaptation is use of the least mean squares (LMS) adaptation algorithm. To simplify the implementation, only the sign of the error is used in the adaptatation, so the coefficient update equation is [9]:

$$c_k[n+1] = c_k[n] + \mu \times \mathrm{sgn}(\hat{e}[n]) \times \hat{a}[n-k] \tag{2}$$

For mixed-signal implementations, in which the coefficients are digital, the update function can be performed using an up/down counter, greatly simplifying the implementation. The number of bits in the up/down counter effectively determines the μ. Figure 8 shows such a coefficient adaptation scheme which was presented in [1].

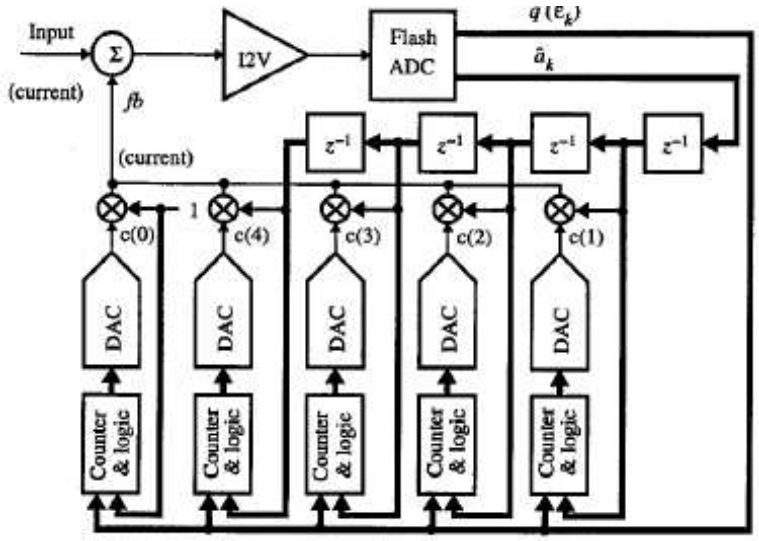

Figure 8: *Coefficient Adaptation Using Up/Down Counters and DACs. [1]*

In [9], another mixed-signal implementation is presented. Discrete-time integrators are used to

implement the coefficient update. These integrators consist of a 4-bit up/down counter followed by a charge pump integrator, and are illustrated in Figure 9.

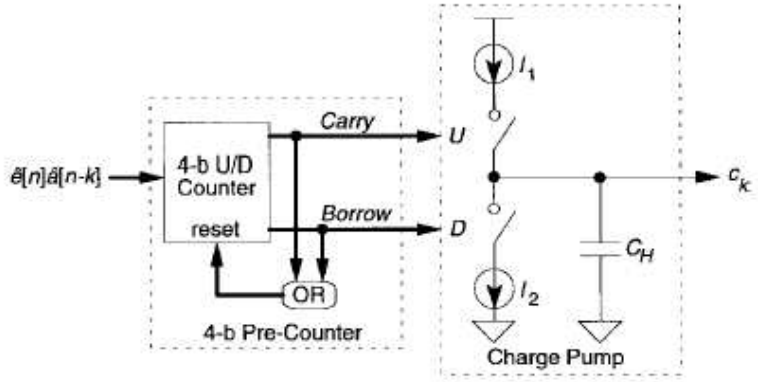

Figure 9: *Discrete-time Integrator for Coefficient Adaptation. [9]*

The 4-bit counter records small updates and the coefficient c_k is only updated when an overflow or underflow of the counter occurs. The reason for this is that 10-bits is identified as the necessary resolution of the coefficients for adaptation purposes, but a 6-bit DAC is sufficient for ISI cancellation. A 10-bit counter could alternatively be used, but the charge pump integrator effectively replaces a 6-bit counter and DAC, achieving lower power consumption. The error signal is determined from the difference between the output and input to the slicer. The error is then quantized to 1-bit to get the sign of the error and then fed into the integrator. A block diagram showing the coefficient update in this case is given in Figure 10. Analog signal paths are denoted by thin lines, while digital signal paths are denoted by thick lines.

In [8], a fully analog solution is employed, and the error signal e_k is used rather than $\text{sgn}(e_k)$. A switched-capacitor integrator is used to implement the coefficient update.

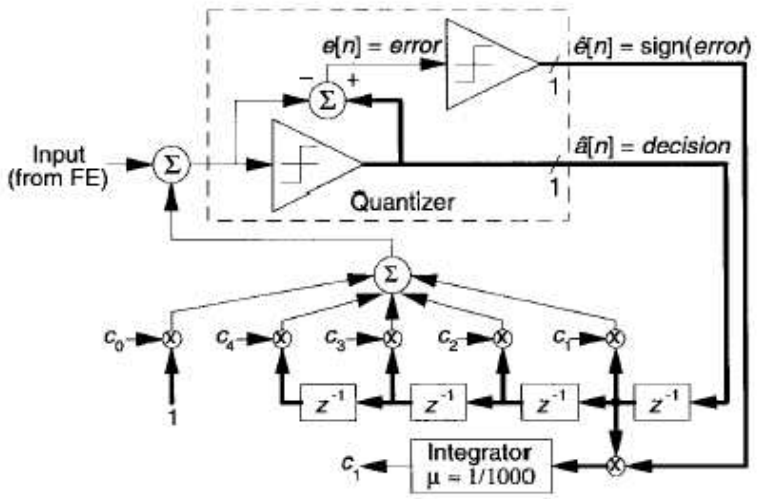

Figure 10: *Block Diagram showing Alternative Mixed-Signal Coefficient Adaptation. [9]*

4.4 Slicer / Analog-Digital Converter

The DFE consists of a decision circuit, or slicer. The slicer is a clocked comparator circuit, which analyzes its input at the sampling instants and decides whether to drive its output high or low. Since the sign of the output signal is also desired for adaptation purposes, the 1-bit slicer and 1-bit error quantizer are often replaced by a small flash ADC. This ADC provides both the output decision, $\hat{a}_k$ and the $\text{sgn}(e_k)$ signals.

In [1], a flash ADC with 5 comparators is used to generate the output decision and an error signal $q(e_k)$ which has three possible values, -1 if the error is negative, +1 if the error is positive, and 0 if the error is negligible.

4.5 Current-to-Voltage (I2V) Converter

The final component in the DFE is the I2V converter. This block is necessary because although the summation is most easily performed using current signals, the decision circuitry is voltage-mode. This conversion is performed in [1] and [9] using the circuit in Figure 11. The current through the

500Ω resistors is inversely proportional to the input currents. Thus, if In+ increases, I_{R+} decreases, increasing Out+, and vice versa for the opposite side.

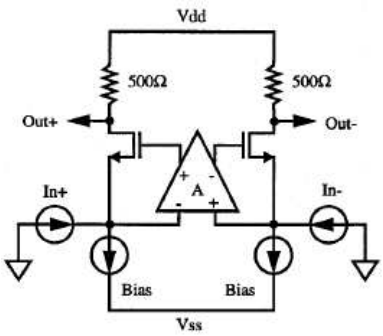

Figure 11: *Block Diagram showing I2V Circuit. [1]*

5 Recent Architecture Innovations for DFEs in Magnetic Storage Read Channels

In Section 4, recent implementations for various building blocks of the DFE have been presented. In this section, innovative architectures are studied. These architectures improve on the basic DFE structure of Figure 2.

In [2], a DFE is presented which allows much higher clock rates due to the use of parallelism. The block diagram for this system is given in Figure 12. The feedback loop containing the slicer and the multiplier tap corresponding to the most recent decision is the speed-limiting path in the device. This is because the delay through the decision circuitry is large, and the decision must then be multiplied and summed all in one bit period. The LADFE exploits parallelism to move the critical path to the path involving the second most recent decision. This is done by performing the equalization in parallel for both possible output decisions, $\hat{a}_k$, and then using a multiplexer to select the appropriate one when the decision is valid. While this involves an increase in hardware, for high-speed applications this may be required. The system was shown to achieve a 43% increase

in data rate compared to a conventional DFE.

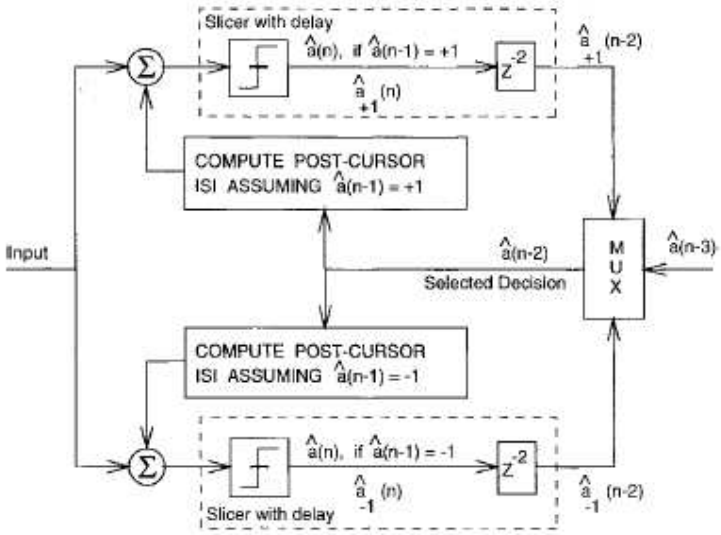

Figure 12: *Block Diagram showing LADFE System. [2]*

In [3], an adaptive analog noise-predictive DFE (NPDFE) is presented. The block diagram for the system is given in Figure 13. This system was developed to address the fact that the FE of a typical DFE system intorduces high-frequency boost which enhances noise. To mitigate the noise enhancement of this block, the FE is replaced by an all-pass FE (APFE) which cancels ISI without enhancing noise. The APFE consists of the FE with frequency response A(z) and the noise-predictive equalizer with frequency response B(z) in Figure 13. Analog components are used to achieve lower area and power. This system is shown to achieve a 2dB improvement in signal to noise ratio (SNR) with PW_{50}=2.5T.

6 Conclusion

In conclusion, the state of the art in analog and mixed-signal DFE implementations for magnetic storage read channels has been presented. The motivation for channel equalization and DFE sys-

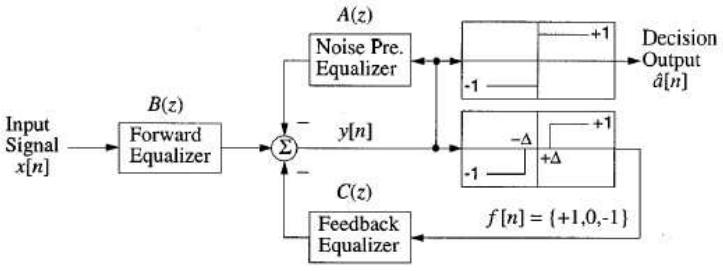

Figure 13: *Block Diagram showing NPDFE System. [3]*

tems has been developed. The operation and architecture of the DFE have been outlined, with many disk-drive implementation examples from the literature. Finally, recent system-level innovations have been described. The LADFE and the NPDFE have been shown to provide improvement over current DFE topologies.

The ongoing aim of DFE research is to develop systems which can operate at higher speeds and provide more accurate detection. Cost is a constant motivation, and researchers must push the limits of CMOS technology to achieve integrated DFEs capable of meeting high speed requirements. At the present-time, analog and mixed-signal DFE systems provide an attractive alternative to digital DFEs, due to savings in power and area at high operational speeds.

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