Avalanche Multiplication in a Compact Bipolar Transistor Model for Circuit Simulation

W. J. KLOOSTERMAN AND H. C. DE GRAAFF

Abstract—**A new and simple weak avalanche model will be presented, valid in a wide range of voltages and currents. The proposed model is derived by using the base-collector depletion capacitance for predicting the avalanche current. The model needs only one additional transistor parameter; the extraction method and temperature dependence of this parameter are discussed. The decrease in avalanche current at high collector current densities may originate from internal device heating, a voltage drop in the epilayer, or mobile carriers in the depleted part. From experimental results we conclude that, below a critical hot-carrier current, the decrease in avalanche current due to mobile carriers is negligible.**

I. Introduction

In a bipolar transistor, avalanche currents are generated in the base–collector depletion region when the transistor operates in the forward mode nearby the breakdown voltage. For high-frequency transistors, the breakdown voltage is low and avalanche currents are already generated below a collector voltage of 10 V. Therefore in circuit design accurate simulation of these effects is essential.

The following commonly used avalanche model was proposed first by Dutton [1]:

$$I_g = k_1 \cdot (M - 1) \cdot I_n$$

$$M = \frac{1}{1 - (V_{cb}/V_{cb0})^n} \tag{1}$$

where I_g is the generated avalanche current, I_n is the collector current without avalanche (initial electron current), and V_{cb} is the external applied base-to-collector voltage. The model parameters are k_1, V_{cb0}, and n. This empirical model is only accurate at relatively low collector current densities because the ohmic voltage drop and space-charge modulation of the collector epilayer are not taken into account. Divekar and Lovelace [2] extended this model to larger collector currents by making the parameters current dependent, resulting in an avalanche model with seven parameters. Poon and Meckwood [3] introduced a model for weak avalanche that had a more physical origin. Based on Chynoweth's empirical law [4] for the ionization coefficient

Manuscript received November 16, 1988; revised February 17, 1989. The review of this paper was arranged by Associate Editor T. H. Ning.

The authors are with the Philips Research Laboratories, 5600 JA Eindhoven, The Netherlands.

IEEE Log Number 8928078.

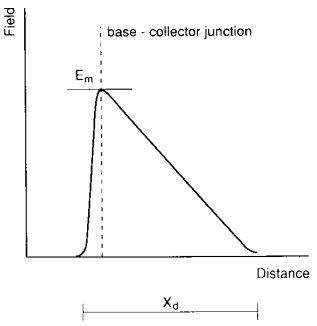


Fig. 1. Electric field distribution.

$$P_n = \alpha_n \cdot \exp\left(\frac{-b_n}{|E|}\right) \tag{2}$$

the generated avalanche current I_g was approximated by

$$I_g = I_n \cdot \frac{\alpha_n}{b_n} \cdot X_d \cdot E_m \cdot \exp\left(\frac{-b_n}{E_m}\right) \tag{3}$$

where X_d is the depletion layer thickness, E_m is the maximum electric field around the b-c junction, α_n is the avalanche coefficient and b_n is a critical electric field. Because I_g is taken as being proportional to I_n instead of the collector current I_c, the generated avalanche current should be much smaller than I_n (weak avalanche). The appropriate electric field distribution is shown in Fig. 1. In [3], E_m and X_d were modeled as a function of V_{cb} and I_c, taking into account space-charge modulation by mobile carriers (Kirk effect). This resulted in a rather complex and computationally expensive model with four parameters.

In the new avalanche model, we also start with (3). However, in contrast to Poon and Meckwood, we directly relate the depletion layer thickness X_d and the maximum electric field E_m to the collector depletion capacitance. So, in theory the model of the collector depletion capacitance determines the avalanche current and no extra parameters are required. In practice, we need one parameter to obtain the desired accuracy. The temperature dependence of this avalanche parameter is investigated and a temperature rule is established. We have extended the derived model to high collector current densities by taking mobile carriers

into account. However, from experimental results we conclude that below the critical current for hot carriers, the influence of mobile carriers is small.

II. Model Derivation

To derive the avalanche model we start with (3). The new approach taken here is that X_d and E_m are calculated directly from the base–collector depletion capacitance. A generally used depletion capacitance model is

$$C_{jc} = \frac{C_{0c}}{(1 + V_{c'b'}/V_{dc})^{P_c}} \tag{4}$$

where C_{0c} is the zero bias depletion capacitance, V_{dc} the diffusion voltage, P_c the grading coefficient, and $V_{c'b'}$ the internal base–collector voltage. This internal $V_{c'b'}$ is defined by

$$V_{c'b'} = V_{cb} - I_n \cdot R_{\text{epi}} \tag{5}$$

where R_{epi} represents the unmodulated resistance of the entire collector epilayer [5]; it is bias independent. The depletion layer thickness X_d follows from

$$X_d = \frac{\epsilon \cdot A_{\text{base}}}{C_{jc}} \tag{6}$$

where ϵ is the permittivity of silicon and A_{base} the area of the base region. The product of $X_d \cdot E_m$ is calculated by integrating the electric field in the depletion layer. A general approximating expression is

$$X_d \cdot E_m = \frac{V_{dc} + V_{c'b'}}{1 - P_c}. \tag{7}$$

This expression is exact for a step junction ($P_c = 0.5$) and a linear graded junction ($P_c = 0.33$). The final avalanche model follows from substituting (4), (6), and (7) into (3)

$$I_g = I_n \cdot \frac{\alpha_n}{b_n} \cdot \frac{V_{dc} + V_{c'b'}}{1 - P_c} \cdot \exp\left\{-AVL \cdot (V_{dc} + V_{c'b'})^{P_c - 1}\right\} \tag{8}$$

with

$$AVL = \frac{\epsilon \cdot b_n \cdot A_{\text{base}} \cdot (1 - P_c)}{C_{0c} \cdot V_{dc}^{P_c}}. \tag{9}$$

The expression for the avalanche current, as given here by (8) and (9), is more general than [3, eq. (10)] because it is not limited to one sided step junctions. The avalanche parameter AVL is given by the model parameters of the collector depletion capacitance. However, because of the high sensitivity of I_g with respect to AVL, it is preferred to consider it as an additional parameter, in order to make the model more accurate. Values for α_n and b_n can be found in the literature [6]–[9]. We use for an n-p-n transistor $\alpha_n = 7.05 \times 10^5\ \text{cm}^{-1}$ and $b_n = 1.23 \times 10^6\ \text{V/cm}$ and for a p-n-p transistor $\alpha_p = 1.58 \times 10^6\ \text{cm}^{-1}$ and $b_p = 2.04 \times 10^6\ \text{V/cm}$.

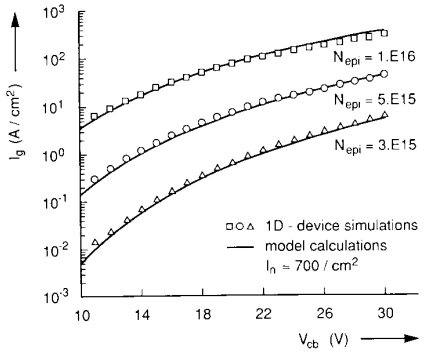


Fig. 2. Simulated avalanche current with different epilayer dopes.

TABLE I
Calculated and Extracted Avalanche Parameters

N_{epi}	C_{0c}	V_{dc}	P_c	AVL	AVL
cm^{-3}	F/cm^2	V		calc.	extracted
3.10^{15}	187.10^{-10}	0.685	0.491	41.8	43.6
5.10^{15}	233.10^{-10}	0.692	0.490	33.4	34.0
1.10^{16}	312.10^{-10}	0.761	0.489	23.9	24.8

The consistency of the model is checked by 1-D device simulations. In the device simulator the avalanche current is calculated directly, using numerical integration of the electric field in the b-c depletion layer. The doping level in the epitaxial layer has been varied from 3×10^{15} to $1 \times 10^{16}\ \text{cm}^{-3}$ with a thickness of 5 μm. The depletion capacitance parameters are determined according to (4), and the avalanche parameter is calculated from (9) and listed in Table I.

The avalanche parameter is also directly extracted from the simulated avalanche currents (the parameter extraction will be discussed in more detail in the next section). The extracted value also is listed in Table I and in Fig. 2 the simulated avalanche current is plotted together with the avalanche current predicted by the model, using the extracted values for AVL. The extracted AVL parameter agrees rather well with the calculated one, and the predicted V_{cb} dependence of the avalanche current is also in good agreement with the simulated data.

III. Measurement Setup and Parameter Extraction

In the measurement setup the base–emitter voltage is kept constant and V_{cb} is increased until the base current I_b has significantly decreased due to avalanche (Fig. 3). To avoid high current effects and internal heating, the base–emitter voltage is set to a low value of e.g., 600 mV. The difference between I_b at low and high V_{cb} is the generated avalanche current. The parameter AVL can be extracted by the usual least squares methods. The parameters P_c and V_{dc} in (8) are obtained from the base–collector depletion capacitance measurement. The parameter AVL is not sen-

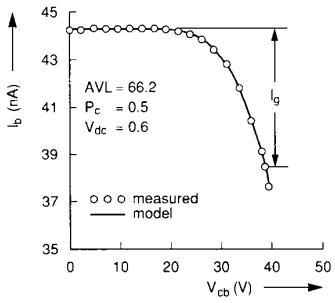


Fig. 3. Decrease of I_b due to avalanche. I_g is the generated avalanche current.

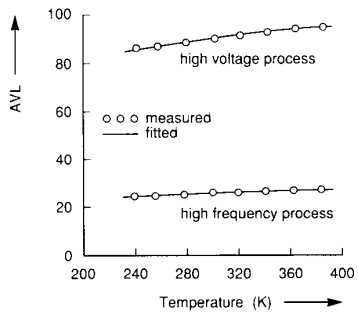


Fig. 4. The avalanche parameter versus temperature. The fitted curves give $\lambda_1 = 7.2 \times 10^{-4}$ and $\lambda_2 = -1.6 \times 10^{-6}$.

sitive to V_{dc}. The grading coefficient P_c determines the curvature of the base current with respect to V_{cb}.

IV. Temperature Dependence

The temperature dependence of the avalanche current is mainly due to the temperature dependence of AVL. The temperature dependencies of α_n and b_n in the pre-exponential term in (8) roughly cancel each other and can be neglected compared to the exponential variation. In the avalanche parameter AVL (see (9)) the product of $C_{0c} \cdot V_{dc}^{P_c}$ is temperature independent, so only the temperature dependence of $\epsilon \cdot b_n$ in the exponential term remains. For different IC processes (from high frequency to high voltage), the temperature dependence of AVL was determined (Fig. 4). The high-voltage device had $A_{em} = 10 \times 10$ μm, $N_{epi} = 1 \times 10^{15}$, $W_{epi} = 9$ μm, and the high-frequency device had $A_{em} = 2.7 \times 4$ μm, $N_{epi} = 2 \times 10^{16}$, $W_{epi} = 0.2$ μm. It became clear from these results that AVL increases with temperature as expected. For all investigated processes the avalanche parameter can be expanded in a Taylor series around $T_{ref} = 300$ K

$$AVL(T) = AVL(T_{ref}) \cdot (1 + \lambda_1 \Delta T + \lambda_2 \Delta T^2) \quad (10)$$

where ΔT is the device temperature minus the reference temperature. The extracted avalanche parameters are fitted with $\lambda_1 = 7.2 \times 10^{-4}$ and $\lambda_2 = -1.6 \times 10^{-6}$.

Rang [7] gives 6.43×10^{-4} as an empirical value, whereas Hall [9] gives 8.3×10^{-4} as a theoretical value for λ_1. These figures indicate that our value for λ_1 is certainly plausible.

V. Model Validity

The avalanche model has been derived with the assumptions that the collector current does not affect the electric field distribution in the depletion layer and that the thickness of the epilayer is larger than the thickness of the depletion layer. The thickness of the epilayer is not so critical because the maximum electric field remains at the b-c junction as long as a certain critical current is not exceeded (see (12)) and this field mainly accounts for the generation of avalanche currents. In the situation of high collector current densities (Fig. 5), however, the collector current can decrease the maximum electric field (space-charge modulation), and this results in a decrease in avalanche current.

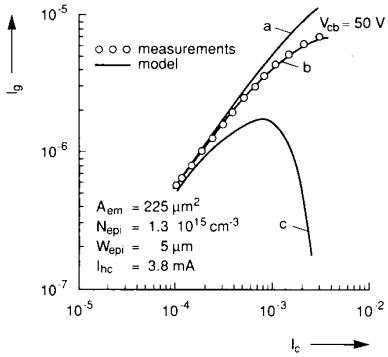


Fig. 5. Influence of space-charge modulation, temperature rise, and internal voltage drop. Curve a: Model calculations without temperature increase and space-charge modulation ($\theta = 0$). Internal voltage drop is included in the model. Curve b: Same, but with temperature increase ($r_{th} = 150$°C/W). Curve c: Same, without temperature increase, but with $\theta = 1$.

Besides space-charge modulation, a voltage drop in the epilayer and internal transistor heating may also result in a lowering of the avalanche current. To investigate the different mechanisms of avalanche current reduction we first extend the model with space-charge modulation. For a one-sided step junction the collector capacitance may be written as

$$C_{jc} = C_{jc}^{In=0} \cdot \sqrt{1 - I_n/I_{hc}}. \quad (11)$$

Equation (11) incorporates modulation of the fixed ionized donor charge N_{epi} due to mobile hot carriers moving with the saturated drift velocity ($v_s = 8 \times 10^6$ cm/s) in the depletion region. Then the space charge is given by [10], [11] $N_{epi} - I_n/(q \cdot A_{em} \cdot v_s) = N_{epi} \cdot (1 - I_n/I_{hc})$. I_{hc} is a critical current for hot-carrier behavior, and it is given by

$$I_{hc} = q \cdot N_{epi} \cdot A_{em} \cdot v_s. \quad (12)$$

In linearly graded junctions the space-charge modulation causes the maximum electric field to change its position but not its magnitute [12]; thus, I_g is not affected.

We can now rewrite (8) as

$$I_g = I_n \cdot \frac{\alpha_n}{b_n} \cdot \frac{V_{dc} + V_{c'b'}}{1 - P_c} \cdot \exp\left[-AVL \cdot \left\{(V_{dc} + V_{c'b'}) \cdot (1 - \theta \cdot I_n/I_{hc})\right\}^{P_c - 1}\right] \quad (13)$$

where now θ/I_{hc} is an extra model parameter. Theoretically we have for a step junction $P_c = 0.5$ and $\theta = 1$ and for a linearly graded junction $P_c = 0.33$ and $\theta = 0$. In practice we will be somewhere in between. Fig. 5 shows the influence of θ on I_g: in the same figure the measured I_g at constant external V_{cb} is plotted as a function of I_c. The use of (13) with $\theta = 0$ only shows a slight decrease in slope due to the internal voltage drop (see (5)), whereas $\theta = 1$ gives too strong an influence with respect to the measured I_g. A good fit can be obtained with $\theta \approx 0.2$. However, the measured base and collector currents of the same transistor are plotted in Fig. 6. The observed greater-than-exponential increase in collector current indicates internal heating. From the power dissipation the increase of the internal device temperature is calculated as

$$\Delta T = r_{th} \cdot I_c \cdot V_{cb}. \quad (14)$$

Using the Mextram model equations [13], [14] and the temperature dependence of its parameters, we can fit the measurements in Fig. 6 for $r_{th} = 150°$ C/W. This is an acceptible value for the thermal resistance of an encapsulated device under pulsed test conditions (HP 4145). Similar results can be obtained with other device models (Gummel-Poon). The measured I_g values in Fig. 5 can now also be explained by the temperature increase given by (14), and using (10). This latter explanation must be the right one because Fig. 6 tells us that internal heating does occur, and that leaves hardly any room for space-charge modulation as an additional effect.

In a second example, the internal heating is kept small (the temperature rise is less than 2°C). The emitter area of this transistor is about 12 μm^2 and the epilayer dope is $3 \times 10^{15} cm^{-3}$ resulting in a lower V_{cb} for generating avalanche currents. The thickness of the epilayer is about 0.8 μm, and with the applied V_{cb} the epilayer is fully depleted. The transistor gain is very sensitive to the generated avalanche current, and by plotting the gain we can observe accurately slight variations in avalanche current, which are not perceptible in a plot like that in Fig. 5. At medium current levels ($I_c \approx 10^{-4}$ A), the gain is already (Fig. 7) decreasing before it falls off due to high injection and saturation ($I_c \approx 10^{-3}$ A). The measured h_{FE} again increases at still higher I_c due to increasing avalanche current. The physical phenomena might be explained as follows. Because the epilayer is thin, the depletion layer extends into the buried layer. At medium current levels the position of the maximum electric field remains at the b-c junction, but its magnitute is lowered due to space-charge modulation. For $I_c > I_{hc}$ the slope of the field changes sign; the maximum now appears at the buried-layer side and increases again with increasing current [11]. This kind of electric field distribution is quite different from the one

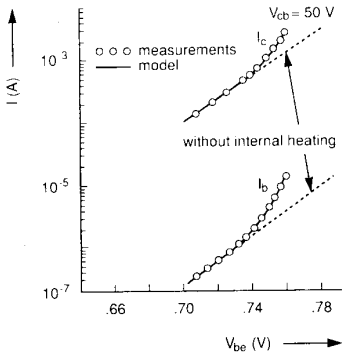


Fig. 6. Measured collector and base current. The model calculations are done with $r_{th} = 150°C/W$.

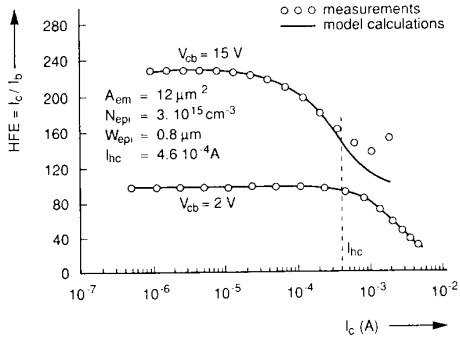


Fig. 7. Influence of avalanche current on current gain. At $V_{cb} = 2$ V is $I_g \approx 0$. The model calculations are carried out for $\theta = 0$ and no temperature increase.

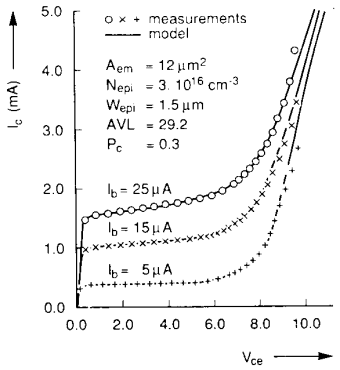


Fig. 8. Measured and predicted I_c versus V_{ce} curves.

sketched in Fig. 1 and our avalanche model is not valid anymore. However, for $I_c < I_{hc}$ the original model (see (5) and (8)) still gives a good fit of the h_{FE} decrease, thanks to the incorporated internal voltage drop, although this is probably not the right physical explanation. So, in conclusion we can say that for different IC processes, we can describe, up to the current I_{hc}, the decreasing avalanche current by the internal heating or the voltage drop in the epilayer. In most practical cases this is sufficient. It is demonstrated once more in Fig. 8, showing measured and calculated I_c versus V_{ce} curves with constant base current.

In this example the doping of the epilayer is 10 times higher, and the thickness is about two times larger than in the previous one. We see good agreement between the measured and calculated collector currents.

VI. Conclusion

Weak avalanche in bipolar transistors can be accurately modeled by using the collector depletion capacitance. The model has the advantages of a relatively fast numerical evaluation and the avalanche parameter can be extracted easily. The model incorporates an internal voltage drop, and the temperature dependence of the avalanche parameter is given. With this model we can accurately describe avalanche currents in a wide range of voltages and currents (Figs. 5, 7, and 8). The decrease in avalanche current at high collector current densities is ascribed to internal device heating or a voltage drop in the epilayer. From experimental results we conclude that the decrease in avalanche current due to mobile carriers is small below the critical current for hot carriers I_{hc}. The increase in avalanche current above I_{hc} is not described by the model.

References

[1] R. W. Dutton, "Bipolar transistor modeling of avalanche generation for computer circuit simulation," *IEEE Trans. Electron Devices*, vol. ED-22, p. 334, 1975.

[2] D. A. Divekar and R. E. Lovelace, "Modeling of avalanche current of junction transistors for computer circuit simulation," *IEEE Trans. Computer-Aided Design of ICAS*, vol. CAD-1, p. 112, 1982.

[3] H. C. Poon and J. C. Meckwood, "Modeling of avalanche effect in integral charge control model," *IEEE Trans. Electron Devices*, vol. ED-19, p. 90, 1972.

[4] A. G. Chynoweth, "Ionization rates for electron and holes in silicon," *Phys. Rev.*, vol. 109, p. 1537, 1958.

[5] H. C. de Graaff, "A modified charge-control theory for saturated transistors," *Philips Res. Reports*, vol. 26, p. 191, 1971.

[6] S. L. Miller, "Ionization rates for holes and electrons in silicon," *Phys. Rev.*, vol. 105, p. 1246, 1957.

[7] T. Rang, "The impact ionization coefficient of carriers and their temperature dependence in silicon," *Izv. VUZ, Radio Electr. Comm. Sys.*, vol. 28, p. 83, 1985.

[8] R. van Overstraten and H. de Man, "Measurement of the ionization rate in diffused silicon p-n junctions," *Solid-State Electron.*, vol. 13, p. 583, 1970.

[9] R. Hall, "Temperature coefficient of the breakdown voltage of silicon p-n junctions," *Int. J. Electron.*, vol. 22, p. 513, 1967.

[10] C. T. Kirk, "A theory of transistor cut-off frequency (f_t) falloff at high current densities," *IRE Trans. Electron Devices*, vol. ED-9, p. 164, 1962.

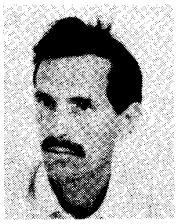
[11] H. C. de Graaff, "High current density effects in the collector of bipolar transistors, in *Process and Device Modeling for Integrated Circuit Design*, F v.d. Wiele, W. L. Engl and P. G. Jespers, Eds. Leyden, The Netherlands: Noordhoff, 1977.

[12] ——, "Compact bipolar transistor modeling," in *Process and Device modeling*, W. L. Engl, Ed. Amsterdam: North-Holland, 1986.

[13] H. C. de Graaff and W. J. Kloosterman, "New formulation of the current and charge relations in bipolar transistor modeling for CACD purposes," *IEEE Trans. Electron Devices*, vol. ED-32, p. 2415, 1985.

[14] H. C. de Graaff, W. J. Kloosterman, and T. N. Jansen, "Compact bipolar transistor model for CACD, with accurate description of collector behavior," in *Proc. Ext. Conf. Solid State Dev. and Mat.* (Tokyo), 1986, p. 287.

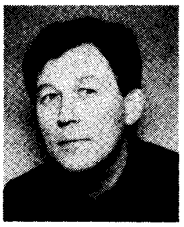
*



W. J. Kloosterman was born in July 1951 in Olst, The Netherlands. He graduated from the Technical College in Zwolle in 1974.

He joined the Philips Research Laboratories in 1974. First he worked on finite-element methods in mechanical engineering, and since 1980, has been involved in CACD, transistor modeling, and parameter extraction.

*



H. C. de Graaff was born in 1933 in Rotterdam, The Netherlands. He received the M.S. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1956, and the Ph.D. degree from the Eindhoven University of Technology, The Netherlands, in 1975.

He joined the Philips Research Laboratories in 1964, and has been working on thin-film transistors, MOST, bipolar devices, and materials research on polycrystalline silicon. His present field of interest is device modeling for circuit simulation.