A Full Duplex Ethernet Physical Layer Specification for 1000Mb/s or greater operating over Category 6 Balanced Twisted Pair Cabling 1000BASE-TX

DRAFT 2
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NOTICE:

This contribution has been prepared to assist the TR41.5 Standards Committee. It is offered to the Committee as a draft for PN-4657 and is not a binding proposal on the members of the TR41.5. The proposed requirements presented in this document are subject to change in form and technical content after more study. It is intended to serve as the basis for discussion and further development.

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1. INTRODUCTION

1.1 General

This standard specifies a full duplex Ethernet physical layer interface for 1000Mb/s or greater operation over a 100 meters of a Category 6 twisted pair cabling channel, 1000BASE-TX. To be compliant with this Standard implementers shall meet the minimum requirements defined in this Standard.

1.2 Purpose

The purpose of this Standard, 1000BASE-TX, is to provide an Ethernet physical layer specification that is low complexity and can easily be implemented by many vendors. This Standard will take advantage of the improved transmission parameters provided by Category 6 cabling currently under development in TIA TR-42 and ISO/IEC JTC1 SC25 WG3. It is believed by the members of this project that a much simpler solution for data rates of 1000Mb/s or greater operating over a 100 meters of Category 6 UTP cabling would be a benefit to users' who migrate to the higher data rates. It eliminates the complicated requirements in the 1000BASE-T Standard of canceling the effects of crosstalk and return loss. This provides a solution that can operate at a much lower power level, the potential for multiple ports per chip, and can be implemented at a lower cost.

In addition with the solution specified in this standard some of the Category 6 cabling requirements can be relaxed. This allows for the definition of a migration path for users who have not yet upgraded their cabling to Category 6 of an alternate cable plant for installed Category 5 or 5e.

2. OVERVIEW

2.1 Scope

This Standard specifies a 1000BASE-TX PHY layer as defined in the ISO/IEC Open Systems Interconnection (OSI) reference model. Included in this specification will be the required scrambling, coding, and modulation necessary to provide a 10^-10 or greater Bit Error Rate. A MAC layer interface with 8 bit wide data bus, transmit/receive clock, error, control; and a MDI interface that will support a dedicated channel of 100 meters of Category 6 twisted pair cabling will be specified. The 1000BASE-TX PHY will support a full duplex data rate of 1000Mb/s or greater. This Standard will only specify the minimum requirements, other requirements as defined in other standards are not excluded and are at the discretion of the implementer. Where possible this standard will defer to specifications in other standards.

2.2 Model

A model is illustrated in Figure 2.1 for a 1000BASE-TX PHY. Although sublayers within the 1000BASE-TX PHY may be defined, these may not be accessible. Not illustrated are possible sublayers as defined in IEEE 802.3 standards for management, reconciliation, or autonegotiation; these are left to the discretion of the implementer and are not specifically excluded.

It is recommended that a management interface should be provided that will provide access to management parameters and services as specified in Clause 22 of IEEE std 802.3. Clause 14 of this Standard recommends an implementation for autonegotiation.

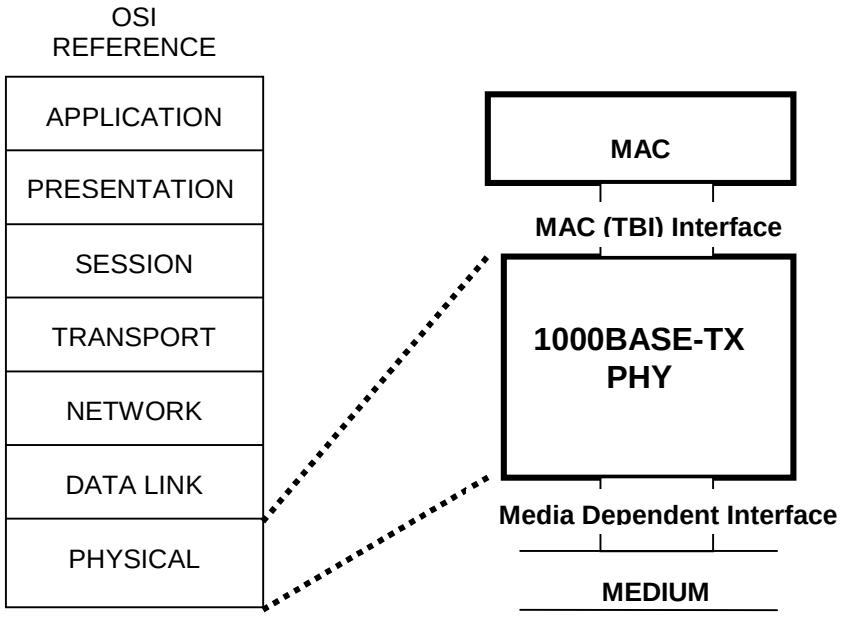

Figure 2.1 – Model

2.3 Relation to other Standards

This Standard specifies a dedicated Full Duplex Ethernet PHY layer as defined in the ISO/IEC Open Systems Interconnection (OSI) reference model, but does not support Carrier Sense or Collision Detect. The MAC interface will inter-operate with the GMII interface specified in IEEE std. 802.3 at full duplex. Support for addition clauses from IEEE std. 802.3 standards are beyond the scope of this standard. An Implementer may chose to be compliant with this standard along with clauses in other standards. In addition any forthcoming addenda to this Standard may provide alternate specifications to this Standard.

2.4 Normative References

The following standards contain provisions that, through reference in the text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision; parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated. ANSI and TIA maintain registers of currently valid national standards published by them.

ANSI/TIA/EIA-568-A: 1995, and Addenda: *Commercial Building Telecommunications Cabling Standard*

IEEE std. 802.3, 2000 edition: *Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications*

ISO/IEC 11801: 1995, *Information technology—Generic cabling for customer premises*

3. DEFINITIONS AND ABBREVIATIONS

3.1 Definitions

For the purposes of this Standard, the following definitions apply. The definitions do not contain mandatory requirements for this Standard. Specific requirements are found in the normative sections of this Standard.

Code Set: A set of two code groups representing symbols for transmission sequentially over two pairs of a four pair cable. Specified in this Standard.

Gigabit Media Independent Interface (GMII): The interface between the PHY and MAC as defined in IEEE std. 802.3 Clause 35.

Media Access Control (MAC): The Phy access layer defined in IEEE std. 802.3-1998.

Media-Dependent Interface (MII): The interface between the medium and PMD as defined in IEEE std. 802.3 Clause 18.

Physical Layer entity (PHY): The part of the Physical Layer between the MII and MDI interfaces as defined in IEEE std. 802.3.

Physical Medium Dependent sublayer (PMD): The part of the IEEE std. 802.3 PHY that is between the PMA and Media Conversion sublayer.

Ten Bit Interface (TBI): A ten bit interface as specified in IEEE std. 802.3 Clause 36.

3.2 Abbreviations

BER Bit Error Rate
EF End of Frame
GMII Gigabit Media Independent Interface
MAC Media Access Control
MDI Medium Dependent Interface
MII Medium Independent Interface
PHY Physical Layer entity
PMD Physical Medium Dependent
SF Start of Frame
TBI Ten Bit Interface

4. MAC INTERFACE

4.1 General

This section specifies the logical and electrical service interface between the MAC and 1000BASE-TX PHY. The purpose of this clause is to specify the minimum requirements to comply with this standard. This interface shall be compliant with IEEE std 802.3 clauses as referenced in this Clause.

4.2 Overview

Figure 4.1 illustrates the required interface. Each direction of data is serviced by a eight bit wide data bus, data valid, error, and clock signals. The interface is intended as a chip-to chip interface. The interface provides a media independent interface to a MAC and intended as a minimum set of requirements. Additional signals that support other standards and/or clauses are not specifically excluded.

This interface supports only 1000 Mb/s operation. Operation at other rates, such as 10Mb/s and 100 Mb/s is defined in IEEE std 802.3 Clause 22.

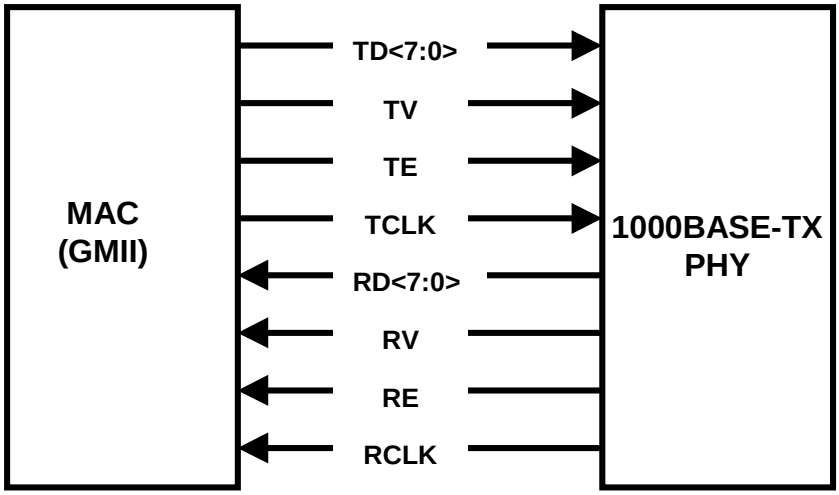

Figure 4.1: MAC Interface

4.3 Detailed Specification

The receive (RD<7:0>, RV, RE, RCLK) and the transmit (TD<7:0>, TV, TE, TCLK) signals shall meet the following requirements. Other uses for the signals that support additional functions, such as that defined in IEEE std 802.3 Clause 35, are not specifically excluded.

This standard does not require support of Carrier Extend or Carrier Extend Error.

4.3.1 RD<7:0> Received Data

The eight bits of the RD<7:0> is the received data from the 1000BASE-TX PHY. The received data is valid when RV is true and on the rising edge of the RCLK. All data transfers are aligned on eight bit boundaries. RD<0> is the least significant bit. The eight data signals shall meet the dc characteristics defined in 4.3.9 and the ac characteristics in 4.3.10.

4.3.2 RV Receive Valid

The RV shall indicate that on the next rising edge of the RCLK that the data is valid. RV shall become true before the rising edge of RCLK and remain true during all data transfers from the 1000BASE-TX PHY until the last valid data byte. The RV signal shall meet the dc characteristics defined in 4.3.9 and the ac characteristics in 4.3.10.

4.3.3 RE Receive Error

When RE is true at least one full clock cycle while RV is true, indicates that the 1000BASE-TX PHY has determined there is an unrecoverable error in the data stream. The RV signal shall meet the dc characteristics defined in 4.3.9 and the ac characteristics in 4.3.10.

4.3.4 RCLK Receive Clock

The RCLK is the received data clock sourced from the 1000BASE-TX PHY. The RCLK is a continuous clock that is the timing reference for RD<7:0>, RV, and RE. During non data transfer times the RCLK can extend a half cycle period by no more than two clock cycles. The RCLK signal shall meet the dc characteristics defined in 4.3.9 and the ac characteristics in 4.3.10.

The nominal frequency of RCLK is 125MHz.

4.3.5 TD<7:0> Transmit Data

The eight bits of the TD<7:0> is the transmit data for the 1000BASE-TX PHY. The transmit data is valid when TV is true and on the rising edge of the TCLK. All data transfers are aligned on eight bit boundaries. TD<0> is the least significant bit. The eight data signals shall meet the dc characteristics defined in 4.3.9 and the ac characteristics in 4.3.10.

4.3.6 TV Transmit Valid

The TV shall indicate to the 1000BASE-TX PHY that on the next rising edge of the TCLK that the data is valid. TV shall become true before the rising edge of TCLK and remain true during all data transfers to the 1000BASE-TX PHY until the last valid data byte. The TV signal shall meet the dc characteristics defined in 4.3.9 and the ac characteristics in 4.3.10.

4.3.7 TE Transmit Error

When TE is true at least one full clock cycle while TV is true, indicates to the 1000BASE-TX PHY that it shall insert a transmit error into the output data stream. The TV signal shall meet the dc characteristics defined in 4.3.9 and the ac characteristics in 4.3.10.

4.3.8 TCLK Transmit Clock

The TCLK is the transmit data clock to the 1000BASE-TX PHY. The TCLK is a continuous clock that is the timing reference for TD<7:0>, TV, and TE. During non data transfer times the TCLK can extend a half cycle period by no more than two clock cycles. The TCLK signal shall meet the dc characteristics defined in 4.3.9 and the ac characteristics in 4.3.10.

The nominal frequency of TCLK is 125 MHz.

4.3.9 DC Characteristics

All MAC interface signals shall meet the dc specifications in Table 4.1.

Symbol	Parameter	Conditions		Min	Max	Units
VOH	Output high voltage	IOH=-1.0mA	VCC= Min	2.10	3.60	V
VOL	Output low voltage	IOL=1.0mA	VCC= Min	GND	0.50	V
VIH	Input high voltage			1.70		V
VIL	Input low voltage				0.90	V
IIH	Input high current	VCC= Max	VIN= 2.1V		40	uA
IIL	Input low current	VCC= Max	VIN= 0.5V	-600		uA

Table 4.1 DC characteristics

4.3.10 AC Characteristics

All MAC interface signals shall meet the ac specifications in Table 4.2.

Symbol	Parameter	Condition	Min	Max	Units
VIL	Input low			0.70	V
VIH	Input high		1.90		V
Freq.	R/TCLK		1.25		MHz
Tr/f	CLK rise/fall time		0.1/Freq.		ns
Tsetup	R/TV,E,D<7:0>		0.5/Freq.		ns
Thold	R/TV,E,D<7:0>		0		ns

Table 4.2 AC Characteristics

4.3.11 MAC, GMII, and MII interfaces

The Mac interface signals defined in 4.3.1 to 4.3.8 are equivalent to GMII signals illustrated in Table 4.3. If a MII interface as defined in IEEE std. 802.3 Clause 22 is implemented it shall conform to the signal mapping specified in Table 4.3 and the specifications in Clause 22.

Mac Interface	GMII	MII
TE	TX_ER	TX_ER
TV	TX_EN	TX_EN
TD<7>	TXD<7>	
TD<6>	TXD<6>	
TD<5>	TXD<5>	
TD<4>	TXD<4>	
TD<3>	TXD<3>	TX<3>
TD<2>	TXD<2>	TX<2>
TD<1>	TXD<1>	TX<1>
TD<0>	TXD<0>	TX<0>
TCLK	GTX_CLK	TX_CLK
RE	RX_ER	RX_ER
RV	RX_EN	RX_EN
RD<7>	RXD<7>	
RD<6>	RXD<6>	
RD<5>	RXD<5>	
RD<4>	RXD<4>	
RD<3>	RXD<3>	RX<3>
RD<2>	RXD<2>	RX<2>
RD<1>	RXD<1>	RX<1>
RD<0>	RXD<0>	RX<0>
RCLK	RX_CLK	RX_CLK

Table 4.3 Signal Mapping

4.4 Testing

All MAC interface signals that are equivalent to a GMII interface shall be tested accordance with specifications defined in IEEE std. 802.3 Clause 35.4.2.1 and 35.4.2.2 for GMII devices.

4.5 Data Stream

Data streams transmitted to and from the MAC interface, defined in Clause 4.3, shall be transferred with the field shown in Figure 4.2.

Figure 4.2 – MAC interface data stream

The preamble and sfd are defined in IEEE std. 802.3 Clause 35.2.3.2 for both transmit and receive. The data consists of a continuous stream of octets. An end of transmission is indicated by de-assertion of TV. The preamble may be omitted when transmitting to the MAC.

4.6 Service Control Functions

The are no service control functions required for 1000BASE-TX PHY control across the MAC interface. A management control is specified in IEEE std. 802.3 Clause 22.2.4, 28.2.4, and 37.2.6.

4.7 Timers

There no required timers for 1000BASE-TX PHY control at the MAC interface.

4.8 Delay Requirements

Operating in full duplex mode, devices shall conform to the MAC/Media interface delay requirements specified in Table 4.4.

Event	Max (bit time)	Timing Reference
TV=1 to MDI Output	136	TD<7:0> to TP1/TP2
MDI Input to RV=1	192	TP1/TP2 to RD<7:0>

Table 4.4 Delay Requirements

Note: Need to review delay requirements

4.9 Reset

A 1000BASE-TX PHY reset shall be executed at power up or when requested by a management function.

5. TEN BIT INTERFACE (TBI)

Implementers may chose to implement a TBI interface as specified in IEEE std. 802.3 Clause 36. A recommended mapping of the signals for the interface to a GMII is illustrated in IEEE std. 802.3 Clause 35.3. See Table 4.3 for equivalent MAC Interface signals. The Ten Bit Interface shall comply with the requirements in Clause 36.

A TBI interface is intended to be used as simple 1000 Mb/s Physical Media Dependent, PMD, interface on a full duplex point to point link whose link partner is the same type of device. Management or auto-negotiation of the device(s) is not required.

6. OPERATION

The 1000BASE-TX PHY employs a full duplex baseband transmission over four pairs of Category 6 cabling. The full duplex data rate is achieved by operation at a data rate of 500Mb/s over each pair, two pairs for transmit and a separate two pairs for receive. A 250 Mbaud baseband 5 level Pulse Amplitude Modulation scheme (PAM5) is used on each pair. The modulation rate is twice the MAC interface clock rate. The 1000BASE-TX PHY's do not require a master/slave relationship.

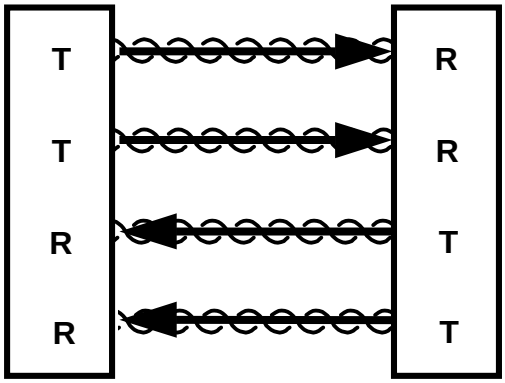

Figure 6.1 1000BASE-TX PHY Transmission

6.1 Signaling

Each 8 bits of data TD<7:0> is converted to two transmissions of two quinary symbols, 8B/2Q2, over two pairs. The transmitted symbol is selected from a 5 level set {2, 1, 0, -1, -2}. A code set of 2Q2 code groups is concurrently generated at time n, the MAC data period of 8 ns. These are then transmitted at symbol time t and t+1, where the symbol period is 4 ns. Note, the word code set is used to denote a sequence two code groups, 2Q2, representing the 8 bits of data.

Special code sets are used to transmit IDLE and control: Start of Frame (SF), End of Frame (EF), and a Transmit Error. The 1000BASE-TX PHY uses a continuous signaling, where IDLE code sets are transmitted in the absence of data.

6.2 Frame Format

Frames passed to the coding sublayer shall have the following structure, illustrated in Figure 6.2.

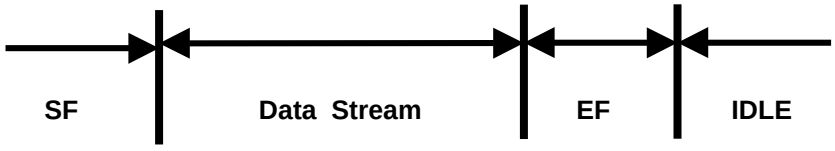

Figure 6.2 Frame Format

At the beginning of a frame of transmission indicated by the TV at the MAC interface two code sets representing a start of frame, SF, is transmitted followed by the data stream from the MAC, defined in Clause 4.5. The SF replaces the first two bytes of the MAC data stream (preamble). The completion of a frame, determined by TV, is followed by two code sets of end of frame, EF;

then the idle code sets, IDLE. A Transmit Error code set is transmitted when indicated by the TE signal at the MAC interface.

At the detection of SF by the receiving 1000BASE-TX PHY the MAC interface shall indicate a start of data with the RV signal. The SF is not passed on to the MAC interface. When the 1000BASE-TX PHY receives the EF frame signal it will indicate the end of data by the RV signal. Only decoded data octets are transmitted to the MAC interface. If the 1000BASE-TX PHY receives a Transmit Error code set or an invalid coding it will indicate this to the MAC interface with the RE signal.

A TBI implementation signals a start and end of data with a start of frame and end of frame delimiter code group. The SF will replace the start of frame delimiter and the previous byte of the idle TBI code group. The EF will replace the end of frame delimiter and the following first byte of the idle TBI code group. Data and Idle TBI code groups are transmitted as data and idle code sets. Error propagation or a decoded error is transmitted as a running disparity error.

6.3 Functions

The coding layer internal functions defined for control and status are left up to the implementer. Table 6.1 lists a cross reference of parameters used to those defined in IEEE std. 802.3 Clause 40.

1000BASE-TX	Clause 40
TD<7:0>	TXD[7:0]
RD<7:0>	RXD[7:0]
time t and t+1 code set n	n
Transmitting	tx_enable, tx_mode
Undefined	SEND_Z
Transmit IDLE	SEND_I
Receiving	rcvr_status = OK
Undefined	Csreset
Undefined	cext_, CSExtend
Transmit Error	tx_error, TX_ER, xmt_err
SF	SSD
EF	ESD

Table 6.1 Functions

7. CODING

Each data byte generates a code set, A and B; which is comprised of four code groups, A1, A2, B1, and B2. The code groups are then randomized and the code groups A are transmitted over the transmit pairs TP1 and the code groups B are transmitted over the transmit pairs TP2. Code groups A1 and B1 are transmitted at t and code groups A2 and B2 at time t+1.

7.1 Scrambling

To provide an uncorrected symbol stream the 1000BASE-TX PHY shall implement the following scrambling scheme by a linear-feedback shift register. It is not required for the transmit and receive clocks to be synchronized.

The 1000BASE-TX PHY shall employ the side-stream scrambler generator polynomial S(x):

S(x) = 1 + X^13 + X^33

Note: Reset on EF ?

7.2 Generation of a Code Set

7.2.1 Encoding Rules

The encoding of the data uses the bits from the side stream scrambler S[32:0] to generate the encoded bits E[8:0] for the symbol mapping in Tables 7.1 to 7.8 and R[3:0] to randomize the output symbol stream. The bits E[8:0] are defined by:

Note: The following is not complete.

E[0] = T<0> ^ S[0]

E[1] = T<1> ^ S[3] ^ S[8]

E[2] = T<2> ^ S[6] ^ S[16]

E[3] = T<3> ^ S[9] ^ S[14] ^ S[19] ^ S[24]

E[4] = T<4> ^ S[4] ^ S[6]

E[5] = T<5> ^ S[7] ^ S[9] ^ S[12] ^ S[14]

E[6] = T<6> ^ S[10] ^ S[12] ^ S[20] ^ S[22]

E[7] = T<7> ^ S[13] ^ S[15] ^ S[18] ^ S[20] ^ S[23] ^ S[25] ^ S[28] ^ S[30]

When not transmitting data, T<7:0> = 0

E[8] = { E[7], from code set n-1} ^ { E[6], from code set n-2} ^ { E[8], from code set n-3}

7.2.2 Data Symbol Mapping

Then E[8:0] is used in the following Tables to generate the code set, A and B:

S[3:0]	S[5:4]= 00 A1,B1	A2,B2	S[5:4]= 01 A1,B1	A2,B2	S[5:4]= 10 A1,B1	A2,B2	S [5:4]= 11 A1,B1	A2,B2
0000	0, 0	0, 0	+1,+1	+1,+1	+2, 0	0, 0	0,+2	0, 0
0001	-2, 0	0, 0	-1,+1	+1,+1	+2,-2	0, 0	-2,+2	0, 0
0010	0,-2	0, 0	+1,-1	+1,+1	+2, 0	-2, 0	0,+2	-2, 0
0011	-2,-2	0, 0	-1,-1	+1,+1	+2,-2	-2, 0	-2,+2	-2, 0
0100	0, 0	-2, 0	+1,+1	-1,+1	+2, 0	0,-2	0,+2	0,-2
0101	-2, 0	-2, 0	-1,+1	-1,+1	+2,-2	0,-2	-2,+2	0,-2
0110	0,-2	-2, 0	+1,-1	-1,+1	+2, 0	-2,-2	0,+2	-2,-2
0111	-2,-2	-2, 0	-1,-1	-1,+1	+2,-2	-2,-2	-2,+2	-2,-2
1000	0, 0	0,-2	+1,+1	+1,-1	0, 0	+2, 0	0, 0	0,+2
1001	-2, 0	0,-2	-1,+1	+1,-1	-2, 0	+2, 0	-2, 0	0,+2
1010	0,-2	0,-2	+1,-1	+1,-1	0,-2	+2, 0	0,-2	0,+2
1011	-2,-2	0,-2	-1,-1	+1,-1	-2,-2	+2, 0	-2,-2	0,+2
1100	0, 0	-2,-2	+1,+1	-1,-1	0, 0	+2,-2	0, 0	-2,+2
1101	-2, 0	-2,-2	-1,+1	-1,-1	-2, 0	+2,-2	-2, 0	-2,+2
1110	0,-2	-2,-2	+1,-1	-1,-1	0,-2	+2,-2	0,-2	-2,+2
1111	-2,-2	-2,-2	-1,-1	-1,-1	-2,-2	+2,-2	-2,-2	-2,+2

Table 7.1 Symbol Mapping for S[8:6]=[000]

S[3:0]	S[5:4]= 00 A1,B1	A2,B2	S[5:4]= 01 A1,B1	A2,B2	S[5:4]= 10 A1,B1	A2,B2	S [5:4]= 11 A1,B1	A2,B2
0000	0,+1	+1, 0	+1,0	0,+1	+2,+1	+1, 0	+1,+2	0,+1
0001	-2,+1	+1, 0	-1, 0	0,+1	+2,-1	+1, 0	-1,+2	0,+1
0010	0,-1	+1, 0	+1,-2	0,+1	+2,+1	-1, 0	+1,+2	-2,+1
0011	-2,-1	+1, 0	-1,-2	0,+1	+2,-1	-1, 0	-1,+2	-2,+1
0100	0,+1	-1, 0	+1, 0	-2,+1	+2,+1	+1,-2	+1,+2	0,-1
0101	-2,+1	-1, 0	-1, 0	-2,+1	+2,-1	+1,-2	-1,+2	0,-1
0110	0,-1	-1, 0	+1,-2	-2,+1	+2,+1	-1,-2	+1,+2	-2,-1
0111	-2,-1	-1, 0	-1,-2	-2,+1	+2,-1	-1,-2	-1,+2	-2,-1
1000	0,+1	+1,-2	+1, 0	0,-1	+1, 0	+2,+1	0,+1	+1,+2
1001	-2,+1	+1,-2	-1, 0	0,-1	-1, 0	+2,+1	-2,+1	+1,+2
1010	0,-1	+1,-2	+1,-2	0,-1	+1,-2	+2,+1	0,-1	+1,+2
1011	-2,-1	+1,-2	-1,-2	0,-1	-1,-2	+2,+1	-2,-1	+1,+2
1100	0,+1	-1,-2	+1, 0	-2,-1	+1, 0	+2,-1	0,+1	-1,+2
1101	-2,+1	-1,-2	-1, 0	-2,-1	-1, 0	+2,-1	-2,+1	-1,+2
1110	0,-1	-1,-2	+1,-2	-2,-1	+1,-2	+2,-1	0,-1	-1,+2
1111	-2,-1	-1,-2	-1,-2	-2,-1	-1,-2	+2,-1	-2,-1	-1,+2

Table 7.2 Symbol Mapping for S[8:6]=[001]

S[3:0]	S[5:4]= 00 A1,B1	A2,B2	S[5:4]= 01 A1,B1	A2,B2	S[5:4]= 10 A1,B1	A2,B2	S [5:4]= 11 A1,B1	A2,B2
0000	0, 0	+1,+1	+1,+1	0, 0	+2, 0	+1,+1	0,+2	+1,+1
0001	-2, 0	+1,+1	-1,+1	0, 0	+2,-2	+1,+1	-2,+2	+1,+1
0010	0,-2	+1,+1	+1,-1	0, 0	+2, 0	-1,+1	0,+2	-1,+1
0011	-2,-2	+1,+1	-1,-1	0, 0	+2,-2	-1,+1	-2,+2	-1,+1
0100	0, 0	-1,+1	+1,+1	-2, 0	+2, 0	+1,-1	0,+2	+1,-1
0101	-2, 0	-1,+1	-1,+1	-2, 0	+2,-2	+1,-1	-2,+2	+1,-1
0110	0,-2	-1,+1	+1,-1	-2, 0	+2, 0	-1,-1	0,+2	-1,-1
0111	-2,-2	-1,+1	-1,-1	-2, 0	+2,-2	-1,-1	-2,+2	-1,-1
1000	0, 0	+1,-1	+1,+1	0,-2	+1,+1	+2, 0	+1,+1	0,+2
1001	-2, 0	+1,-1	-1,+1	0,-2	-1,+1	+2, 0	-1,+1	0,+2
1010	0,-2	+1,-1	+1,-1	0,-2	+1,-1	+2, 0	+1,-1	0,+2
1011	-2,-2	+1,-1	-1,-1	0,-2	-1,-1	+2, 0	-1,-1	0,+2
1100	0, 0	-1,-1	+1,+1	-2,-2	+1,+1	+2,-2	+1,+1	-2,+2
1101	-2, 0	-1,-1	-1,+1	-2,-2	-1,+1	+2,-2	-1,+1	-2,+2
1110	0,-2	-1,-1	+1,-1	-2,-2	+1,-1	+2,-2	+1,-1	-2,+2
1111	-2,-2	-1,-1	-1,-1	-2,-2	-1,-1	+2,-2	-1,-1	-2,+2

Table 7.3 Symbol Mapping for S[8:6]=[010]

S[3:0]	S[5:4]= 00 A1,B1	A2,B2	S[5:4]= 01 A1,B1	A2,B2	S[5:4]= 10 A1,B1	A2,B2	S [5:4]= 11 A1,B1	A2,B2
0000	0,+1	0,+1	+1,0	+1, 0	+2,+1	0,+1	+1,+2	+1, 0
0001	-2,+1	0,+1	-1, 0	+1, 0	+2,-1	0,+1	-1,+2	+1, 0
0010	0,-1	0,+1	+1,-2	+1, 0	+2,+1	-2,+1	+1,+2	-1, 0
0011	-2,-1	0,+1	-1,-2	+1, 0	+2,-1	-2,+1	-1,+2	-1, 0
0100	0,+1	-2,+1	+1, 0	-1, 0	+2,+1	0,-1	+1,+2	+1,-2
0101	-2,+1	-2,+1	-1, 0	-1, 0	+2,-1	0,-1	-1,+2	+1,-2
0110	0,-1	-2,+1	+1,-2	-1, 0	+2,+1	-2,-1	+1,+2	-1,-2
0111	-2,-1	-2,+1	-1,-2	-1, 0	+2,-1	-2,-1	-1,+2	-1,-2
1000	0,+1	0,-1	+1, 0	+1,-2	0,+1	+2,+1	+1, 0	+1,+2
1001	-2,+1	0,-1	-1, 0	+1,-2	-2,+1	+2,+1	-1, 0	+1,+2
1010	0,-1	0,-1	+1,-2	+1,-2	0,-1	+2,+1	+1,-2	+1,+2
1011	-2,-1	0,-1	-1,-2	+1,-2	-2,-1	+2,+1	-1,-2	+1,+2
1100	0,+1	-2,-1	+1, 0	-1,-2	0,+1	+2,-1	+1, 0	-1,+2
1101	-2,+1	-2,-1	-1, 0	-1,-2	-2,+1	+2,-1	-1, 0	-1,+2
1110	0,-1	-2,-1	+1,-2	-1,-2	0,-1	+2,-1	+1,-2	-1,+2
1111	-2,-1	-2,-1	-1,-2	-1,-2	-2,-1	+2,-1	-1,-2	-1,+2

Table 7.4 Symbol Mapping for S[8:6]=[011]

S[3:0]	S[5:4]= 00 A1,B1	A2,B2	S[5:4]= 01 A1,B1	A2,B2	S[5:4]= 10 A1,B1	A2,B2	S [5:4]= 11 A1,B1	A2,B2
0000	0, 0	0,+1	+1,+1	+1, 0	+2, 0	0,+1	0,+2	0,+1
0001	-2, 0	0,+1	-1,+1	+1, 0	+2,-2	0,+1	-2,+2	0,+1
0010	0,-2	0,+1	+1,-1	+1, 0	+2, 0	-2,+1	0,+2	-2,+1
0011	-2,-2	0,+1	-1,-1	+1, 0	+2,-2	-2,+1	-2,+2	-2,+1
0100	0, 0	-2,+1	+1,+1	-1, 0	+2, 0	0,-1	0,+2	0,-1
0101	-2, 0	-2,+1	-1,+1	-1, 0	+2,-2	0,-1	-2,+2	0,-1
0110	0,-2	-2,+1	+1,-1	-1, 0	+2, 0	-2,-1	0,+2	-2,-1
0111	-2,-2	-2,+1	-1,-1	-1, 0	+2,-2	-2,-1	-2,+2	-2,-1
1000	0, 0	0,-1	+1,+1	+1,-2	0, 0	+2,+1	+1,+1	+1,+2
1001	-2, 0	0,-1	-1,+1	+1,-2	-2, 0	+2,+1	-1,+1	+1,+2
1010	0,-2	0,-1	+1,-1	+1,-2	0,-2	+2,+1	+1,-1	+1,+2
1011	-2,-2	0,-1	-1,-1	+1,-2	-2,-2	+2,+1	-1,-1	+1,+2
1100	0, 0	-2,-1	+1,+1	-1,-2	0, 0	+2,-1	+1,+1	-1,+2
1101	-2, 0	-2,-1	-1,+1	-1,-2	-2, 0	+2,-1	-1,+1	-1,+2
1110	0,-2	-2,-1	+1,-1	-1,-2	0,-2	+2,-1	+1,-1	-1,+2
1111	-2,-2	-2,-1	-1,-1	-1,-2	-2,-2	+2,-1	-1,-1	-1,+2

Table 7.5 Symbol Mapping for S[8:6]=[100]

S[3:0]	S[5:4]= 00 A1,B1	A2,B2	S[5:4]= 01 A1,B1	A2,B2	S[5:4]= 10 A1,B1	A2,B2	S [5:4]= 11 A1,B1	A2,B2
0000	0,+1	+1,+1	+1,0	0, 0	+2,+1	+1,+1	+1,+2	0, 0
0001	-2,+1	+1,+1	-1, 0	0, 0	+2,-1	+1,+1	-1,+2	0, 0
0010	0,-1	+1,+1	+1,-2	0, 0	+2,+1	-1,+1	+1,+2	-2, 0
0011	-2,-1	+1,+1	-1,-2	0, 0	+2,-1	-1,+1	-1,+2	-2, 0
0100	0,+1	-1,+1	+1, 0	-2, 0	+2,+1	+1,-1	+1,+2	0,-2
0101	-2,+1	-1,+1	-1, 0	-2, 0	+2,-1	+1,-1	-1,+2	0,-2
0110	0,-1	-1,+1	+1,-2	-2, 0	+2,+1	-1,-1	+1,+2	-2,-2
0111	-2,-1	-1,+1	-1,-2	-2, 0	+2,-1	-1,-1	-1,+2	-2,-2
1000	0,+1	+1,-1	+1, 0	0,-2	+1, 0	+2, 0	+1, 0	0,+2
1001	-2,+1	+1,-1	-1, 0	0,-2	-1, 0	+2, 0	-1, 0	0,+2
1010	0,-1	+1,-1	+1,-2	0,-2	+1,-2	+2, 0	+1,-2	0,+2
1011	-2,-1	+1,-1	-1,-2	0,-2	-1,-2	+2, 0	-1,-2	0,+2
1100	0,+1	-1,-1	+1, 0	-2,-2	+1, 0	+2,-2	+1, 0	-2,+2
1101	-2,+1	-1,-1	-1, 0	-2,-2	-1, 0	+2,-2	-1, 0	-2,+2
1110	0,-1	-1,-1	+1,-2	-2,-2	+1,-2	+2,-2	+1,-2	-2,+2
1111	-2,-1	-1,-1	-1,-2	-2,-2	-1,-2	+2,-2	-1,-2	-2,+2

Table 7.6 Symbol Mapping for S[8:6]=[101]

S[3:0]	S[5:4]= 00 A1,B1	A2,B2	S[5:4]= 01 A1,B1	A2,B2	S[5:4]= 10 A1,B1	A2,B2	S [5:4]= 11 A1,B1	A2,B2
0000	0, 0	+1, 0	+1,+1	0,+1	+2, 0	+1, 0	0,+2	+1, 0
0001	-2, 0	+1, 0	-1,+1	0,+1	+2,-2	+1, 0	-2,+2	+1, 0
0010	0,-2	+1, 0	+1,-1	0,+1	+2, 0	-1, 0	0,+2	-1, 0
0011	-2,-2	+1, 0	-1,-1	0,+1	+2,-2	-1, 0	-2,+2	-1, 0
0100	0, 0	-1, 0	+1,+1	-2,+1	+2, 0	+1,-2	0,+2	+1,-2
0101	-2, 0	-1, 0	-1,+1	-2,+1	+2,-2	+1,-2	-2,+2	+1,-2
0110	0,-2	-1, 0	+1,-1	-2,+1	+2, 0	-1,-2	0,+2	-1,-2
0111	-2,-2	-1, 0	-1,-1	-2,+1	+2,-2	-1,-2	-2,+2	-1,-2
1000	0, 0	+1,-2	+1,+1	0,-1	+1,+1	+2,+1	0, 0	+1,+2
1001	-2, 0	+1,-2	-1,+1	0,-1	-1,+1	+2,+1	-2, 0	+1,+2
1010	0,-2	+1,-2	+1,-1	0,-1	+1,-1	+2,+1	0,-2	+1,+2
1011	-2,-2	+1,-2	-1,-1	0,-1	-1,-1	+2,+1	-2,-2	+1,+2
1100	0, 0	-1,-2	+1,+1	-2,-1	+1,+1	+2,-1	0, 0	-1,+2
1101	-2, 0	-1,-2	-1,+1	-2,-1	-1,+1	+2,-1	-2, 0	-1,+2
1110	0,-2	-1,-2	+1,-1	-2,-1	+1,-1	+2,-1	0,-2	-1,+2
1111	-2,-2	-1,-2	-1,-1	-2,-1	-1,-1	+2,-1	-2,-2	-1,+2

Table 7.7 Symbol Mapping for S[8:6]=[110]

S[3:0]	S[5:4]= 00 A1,B1	A2,B2	S[5:4]= 01 A1,B1	A2,B2	S[5:4]= 10 A1,B1	A2,B2	S [5:4]= 11 A1,B1	A2,B2
0000	0,+1	0, 0	+1,0	+1,+1	+2,+1	0, 0	+1,+2	+1,+1
0001	-2,+1	0, 0	-1, 0	+1,+1	+2,-1	0, 0	-1,+2	+1,+1
0010	0,-1	0, 0	+1,-2	+1,+1	+2,+1	-2, 0	+1,+2	-1,+1
0011	-2,-1	0, 0	-1,-2	+1,+1	+2,-1	-2, 0	-1,+2	-1,+1
0100	0,+1	-2, 0	+1, 0	-1,+1	+2,+1	0,-2	+1,+2	+1,-1
0101	-2,+1	-2, 0	-1, 0	-1,+1	+2,-1	0,-2	-1,+2	+1,-1
0110	0,-1	-2, 0	+1,-2	-1,+1	+2,+1	-2,-2	+1,+2	-1,-1
0111	-2,-1	-2, 0	-1,-2	-1,+1	+2,-1	-2,-2	-1,+2	-1,-1
1000	0,+1	0,-2	+1, 0	+1,-1	0,+1	+2, 0	0,+1	0,+2
1001	-2,+1	0,-2	-1, 0	+1,-1	-2,+1	+2, 0	-2,+1	0,+2
1010	0,-1	0,-2	+1,-2	+1,-1	0,-1	+2, 0	0,-1	0,+2
1011	-2,-1	0,-2	-1,-2	+1,-1	-2,-1	+2, 0	-2,-1	0,+2
1100	0,+1	-2,-2	+1, 0	-1,-1	0,+1	+2,-2	0,+1	-2,+2
1101	-2,+1	-2,-2	-1, 0	-1,-1	-2,+1	+2,-2	-2,+1	-2,+2
1110	0,-1	-2,-2	+1,-2	-1,-1	0,-1	+2,-2	0,-1	-2,+2
1111	-2,-1	-2,-2	-1,-2	-1,-1	-2,-1	+2,-2	-2,-1	-2,+2

Table 7.8 Symbol Mapping for S[8:6]=[111]

7.2.3 Idle Mapping

S[3:0]	A1,B1	A2,B2
0000	0, 0	0, 0
0001	-2, 0	0, 0
0010	0,-2	0, 0
0011	-2,-2	0, 0
0100	0, 0	-2, 0
0101	-2, 0	-2, 0
0110	0,-2	-2, 0
0111	-2,-2	-2, 0
1000	0, 0	0,-2
1001	-2, 0	0,-2
1010	0,-2	0,-2
1011	-2,-2	0,-2
1100	0, 0	-2,-2
1101	-2, 0	-2,-2
1110	0,-2	-2,-2
1111	-2,-2	-2,-2

Table 7.9 Idle Symbol Mapping

7.2.4 Control Symbol Mapping

SYMBOL	A1,B1	A2,B2
SF	+2,+2	+2,+2
	+2,+2	+2,-2
EF	+2,+2	+2,+2
	+2,+2	+2,-2

Table 7.10 Start of Frame and End of Frame Mapping

Transmit Error	S[5:4]= 00 A1,B1	A2,B2	S[5:4]= 01 A1,B1	A2,B2	S[5:4]= 10 A1,B1	A2,B2	S [5:4]= 11 A1,B1	A2,B2
S[8]=0	0,+2	+2, 0	+1,+1	+2,+2	+2,+1	+1,+2	+2,+1	+2,+1
S[8]=1	+2,+2	0,+1	0,+2	+1,+2	+1,+2	+2, 0	+2,+1	+2, 0

Table 7.11 Transmit Error Mapping

8. SYMBOLS

The section defines the transmit and receive symbols.

8.1 Transmit Symbols

The symbols TA1 and TB1 are transmitted over transmit pairs TP1 and TP2 respectively at time t and TA2 and TB2 are transmitted over transmit pairs TP1 and TP2 respectively at time t+1; representing the transmission of a complete code set. The transmitted symbols (TA1, TB1, TA2, and TB2) are generated as the product of (A1, B1, A2, B2) and R[3:0]. R[3:0] is defined by:

R[0] = +1 if (S[1] ^ S[6] ^ 1 = 0) and transmitting IDLE or SF
or +1 if (S[1] ^ S[6] ^ 0 = 0)
-1 else

R[1] = +1 if (S[7] ^ S[9] ^ S[12] ^ S[14] ^ 1 = 0) and transmitting IDLE or SF
or +1 if (S[7] ^ S[9] ^ S[12] ^ S[14] ^ 0 = 0)
-1 else

R[2] = +1 if (S[7] ^ S[11] ^ S[17] ^ S[21] ^ 1 = 0) and transmitting IDLE or SF
or +1 if (S[7] ^ S[11] ^ S[17] ^ S[21] ^ 0 = 0)
-1 else

R[3] = +1 if (S[10] ^ S[14] ^ S[15] ^ S[19] ^ S[20] ^ S[24] ^ S[25] ^ S[29] ^ 1 = 0) and
transmitting IDLE or SF
or +1 if (S[10] ^ S[14] ^ S[15] ^ S[19] ^ S[20] ^ S[24] ^ S[25] ^ S[29] ^ 0 = 0)
-1 else

8.2 Receive Symbols

The 1000BASE-TX PHY shall use the same coding rules to decode the received data.

8.3 Timers

There are no required timers for transmit or receive operation.

8.4 Errors

The 1000BASE-TX PHY shall use the transmit Error code set to transmit an error when indicated by the TE signal from the MAC interface. Decoding errors or a received error code shall be indicated to the MAC with the interface RE signal.

8.5 PHY Control

After power up, a successful autonegotiation (See Clause 14), and the 1000BASE-TX PHY is transmitting and receiving IDLE's, normal operation begins.

9. TEST

A test mode shall be provided to allow for testing of the transmit waveform. Enabling the test mode is left to the implementer.

9.1 Tests

When the test mode is enabled the 1000BASE-TX PHY shall transmit the following sequence continuously: +2 followed by 127 0 symbols; -2 followed by 127 0 symbols; +1 followed by 127 0 symbols; -1 followed by 127 0 symbols; 128 +2 symbols; 128 -2 symbols; 128 +2 symbols; 128 –2 symbols; 1024 0 symbols.

9.2 Fixtures

To perform the test the 1000BASE-TX PHY shall terminate the transmission pair in 100 ohms while measuring the output waveform with a oscilloscope or data acquisition device with a high impedance differential probe.

10. TRANSMITTER SIGNAL

This section details the requirements for the transmitter output signal. The electrical requirements for any MDI port are defined in Section 11.

10.1 Differential Output Voltage and Accuracy

The peak voltage of the output waveform during the transmission of a single +2 and –2 symbol shall fall within the range of +/- (0.67 to 0.82 V), and during the transmission of a single +1 and –1 the absolute peak voltage shall differ by no more than 0.5 times the average of the +2 and –2 peak voltage, less 2%. The absolute value of the +/- peak voltage shall differ by no more that 1%.

10.2 Maximum Output Droop

The maximum output droop from a positive or negative peak voltage (with a continuous transmission of symbols) shall be less than 26.9% after 500 ns.

10.3 Output Voltage Templates

The output voltage waveform shall fall within the time domain templates of Figure 10.1 and 10.2 and Table 10.1 and 10.2 , using a piecewise linear interpolation between points in the table. The measured waveforms may be shifted in time as appropriate to fit within the template.

Note: Templates need to be changed.

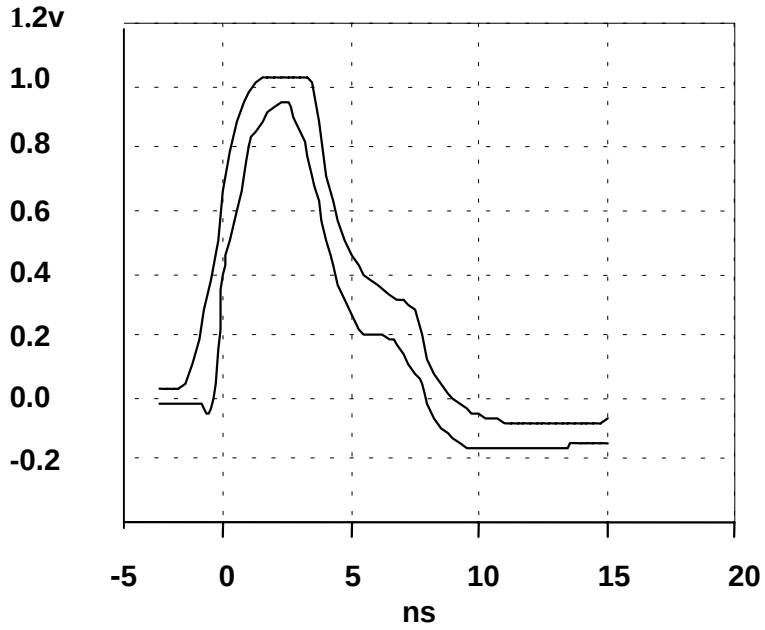

Figure 10.1 Peak Template

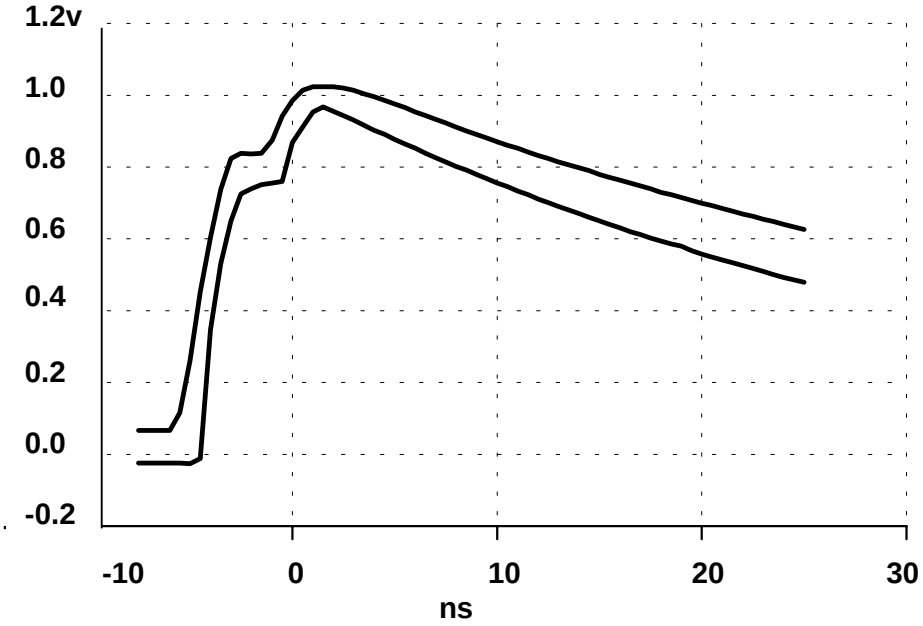

Figure 10.2 Droop Template

Time ns	Upper Limit V	Lower Limit V	Time ns	Upper Limit V	Lower Limit V
-2.50	0.025	-0.026	6.50	0.326	0.192
-2.25	0.025	-0.026	6.75	0.315	0.169
-2.00	0.025	-0.026	7.00	0.307	0.140
-1.75	0.025	-0.026	7.25	0.300	0.108
-1.5	0.050	-0.26	7.50	0.278	0.074
-1.25	0.110	-0.026	7.75	0.200	0.039
-1.00	0.190	-0.027	8.00	0.128	-0.023
-0.75	0.281	-0.028	8.25	0.083	-0.068
-0.50	0.378	-0.028	8.50	0.047	-0.098
-0.25	0.496	-0.152	8.75	0.019	-0.119
0.00	0.669	0.398	9.00	-0.004	-0.133
0.25	0.796	0.499	9.25	-0.022	-0.152
0.50	0.882	0.601	9.50	-0.037	-0.158
0.75	0.940	0.701	9.75	-0.048	-0.159
1.00	0.977	0.797	10.00	-0.053	-0.159
1.25	1.010	0.845	10.25	-0.064	-0.159
1.50	1.024	0.881	10.50	-0.070	-0.159
1.75	1.025	0.909	10.75	-0.074	-0.158
2.00	1.025	0.931	11.00	-0.077	-0.158
2.25	1.025	0.946	11.25	-0.079	-0.158
2.50	1.025	0.951	11.50	-0.079	-0.157
2.75	1.025	0.905	11.75	-0.080	-0.157
3.00	1.025	0.846	12.00	-0.080	-0.156
3.25	1.025	0.779	12.25	-0.080	-0.156
3.50	1.014	0.707	12.50	-0.080	-0.156
3.75	0.888	0.634	12.75	-0.080	-0.156
4.00	0.714	0.510	13.00	-0.079	-0.156
4.25	0.629	0.418	13.25	-0.079	-0.156
4.50	0.561	0.354	13.50	-0.079	-0.155
4.75	0.507	0.309	13.75	-0.078	-0.154
5.00	0.462	0.268	14.00	-0.077	-0.154
5.25	0.427	0.223	14.25	-0.077	-0.153
5.50	0.398	0.208	14.50	-0.076	-0.153
5.75	0.374	0.201	14.75	-0.076	-0.152
6.00	0.355	0.198	15.00	-0.075	-0.151

Table 10.1 Peak Template

Time ns	Upper Limit V	Lower Limit V	Time ns	Upper Limit V	Lower Limit V
-7.50	0.066	-0.025	9.00	0.891	0.779
-7.00	0.066	-0.025	9.50	0.881	0.767
-6.50	0.066	-0.025	10.00	0.871	0.756
-6.00	0.066	-0.025	10.50	0.861	0.745
-5.50	0.116	-0.025	11.00	0.852	0.734
-5.00	0.261	-0.027	11.50	0.842	0.723
-4.50	0.452	-0.013	12.00	0.833	0.712
-4.00	0.604	-0.347	12.50	0.824	0.701
-3.50	0.737	0.531	13.00	0.815	0.691
-3.00	0.825	0.651	13.50	0.806	0.680
-2.50	0.839	0.725	14.00	0.797	0.670
-2.00	0.837	0.739	14.50	0.789	0.660
-1.50	0.839	0.752	15.00	0.780	0.650
-1.00	0.875	0.755	15.50	0.772	0.641
-0.50	0.941	0.760	16.00	0.763	0.631
0.00	0.986	0.869	16.50	0.755	0.621
0.50	1.014	0.912	17.00	0.747	0.612
1.00	1.025	0.954	17.50	0.739	0.603
1.50	1.025	0.967	18.00	0.730	0.594
2.00	1.025	0.956	18.50	0.723	0.585
2.50	1.020	0.944	19.00	0.715	0.580
3.00	1.014	0.931	19.50	0.707	0.567
3.50	1.005	0.917	20.00	0.699	0.558
4.00	0.996	0.903	20.50	0.692	0.550
4.50	0.986	0.890	21.00	0.684	0.541
5.00	0.976	0.877	21.50	0.677	0.533
5.50	0.965	0.864	22.00	0.669	0.525
6.00	0.954	0.852	22.50	0.662	0.517
6.50	0.944	0.839	23.00	0.655	0.509
7.00	0.933	0.827	23.50	0.648	0.501
7.50	0.923	0.814	24.00	0.641	0.493
8.00	0.912	0.802	25.00	0.627	0.478
8.50	0.902	0.791			

Table 10.2 Droop Template

11. ELECTRICAL AND MECHANICAL REQUIREMENTS

The sections defines the electrical requirements of the 1000BASE-TX PHY.

11.1 Isolation

The 1000BASE-TX PHY shall be electrically isolated between the ports and the media leads as specified in Section 5.3.2 of IEC Publication 950 for RMS and DC voltage isolation and IEC Publication 60 for impulse isolation.

11.2 Clock Frequency

The symbol transmission rate shall be 250 MHz +/- 0.01% and the receiver shall properly receive incoming symbols within this clock frequency.

11.3 Receiver Common Mode Rejection

While receiving packets the 1000BASE-TX PHY shall maintain the required BER while a 25 V peak-to-peak square wave 500kHz signal is applied common through 148 ohms to the differential pins of each pair.

11.4 Transmitter Common Mode Output Voltage

While transmitting the peak-to-peak common mode voltage measured according to Figure 11.1 shall be –30dB less than the differential voltage measured for that pair.

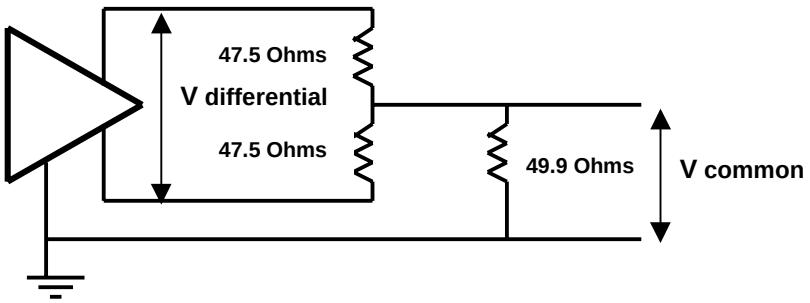

Figure 11.1 Common Mode Voltage Test

11.5 Input Tolerance

A 1000BASE-TX PHY transmitter or receiver shall withstand a short circuit across any pair for an indefinite period where the magnitude of the current through the short shall not exceed 300mA. In addition any pair shall withstand a common mode voltage of 1000 V as defined in IEC Publication 60.

11.6 Return Loss

The transmitter and receiver ports shall have a return loss better than 19 dB from 1.0 to 20 MHz, and at least 12 – 10log(f/100) dB from 20 to 250 MHz.

11.7 Connector

The media interface shall use an eight-pin connector defined in TIA/EIA-568-A and shall meet or exceed the Category 6 connector specifications. The pin assignment are shown in Table 11.1.

Contact	PHY	MDI	MDI w/crossover
1	TP1+	A+	B+
2	TP1 -	A-	B-
3	RP1+	B+	A+
4	TP2+	C+	D+
5	TP2 -	C-	D-
6	RP1 -	B-	A-
7	RP2+	D+	C+
8	RP2 -	D-	C-

Table 11.1 PHY/MDI Pin Out

11.8 Connector Configuration

If automatic configuration is implemented to eliminate the need for crossover cables, an automatic configuration method is described in IEEE std 802.3 Clause 40.8.3.

12. CABLING LINK

The cabling link shall meet or exceed the requirements specified in this clause. The cabling specified herein does meet, with the exceptions noted, the requirements for an ISO Class E and TIA Category 6 cabling channel as defined in ISO/IEC JTC1 SC25 WG3 and ANSI/EIA/TIA 568 Addendum 7 and constructed according to ANSI/EIA/TIA-568-B.

Alternate link configurations are possible if the cabling link still maintains a similar attenuation to crosstalk margin, see alternate cable plants, Annex A.

12.1 Attenuation Loss

The cabling link shall meet the attenuation loss specified in Table 12.1 when measured in accordance with ASTM D 4566. The link is defined as comprised of Category 6 components which are: 90 meters of horizontal cable, 10 meters of equipment cords or jumpers, and up to four connectors.

Frequency (MHz)	Attenuation (dB)
1.0	2.2
4.0	4.0
8.0	5.7
10.0	6.4
16.0	8.1
20.0	9.1
25.0	10.2
31.25	11.4
62.5	16.4
100.0	21.1
200.0	30.9
250.0	35.0

Table 12.1 Attenuation Loss

12.2 NEXT Loss

The cabling link shall meet the pair to pair NEXT Loss specified in Table 12.2 and a Power Sum NEXT Loss specified in Table 12.3 when measured in accordance ASTM D 4566.

Frequency (MHz)	NEXT (dB)
1.0	65.0
4.0	63.0
8.0	58.2
10.0	56.6
16.0	53.2
20.0	51.6
25.0	50.0
31.25	48.4
62.5	43.4
100.0	39.9
200.0	34.8
250.0	33.1

Table 12.2 Pair to Pair NEXT Loss

Frequency (MHz)	NEXT (dB)
1.0	65.0
4.0	60.6
8.0	55.6
10.0	54.0
16.0	50.6
20.0	49.0
25.0	47.4
31.25	45.7
62.5	40.6
100.0	37.1
200.0	31.9
250.0	30.2

Table 12.3 Power Sum NEXT Loss

12.3 ELFEXT Loss

The cabling link shall meet the pair to pair ELFEXT Loss specified in Table 12.4 when measured in accordance ASTM D 4566. Since transmission takes place on only two pairs ELFEXT Power Sum Loss is not required.

Frequency (MHz)	ELFEXT (dB)
1.0	63.2
4.0	51.2
8.0	45.2
10.0	43.2
16.0	39.1
20.0	37.2
25.0	35.3
31.25	33.3
62.5	27.3
100.0	23.2
200.0	17.2
250.0	15.3

Table 12.4 Pair to Pair ELFEXT Loss

12.4 Return Loss

The cabling link shall meet the Return Loss specified in Table 12.5 when measured in accordance ASTM D 4566. Since dual-duplex operation is not required the Return Loss limits have been relaxed to meet a Category 5e cabling link.

Frequency (MHz)	Return Loss (dB)
1<=f<20	17
20<=f<250	17-10log(f/20)

Table 12.5 Return Loss

12.5 Propagation Delay

The propagation delay of any pair measured in accordance with TIA/EIA-568-A-1 and ASTM D4566 shall meet equation (1) from 1 to 250MHz.

Equation (1):

$$delay(ns/100m) \leq 534 + \frac{36}{\sqrt{f_{MHz}}}$$

12.6 Propagation Delay Skew

The difference in propagation delay between the fastest and slowest pair in a cable shall not exceed 45 ns/100 m between 1 MHz and 250 MHz and the skew between all pair combinations shall not vary more than +/- 10 ns when measured in accordance with TIA/EIA-568-A-1 and ASTM D 4566.

12.7 External Noise

Noise may be coupled into the cabling link from external cabling or other sources of EMI. This noise shall not exceed 40 mv peak to peak.

13 ENVIORMENTAL

13.1 Safety

All equipment shall conform to IEC Publication 950

13.2 Grounding

Any safety grounding for the 1000BASE-TX PHY shall be provided through the PHY circuit ground.

13.3 Telephone Voltages

Building wiring may contain wiring errors that may result in connection to telephone circuits. The 1000BASE-TX PHY should be able to withstand a ringing voltage.

13.4 Susceptibility

When initially connecting to cabling links it is possible that a large static potential may exist on the cabling or connector. The 1000BASE-TX PHY media interface should provide protection from a potential static discharge.

13.5 Labeling

It is recommended that the 1000BASE-TX PHY should be labeled for its data rate, power consumption, port configuration, and any safety warnings.

14. MANAGEMENT AND AUTO-NEGOIATION

Providing a management interface or auto-negotiation is not required by this Standard. If implemented it is recommended that it should conform to the requirements specified in IEEE Std. 802.3 Clause 40 and its associated references.

14.1 Configuration

In order to distinguish between a 1000BASE-TX and IEEE std. 802.3 Clause 40 during autonegotiation, it is recommended that the 1000BASE-TX PHY configure itself as manual Master. At the completion of autonegotiation if the remote PHY is also a manual Master the 1000BASE-TX PHY should begin transmission. At this point the 1000BASE-TX PHY should be able to recognize the transmission from its link partner, if compatible. Otherwise restart autonegotiation and a lower ability should be assumed.

ANNEX A: ALTERNATE CABLE PLANT

The cabling link is specified for a maximum distance of 100 meters. Most studies have shown that over 90% of cabling links are 50 meters or less. In order to provide a migration path for users it is possible for cabling of lesser categories, Category 5 and Category 5e, to support the 1000BASE-TX PHY specified in this Standard at a data rate of 1000Mb/s for distances of at least 50 meters. At these distances the attenuation is approximately half that of 100 meters, this would offset the increased crosstalk. Although these lesser categories are not specified for frequencies over 100 MHz, it is expected that the characteristics will scale linearly. Figure A.1 illustrates the typical margin between the attenuation and NEXT for a ISO Class D (Category 5) 50 meter link and a Class E (Category 6) 100 meter link.

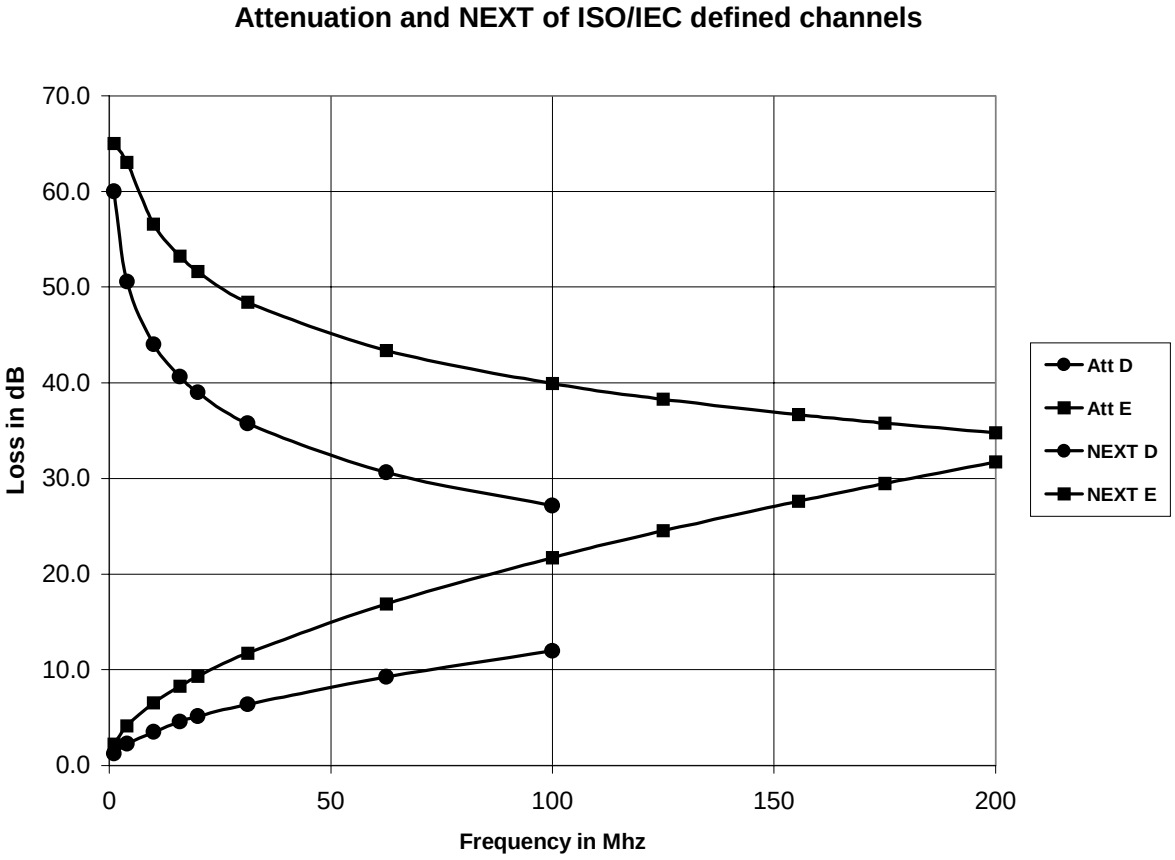

Figure A.1

A.1 Alternate Cabling Plant Requirements

The alternate cabling link shall meet or exceed the requirements specified in this Annex.

A.1.1 Attenuation Loss

The Cabling link shall meet the attenuation loss specified in Table A.1 when measured in accordance to ASTM D 4556. It is recommended that Category 6 equipment cords and patch cords should be used.

Note: Attenuation and NEXT are only an example.

Frequency (MHz)	Attenuation (dB)
1.0	1.1
4.0	2.2
8.0	3.2
10.0	3.6
16.0	4.6
20.0	5.1
25.0	5.7
31.25	6.6
62.5	9.3
100.0	12.0
200.0	22.0
250.0	26.3

Table A.1 Attenuation Loss

A.1.2 NEXT Loss

The cabling link shall meet the pair to pair NEXT Loss specified in Table A.2 and the Power Sum NEXT Loss specified in Table A.3 when measured in accordance to ASTM D 4556. It is recommended that Category 6 equipment cords and patch cords should be used.

Frequency (MHz)	NEXT (dB)
1.0	63.0
4.0	54.0
8.0	49.0
10.0	47.0
16.0	44.0
20.0	42.0
25.0	40.0
31.25	39.0
62.5	34.0
100.0	30.0
200.0	25.0
250.0	23.0

Table A.2 Pair to Pair NEXT Loss

Frequency (MHz)	NEXT (dB)
1.0	60.0
4.0	50.9
8.0	45.7
10.0	44.1
16.0	40.6
20.0	39.0
25.0	37.3
31.25	35.7
62.5	30.6
100.0	27.1
200.0	22.0
250.0	20.3

Table A.3 Power Sum NEXT Loss

A.1.3 Other Requirements

The cabling link shall meet the requirements specified in Clause 12.3, 12.4, 12.5, 12.6, and 12.7 of this Standard. The ELFEXT requirements for Category 5 and 5e at the lower attenuation should meet the requirements specified in 12.3 and return loss in 12.4 is already relaxed.

A.2 Implementation

It is recommended that the 1000BASE-TX PHY should attempt operation over the attached cabling. Successful operation at the specified bit error rate will indicate that the cabling link could support the data rate.

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