AMD Athlon™ XP Processor Model 10 Data Sheet

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Table of Contents

Revision History xi

1 Overview 1

1.1 QuantiSpeed™ Architecture Summary. 2

2 Interface Signals 5

2.1 Overview 5
2.2 Signaling Technology 5
2.3 Push-Pull (PP) Drivers 6
2.4 AMD Athlon™ System Bus Signals 6

3 Logic Symbol Diagram 7

4 Power Management 9

4.1 Power Management States 9
  Working State. 10
  Halt State 10
  Stop Grant States. 10
  Probe State. 12
4.2 Connect and Disconnect Protocol 12
  Connect Protocol 12
  Connect State Diagram 16
4.3 Clock Control 18

5 CPUID Support 19

6 AMD Athlon™ XP Processor Model 10 Electrical and Thermal Specifications 21

7 Electrical Data 23

7.1 Conventions 23
7.2 Interface Signal Groupings 23
7.3 Voltage Identification (VID[4:0]) 25
7.4 Frequency Identification (FID[3:0]) 25
7.5 VCCA AC and DC Characteristics. 25
7.6 Decoupling 26
7.7 V_{CC_CORE} Characteristics. 26
7.8 Absolute Ratings 28
7.9 SYSCLK and SYSCLK# AC and DC Characteristics 29
7.10 AMD Athlon System Bus AC and DC Characteristics 31
7.11 General AC and DC Characteristics 33
7.12 Open Drain Test Circuit 35
7.13 Thermal Diode Characteristics 36
  Thermal Diode Electrical Characteristics. 36
  Thermal Protection Characterization 37
7.14 APIC Pins AC and DC Characteristics 38

8 Signal and Power-Up Requirements 39
8.1 Power-Up Requirements 39
Signal Sequence and Timing Description 39
Clock Multiplier Selection (FID[3:0]) 42
8.2 Processor Warm Reset Requirements. 42
Northbridge Reset Pins. 42
9 Mechanical Data. 43
9.1 Introduction 43
9.2 Die Loading 43
9.3 AMD Athlon XP Processor Model 10 OPGA Package Dimensions. 44
10 Pin Descriptions 47
10.1 Pin Diagram and Pin Name Abbreviations. 47
10.2 Pin List 57
10.3 Detailed Pin Descriptions. 65
A20M# Pin 65
AMD Pin 65
AMD Athlon System Bus Pins 65
Analog Pin 65
APIC Pins, PICCLK, PICD[1:0]# 65
CLKFWDRST Pin 65
CLKIN, RSTCLK (SYSCLK) Pins. 65
CONNECT Pin 66
COREFB and COREFB# Pins. 66
CPU_PRESENCE# Pin 66
DBRDY and DBREQ# Pins 66
FERR Pin 66
FID[3:0] Pins 67
FSB_Sense[1:0] Pins 68
FLUSH# Pin. 68
IGNNE# Pin 68
INIT# Pin 68
INTR Pin. 68
JTAG Pins. 69
K7CLKOUT and K7CLKOUT# Pins. 69
Key Pins 69
NC Pins 69
NMI Pin. 69
PGA Orientation Pins 69
PLL Bypass and Test Pins. 69
PWROK Pin 69
SADDIN[1:0]# and SADDOUT[1:0]# Pins. 70
Scan Pins 70
SMI# Pin. 70
STPCLK# Pin 70

SYSCLK and SYSCLK# 70
THERMDA and THERMDC Pins 70
VCCA Pin 70
VID[4:0] Pins 70
VREFSYS Pin 71
ZN and ZP Pins 71

11 Ordering Information. 73

Standard AMD Athlon XP Processor Model 10 Products 73

Appendix A Thermal Diode Calculations 75

Ideal Diode Equation 75
Temperature Offset Correction 76

Appendix B Conventions and Abbreviations 79

Signals and Bits 79
Data Terminology 80
Abbreviations and Acronyms. 81

List of Figures

Figure 1. Typical AMD Athlon™ XP Processor Model 10 System Block Diagram 3
Figure 2. Logic Symbol Diagram. 7
Figure 3. AMD Athlon XP Processor Model 10 Power Management States 9
Figure 4. AMD Athlon System Bus Disconnect Sequence in the Stop Grant State 14
Figure 5. Exiting the Stop Grant State and Bus Connect Sequence 15
Figure 6. Northbridge Connect State Diagram 16
Figure 7. Processor Connect State Diagram 17
Figure 8. V_{CC_CORE} Voltage Waveform 27
Figure 9. SYSCLK and SYSCLK# Differential Clock Signals 29
Figure 10. SYSCLK Waveform 30
Figure 11. General ATE Open-Drain Test Circuit. 35
Figure 12. Signal Relationship Requirements During Power-Up Sequence 39
Figure 13. AMD Athlon XP Processor Model 10 OPGA Package 45
Figure 14. AMD Athlon XP Processor Model 10 Pin Diagram —Topside View. 48
Figure 15. AMD Athlon XP Processor Model 10 Pin Diagram —Bottomside View 49
Figure 16. OPN Example for the AMD Athlon XP Processor Model 10 73

List of Tables

Table 1. Electrical and Thermal Specifications for the AMD Athlon™ XP Processor Model 10 21
Table 2. Interface Signal Groupings 23
Table 3. VID[4:0] DC Characteristics 25
Table 4. FID[3:0] DC Characteristics 25
Table 5. VCCA AC and DC Characteristics 25
Table 6. V_{CC_CORE} AC and DC Characteristics 26
Table 7. Absolute Ratings 28
Table 8. SYSCLK and SYSCLK# DC Characteristics 29
Table 9. SYSCLK and SYSCLK# AC Characteristics for the AMD Athlon XP Processor Model 10. 30
Table 10. AMD Athlon System Bus DC Characteristics 31
Table 11. AMD Athlon System Bus AC Characteristics 32
Table 12. General AC and DC Characteristics. 33
Table 13. Thermal Diode Electrical Characteristics 36
Table 14. Guidelines for Platform Thermal Protection of the Processor 38
Table 15. APIC Pin AC and DC Characteristics. 38
Table 16. Mechanical Loading. 43
Table 17. Dimensions for the AMD Athlon XP Processor Model 10 OPGA Package. 44
Table 18. Pin Name Abbreviations 50
Table 19. Cross-Reference by Pin Location 58
Table 20. FID[3:0] Clock Multiplier Encodings 67
Table 21. Front Side Bus Sense Truth Table 68
Table 22. VID[4:0] Code to Voltage Definition 71
Table 23. Constants and Variables for the Ideal Diode Equation 75
Table 24. Constants and Variables Used in Temperature Offset Equations 76
Table 25. Abbreviations 81
Table 26. Acronyms. 82

Revision History

Date	Rev	Description
February 2003	B	Initial public release of the *AMD Athlon™ XP Processor Model 10 Data Sheet*

1 Overview

The AMD Athlon™ XP processor model 10 with QuantiSpeed™ architecture powers the next generation in computing platforms, delivering extreme performance for Windows® XP.

The AMD Athlon™ XP processor model 10, based on leading-edge 0.13 micron technology and increased on-chip cache, integrates the innovative design and manufacturing expertise of AMD to deliver improved performance while maintaining the stable and compatible Socket A infrastructure of the AMD Athlon processor.

Delivered in an OPGA package, the AMD Athlon XP processor model 10 delivers the integer, floating-point, and 3D multimedia performance for highly demanding applications running on x86 system platforms. The AMD Athlon XP processor model 10 delivers compelling performance for cutting-edge software applications that include high-speed Internet capability, digital content creation, digital photo editing, digital video, image compression, video encoding for streaming over the Internet, soft DVD, commercial 3D modeling, workstation-class computer-aided design (CAD), commercial desktop publishing, and speech recognition. The AMD Athlon XP processor model 10 also offers the scalability and reliability that IT managers and business users require for enterprise computing.

The AMD Athlon XP processor model 10 features a seventh-generation microarchitecture with an integrated, exclusive L2 cache, which supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The high-speed execution core of the AMD Athlon XP processor model 10 includes multiple x86 instruction decoders, a dual-ported 128-Kbyte split level-one (L1) cache, an exclusive 512-Kbyte L2 cache, three independent integer pipelines, three address calculation pipelines, and a superscalar, fully pipelined, out-of-order, three-way floating-point engine. The floating-point engine is capable of delivering outstanding performance on numerically complex applications.

The features of the AMD Athlon XP processor model 10 are QuantiSpeed™ architecture, 640 Kbytes of total, high-performance, full-speed, on-chip cache, an Advanced 333 Front-Side Bus, 2.7-Gigabyte per second AMD Athlon system bus, and 3DNow!™ Professional technology. The AMD Athlon system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling to provide an extremely powerful, scalable bus for an x86 processor.

The AMD Athlon XP processor model 10 is binary-compatible with existing x86 software and backwards compatible with applications optimized for MMX™, SSE, and 3DNow! technology. Using a data format and single-instruction multiple-data (SIMD) operations based on the MMX instruction model, the AMD Athlon XP processor model 10 can produce as many as four, 32-bit, single-precision floating-point results per clock cycle. The 3DNow! Professional technology implemented in the AMD Athlon XP processor model 10 includes new integer multimedia instructions and software-directed data movement instructions for optimizing such applications as digital content creation and streaming video for the internet, as well as new instructions for digital signal processing (DSP) and communications applications.

1.1 QuantiSpeed™ Architecture Summary

The following features summarize the AMD Athlon XP processor model 10 QuantiSpeed architecture:

- An advanced nine-issue, superpipelined, superscalar x86 processor microarchitecture designed for increased instructions per cycle (IPC) and high clock frequencies
- Fully pipelined floating-point unit that executes all x87 (floating-point), MMX, SSE and 3DNow! instructions
- Hardware data pre-fetch that increases and optimizes performance on high-end software applications utilizing high-bandwidth system capabilities
- Advanced two-level translation look-aside buffer (TLB) structures for both enhanced data and instruction address translation. The AMD Athlon XP processor model 10 with QuantiSpeed architecture incorporates three TLB optimizations: the L1 DTLB increases from 32 to 40 entries, the L2 ITLB and L2 DTLB both use exclusive architecture, and the TLB entries can be speculatively loaded.

The AMD Athlon XP processor model 10 delivers excellent system performance in a cost-effective, industry-standard form factor. The AMD Athlon XP processor model 10 is compatible with motherboards based on Socket A.

Figure 1 shows a typical AMD Athlon XP processor model 10 system block diagram.

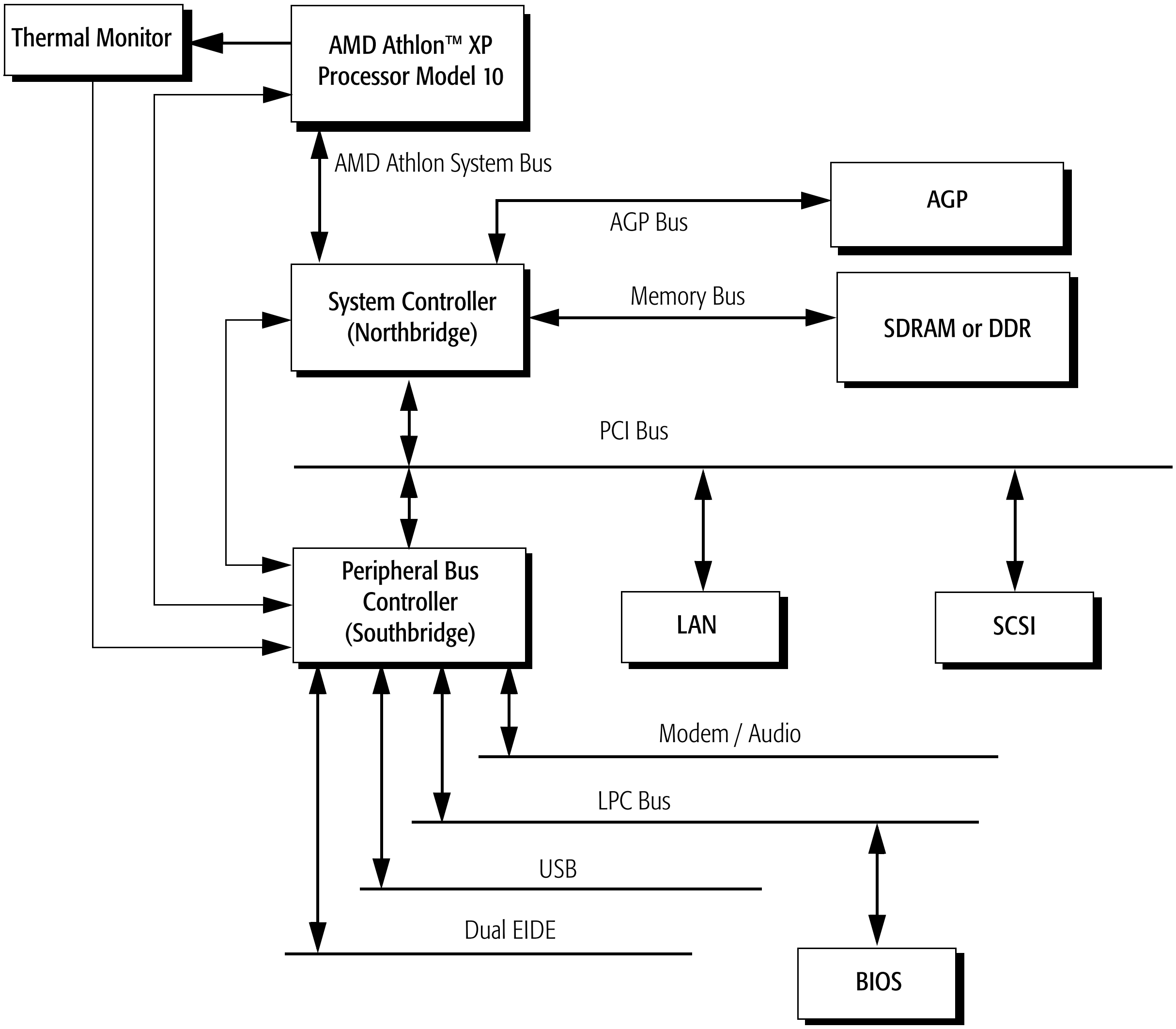


Figure 1. Typical AMD Athlon™ XP Processor Model 10 System Block Diagram

2 Interface Signals

This section describes the interface signals utilized by the AMD Athlon™ XP processor model 10.

2.1 Overview

The AMD Athlon™ system bus architecture is designed to deliver excellent data movement bandwidth for next-generation x86 platforms as well as the high-performance required by enterprise-class application software. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional probe channel, and a 64-bit bidirectional data channel), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use an impedance controlled push-pull, low-voltage, swing-signaling technology contained within the Socket A socket.

For more information, see “AMD Athlon™ System Bus Signals” on page 6, Chapter 10, “Pin Descriptions” on page 47, and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

2.2 Signaling Technology

The AMD Athlon system bus uses a low-voltage, swing-signaling technology, that has been enhanced to provide larger noise margins, reduced ringing, and variable voltage levels. The signals are push-pull and impedance compensated. The signal inputs use differential receivers that require a reference voltage (V_{REF}). The reference signal is used by the receivers to determine if a signal is asserted or deasserted by the source. Termination resistors are not needed because the driver is impedance-matched to the motherboard and a high impedance reflection is used at the receiver to bring the signal past the input threshold.

For more information about pins and signals, see Chapter 10, “Pin Descriptions” on page 47.

2.3 Push-Pull (PP) Drivers

The AMD Athlon XP processor model 10 supports push-pull (PP) drivers. The system logic configures the processor with the configuration parameter called SysPushPull (1=PP). The impedance of the PP drivers is set to match the impedance of the motherboard by two external resistors connected to the ZN and ZP pins.

See "ZN and ZP Pins" on page 71 for more information.

2.4 AMD Athlon™ System Bus Signals

The AMD Athlon system bus is a clock-forwarded, point-to-point interface with the following three point-to-point channels:

- A 13-bit unidirectional output address/command channel
- A 13-bit unidirectional input address/command channel
- A 72-bit bidirectional data channel

For more information, see Chapter 7, "Electrical Data" on page 23 and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

3 Logic Symbol Diagram

Figure 2 is the logic symbol diagram of the processor. This diagram shows the logical grouping of the input and output signals.

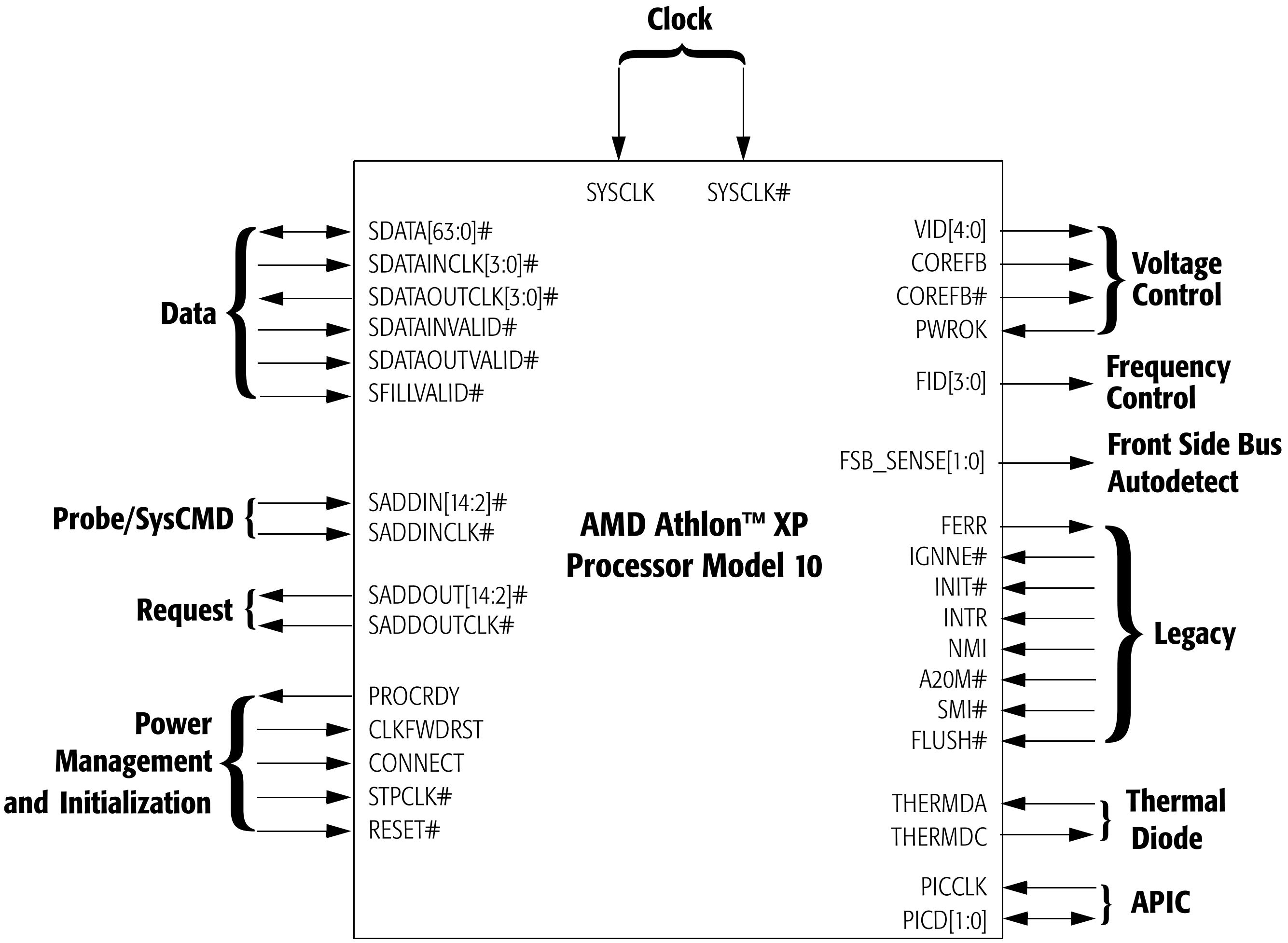


Figure 2. Logic Symbol Diagram

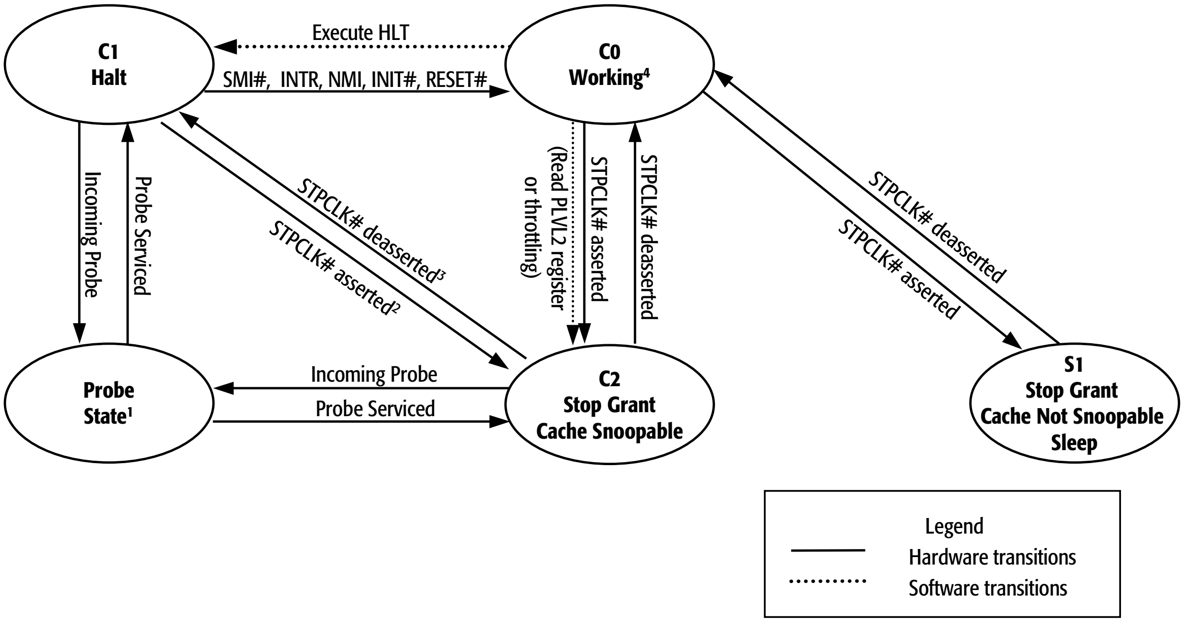
4 Power Management

This chapter describes the power management control system of the AMD Athlon™ XP processor model 10. The power management features of the processor are compliant with the ACPI 1.0b and ACPI 2.0 specifications.

4.1 Power Management States

The AMD Athlon XP processor model 10 supports low-power Halt and Stop Grant states. These states are used by advanced configuration and power interface (ACPI) enabled operating systems for processor power management.

Figure 3 shows the power management states of the processor. The figure includes the ACPI "Cx" naming convention for these states.



Note: The AMD Athlon™ System Bus is connected during the following states:

1) The Probe state
2) During transitions between the Halt state and the C2 Stop Grant state
3) During transitions between the C2 Stop Grant state and the Halt state
4) C0 Working state

Figure 3. AMD Athlon™ XP Processor Model 10 Power Management States

The following sections provide an overview of the power management states. For more details, refer to the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

Note: *In all power management states that the processor is powered, the system must not stop the system clock (SYSCLK/SYSCLK#) to the processor.*

Working State

The Working state is the state in which the processor is executing instructions.

Halt State

When the processor executes the HLT instruction, the processor enters the Halt state and issues a Halt special cycle to the AMD Athlon system bus. The processor only enters the low power state dictated by the CLK_Ctl MSR if the system controller (Northbridge) disconnects the AMD Athlon system bus in response to the Halt special cycle.

If STPCLK# is asserted, the processor will exit the Halt state and enter the Stop Grant state. The processor will initiate a system bus connect, if it is disconnected, then issue a Stop Grant special cycle. When STPCLK# is deasserted, the processor will exit the Stop Grant state and re-enter the Halt state. The processor will issue a Halt special cycle when re-entering the Halt state.

The Halt state is exited when the processor detects the assertion of INIT#, RESET#, SMI#, or an interrupt via the INTR or NMI pins, or via a local APIC interrupt message. When the Halt state is exited, the processor will initiate an AMD Athlon system bus connect if it is disconnected.

Stop Grant States

The processor enters the Stop Grant state upon recognition of assertion of STPCLK# input. After entering the Stop Grant state, the processor issues a Stop Grant special bus cycle on the AMD Athlon system bus. The processor is not in a low-power state at this time, because the AMD Athlon system bus is still connected. After the Northbridge disconnects the AMD Athlon system bus in response to the Stop Grant special bus cycle, the processor enters a low-power state dictated by the CLK_Ctl MSR. If the Northbridge needs to probe the processor during the Stop Grant state while the system bus is disconnected, it must first connect the system bus. Connecting the system bus places the processor into the higher power probe state. After the Northbridge has completed all probes of the processor, the Northbridge must disconnect the AMD Athlon system bus again so that the processor can return to the low-power state. During the Stop Grant states, the processor latches INIT#, INTR, NMI, SMI#, or a local APIC interrupt message, if they are asserted.

The Stop Grant state is exited upon the deassertion of STPCLK# or the assertion of RESET#. When STPCLK# is deasserted, the processor initiates a connect of the AMD Athlon system bus if it is disconnected. After the processor enters the Working state, any pending interrupts are recognized and serviced and the processor resumes execution at the instruction boundary where STPCLK# was initially recognized. If RESET# is sampled asserted during the Stop Grant state, the processor exits the Stop Grant state and the reset process begins.

There are two mechanisms for asserting STPCLK#—hardware and software.

The Southbridge can force STPCLK# assertion for throttling to protect the processor from exceeding its maximum case temperature. This is accomplished by asserting the THERM# input to the Southbridge. Throttling asserts STPCLK# for a percentage of a predefined throttling period: STPCLK# is repetitively asserted and deasserted until THERM# is deasserted.

Software can force the processor into the Stop Grant state by accessing ACPI-defined registers typically located in the Southbridge.

The operating system places the processor into the C2 Stop Grant state by reading the P_LVL2 register in the Southbridge.

If an ACPI Thermal Zone is defined for the processor, the operating system can initiate throttling with STPCLK# using the ACPI defined P_CNT register in the Southbridge. The Northbridge connects the AMD Athlon system bus, and the processor enters the Probe state to service cache snoops during Stop Grant for C2 or throttling.

In C2, probes are allowed, as shown in Figure 3 on page 9

The Stop Grant state is also entered for the S1, Powered On Suspend, system sleep state based on a write to the SLP_TYP and SLP_EN fields in the ACPI-defined Power Management 1 control register in the Southbridge. During the S1 Sleep state, system software ensures no bus master or probe activity occurs. The Southbridge deasserts STPCLK# and brings the processor out of the S1 Stop Grant state when any enabled resume event occurs.

Probe State

The Probe state is entered when the Northbridge connects the AMD Athlon system bus to probe the processor (for example, to snoop the processor caches) when the processor is in the Halt or Stop Grant state. When in the Probe state, the processor responds to a probe cycle in the same manner as when it is in the Working state. When the probe has been serviced, the processor returns to the same state as when it entered the Probe state (Halt or Stop Grant state). When probe activity is completed the processor only returns to a low-power state after the Northbridge disconnects the AMD Athlon system bus again.

4.2 Connect and Disconnect Protocol

Significant power savings of the processor only occur if the processor is disconnected from the system bus by the Northbridge while in the Halt or Stop Grant state. The Northbridge can optionally initiate a bus disconnect upon the receipt of a Halt or Stop Grant special cycle. The option of disconnecting is controlled by an enable bit in the Northbridge. If the Northbridge requires the processor to service a probe after the system bus has been disconnected, it must first initiate a system bus connect.

Connect Protocol

In addition to the legacy STPCLK# signal and the Halt and Stop Grant special cycles, the AMD Athlon system bus connect protocol includes the CONNECT, PROCRDY, and CLKFWDRST signals and a Connect special cycle.

AMD Athlon system bus disconnects are initiated by the Northbridge in response to the receipt of a Halt or Stop Grant. Reconnect is initiated by the processor in response to an interrupt for Halt or STPCLK# deassertion. Reconnect is initiated by the Northbridge to probe the processor.

The Northbridge contains BIOS programmable registers to enable the system bus disconnect in response to Halt and Stop Grant special cycles. When the Northbridge receives the Halt or Stop Grant special cycle from the processor and, if there are no outstanding probes or data movements, the Northbridge deasserts CONNECT a minimum of eight SYSCLK periods after the last command sent to the processor. The processor detects the deassertion of CONNECT on a rising edge of SYSCLK and deasserts PROCRDY to the Northbridge. In return, the Northbridge asserts CLKFWDRST in anticipation of reestablishing a connection at some later point.

Note: *The Northbridge must disconnect the processor from the AMD Athlon system bus before issuing the Stop Grant special cycle to the PCI bus or passing the Stop Grant special cycle to the Southbridge for systems that connect to the Southbridge with HyperTransport™ technology.*

This note applies to current chipset implementation—alternate chipset implementations that do not require this are possible.

Note: *In response to Halt special cycles, the Northbridge passes the Halt special cycle to the PCI bus or Southbridge immediately.*

The processor can receive an interrupt after it sends a Halt special cycle, or STPCLK# deassertion after it sends a Stop Grant special cycle to the Northbridge but before the disconnect actually occurs. In this case, the processor sends the Connect special cycle to the Northbridge, rather than continuing with the disconnect sequence. In response to the Connect special cycle, the Northbridge cancels the disconnect request.

The system is required to assert the CONNECT signal before returning the C-bit for the connect special cycle (assuming CONNECT has been deasserted).

For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for the definition of the C-bit and the Connect special cycle.

Figure 4 shows STPCLK# assertion resulting in the processor in the Stop Grant state and the AMD Athlon system bus disconnected.

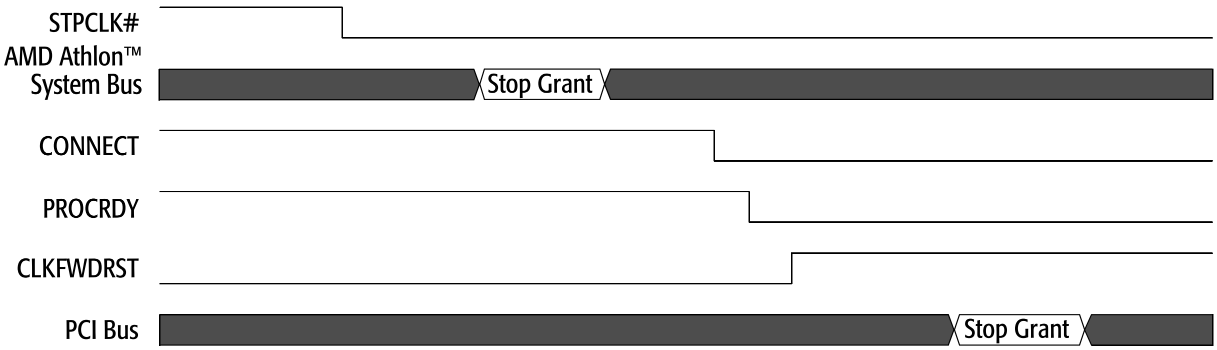


Figure 4. AMD Athlon™ System Bus Disconnect Sequence in the Stop Grant State

An example of the AMD Athlon system bus disconnect sequence is as follows:

1. The peripheral controller (Southbridge) asserts STPCLK# to place the processor in the Stop Grant state.
2. When the processor recognizes STPCLK# asserted, it enters the Stop Grant state and then issues a Stop Grant special cycle.
3. When the special cycle is received by the Northbridge, it deasserts CONNECT, assuming no probes are pending, initiating a bus disconnect to the processor.
4. The processor responds to the Northbridge by deasserting PROCRDY.
5. The Northbridge asserts CLKFWDRST to complete the bus disconnect sequence.
6. After the processor is disconnected from the bus, the processor enters a low-power state. The Northbridge passes the Stop Grant special cycle along to the Southbridge.

Figure 5 shows the signal sequence of events that takes the processor out of the Stop Grant state, connects the processor to the AMD Athlon system bus, and puts the processor into the Working state.

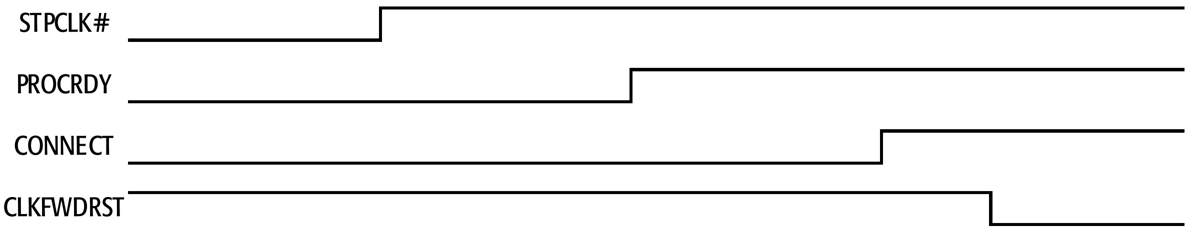


Figure 5. Exiting the Stop Grant State and Bus Connect Sequence

The following sequence of events removes the processor from the Stop Grant state and connects it to the system bus:

1. The Southbridge deasserts STPCLK#, informing the processor of a wake event.

2. When the processor recognizes STPCLK# deassertion, it exits the low-power state and asserts PROCRDY, notifying the Northbridge to connect to the bus.

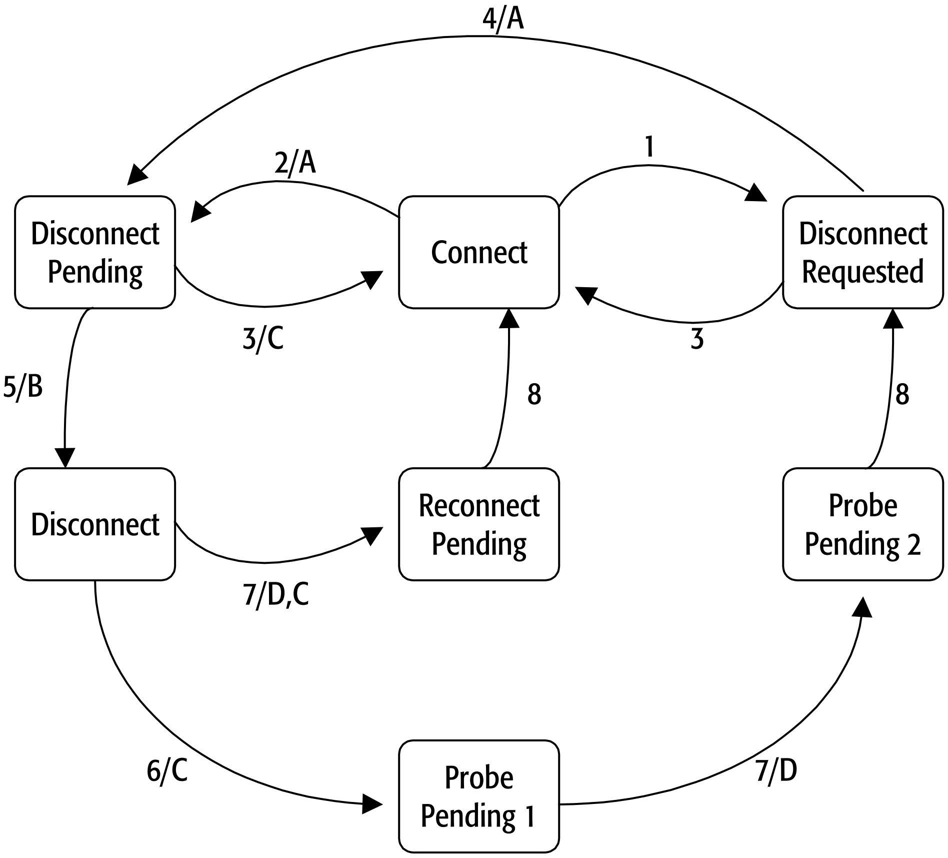
3. The Northbridge asserts CONNECT.

4. The Northbridge deasserts CLKFWDRST, synchronizing the forwarded clocks between the processor and the Northbridge.

5. The processor issues a Connect special cycle on the system bus and resumes operating system and application code execution.

Connect State Diagram

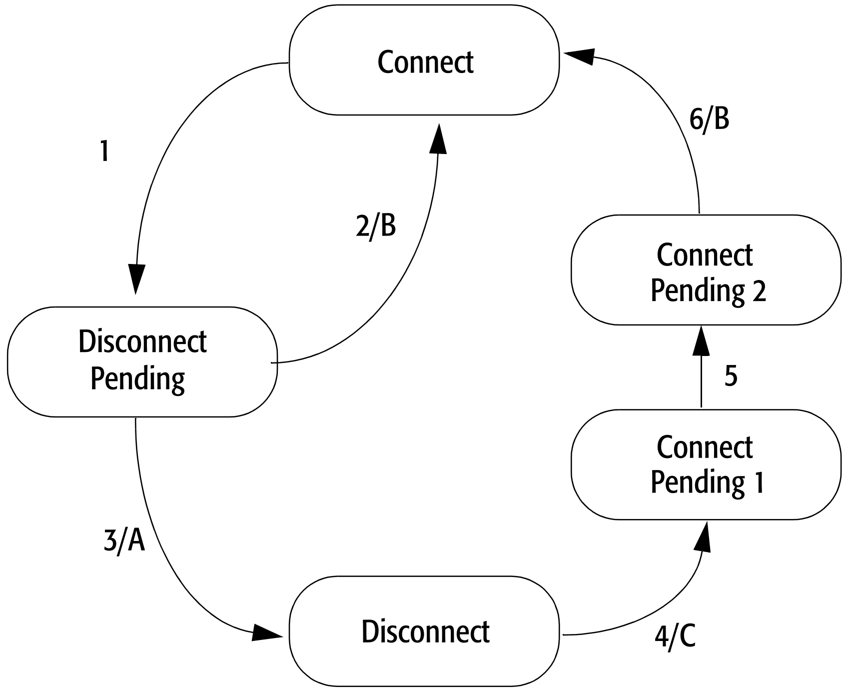
Figure 6 below and Figure 7 on page 17 show the Northbridge and processor connect state diagrams, respectively.



	Condition
1	A disconnect is requested and probes are still pending.
2	A disconnect is requested and no probes are pending.
3	A Connect special cycle from the processor.
4	No probes are pending.
5	PROCRDY is deasserted.
6	A probe needs service.
7	PROCRDY is asserted.
8	Three SYSCLK periods after CLKFWDRST is deasserted. *Although reconnected to the system interface, the Northbridge must not issue any non-NOP SysDC commands for a minimum of four SYSCLK periods after deasserting CLKFWDRST.*

	Action
A	Deassert CONNECT eight SYSCLK periods after last SysDC sent.
B	Assert CLKFWDRST.
C	Assert CONNECT.
D	Deassert CLKFWDRST.

Figure 6. Northbridge Connect State Diagram



	Condition
1	CONNECT is deasserted by the Northbridge (for a previously sent Halt or Stop Grant special cycle).
2	Processor receives a wake-up event and must cancel the disconnect request.
3	Deassert PROCRDY and slow down internal clocks.
4	Processor wake-up event or CONNECT asserted by Northbridge.
5	CLKFWDRST is deasserted by the Northbridge.
6	Forward clocks start three SYSCLK periods after CLKFWDRST is deasserted.

	Action
A	CLKFWDRST is asserted by the Northbridge.
B	Issue a Connect special cycle.*
C	Return internal clocks to full speed and assert PROCRDY.

Note:

* *The Connect special cycle is only issued after a processor wake-up event (interrupt or STPCLK# deassertion) occurs. If the AMD Athlon™ system bus is connected so the Northbridge can probe the processor, a Connect special cycle is not issued at that time (it is only issued after a subsequent processor wake-up event).*

Figure 7. Processor Connect State Diagram

4.3 Clock Control

The processor implements a Clock Control (CLK_Ctl) MSR (address C001_001Bh) that determines the internal clock divisor when the AMD Athlon system bus is disconnected.

Refer to the *AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656, for more details on the CLK_Ctl register.

5 CPUID Support

AMD Athlon™ XP processor model 10 version and feature set recognition can be performed through the use of the CPUID instruction, that provides complete information about the processor—vendor, type, name, etc., and its capabilities. Software can make use of this information to accurately tune the system for maximum performance and benefit to users.

For information on the use of the CPUID instruction see the following documents:

- *AMD Processor Recognition Application Note*, order# 20734
- *AMD Athlon™ Processor Recognition Application Note Addendum*, order# 21922
- *AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide,* order# 21656

6 AMD Athlon™ XP Processor Model 10 Electrical and Thermal Specifications

This chapter provides the electrical and thermal specifications for the AMD Athlon™ XP processor model 10.

Table 1 shows the electrical and thermal specifications in the C0 working state and the S1 Stop Grant state for the AMD Athlon XP processor model 10

Table 1. Electrical and Thermal Specifications for the AMD Athlon™ XP Processor Model 10

Frequency in MHz (Model Number)	V_{CC_CORE} (Core Voltage)	I_{CC} (Processor Current)				Thermal Power[5]		Maximum Die Temperature
		Working State C0		Stop Grant S1[1, 2, 3, 4]				
		Maximum	Typical	Maximum	Typical	Maximum	Typical	
1833 (2500+)	1.65 V	41.4 A	32.5 A	12.1 A	7.2 A	68.3 W	53.7 W	85°C
2083 (2800+)								
2167 (3000+)		45.0 A	35.4 A			74.3 W	58.4 W	

Notes:

1. *See Figure 3, "AMD Athlon™ XP Processor Model 10 Power Management States" on page 9.*
2. *The maximum Stop Grant currents are absolute worst case currents for parts that may yield from the worst case corner of the process and are not representative of the typical Stop Grant current that is currently about one-third of the maximum specified current.*
3. *These currents occur when the AMD Athlon™ system bus is disconnected and has a low power ratio of 1/8 for Stop Grant disconnect and a low power ratio of 1/8 Halt disconnect applied to the core clock grid of the processor as dictated by a value of 2003_1223h programmed into the Clock Control (CLK_Ctl) MSR. For more information, refer to the* AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656.*
4. *The Stop Grant current consumption is characterized at 50°C and not tested.*
5. *Thermal design power represents the maximum sustained power dissipated while executing publicly-available software or instruction sequences under normal system operation at nominal V_{CC_CORE}. Thermal solutions must monitor the temperature of the processor to prevent the processor from exceeding its maximum die temperature.*

7 Electrical Data

This chapter provides electrical characteristics for the AMD Athlon™ XP processor model 10.

7.1 Conventions

The conventions used in this chapter are as follows:

- Current specified as being sourced by the processor is *negative*.
- Current specified as being sunk by the processor is *positive*.

7.2 Interface Signal Groupings

The electrical data in this chapter is presented separately for each signal group.

Table 2 defines each group and the signals contained in each group.

Table 2. Interface Signal Groupings

Signal Group	Signals	Notes
Power	VID[4:0], VCCA, V_{CC_CORE}, COREFB, COREFB#	See “Voltage Identification (VID[4:0])” on page 25, “VID[4:0] Pins” on page 70, “VCCA AC and DC Characteristics” on page 25, “V_{CC_CORE} Characteristics” on page 26, “VCCA Pin” on page 70, and “COREFB and COREFB# Pins” on page 66.
Frequency	FID[3:0]	See “Frequency Identification (FID[3:0])” on page 25 and “FID[3:0] Pins” on page 67.
System Clocks	SYSCLK, SYSCLK# (Tied to CLKIN/CLKIN# and RSTCLK/RSTCLK#), PLLBYPASSCLK#, PLLBYPASSCLK	See Table 8, “SYSCLK and SYSCLK# DC Characteristics,” on page 29, Table 9, “SYSCLK and SYSCLK# AC Characteristics for the AMD Athlon™ XP Processor Model 10,” on page 30, “SYSCLK and SYSCLK#” on page 70, and “PLL Bypass and Test Pins” on page 69.

Table 2. Interface Signal Groupings (continued)

Signal Group	Signals	Notes
AMD Athlon™ System Bus	SADDIN[14:2]#, SADDOUT[14:2]#, SADDINCLK#, SADDOUTCLK#, SFILLVAL#, SDATAINVAL#, SDATAOUTVAL#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAOUTCLK[3:0]#, CLKFWDRST, PROCRDY, CONNECT	See "AMD Athlon™ System Bus AC and DC Characteristics" on page 31, and "CLKFWDRST Pin" on page 65.
Southbridge	RESET#, INTR, NMI, SMI#, INIT#, A20M#, FERR, IGNNE#, STPCLK#, FLUSH#	See "General AC and DC Characteristics" on page 33, "INTR Pin" on page 68, "NMI Pin" on page 69, "SMI# Pin" on page 70, "INIT# Pin" on page 68, "A20M# Pin" on page 65, "FERR Pin" on page 66,"IGNNE# Pin" on page 68, "STPCLK# Pin" on page 70, and "FLUSH# Pin" on page 68.
JTAG	TMS, TCK, TRST#, TDI, TDO	See "General AC and DC Characteristics" on page 33.
Test	PLLBYPASS#, PLLTEST#, PLLMON1, PLLMON2, SCANCLK1, SCANCLK2, SCANSHIFTEN, SCANINTEVAL, ANALOG	See "General AC and DC Characteristics" on page 33, "PLL Bypass and Test Pins" on page 69, "Scan Pins" on page 70, "Analog Pin" on page 65.
Miscellaneous	DBREQ#, DBRDY, PWROK	See "General AC and DC Characteristics" on page 33, "DBRDY and DBREQ# Pins" on page 66, "PWROK Pin" on page 69.
APIC	PICD[1:0]#, PICCLK	See "APIC Pins AC and DC Characteristics" on page 38, and "APIC Pins, PICCLK, PICD[1:0]#" on page 65.
Thermal	THERMDA, THERMDC	See Table 13, "Thermal Diode Electrical Characteristics," on page 36, and "THERMDA and THERMDC Pins" on page 70.

7.3 Voltage Identification (VID[4:0])

Table 3 shows the VID[4:0] DC Characteristics. For more information on VID[4:0] DC Characteristics, see "VID[4:0] Pins" on page 70.

Table 3. VID[4:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low	6 mA	
V_{OH}	Output High Voltage	–	5.25 V *

Note:

* *The VID pins are either open circuit or pulled to ground. It is recommended that these pins are not pulled above 5.25 V, which is 5.0 V + 5%..*

7.4 Frequency Identification (FID[3:0])

Table 4 shows the FID[3:0] DC characteristics. For more information, see "FID[3:0] Pins" on page 67.

Table 4. FID[3:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low	6 mA	
V_{OH}	Output High Voltage	–	2.625 V *

Note:

* *The FID pins must not be pulled above this voltage by an external pullup resistor.*

7.5 VCCA AC and DC Characteristics

Table 5 shows the AC and DC characteristics for VCCA. For more information, see "VCCA Pin" on page 70.

Table 5. VCCA AC and DC Characteristics

Symbol	Parameter	Min	Nominal	Max	Units	Notes
V_{VCCA}	VCCA Pin Voltage	2.25	2.5	2.75	V	1
I_{VCCA}	VCCA Pin Current	0		50	mA/GHz	2

Notes:

1. *Minimum and Maximum voltages are absolute. No transients below minimum nor above maximum voltages are permitted.*
2. *Measured at 2.5 V.*

7.6 Decoupling

See the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, or contact your local AMD office for information about the decoupling required on the motherboard for use with the AMD Athlon™ XP processor model 10.

7.7 V_{CC_CORE} Characteristics

Table 6 shows the AC and DC characteristics for V_{CC_CORE}. See Figure 8 on page 27 for a graphical representation of the V_{CC_CORE} waveform.

Table 6. V_{CC_CORE} AC and DC Characteristics

Symbol	Parameter	Limit in Working State	Units
$V_{CC\_CORE\_DC\_MAX}$	Maximum static voltage above $V_{CC\_CORE\_NOM}$*	50	mV
$V_{CC\_CORE\_DC\_MIN}$	Maximum static voltage below $V_{CC\_CORE\_NOM}$*	–50	mV
$V_{CC\_CORE\_AC\_MAX}$	Maximum excursion above $V_{CC\_CORE\_NOM}$*	150	mV
$V_{CC\_CORE\_AC\_MIN}$	Maximum excursion below $V_{CC\_CORE\_NOM}$*	–100	mV
t_{MAX_AC}	Maximum excursion time for AC transients	10	µs
t_{MIN_AC}	Negative excursion time for AC transients	5	µs

Note:

* *All voltage measurements are taken differentially at the COREFB/COREFB# pins.*

Figure 8 shows the processor core voltage (V_{CC_CORE}) waveform response to perturbation. The t_{MIN_AC} (negative AC transient excursion time) and t_{MAX_AC} (positive AC transient excursion time) represent the maximum allowable time below or above the DC tolerance thresholds.

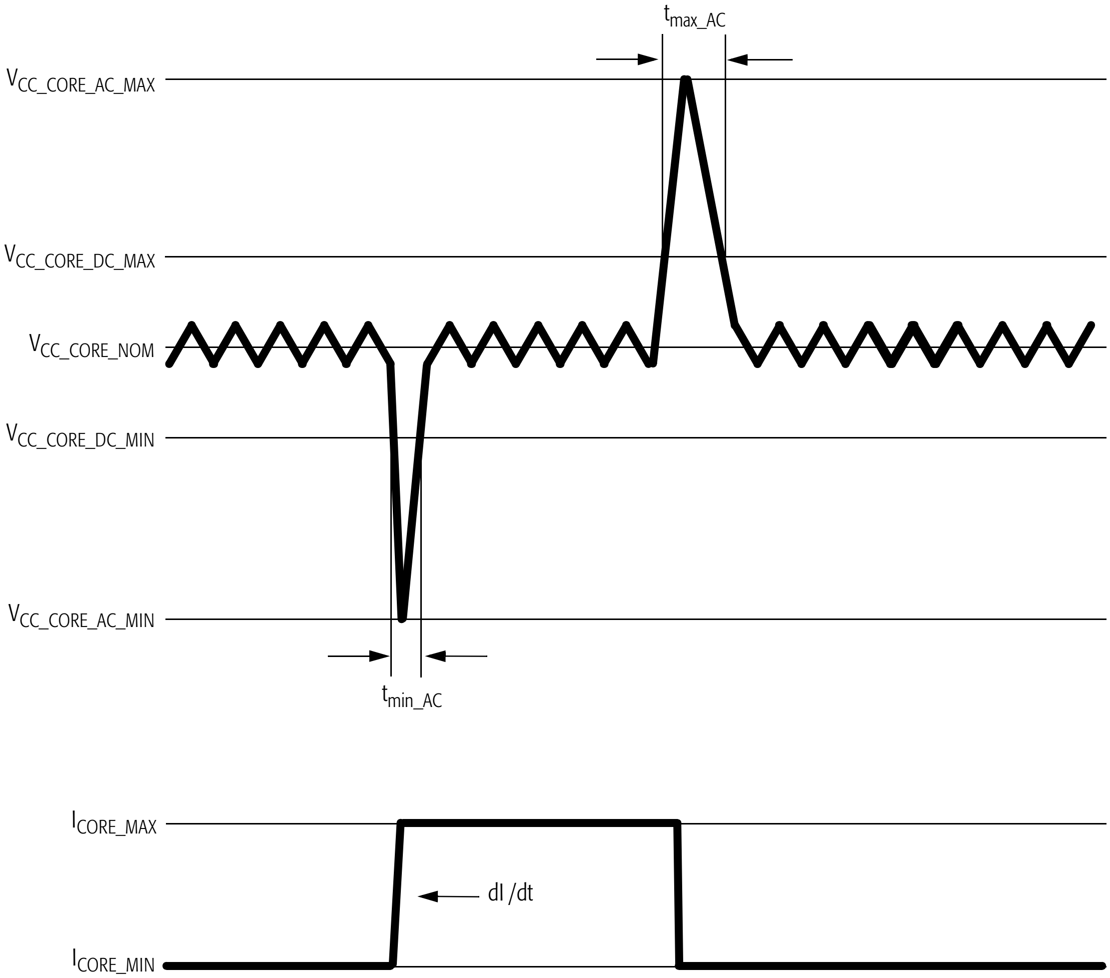


Figure 8. V_{CC_CORE} **Voltage Waveform**

7.8 Absolute Ratings

The AMD Athlon XP processor model 10 should not be subjected to conditions exceeding the absolute ratings, as such conditions can adversely affect long-term reliability or result in functional damage.

Table 7 lists the maximum absolute ratings of operation for the AMD Athlon XP processor model 10.

Table 7. Absolute Ratings

Parameter	Description	Min	Max
V_{CC_CORE}	AMD Athlon™ XP processor model 10 core supply	–0.5 V	V_{CC_CORE} Max + 0.5 V
VCCA	AMD Athlon XP processor model 10 PLL supply	–0.5 V	VCCA Max + 0.5 V
V_{PIN}	Voltage on any signal pin	–0.5 V	V_{CC_CORE} Max + 0.5 V
$T_{STORAGE}$	Storage temperature of processor	–40ºC	100ºC

7.9 SYSCLK and SYSCLK# AC and DC Characteristics

Table 8 shows the DC characteristics of the SYSCLK and SYSCLK# differential clocks. The SYSCLK signal represents CLKIN and RSTCLK tied together while the SYSCLK# signal represents CLKIN# and RSTCLK# tied together. For more information about SYSCLK and SYSCLK#, see "SYSCLK and SYSCLK#" on page 70 and Table 18, "Pin Name Abbreviations," on page 50.

Table 8. SYSCLK and SYSCLK# DC Characteristics

Symbol	Description	Min	Max	Units
$V_{Threshold\text{-}DC}$	Crossing before transition is detected (DC)	400		mV
$V_{Threshold\text{-}AC}$	Crossing before transition is detected (AC)	450		mV
I_{LEAK_P}	Leakage current through P-channel pullup to V_{CC_CORE}	–1		mA
I_{LEAK_N}	Leakage current through N-channel pulldown to VSS (Ground)		1	mA
V_{CROSS}	Differential signal crossover		V_{CC_CORE} / 2±100	mV
C_{PIN}	Capacitance *	4	25 *	pF

Note:

* *The following processor inputs have twice the listed capacitance because they connect to two input pads—SYSCLK and SYSCLK#. SYSCLK connects to CLKIN/RSTCLK. SYSCLK# connects to CLKIN#/RSTCLK#.*

Figure 9 shows the DC characteristics of the SYSCLK and SYSCLK# signals.

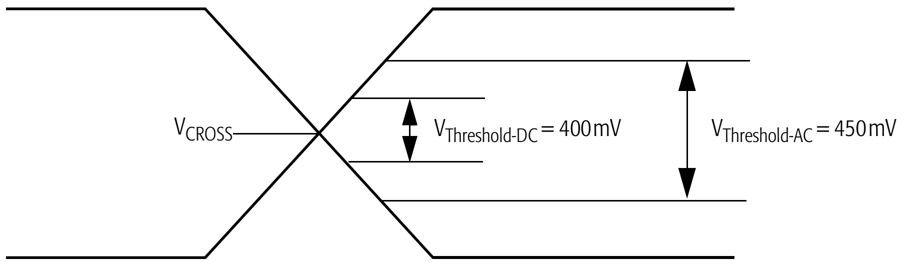


Figure 9. SYSCLK and SYSCLK# Differential Clock Signals

Table 9 shows the SYSCLK/SYSCLK# differential clock AC characteristics of the AMD Athlon XP processor model 10.

Table 9. SYSCLK and SYSCLK# AC Characteristics for the AMD Athlon™ XP Processor Model 10

Symbol	Parameter Description	Minimum	Maximum	Units	Notes
	Clock Frequency	50	166	MHz	1
	Duty Cycle	30%	70%		
t_1	Period	6		ns	2, 3
t_2	High Time	1.05		ns	
t_3	Low Time	1.05		ns	
t_4	Fall Time		2	ns	
t_5	Rise Time		2	ns	
	Period Stability		± 300	ps	

Notes:

1. *The AMD Athlon™ system bus operates at twice this clock frequency.*
2. *Circuitry driving the AMD Athlon™ system bus clock inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The –20dB attenuation point, as measured into a 20- or 30-pF load must be less than 500 kHz.*
3. *Circuitry driving the AMD Athlon system bus clock inputs may purposely alter the AMD Athlon system bus clock frequency (spread spectrum clock generators). In no cases can the AMD Athlon system bus period violate the minimum specification above. AMD Athlon system bus clock inputs can vary from 100% of the specified frequency to 99% of the specified frequency at a maximum rate of 100 kHz.*

Figure 10 shows a sample waveform of the SYSCLK signal.

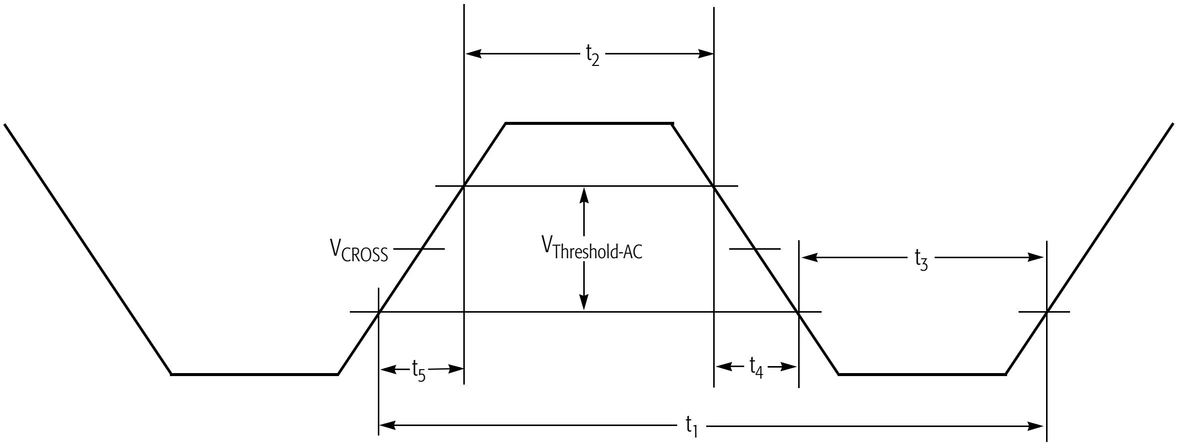


Figure 10. SYSCLK Waveform

7.10 AMD Athlon™ System Bus AC and DC Characteristics

Table 10 shows the DC characteristics of the AMD Athlon system bus used by the AMD Athlon XP processor model 10.

Table 10. AMD Athlon™ System Bus DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{REF}	DC Input Reference Voltage		$(0.5 \times V_{CC\_CORE}) -50$	$(0.5 \times V_{CC\_CORE}) +50$	mV	1
$I_{VREF\_LEAK\_P}$	V_{REF} Tristate Leakage Pullup	$V_{IN} = V_{REF}$ Nominal	−100		µA	
$I_{VREF\_LEAK\_N}$	V_{REF} Tristate Leakage Pulldown	$V_{IN} = V_{REF}$ Nominal		100	µA	
V_{IH}	Input High Voltage		$V_{REF} + 200$	$V_{CC\_CORE} + 500$	mV	
V_{IL}	Input Low Voltage		−500	$V_{REF} - 200$	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	−1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	$V_{IN} = V_{CC\_CORE}$ Nominal		1	mA	
C_{IN}	Input Pin Capacitance		4	7	pF	
R_{ON}	Output Resistance		$0.90 \times R_{setN,P}$	$1.1 \times R_{setN,P}$	Ω	2
R_{setP}	Impedance Set Point, P Channel		40	70	Ω	2
R_{setN}	Impedance Set Point, N Channel		40	70	Ω	2

Notes:

1. *V_{REF} is nominally set to 50% of V_{CC_CORE} with actual values that are specific to motherboard design implementation. V_{REF} must be created with a sufficiently accurate DC source and a sufficiently quiet AC response to adhere to the ± 50 mV specification listed above.*
2. *Measured at V_{CC_CORE} / 2.*

The AC characteristics of the AMD Athlon system bus are shown in Table 11. The parameters are grouped based on the source or destination of the signals involved.

Table 11. AMD Athlon™ System Bus AC Characteristics

Group	Symbol	Parameter	Min	Max	Units	Notes
All Signals	T_{RISE}	Output Rise Slew Rate	1	3	V/ns	1
	T_{FALL}	Output Fall Slew Rate	1	3	V/ns	1
Forward Clocks	$T_{SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge	–	770	ps	2
	T_{SU}	Input Data Setup Time	300		ps	3
	T_{HD}	Input Data Hold Time	300		ps	3
	C_{IN}	Capacitance on input Clocks	4	25	pF	
	C_{OUT}	Capacitance on output Clocks	4	12	pF	
Sync	T_{VAL}	RSTCLK to Output Valid	800	2000	ps	4, 5
	T_{SU}	Setup to RSTCLK	500		ps	4, 6
	T_{HD}	Hold from RSTCLK	500		ps	4, 6

Notes:

1. *Rise and fall time ranges are guidelines over which the I/O has been characterized.*
2. *$T_{SKEW-DIFFEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.*
3. *Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.*
4. *The synchronous signals include PROCRDY, CONNECT, and CLKFWDRST.*
5. *T_{VAL} is RSTCLK rising edge to output valid for PROCRDY. Test Load is 25 pF.*
6. *T_{SU} is setup of CONNECT/CLKFWDRST to rising edge of RSTCLK. T_{HD} is hold of CONNECT/CLKFWDRST from rising edge of RSTCLK.*

7.11 General AC and DC Characteristics

Table 12 shows the AMD Athlon XP processor model 10 AC and DC characteristics of the Southbridge, JTAG, test, and miscellaneous pins.

Table 12. General AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		$(V_{CC\_CORE}/2)$ + 200 mV	V_{CC_CORE} + 300 mV	V	1, 2
V_{IL}	Input Low Voltage		–300	350	mV	1, 2
V_{OH}	Output High Voltage		V_{CC_CORE} – 400	V_{CC_CORE} + 300	mV	
V_{OL}	Output Low Voltage		–300	400	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	$V_{IN} = V_{CC\_CORE}$ Nominal		600	µA	
I_{OH}	Output High Current			–6	mA	3
I_{OL}	Output Low Current		6		mA	3
T_{SU}	Sync Input Setup Time		2.0		ns	4, 5
T_{HD}	Sync Input Hold Time		0.0		ps	4, 5
T_{DELAY}	Output Delay with respect to RSTCLK		0.0	6.1	ns	5

Notes:

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal V_{CC_CORE}. Scale parameters between $V_{CC\_CORE.}$ minimum and $V_{CC\_CORE.}$ maximum.*
3. *I_{OL} and I_{OH} are measured at V_{OL} maximum and V_{OH} minimum, respectively.*
4. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
5. *These are aggregate numbers.*
6. *Edge rates indicate the range over which inputs were characterized.*
7. *In asynchronous operation, the signal must persist for this time to enable capture.*
8. *This value assumes RSTCLK period is 10 ns ==> TBIT = 2*fRST.*
9. *The approximate value for standard case in normal mode operation.*
10. *This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.*
11. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
12. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
13. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*
14. *Time to valid is for any open-drain pins. See requirements 7 and 8 in the "Power-Up Timing Requirements" Chapter for more information.*

Table 12. General AC and DC Characteristics (continued)

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
T_{BIT}	Input Time to Acquire		20.0		ns	7, 8
T_{RPT}	Input Time to Reacquire		40.0		ns	9–13
T_{RISE}	Signal Rise Time		1.0	3.0	V/ns	6
T_{FALL}	Signal Fall Time		1.0	3.0	V/ns	6
C_{PIN}	Pin Capacitance		4	12	pF	
T_{VALID}	Time to data valid			100	ns	14

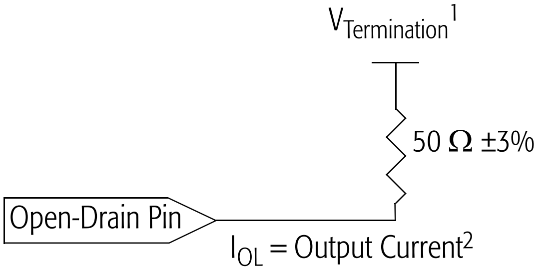
Notes:

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal* V_{CC_CORE} *. Scale parameters between* $V_{CC\_CORE.}$ *minimum and* $V_{CC\_CORE.}$ *maximum.*
3. I_{OL} *and* I_{OH} *are measured at* V_{OL} *maximum and* V_{OH} *minimum, respectively.*
4. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
5. *These are aggregate numbers.*
6. *Edge rates indicate the range over which inputs were characterized.*
7. *In asynchronous operation, the signal must persist for this time to enable capture.*
8. *This value assumes RSTCLK period is 10 ns ==> TBIT = 2*fRST.*
9. *The approximate value for standard case in normal mode operation.*
10. *This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.*
11. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
12. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
13. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*
14. *Time to valid is for any open-drain pins. See requirements 7 and 8 in the "Power-Up Timing Requirements" Chapter for more information.*

7.12 Open Drain Test Circuit

Figure 11 is a test circuit that may be used on automated test equipment (ATE) to test for validity on open drain pins.

Refer to Table 12, "General AC and DC Characteristics," on page 33 for timing requirements.



Notes:

1. $V_{Termination}$ = 1.2 V for VID and FID pins
   $V_{Termination}$ = 1.0 V for APIC pins
2. I_{OL} = –6 mA for VID and FID pins
   I_{OL} = –9 mA for APIC pins

Figure 11. General ATE Open-Drain Test Circuit

7.13 Thermal Diode Characteristics

The AMD Athlon XP processor model 10 provides a diode that can be used in conjunction with an external temperature sensor to determine the die temperature of the processor. The diode anode (THERMDA) and cathode (THERMDC) are available as pins on the processor, as described in "THERMDA and THERMDC Pins" on page 70.

For information about thermal design for the AMD Athlon XP processor model 10, including layout and airflow considerations, see the *AMD Processor Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794, and the cooling guidelines on *http://www.amd.com*.

Thermal Diode Electrical Characteristics

Table 13 shows the AMD Athlon XP processor model 10 characteristics of the on-die thermal diode. For information about calculations for the ideal diode equation and temperature offset correction, see Appendix A, "Thermal Diode Calculations," on page 77.

Table 13. Thermal Diode Electrical Characteristics

Symbol	Parameter Description	Min	Nom	Max	Units	Notes
I	Sourcing current	5		300	µA	1
$n_{f,\text{ lumped}}$	Lumped ideality factor	1.00000	1.00374	1.00900		2, 3, 4
$n_{f,\text{ actual}}$	Actual ideality factor		1.00261			3, 4
R_T	Series Resistance		0.93		Ω	3, 4

Notes:

1. *The sourcing current should always be used in forward bias only.*
2. *Characterized at 95°C with a forward bias current pair of 10 µA and 100 µA. AMD recommends using a minimum of two sourcing currents to accurately measure the temperature of the thermal diode.*
3. *Not 100% tested. Specified by design and limited characterization.*
4. *The lumped ideality factor adds the effect of the series resistance term to the actual ideality factor. The series resistance term indicates the resistance from the pins of the processor to the on-die thermal diode. The value of the lumped ideality factor depends on the sourcing current pair used.*

Thermal Protection Characterization

The following section describes parameters relating to thermal protection. The implementation of thermal control circuitry to control processor temperature is left to the manufacturer to determine how to implement.

Thermal limits in motherboard design are necessary to protect the processor from thermal damage. $T_{SHUTDOWN}$ is the temperature for thermal protection circuitry to initiate shutdown of the processor. T_{SD_DELAY} is the maximum time allowed from the detection of the over-temperature condition to processor shutdown to prevent thermal damage to the processor.

Systems that do not implement thermal protection circuitry or that do not react within the time specified by T_{SD_DELAY} can cause thermal damage to the processor during the unlikely events of fan failure or powering up the processor without a heat-sink. The processor relies on thermal circuitry on the motherboard to turn off the regulated core voltage to the processor in response to a thermal shutdown event.

Thermal protection circuitry reference designs and thermal solution guidelines are found in the following documents:

- *AMD Athlon™ Processor-Based Motherboard Design Guide,* order# 24363
- *AMD Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794

See *http://www.amd.com* for more information about thermal solutions.

Table 14 on page 38 shows the $T_{SHUTDOWN}$ and T_{SD_DELAY} specifications for circuitry in motherboard design necessary for thermal protection of the processor.

Table 14. Guidelines for Platform Thermal Protection of the Processor

Symbol	Parameter Description	Max	Units	Notes
$T_{SHUTDOWN}$	Thermal diode shutdown temperature for processor protection	125	°C	1, 2, 3
T_{SD_DELAY}	Maximum allowed time from $T_{SHUTDOWN}$ detection to processor shutdown	500	ms	1, 3

Notes:

1. *The thermal diode is not 100% tested, it is specified by design and limited characterization.*
2. *The thermal diode is capable of responding to thermal events of 40°C/s or faster.*
3. *The AMD Athlon™ XP processor model 10 provides a thermal diode for measuring die temperature of the processor. The processor relies on thermal circuitry on the motherboard to turn off the regulated core voltage to the processor in response to a thermal shutdown event. Refer to* AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, for thermal protection circuitry designs.*

7.14 APIC Pins AC and DC Characteristics

Table 15 shows the AMD Athlon XP processor model 10 AC and DC characteristics of the APIC pins.

Table 15. APIC Pin AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		1.7	2.625	V	1, 2
V_{IL}	Input Low Voltage		–300	700	mV	1
V_{OH}	Output High Voltage			2.625	V	2
V_{OL}	Output Low Voltage		–300	400	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN} = 2.5 V		1	mA	
I_{OL}	Output Low Current	V_{OL} Max	9		mA	
T_{RISE}	Signal Rise Time		1.0	3.0	V/ns	3
T_{FALL}	Signal Fall Time		1.0	3.0	V/ns	3
T_{SU}	Setup Time		1		ns	
T_{HD}	Hold Time		1		ns	
C_{PIN}	Pin Capacitance		4	12	pF	

Notes:

1. *Characterized across DC supply voltage range.*
2. *The 2.625-V value is equal to 2.5 V plus a maximum of five percent.*
3. *Edge rates indicate the range for characterizing the inputs.*

8 Signal and Power-Up Requirements

The AMD Athlon™ XP processor model 10 is designed to provide functional operation if the voltage and temperature parameters are within the limits of normal operating ranges.

8.1 Power-Up Requirements

Signal Sequence and Timing Description

Figure 12 shows the relationship between key signals in the system during a power-up sequence. This figure details the requirements of the processor.

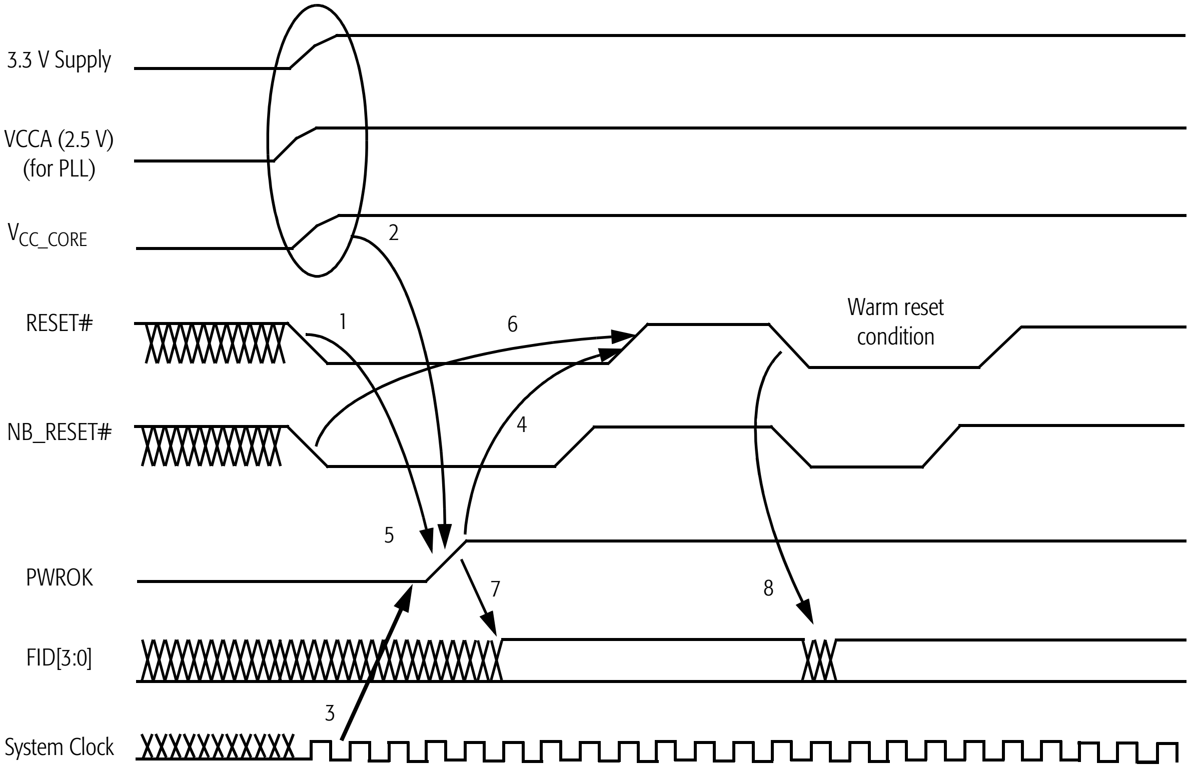


Figure 12. Signal Relationship Requirements During Power-Up Sequence

Notes: 1. *Figure 12 represents several signals generically by using names not necessarily consistent with any pin lists or schematics.*

2. *Requirements 1–8 in Figure 12 are described in "Power-Up Timing Requirements" on page 40.*

Power-Up Timing Requirements. The signal timing requirements are as follows:

1. RESET# must be asserted before PWROK is asserted.

   The AMD Athlon XP processor model 10 does not set the correct clock multiplier if PWROK is asserted prior to a RESET# assertion. It is recommended that RESET# be asserted at least **10 nanoseconds** prior to the assertion of PWROK.

   In practice, a Southbridge asserts RESET# milliseconds before PWROK is asserted.

2. All motherboard voltage planes must be within specification before PWROK is asserted.

   PWROK is an output of the voltage regulation circuit on the motherboard. PWROK indicates that V_{CC_CORE} and all other voltage planes in the system are within specification.

   The motherboard is required to delay PWROK assertion for a minimum of three milliseconds from the 3.3 V supply being within specification. This delay ensures that the system clock (SYSCLK/SYSCLK#) is operating within specification when PWROK is asserted.

   The processor core voltage, V_{CC_CORE}, must be within specification as dictated by the VID[4:0] pins driven by the processor before PWROK is asserted. Before PWROK assertion, the AMD Athlon processor is clocked by a ring oscillator.

   The processor PLL is powered by VCCA. The processor PLL does not lock if VCCA is not high enough for the processor logic to switch for some period before PWROK is asserted. VCCA must be within specification at least five microseconds before PWROK is asserted.

   In practice VCCA, V_{CC_CORE}, and all other voltage planes must be within specification for several milliseconds before PWROK is asserted.

   After PWROK is asserted, the processor PLL locks to its operational frequency.

3. The system clock (SYSCLK/SYSCLK#) must be running before PWROK is asserted.

   When PWROK is asserted, the processor switches from driving the internal processor clock grid from the ring oscillator to driving from the PLL. The reference system clock must be valid at this time. The system clocks are designed to be running after 3.3 V has been within specification for three milliseconds.

4. PWROK assertion to deassertion of RESET#

   The duration of RESET# assertion during cold boots is intended to satisfy the time it takes for the PLL to lock with a less than 1 ns phase error. The processor PLL begins to run after PWROK is asserted and the internal clock grid is switched from the ring oscillator to the PLL. The PLL lock time may take from hundreds of nanoseconds to tens of microseconds. It is recommended that the minimum time between PWROK assertion to the deassertion of RESET# be at least **1.0 milliseconds**. Southbridges enforce a delay of 1.5 to 2.0 milliseconds between PWRGD (Southbridge version of PWROK) assertion and NB_RESET# deassertion.

5. PWROK must be monotonic and meet the timing requirements as defined in Table 12, "General AC and DC Characteristics," on page 33. The processor should not switch between the ring oscillator and the PLL after the initial assertion of PWROK.

6. NB_RESET# must be asserted (causing CONNECT to also assert) before RESET# is deasserted. In practice all Southbridges enforce this requirement.

   If NB_RESET# does not assert until after RESET# has deasserted, the processor misinterprets the CONNECT assertion (due to NB_RESET# being asserted) as the beginning of the SIP transfer. There must be sufficient overlap in the resets to ensure that CONNECT is sampled asserted by the processor before RESET# is deasserted.

7. The FID[3:0] signals are valid within 100 ns after PWROK is asserted. The chipset must not sample the FID[3:0] signals until they become valid. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, for the specific implementation and additional circuitry required.

8. The FID[3:0] signals become valid within 100 ns after RESET# is asserted. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, for the specific implementation and additional circuitry required.

Clock Multiplier Selection (FID[3:0])

The chipset samples the FID[3:0] signals in a chipset-specific manner from the processor and uses this information to determine the correct serial initialization packet (SIP). The chipset then sends the SIP information to the processor for configuration of the AMD Athlon system bus for the clock multiplier that determines the processor frequency indicated by the FID[3:0] code. The SIP is sent to the processor using the SIP protocol. This protocol uses the PROCRDY, CONNECT, and CLKFWDRST signals, that are synchronous to SYSCLK.

For more information about FID[3:0], see “FID[3:0] Pins” on page 67.

Serial Initialization Packet (SIP) Protocol. Refer to *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for details of the SIP protocol.

8.2 Processor Warm Reset Requirements

Northbridge Reset Pins

RESET# cannot be asserted to the processor without also being asserted to the Northbridge. RESET# to the Northbridge is the same as PCI RESET#. The minimum assertion for PCI RESET# is one millisecond. Southbridges enforce a minimum assertion of RESET# for the processor, Northbridge, and PCI of 1.5 to 2.0 milliseconds.

9 Mechanical Data

9.1 Introduction

The AMD Athlon™ XP processor model 10 connects to the motherboard through a pin grid array (PGA) socket named Socket A. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

9.2 Die Loading

The processor die on the OPGA package is exposed at the top of the package. This feature facilitates heat transfer from the die to an approved heat sink. Any heat sink design should avoid loads on corners and edges of die. The OPGA package has compliant pads that serve to bring surfaces in planar contact. Tool-assisted zero insertion force sockets should be designed so that no load is placed on the ceramic substrate of the package.

Table 16 shows the mechanical loading specifications for the processor die. It is critical that the mechanical loading of the heat sink does not exceed the limits shown in Table 16.

Table 16. Mechanical Loading

Location	Dynamic (MAX)	Static (MAX)	Units	Note
Die Surface	100	30	lbf	1
Die Edge	10	10	lbf	2

Notes:

1. *Load specified for coplanar contact to die surface.*
2. *Load defined for a surface at no more than a two-degree angle of inclination to die surface.*

9.3 AMD Athlon™ XP Processor Model 10 OPGA Package Dimensions

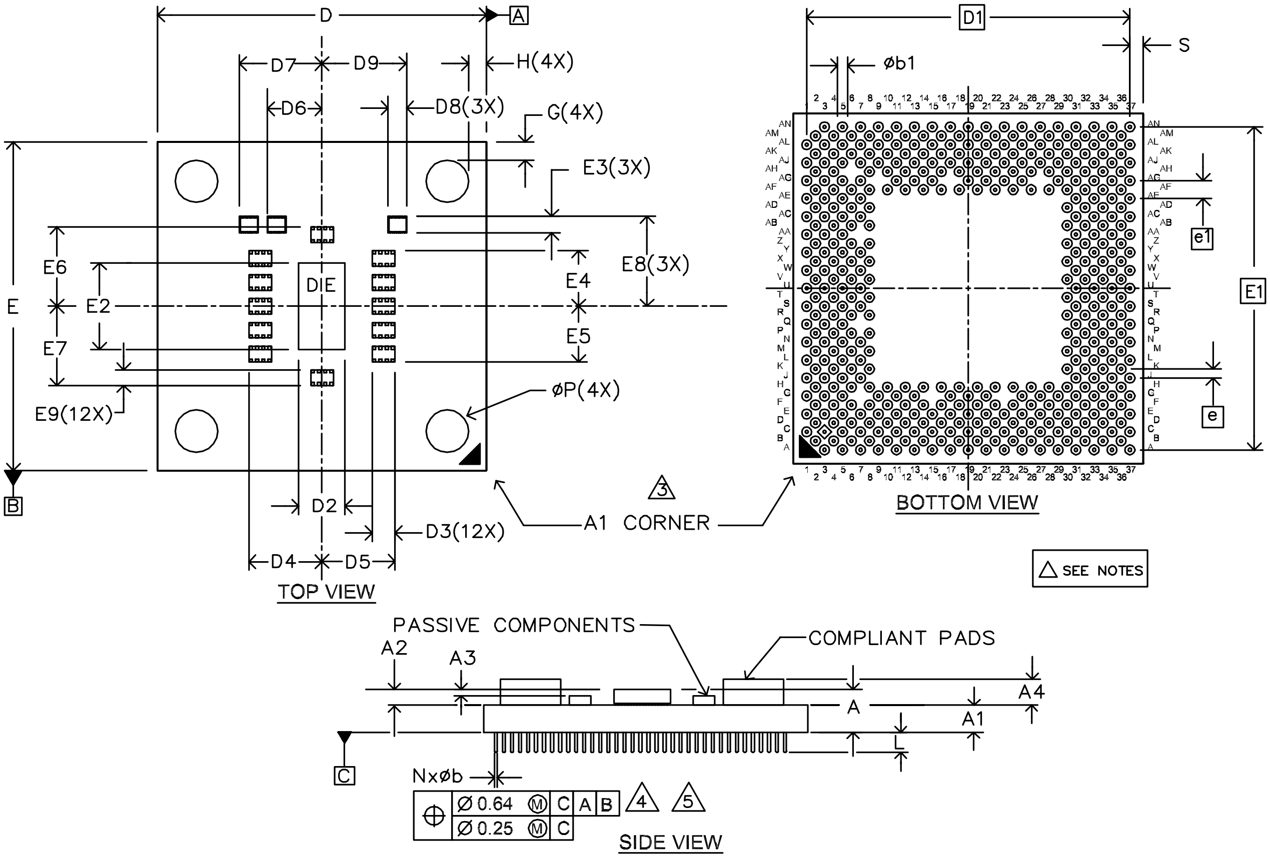
Table 17 shows the AMD Athlon XP processor model 10 package dimensions, and Figure 13 on page 45 shows the OPGA package diagram.

Table 17. Dimensions for the AMD Athlon™ XP Processor Model 10 OPGA Package

Letter or Symbol	Minimum Dimension[1]	Maximum Dimension[1]	Letter or Symbol	Minimum Dimension[1]	Maximum Dimension[1]
D/E	49.27	49.78	E9	1.66	1.96
D1/E1	45.72 BSC		G/H	–	4.50
D2	7.42 REF		A	1.942 REF	
D3	3.30	3.60	A1	1.00	1.20
D4	10.78	11.33	A2	0.80	0.88
D5	10.78	11.33	A3	0.116	–
D6	8.13	8.68	A4	–	1.90
D7	12.33	12.88	ϕP	–	6.60
D8	3.05	3.35	ϕb	0.43	0.50
D9	12.71	13.26	ϕb1	1.40 REF	
E2	13.61 REF		S	1.435	2.375
E3	2.35	2.65	L	3.05	3.31
E4	7.87	8.42	M	37	
E5	7.87	8.42	N	453	
E6	11.41	11.96	e	1.27 BSC	
E7	11.41	11.96	e1	2.54 BSC	
E8	13.28	13.83	Mass[2]	11.0 g REF	

Note:

1. *Dimensions are given in millimeters.*
2. *The mass consists of the completed package, including processor, surface mounted parts and pins.*



GENERAL NOTES

1. All dimensions are specified in millimeters (mm).
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. This corner is marked with a triangle on both sides of the package to identify the pin A1 corner for orientation purposes.
4. Symbol "M" determines pin matrix size and "N" is number of pins.
5. Dimension "b" is measured at maximum solder pin diameter on a plane parallel to datum C.

Figure 13. AMD Athlon™ XP Processor Model 10 OPGA Package

10 Pin Descriptions

10.1 Pin Diagram and Pin Name Abbreviations

Figure 14 on page 48 shows the staggered Pin Grid Array (PGA) for the AMD Athlon™ XP processor model 10. Because some of the pin names are too long to fit in the grid, they are abbreviated. Figure 15 on page 49 shows the bottomside view of the array. Table 18 on page 50 lists all the pins in alphabetical order by pin name, along with the abbreviation where necessary.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	
A			SAO#12		SAO#5		SAO#3		SD#55		SD#61		SD#53		SD#63		SD#62		NC		SD#57		SD#39		SD#35		SD#34		SD#44		NC		SDOC#2		SD#40		SD#30	A
B		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		B
C	SAO#7		SAO#9		SAO#8		SAO#2		SD#54		SDOC#3		NC		SD#51		SD#60		SD#59		SD#56		SD#37		SD#47		SD#38		SD#45		SD#43		SD#42		SD#41		SDOC#1	C
D		VCC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VSS		D
E	SAO#11		SAOC#		SAO#4		SAO#6		SD#52		SD#50		SD#49		SDIC#3		SD#48		SD#58		SD#36		SD#46		NC		SDIC#2		SD#33		SD#32		NC		SD#31		SD#22	E
F		VSS		VSS		VSS		NC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		NC		VCC		VCC		VCC		F
G	SAO#10		SAO#14		SAO#13		KEY		KEY		NC		NC		KEY		KEY		NC		NC		KEY		KEY		NC		NC		NC		SD#20		SD#23		SD#21	G
H		VCC		VCC		NC		NC		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		NC		NC		NC		VSS		VSS		H
J	SAO#0		SAO#1		NC		VID[4]																								NC		SD#19		SDIC#1		SD#29	J
K		VSS		VSS		VSS		NC																					NC		VCC		VCC		VCC		K
L	VID[0]		VID[1]		VID[2]		VID[3]																								NC		SD#26		NC		SD#28	L
M		VCC		VCC		VCC		VCC																					VSS		VSS		VSS		VSS		M
N	PICCLK		PICD#0		PICD#1		KEY																								NC		SD#25		SD#27		SD#18	N
P		VSS		VSS		VSS		VSS																					VCC		VCC		VCC		VCC		P
Q	TCK		TMS		SCNSN		KEY																								NC		SD#24		SD#17		SD#16	Q
R		VCC		VCC		VCC		VCC																					VSS		VSS		VSS		VSS		R
S	SCNCK1		SCNINV		SCNCK2		THDA																								NC		SD#7		SD#15		SD#6	S
T		VSS		VSS		VSS		VSS																					VCC		VCC		VCC		VCC		T
U	TDI		TRST#		TDO		THDC																								NC		SD#5		SD#4		NC	U
V		VCC		VCC		VCC		VCC																					VSS		VSS		VSS		VSS		V
W	FID[0]		FID[1]		VREF_S		NC																								NC		SDIC#0		SD#2		SD#1	W
X		VSS		VSS		VSS		VSS																					VCC		VCC		VCC		VCC		X
Y	FID[2]		FID[3]		NC		KEY																								NC		NC		SD#3		SD#12	Y
Z		VCC		VCC		VCC		VCC																					VSS		VSS		VSS		VSS		Z
AA	DBRDY		DBREQ#		NC		KEY																								NC		SD#8		SD#0		SD#13	AA
AB		VSS		VSS		VSS		VSS																					VCC		VCC		VCC		VCC		AB
AC	STPC#		PLTST#		ZN		NC																								NC		SD#10		SD#14		SD#11	AC
AD		VCC		VCC		VCC		NC																					NC		VSS		VSS		VSS		AD
AE	A20M#		PWROK		ZP		NC																								NC		SAI#5		SDOC#0		SD#9	AE
AF		VSS		VSS		NC		NC		NC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		NC		NC		NC		VCC		VCC		AF
AG	FERR		RESET#		NC		KEY		KEY		COREFB		COREFB#		KEY		KEY		NC		NC		NC		NC		KEY		KEY		FSB0		SAI#2		SAI#11		SAI#7	AG
AH		VCC		VCC		AMD		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		FSB1		VSS		VSS		VSS		AH
AJ	IGNNE#		INIT#		VCC		NC		NC		NC		ANLOG		NC		NC		NC		CLKFR		VCCA		PLBYP#		NC		SAI#0		SFILLV#		SAIC#		SAI#6		SAI#3	AJ
AK		VSS		VSS		CPR#		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VCC		AK
AL	INTR		FLUSH#		VCC		NC		NC		NC		PLMN2		PLBYC#		CLKIN#		RCLK#		K7CO		CNNCT		NC		NC		SAI#1		SDOV#		SAI#8		SAI#4		SAI#10	AL
AM		VCC		VSS		VSS		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		AM
AN			NMI		SMI#		NC		NC		NC		PLMN1		PLBYC		CLKIN		RCLK		K7CO#		PRCRDY		NC		NC		SAI#12		SAI#14		SDINV#		SAI#13		SAI#9	AN
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	

AMD Athlon™ XP Processor
Model 10
Topside View

Figure 14. AMD Athlon™ XP Processor Model 10 Pin Diagram—Topside View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	
1			SAO#7		SAO#11		SAO#10		SAO#0		VID[0]		PICCLK		TCK		SCNCK1		TDI		FID[0]		FID[2]		DBRDY		STPC#		A20M#		FERR		IGNNE#		INTR			1
2		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		2
3	SAO#12		SAO#9		SAOC#		SAO#14		SAO#1		VID[1]		PICD#0		TMS		SCNINV		TRST#		FID[1]		FID[3]		DBREQ#		PLTST#		PWROK		RESET#		INIT#		FLUSH#		NMI	3
4		VCC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VSS		4
5	SAO#5		SAO#8		SAO#4		SAO#13		NC		VID[2]		PICD#1		SCNSN		SCNCK2		TDO		VREF_S		NC		NC		ZN		ZP		NC		VCC		VCC		SMI#	5
6		VSS		VSS		VSS		NC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		NC		AMD		CPR#		VSS		6
7	SAO#3		SAO#2		SAO#6		KEY		VID[4]		VID[3]		KEY		KEY		THDA		THDC		NC		KEY		KEY		NC		NC		KEY		NC		NC		NC	7
8		VCC		VCC		NC		NC		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		NC		NC		NC		NC		NC		8
9	SD#55		SD#54		SD#52		KEY																								KEY		NC		NC		NC	9
10		VSS		VSS		VSS		NC																						NC		VCC		VCC		VCC		10
11	SD#61		SDOC#3		SD#50		NC																								COREFB		NC		NC		NC	11
12		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		12
13	SD#53		NC		SD#49		NC																								COREFB#		ANLOG		PLMN2		PLMN1	13
14		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		14
15	SD#63		SD#51		SDIC#3		KEY																								KEY		NC		PLBYC#		PLBYC	15
16		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		16
17	SD#62		SD#60		SD#48		KEY																								KEY		NC		CLKIN#		CLKIN	17
18		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		18
19	NC		SD#59		SD#58		NC																								NC		NC		RCLK#		RCLK	19
20		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		20
21	SD#57		SD#56		SD#36		NC																								NC		CLKFR		K7CO		K7CO#	21
22		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		22
23	SD#39		SD#37		SD#46		KEY																								NC		VCCA		CNNCT		PRCRDY	23
24		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		24
25	SD#35		SD#47		NC		KEY																								NC		PLBYP#		NC		NC	25
26		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		26
27	SD#34		SD#38		SDIC#2		NC																								KEY		NC		NC		NC	27
28		VCC		VCC		VCC		NC																						NC		VSS		VSS		VSS		28
29	SD#44		SD#45		SD#33		NC																								KEY		SAI#0		SAI#1		SAI#12	29
30		VSS		VSS		NC		NC		NC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		NC		NC		FSB1		VCC		VCC		30
31	NC		SD#43		SD#32		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		FSB0		SFILLV#		SDOV#		SAI#14	31
32		VCC		VCC		VCC		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		NC		VSS		VSS		VSS		32
33	SDOC#2		SD#42		NC		SD#20		SD#19		SD#26		SD#25		SD#24		SD#7		SD#5		SDIC#0		NC		SD#8		SD#10		SAI#5		SAI#2		SAIC#		SAI#8		SDINV#	33
34		VSS		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VCC		34
35	SD#40		SD#41		SD#31		SD#23		SDIC#1		NC		SD#27		SD#17		SD#15		SD#4		SD#2		SD#3		SD#0		SD#14		SDOC#0		SAI#11		SAI#6		SAI#4		SAI#13	35
36		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		36
37	SD#30		SDOC#1		SD#22		SD#21		SD#29		SD#28		SD#18		SD#16		SD#6		NC		SD#1		SD#12		SD#13		SD#11		SD#9		SAI#7		SAI#3		SAI#10		SAI#9	37
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	

AMD Athlon™ XP Processor
Model 10
Bottomside View

Figure 15. AMD Athlon™ XP Processor Model 10 Pin Diagram—Bottomside View

Table 18. Pin Name Abbreviations

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	A20M#	AE1		KEY	AG27
	AMD	AH6		KEY	AG29
ANLOG	ANALOG	AJ13		NC	A19
CLKFR	CLKFWDRST	AJ21		NC	A31
	CLKIN	AN17		NC	C13
	CLKIN#	AL17		NC	E25
CNNCT	CONNECT	AL23		NC	E33
	COREFB	AG11		NC	F8
	COREFB#	AG13		NC	F30
CPR#	CPU_PRESENCE#	AK6		NC	G11
	DBRDY	AA1		NC	G13
	DBREQ#	AA3		NC	G19
	FERR	AG1		NC	G21
	FID[0]	W1		NC	G27
	FID[1]	W3		NC	G29
	FID[2]	Y1		NC	G31
	FID[3]	Y3		NC	H6
	FLUSH#	AL3		NC	H8
FSB0	FSB_Sense[0]	AG31		NC	H10
FSB1	FSB_Sense[1]	AH30		NC	H28
	IGNNE#	AJ1		NC	H30
	INIT#	AJ3		NC	H32
	INTR	AL1		NC	J5
K7CO	K7CLKOUT	AL21		NC	J31
K7CO#	K7CLKOUT#	AN21		NC	K8
	KEY	G7		NC	K30
	KEY	G9		NC	L31
	KEY	G15		NC	L35
	KEY	G17		NC	N31
	KEY	G23		NC	Q31
	KEY	G25		NC	S31
	KEY	N7		NC	U31
	KEY	Q7		NC	U37
	KEY	Y7		NC	W7
	KEY	AA7		NC	W31
	KEY	AG7		NC	Y5
	KEY	AG9		NC	Y31
	KEY	AG15		NC	Y33
	KEY	AG17		NC	AA5

Table 18. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	NC	AA31		PICCLK	N1
	NC	AC7	PICD#0	PICD[0]#	N3
	NC	AC31	PICD#1	PICD[1]#	N5
	NC	AD8	PLBYP#	PLLBYPASS#	AJ25
	NC	AD30	PLBYC	PLLBYPASSCLK	AN15
	NC	AE7	PLBYC#	PLLBYPASSCLK#	AL15
	NC	AE31	PLMN1	PLLMON1	AN13
	NC	AF6	PLMN2	PLLMON2	AL13
	NC	AF8	PLTST#	PLLTEST#	AC3
	NC	AF10	PRCRDY	PROCREADY	AN23
	NC	AF28		PWROK	AE3
	NC	AF30		RESET#	AG3
	NC	AF32	RCLK	RSTCLK	AN19
	NC	AG5	RCLK#	RSTCLK#	AL19
	NC	AG19	SAI#0	SADDIN[0]#	AJ29
	NC	AG21	SAI#1	SADDIN[1]#	AL29
	NC	AG23	SAI#2	SADDIN[2]#	AG33
	NC	AG25	SAI#3	SADDIN[3]#	AJ37
	NC	AH8	SAI#4	SADDIN[4]#	AL35
	NC	AJ7	SAI#5	SADDIN[5]#	AE33
	NC	AJ9	SAI#6	SADDIN[6]#	AJ35
	NC	AJ11	SAI#7	SADDIN[7]#	AG37
	NC	AJ15	SAI#8	SADDIN[8]#	AL33
	NC	AJ17	SAI#9	SADDIN[9]#	AN37
	NC	AJ19	SAI#10	SADDIN[10]#	AL37
	NC	AJ27	SAI#11	SADDIN[11]#	AG35
	NC	AK8	SAI#12	SADDIN[12]#	AN29
	NC	AL7	SAI#13	SADDIN[13]#	AN35
	NC	AL9	SAI#14	SADDIN[14]#	AN31
	NC	AL11	SAIC#	SADDINCLK#	AJ33
	NC	AL25	SAO#0	SADDOUT[0]#	J1
	NC	AL27	SAO#1	SADDOUT[1]#	J3
	NC	AM8	SAO#2	SADDOUT[2]#	C7
	NC	AN7	SAO#3	SADDOUT[3]#	A7
	NC	AN9	SAO#4	SADDOUT[4]#	E5
	NC	AN11	SAO#5	SADDOUT[5]#	A5
	NC	AN25	SAO#6	SADDOUT[6]#	E7
	NC	AN27	SAO#7	SADDOUT[7]#	C1
	NMI	AN3	SAO#8	SADDOUT[8]#	C5

Table 18. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SAO#9	SADDOUT[9]#	C3	SD#28	SDATA[28]#	L37
SAO#10	SADDOUT[10]#	G1	SD#29	SDATA[29]#	J37
SAO#11	SADDOUT[11]#	E1	SD#30	SDATA[30]#	A37
SAO#12	SADDOUT[12]#	A3	SD#31	SDATA[31]#	E35
SAO#13	SADDOUT[13]#	G5	SD#32	SDATA[32]#	E31
SAO#14	SADDOUT[14]#	G3	SD#33	SDATA[33]#	E29
SAOC#	SADDOUTCLK#	E3	SD#34	SDATA[34]#	A27
SCNCK1	SCANCLK1	S1	SD#35	SDATA[35]#	A25
SCNCK2	SCANCLK2	S5	SD#36	SDATA[36]#	E21
SCNINV	SCANINTEVAL	S3	SD#37	SDATA[37]#	C23
SCNSN	SCANSHIFTEN	Q5	SD#38	SDATA[38]#	C27
SD#0	SDATA[0]#	AA35	SD#39	SDATA[39]#	A23
SD#1	SDATA[1]#	W37	SD#40	SDATA[40]#	A35
SD#2	SDATA[2]#	W35	SD#41	SDATA[41]#	C35
SD#3	SDATA[3]#	Y35	SD#42	SDATA[42]#	C33
SD#4	SDATA[4]#	U35	SD#43	SDATA[43]#	C31
SD#5	SDATA[5]#	U33	SD#44	SDATA[44]#	A29
SD#6	SDATA[6]#	S37	SD#45	SDATA[45]#	C29
SD#7	SDATA[7]#	S33	SD#46	SDATA[46]#	E23
SD#8	SDATA[8]#	AA33	SD#47	SDATA[47]#	C25
SD#9	SDATA[9]#	AE37	SD#48	SDATA[48]#	E17
SD#10	SDATA[10]#	AC33	SD#49	SDATA[49]#	E13
SD#11	SDATA[11]#	AC37	SD#50	SDATA[50]#	E11
SD#12	SDATA[12]#	Y37	SD#51	SDATA[51]#	C15
SD#13	SDATA[13]#	AA37	SD#52	SDATA[52]#	E9
SD#14	SDATA[14]#	AC35	SD#53	SDATA[53]#	A13
SD#15	SDATA[15]#	S35	SD#54	SDATA[54]#	C9
SD#16	SDATA[16]#	Q37	SD#55	SDATA[55]#	A9
SD#17	SDATA[17]#	Q35	SD#56	SDATA[56]#	C21
SD#18	SDATA[18]#	N37	SD#57	SDATA[57]#	A21
SD#19	SDATA[19]#	J33	SD#58	SDATA[58]#	E19
SD#20	SDATA[20]#	G33	SD#59	SDATA[59]#	C19
SD#21	SDATA[21]#	G37	SD#60	SDATA[60]#	C17
SD#22	SDATA[22]#	E37	SD#61	SDATA[61]#	A11
SD#23	SDATA[23]#	G35	SD#62	SDATA[62]#	A17
SD#24	SDATA[24]#	Q33	SD#63	SDATA[63]#	A15
SD#25	SDATA[25]#	N33	SDIC#0	SDATAINCLK[0]#	W33
SD#26	SDATA[26]#	L33	SDIC#1	SDATAINCLK[1]#	J35
SD#27	SDATA[27]#	N35	SDIC#2	SDATAINCLK[2]#	E27

Table 18. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin
SDIC#3	SDATAINCLK[3]#	E15
SDINV#	SDATAINVALID#	AN33
SDOC#0	SDATAOUTCLK[0]#	AE35
SDOC#1	SDATAOUTCLK[1]#	C37
SDOC#2	SDATAOUTCLK[2]#	A33
SDOC#3	SDATAOUTCLK[3]#	C11
SDOV#	SDATAOUTVALID#	AL31
SFILLV#	SFILLVALID#	AJ31
	SMI#	AN5
STPC#	STPCLK#	AC1
	TCK	Q1
	TDI	U1
	TDO	U5
THDA	THERMDA	S7
THDC	THERMDC	U7
	TMS	Q3
	TRST#	U3
VCC	V_{CC_CORE}	B4
VCC	V_{CC_CORE}	B8
VCC	V_{CC_CORE}	B12
VCC	V_{CC_CORE}	B16
VCC	V_{CC_CORE}	B20
VCC	V_{CC_CORE}	B24
VCC	V_{CC_CORE}	B28
VCC	V_{CC_CORE}	B32
VCC	V_{CC_CORE}	B36
VCC	V_{CC_CORE}	D2
VCC	V_{CC_CORE}	D4
VCC	V_{CC_CORE}	D8
VCC	V_{CC_CORE}	D12
VCC	V_{CC_CORE}	D16
VCC	V_{CC_CORE}	D20
VCC	V_{CC_CORE}	D24
VCC	V_{CC_CORE}	D28
VCC	V_{CC_CORE}	D32
VCC	V_{CC_CORE}	F12
VCC	V_{CC_CORE}	F16
VCC	V_{CC_CORE}	F20
VCC	V_{CC_CORE}	F24
VCC	V_{CC_CORE}	F28
VCC	V_{CC_CORE}	F32
VCC	V_{CC_CORE}	F34
VCC	V_{CC_CORE}	F36
VCC	V_{CC_CORE}	H2
VCC	V_{CC_CORE}	H4
VCC	V_{CC_CORE}	H12
VCC	V_{CC_CORE}	H16
VCC	V_{CC_CORE}	H20
VCC	V_{CC_CORE}	H24
VCC	V_{CC_CORE}	K32
VCC	V_{CC_CORE}	K34
VCC	V_{CC_CORE}	K36
VCC	V_{CC_CORE}	M2
VCC	V_{CC_CORE}	M4
VCC	V_{CC_CORE}	M6
VCC	V_{CC_CORE}	M8
VCC	V_{CC_CORE}	P30
VCC	V_{CC_CORE}	P32
VCC	V_{CC_CORE}	P34
VCC	V_{CC_CORE}	P36
VCC	V_{CC_CORE}	R2
VCC	V_{CC_CORE}	R4
VCC	V_{CC_CORE}	R6
VCC	V_{CC_CORE}	R8
VCC	V_{CC_CORE}	T30
VCC	V_{CC_CORE}	T32
VCC	V_{CC_CORE}	T34
VCC	V_{CC_CORE}	T36
VCC	V_{CC_CORE}	V2
VCC	V_{CC_CORE}	V4

Table 18. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin
VCC	V_{CC_CORE}	V6
VCC	V_{CC_CORE}	V8
VCC	V_{CC_CORE}	X30
VCC	V_{CC_CORE}	X32
VCC	V_{CC_CORE}	X34
VCC	V_{CC_CORE}	X36
VCC	V_{CC_CORE}	Z2
VCC	V_{CC_CORE}	Z4
VCC	V_{CC_CORE}	Z6
VCC	V_{CC_CORE}	Z8
VCC	V_{CC_CORE}	AB30
VCC	V_{CC_CORE}	AB32
VCC	V_{CC_CORE}	AB34
VCC	V_{CC_CORE}	AB36
VCC	V_{CC_CORE}	AD2
VCC	V_{CC_CORE}	AD4
VCC	V_{CC_CORE}	AD6
VCC	V_{CC_CORE}	AF14
VCC	V_{CC_CORE}	AF18
VCC	V_{CC_CORE}	AF22
VCC	V_{CC_CORE}	AF26
VCC	V_{CC_CORE}	AF34
VCC	V_{CC_CORE}	AF36
VCC	V_{CC_CORE}	AH2
VCC	V_{CC_CORE}	AH4
VCC	V_{CC_CORE}	AH10
VCC	V_{CC_CORE}	AH14
VCC	V_{CC_CORE}	AH18
VCC	V_{CC_CORE}	AH22
VCC	V_{CC_CORE}	AH26
VCC	V_{CC_CORE}	AK10
VCC	V_{CC_CORE}	AK14
VCC	V_{CC_CORE}	AK18
VCC	V_{CC_CORE}	AK22
VCC	V_{CC_CORE}	AK26
VCC	V_{CC_CORE}	AK30
VCC	V_{CC_CORE}	AK34
VCC	V_{CC_CORE}	AK36
VCC	V_{CC_CORE}	AJ5
VCC	V_{CC_CORE}	AL5
VCC	V_{CC_CORE}	AM2
VCC	V_{CC_CORE}	AM10
VCC	V_{CC_CORE}	AM14
VCC	V_{CC_CORE}	AM18
VCC	V_{CC_CORE}	AM22
VCC	V_{CC_CORE}	AM26
VCC	V_{CC_CORE}	AM22
VCC	V_{CC_CORE}	AM26
VCC	V_{CC_CORE}	AM30
VCC	V_{CC_CORE}	AM34
	VCCA	AJ23
	VID[0]	L1
	VID[1]	L3
	VID[2]	L5
	VID[3]	L7
	VID[4]	J7
VREF_S	VREF_SYS	W5
	VSS	B2
	VSS	B6
	VSS	B10
	VSS	B14
	VSS	B18
	VSS	B22
	VSS	B26
	VSS	B30
	VSS	B34
	VSS	D6
	VSS	D10
	VSS	D14
	VSS	D18

Table 18. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	VSS	D22		VSS	V32
	VSS	D26		VSS	V34
	VSS	D30		VSS	V36
	VSS	D34		VSS	X2
	VSS	D36		VSS	X4
	VSS	F2		VSS	X6
	VSS	F4		VSS	X8
	VSS	F6		VSS	Z30
	VSS	F10		VSS	Z32
	VSS	F14		VSS	Z34
	VSS	F18		VSS	Z36
	VSS	F22		VSS	AB2
	VSS	F26		VSS	AB8
	VSS	H14		VSS	AB4
	VSS	H18		VSS	AB6
	VSS	H22		VSS	AD32
	VSS	H26		VSS	AD34
	VSS	H34		VSS	AD36
	VSS	H36		VSS	AF2
	VSS	K2		VSS	AF4
	VSS	K4		VSS	AF12
	VSS	K6		VSS	AF16
	VSS	M30		VSS	AH12
	VSS	M32		VSS	AH16
	VSS	M34		VSS	AH20
	VSS	M36		VSS	AH24
	VSS	P2		VSS	AH28
	VSS	P4		VSS	AH32
	VSS	P6		VSS	AH34
	VSS	P8		VSS	AH36
	VSS	R30		VSS	AK2
	VSS	R32		VSS	AK4
	VSS	R34		VSS	AK12
	VSS	R36		VSS	AK16
	VSS	T2		VSS	AK20
	VSS	T4		VSS	AK24
	VSS	T6		VSS	AK28
	VSS	T8		VSS	AK32
	VSS	V30		VSS	AM4

Table 18. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin
	VSS	AM6
	VSS	AM12
	VSS	AM16
	VSS	AM20
	VSS	AM24
	VSS	AM28
	VSS	AM32
	VSS	AM36
	ZN	AC5
	ZP	AE5

10.2 Pin List

Table 19 on page 58 cross-references Socket A pin location to signal name.

The “L” (Level) column shows the electrical specification for this pin. “P” indicates a push-pull mode driven by a single source. “O” indicates open-drain mode that allows devices to share the pin.

Note: *The AMD Athlon processor supports push-pull drivers. For more information, see “Push-Pull (PP) Drivers” on page 6.*

The “P” (Port) column indicates if this signal is an input (I), output (O), or bidirectional (B) signal. The “R” (Reference) column indicates if this signal should be referenced to VSS (G) or VCC_CORE (P) planes for the purpose of signal routing with respect to the current return paths.

Table 19. Cross-Reference by Pin Location

Pin	Name	Description	L	P	R
A1	No Pin	page 69	-	-	-
A3	SADDOUT[12]#		P	O	G
A5	SADDOUT[5]#		P	O	G
A7	SADDOUT[3]#		P	O	G
A9	SDATA[55]#		P	B	P
A11	SDATA[61]#		P	B	P
A13	SDATA[53]#		P	B	G
A15	SDATA[63]#		P	B	G
A17	SDATA[62]#		P	B	G
A19	NC Pin	page 69	-	-	-
A21	SDATA[57]#		P	B	G
A23	SDATA[39]#		P	B	G
A25	SDATA[35]#		P	B	P
A27	SDATA[34]#		P	B	P
A29	SDATA[44]#		P	B	G
A31	NC Pin	page 69	-	-	-
A33	SDATAOUTCLK[2]#		P	O	P
A35	SDATA[40]#		P	B	G
A37	SDATA[30]#		P	B	P
B2	VSS		-	-	-
B4	V_{CC_CORE}		-	-	-
B6	VSS		-	-	-
B8	V_{CC_CORE}		-	-	-
B10	VSS		-	-	-
B12	V_{CC_CORE}		-	-	-
B14	VSS		-	-	-
B16	V_{CC_CORE}		-	-	-
B18	VSS		-	-	-
B20	V_{CC_CORE}		-	-	-
B22	VSS		-	-	-
B24	V_{CC_CORE}		-	-	-
B26	VSS		-	-	-
B28	VCC_CORE		-	-	-
B30	VSS		-	-	-
B32	V_{CC_CORE}		-	-	-
B34	VSS		-	-	-
B36	V_{CC_CORE}		-	-	-
C1	SADDOUT[7]#		P	O	G
C3	SADDOUT[9]#		P	O	G
C5	SADDOUT[8]#		P	O	G
C7	SADDOUT[2]#		P	O	G
C9	SDATA[54]#		P	B	P
C11	SDATAOUTCLK[3]#		P	O	G
C13	NC Pin	page 69	-	-	-
C15	SDATA[51]#		P	B	P
C17	SDATA[60]#		P	B	G
C19	SDATA[59]#		P	B	G
C21	SDATA[56]#		P	B	G
C23	SDATA[37]#		P	B	P
C25	SDATA[47]#		P	B	G
C27	SDATA[38]#		P	B	G
C29	SDATA[45]#		P	B	G
C31	SDATA[43]#		P	B	G
C33	SDATA[42]#		P	B	G
C35	SDATA[41]#		P	B	G
C37	SDATAOUTCLK[1]#		P	O	G
D2	V_{CC_CORE}		-	-	-
D4	V_{CC_CORE}		-	-	-
D6	VSS		-	-	-
D8	V_{CC_CORE}		-	-	-
D10	VSS		-	-	-
D12	V_{CC_CORE}		-	-	-
D14	VSS		-	-	-
D16	V_{CC_CORE}		-	-	-
D18	VSS		-	-	-
D20	V_{CC_CORE}		-	-	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
D22	VSS		-	-	-
D24	V_{CC_CORE}		-	-	-
D26	VSS		-	-	-
D28	V_{CC_CORE}		-	-	-
D30	VSS		-	-	-
D32	V_{CC_CORE}		-	-	-
D34	VSS		-	-	-
D36	VSS		-	-	-
E1	SADDOUT[11]#		P	O	P
E3	SADDOUTCLK#		P	O	G
E5	SADDOUT[4]#		P	O	P
E7	SADDOUT[6]#		P	O	G
E9	SDATA[52]#		P	B	P
E11	SDATA[50]#		P	B	P
E13	SDATA[49]#		P	B	G
E15	SDATAINCLK[3]#		P	I	G
E17	SDATA[48]#		P	B	P
E19	SDATA[58]#		P	B	G
E21	SDATA[36]#		P	B	P
E23	SDATA[46]#		P	B	P
E25	NC Pin	page 69	-	-	-
E27	SDATAINCLK[2]#		P	I	G
E29	SDATA[33]#		P	B	P
E31	SDATA[32]#		P	B	P
E33	NC Pin	page 69	-	-	-
E35	SDATA[31]#		P	B	P
E37	SDATA[22]#		P	B	G
F2	VSS		-	-	-
F4	VSS		-	-	-
F6	VSS		-	-	-
F8	NC Pin	page 69	-	-	-
F10	VSS		-	-	-
F12	V_{CC_CORE}		-	-	-
F14	VSS		-	-	-
F16	VC_{CC_CORE}		-	-	-
F18	VSS		-	-	-
F20	V_{CC_CORE}		-	-	-
F22	VSS		-	-	-
F24	V_{CC_CORE}		-	-	-
F26	VSS		-	-	-
F28	V_{CC_CORE}		-	-	-
F30	NC Pin	page 69	-	-	-
F32	V_{CC_CORE}		-	-	-
F34	V_{CC_CORE}		-	-	-
F36	V_{CC_CORE}		-	-	-
G1	SADDOUT[10]#		P	O	P
G3	SADDOUT[14]#		P	O	G
G5	SADDOUT[13]#		P	O	G
G7	Key Pin	page 69	-	-	-
G9	Key Pin	page 69	-	-	-
G11	NC Pin	page 69	-	-	-
G13	NC Pin	page 69	-	-	-
G15	Key Pin	page 69	-	-	-
G17	Key Pin	page 69	-	-	-
G19	NC Pin	page 69	-	-	-
G21	NC Pin	page 69	-	-	-
G23	Key Pin	page 69	-	-	-
G25	Key Pin	page 69	-	-	-
G27	NC Pin	page 69	-	-	-
G29	NC Pin	page 69	-	-	-
G31	NC Pin	page 69	-	-	-
G33	SDATA[20]#		P	B	G
G35	SDATA[23]#		P	B	G
G37	SDATA[21]#		P	B	G
H2	V_{CC_CORE}		-	-	-
H4	V_{CC_CORE}		-	-	-
H6	NC Pin	page 69	-	-	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
H8	NC Pin	page 69	-	-	-
H10	NC Pin	page 69	-	-	-
H12	V_{CC_CORE}		-	-	-
H14	VSS		-	-	-
H16	V_{CC_CORE}		-	-	-
H18	VSS		-	-	-
H20	V_{CC_CORE}		-	-	-
H22	VSS		-	-	-
H24	V_{CC_CORE}		-	-	-
H26	VSS		-	-	-
H28	NC Pin	page 69	-	-	-
H30	NC Pin	page 69	-	-	-
H32	NC Pin	page 69	-	-	-
H34	VSS		-	-	-
H36	VSS		-	-	-
J1	SADDOUT[0]#	page 70	P	O	-
J3	SADDOUT[1]#	page 70	P	O	-
J5	NC Pin	page 69	-	-	-
J7	VID[4]	page 70	O	O	-
J31	NC Pin	page 69	-	-	-
J33	SDATA[19]#		P	B	G
J35	SDATAINCLK[1]#		P	I	P
J37	SDATA[29]#		P	B	P
K2	VSS		-	-	-
K4	VSS		-	-	-
K6	VSS		-	-	-
K8	NC Pin	page 69	-	-	-
K30	NC Pin	page 69	-	-	-
K32	V_{CC_CORE}		-	-	-
K34	V_{CC_CORE}		-	-	-
K36	V_{CC_CORE}		-	-	-
L1	VID[0]	page 70	O	O	-
L3	VID[1]	page 70	O	O	-
L5	VID[2]	page 70	O	O	-
L7	VID[3]	page 70	O	O	-
L31	NC Pin	page 69	-	-	-
L33	SDATA[26]#		P	B	P
L35	NC Pin	page 69	-	-	-
L37	SDATA[28]#		P	B	P
M2	V_{CC_CORE}		-	-	-
M4	V_{CC_CORE}		-	-	-
M6	V_{CC_CORE}		-	-	-
M8	V_{CC_CORE}		-	-	-
M30	VSS		-	-	-
M32	VSS		-	-	-
M34	VSS		-	-	-
M36	VSS		-	-	-
N1	PICCLK	page 65	O	I	-
N3	PICD#[0]	page 65	O	B	-
N5	PICD#[1]	page 65	O	B	-
N7	Key Pin	page 69	-	-	-
N31	NC Pin	page 69	-	-	-
N33	SDATA[25]#		P	B	P
N35	SDATA[27]#		P	B	P
N37	SDATA[18]#		P	B	G
P2	VSS		-	-	-
P4	VSS		-	-	-
P6	VSS		-	-	-
P8	VSS		-	-	-
P30	V_{CC_CORE}		-	-	-
P32	V_{CC_CORE}		-	-	-
P34	V_{CC_CORE}		-	-	-
P36	V_{CC_CORE}		-	-	-
Q1	TCK	page 69	P	I	-
Q3	TMS	page 69	P	I	-
Q5	SCANSHIFTEN	page 70	P	I	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
Q7	Key Pin	page 69	-	-	-	U31	NC Pin	page 69	-	-	-
Q31	NC Pin	page 69	-	-	-	U33	SDATA[5]#		P	B	G
Q33	SDATA[24]#		P	B	P	U35	SDATA[4]#		P	B	G
Q35	SDATA[17]#		P	B	G	U37	NC Pin	page 69	-	-	-
Q37	SDATA[16]#		P	B	G	V2	V_{CC_CORE}		-	-	-
R2	V_{CC_CORE}		-	-	-	V4	V_{CC_CORE}		-	-	-
R4	V_{CC_CORE}		-	-	-	V6	V_{CC_CORE}		-	-	-
R6	V_{CC_CORE}		-	-	-	V8	V_{CC_CORE}		-	-	-
R8	V_{CC_CORE}		-	-	-	V30	VSS		-	-	-
R30	VSS		-	-	-	V32	VSS		-	-	-
R32	VSS		-	-	-	V34	VSS		-	-	-
R34	VSS		-	-	-	V36	VSS		-	-	-
R36	VSS		-	-	-	W1	FID[0]	page 67	O	O	-
S1	SCANCLK1	page 70	P	I	-	W3	FID[1]	page 67	O	O	-
S3	SCANINTEVAL	page 70	P	I	-	W5	VREFSYS	page 71	P	-	-
S5	SCANCLK2	page 70	P	I	-	W7	NC Pin	page 69	-	-	-
S7	THERMDA	page 70	-	-	-	W31	NC Pin	page 69	-	-	-
S31	NC Pin	page 69	-	-	-	W33	SDATAINCLK[0]#		P	I	G
S33	SDATA[7]#		P	B	G	W35	SDATA[2]#		P	B	G
S35	SDATA[15]#		P	B	P	W37	SDATA[1]#		P	B	P
S37	SDATA[6]#		P	B	G	X2	VSS		-	-	-
T2	VSS		-	-	-	X4	VSS		-	-	-
T4	VSS		-	-	-	X6	VSS		-	-	-
T6	VSS		-	-	-	X8	VSS		-	-	-
T8	VSS		-	-	-	X30	V_{CC_CORE}		-	-	-
T30	V_{CC_CORE}		-	-	-	X32	V_{CC_CORE}		-	-	-
T32	V_{CC_CORE}		-	-	-	X34	V_{CC_CORE}		-	-	-
T34	V_{CC_CORE}		-	-	-	X36	V_{CC_CORE}		-	-	-
T36	V_{CC_CORE}		-	-	-	Y1	FID[2]	page 67	O	O	-
U1	TDI	page 69	P	I	-	Y3	FID[3]	page 67	O	O	-
U3	TRST#	page 69	P	I	-	Y5	NC Pin	page 69	-	-	-
U5	TDO	page 69	P	O	-	Y7	Key Pin	page 69	-	-	-
U7	THERMDC	page 70	-	-	-	Y31	NC Pin	page 69	-	-	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
Y33	NC Pin	page 69	-	-	-
Y35	SDATA[3]#		P	B	G
Y37	SDATA[12]#		P	B	P
Z2	V_{CC_CORE}		-	-	-
Z4	V_{CC_CORE}		-	-	-
Z6	V_{CC_CORE}		-	-	-
Z8	V_{CC_CORE}		-	-	-
Z30	VSS		-	-	-
Z32	VSS		-	-	-
Z34	VSS		-	-	-
Z36	VSS		-	-	-
AA1	DBRDY	page 66	P	O	-
AA3	DBREQ#	page 66	P	I	-
AA5	NC		-	-	-
AA7	Key Pin	page 69	-	-	-
AA31	NC Pin	page 69	-	-	-
AA33	SDATA[8]#		P	B	P
AA35	SDATA[0]#		P	B	G
AA37	SDATA[13]#		P	B	G
AB2	VSS		-	-	-
AB4	VSS		-	-	-
AB6	VSS		-	-	-
AB8	VSS		-	-	-
AB30	V_{CC_CORE}		-	-	-
AB32	V_{CC_CORE}		-	-	-
AB34	V_{CC_CORE}		-	-	-
AB36	V_{CC_CORE}		-	-	-
AC1	STPCLK#	page 70	P	I	-
AC3	PLLTEST#	page 69	P	I	-
AC5	ZN	page 71	P	-	-
AC7	NC		-	-	-
AC31	NC Pin	page 69	-	-	-
AC33	SDATA[10]#		P	B	P
AC35	SDATA[14]#		P	B	G
AC37	SDATA[11]#		P	B	G
AD2	V_{CC_CORE}		-	-	-
AD4	V_{CC_CORE}		-	-	-
AD6	V_{CC_CORE}		-	-	-
AD8	NC Pin	page 69	-	-	-
AD30	NC Pin	page 69	-	-	-
AD32	VSS		-	-	-
AD34	VSS		-	-	-
AD36	VSS		-	-	-
AE1	A20M#		P	I	-
AE3	PWROK		P	I	-
AE5	ZP	page 71	P	-	-
AE7	NC		-	-	-
AE31	NC Pin	page 69	-	-	-
AE33	SADDIN[5]#		P	I	G
AE35	SDATAOUTCLK[0]#		P	O	P
AE37	SDATA[9]#		P	B	G
AF2	VSS		-	-	-
AF4	VSS		-	-	-
AF6	NC Pin	page 69	-	-	-
AF8	NC Pin	page 69	-	-	-
AF10	NC Pin	page 69	-	-	-
AF12	VSS		-	-	-
AF14	V_{CC_CORE}		-	-	-
AF16	VSS		-	-	-
AF18	V_{CC_CORE}		-	-	-
AF20	VSS		-	-	-
AF22	V_{CC_CORE}		-	-	-
AF24	VSS		-	-	-
AF26	V_{CC_CORE}		-	-	-
AF28	NC Pin	page 69	-	-	-
AF30	NC Pin	page 69	-	-	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
AF32	NC Pin	page 69	-	-	-
AF34	V_{CC_CORE}		-	-	-
AF36	V_{CC_CORE}		-	-	-
AG1	FERR	page 66	P	O	-
AG3	RESET#		-	I	-
AG5	NC Pin	page 69	-	-	-
AG7	Key Pin	page 69	-	-	-
AG9	Key Pin	page 69	-	-	-
AG11	COREFB	page 66	-	-	-
AG13	COREFB#	page 66	-	-	-
AG15	Key Pin	page 69	-	-	-
AG17	Key Pin	page 69	-	-	-
AG19	NC Pin	page 69	-	-	-
AG21	NC Pin	page 69	-	-	-
AG23	NC Pin	page 69	-	-	-
AG25	NC Pin	page 69	-	-	-
AG27	Key Pin	page 69	-	-	-
AG29	Key Pin	page 69	-	-	-
AG31	FSB_Sense[0]	page 68	-	O	G
AG33	SADDIN[2]#		P	I	G
AG35	SADDIN[11]#		P	I	G
AG37	SADDIN[7]#		P	I	P
AH2	V_{CC_CORE}		-	-	-
AH4	V_{CC_CORE}		-	-	-
AH6	AMD Pin	page 65	-	-	-
AH8	NC Pin	page 69	-	-	-
AH10	V_{CC_CORE}		-	-	-
AH12	VSS		-	-	-
AH14	V_{CC_CORE}		-	-	-
AH16	VSS		-	-	-
AH18	V_{CC_CORE}		-	-	-
AH20	VSS		-	-	-
AH22	VV_{CC_CORE}		-	-	-
AH24	VSS		-	-	-
AH26	V_{CC_CORE}		-	-	-
AH28	VSS		-	-	-
AH30	FSB_Sense[1]	page 68	-	O	G
AH32	VSS		-	-	-
AH34	VSS		-	-	-
AH36	VSS		-	-	-
AJ1	IGNNE#	page 68	P	I	-
AJ3	INIT#	page 68	P	I	-
AJ5	V_{CC_CORE}		-	-	-
AJ7	NC Pin	page 69	-	-	-
AJ9	NC Pin	page 69	-	-	-
AJ11	NC Pin	page 69	-	-	-
AJ13	Analog	page 65	-	-	-
AJ15	NC Pin	page 69	-	-	-
AJ17	NC Pin	page 69	-	-	-
AJ19	NC Pin	page 69	-	-	-
AJ21	CLKFWDRST	page 65	P	I	P
AJ23	VCCA	page 70	-	-	-
AJ25	PLLBYPASS#	page 69	P	I	-
AJ27	NC Pin	page 69	-	-	-
AJ29	SADDIN[0]#	page 70	P	I	-
AJ31	SFILLVALID#		P	I	G
AJ33	SADDINCLK#		P	I	G
AJ35	SADDIN[6]#		P	I	P
AJ37	SADDIN[3]#		P	I	G
AK2	VSS		-	-	-
AK4	VSS		-	-	-
AK6	CPU_PRESENCE#	page 66	-	-	-
AK8	NC Pin	page 69	-	-	-
AK10	V_{CC_CORE}		-	-	-
AK12	VSS		-	-	-
AK14	V_{CC_CORE}		-	-	-
AK16	VSS		-	-	-

Table 19. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
AK18	V_{CC_CORE}		-	-	-
AK20	VSS		-	-	-
AK22	V_{CC_CORE}		-	-	-
AK24	VSS		-	-	-
AK26	V_{CC_CORE}		-	-	-
AK28	VSS		-	-	-
AK30	V_{CC_CORE}		-	-	-
AK32	VSS		-	-	-
AK34	V_{CC_CORE}		-	-	-
AK36	V_{CC_CORE}		-	-	-
AL1	INTR	page 68	P	I	-
AL3	FLUSH#	page 68	P	I	-
AL5	V_{CC_CORE}		-	-	-
AL7	NC Pin	page 69	-	-	-
AL9	NC Pin	page 69	-	-	-
AL11	NC Pin	page 69	-	-	-
AL13	PLLMON2	page 69	O	O	-
AL15	PLLBYPASSCLK#	page 69	P	I	-
AL17	CLKIN#	page 65	P	I	P
AL19	RSTCLK#	page 65	P	I	P
AL21	K7CLKOUT	page 69	P	O	-
AL23	CONNECT	page 66	P	I	P
AL25	NC Pin	page 69	-	-	-
AL27	NC Pin	page 69	-	-	-
AL29	SADDIN[1]#	page 70	P	I	-
AL31	SDATAOUTVALID#		P	O	P
AL33	SADDIN[8]#		P	I	P
AL35	SADDIN[4]#		P	I	G
AL37	SADDIN[10]#		P	I	G
AM2	V_{CC_CORE}		-	-	-
AM4	VSS		-	-	-
AM6	VSS		-	-	-
AM8	NC Pin	page 69	-	-	-
AM10	V_{CC_CORE}		-	-	-
AM12	VSS		-	-	-
AM14	V_{CC_CORE}		-	-	-
AM16	VSS		-	-	-
AM18	V_{CC_CORE}		-	-	-
AM20	VSS		-	-	-
AM22	V_{CC_CORE}		-	-	-
AM24	VSS		-	-	-
AM26	V_{CC_CORE}		-	-	-
AM28	VSS		-	-	-
AM30	V_{CC_CORE}		-	-	-
AM32	VSS		-	-	-
AM34	V_{CC_CORE}		-	-	-
AM36	VSS		-	-	-
AN1	No Pin	page 69	-	-	-
AN3	NMI		P	I	-
AN5	SMI#		P	I	-
AN7	NC Pin	page 69	-	-	-
AN9	NC Pin	page 69	-	-	-
AN11	NC Pin	page 69	-	-	-
AN13	PLLMON1	page 69	O	B	-
AN15	PLLBYPASSCLK	page 69	P	I	-
AN17	CLKIN	page 65	P	I	P
AN19	RSTCLK	page 65	P	I	P
AN21	K7CLKOUT#	page 69	P	O	-
AN23	PROCRDY		P	O	P
AN25	NC Pin	page 69	-	-	-
AN27	NC Pin	page 69	-	-	-
AN29	SADDIN[12]#		P	I	G
AN31	SADDIN[14]#		P	I	G
AN33	SDATAINVALID#		P	I	P
AN35	SADDIN[13]#		P	I	G
AN37	SADDIN[9]#		P	I	G

10.3 Detailed Pin Descriptions

The information in this section pertains to Table 19 on page 58.

A20M# Pin

A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.

AMD Pin

AMD Socket A processors do not implement a pin at location AH6. All Socket A designs must have a top plate or cover that blocks this pin location. When the cover plate blocks this location, a non-AMD part (e.g., PGA370) does not fit into the socket. However, socket manufacturers are allowed to have a contact loaded in the AH6 position. Therefore, motherboard socket design should account for the possibility that a contact could be loaded in this position.

AMD Athlon™ System Bus Pins

See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for information about the system bus pins—PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVALID#, SDATAOUTCLK[3:0]#, SDATAOUTVALID#, SFILLVALID#.

Analog Pin

Treat this pin as a NC.

APIC Pins, PICCLK, PICD[1:0]#

The Advanced Programmable Interrupt Controller (APIC) is a feature that provides a flexible and expandable means of delivering interrupts in a system using an AMD processor. The pins, PICD[1:0], are the bi-directional message-passing signals used for the APIC and are driven to the Southbridge or a dedicated I/O APIC. The pin, PICCLK, must be driven with a valid clock input.

For more information, see Table 15, “APIC Pin AC and DC Characteristics,” on page 38.

CLKFWDRST Pin

CLKFWDRST resets clock-forward circuitry for both the system and processor.

CLKIN, RSTCLK (SYSCLK) Pins

Connect CLKIN with RSTCLK and name it SYSCLK. Connect CLKIN# with RSTCLK# and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor.

See “SYSCLK and SYSCLK#” on page 70 for more information.

CONNECT Pin	CONNECT is an input from the system used for power management and clock-forward initialization at reset.
COREFB and COREFB# Pins	COREFB and COREFB# are outputs to the system that provide processor core voltage feedback to the system.
CPU_PRESENCE# Pin	CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# may be used to detect the presence or absence of a processor in the Socket A-style socket.
DBRDY and DBREQ# Pins	DBRDY and DBREQ# are routed to the debug connector. DBREQ# is tied to V_{CC_CORE} with a pullup resistor.
FERR Pin	FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is a push-pull active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the "Required Circuits" chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

FID[3:0] Pins

FID[3] (Y3), FID[2] (Y1), FID[1] (W3), and FID[0] (W1) are the 4-bit processor clock-to-SYSCLK ratio.

Table 20 describes the encodings of the clock multipliers on FID[3:0].

Table 20. FID[3:0] Clock Multiplier Encodings

FID[3:0][2]	Processor Clock to SYSCLK Frequency Ratio
0000	11
0001	11.5
0010	12
0011	≥ 12.5[1]
0100	5
0101	5.5
0110	6
0111	6.5
1000	7
1001	7.5
1010	8
1011	8.5
1100	9
1101	9.5
1110	10
1111	10.5

Notes:

1. *All ratios greater than or equal to 12.5x have the same FID[3:0] code of 0011b, which causes the SIP configuration for all ratios of 12.5x or greater to be the same.*
2. *BIOS initializes the CLK_Ctl MSR during the POST routine. This CLK_Ctl setting is used with all FID combinations and selects a Halt disconnect divisor and a Stop Grant disconnect divisor. For more information, refer to the* AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656.*

The FID[3:0] signals are open-drain processor outputs that are pulled High on the motherboard and sampled by the chipset to determine the SIP (Serialization Initialization Packet) that is sent to the processor. The FID[3:0] signals are valid after PWROK is asserted. The FID[3:0]signals must not be sampled until they become valid. See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for more information about Serialization Initialization Packets and SIP protocol.

The processor FID[3:0] outputs are open-drain and 2.5-V tolerant. To prevent damage to the processor, if these signals are pulled High to above 2.5 V, they must be electrically isolated from the processor. For information about the FID[3:0] isolation circuit, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

See "Frequency Identification (FID[3:0])" on page 25 for the DC characteristics for FID[3:0].

FSB_Sense[1:0] Pins

FSB_Sense[1:0] pins are either open circuit (logic level of 1) or are pulled to ground (logic level of 0) on the processor package with a 1 kΩ resistor. In conjunction with a circuit on the motherboard, these pins may be used to automatically detect the front side bus (FSB) setting of this processor. Proper detection of the FSB setting requires the implementation of a pull-up resistor on the motherboard. Refer to the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363 and the technical note *FSB_Sense Auto Detection Circuitry for Desktop Processors*, order# TN26673 for more information.

Table 21 is the truth table to determine the FSB of desktop processors.

Table 21. Front Side Bus Sense Truth Table

FSB_Sense[1]	FSB_Sense[0]	Bus Frequency
1	0	RESERVED
1	1	133 MHz
0	1	166 MHz
0	0	RESERVED

The FSB_Sense[1:0] pins are 3.3-V tolerant.

FLUSH# Pin

FLUSH# must be tied to V_{CC_CORE} with a pullup resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.

IGNNE# Pin

IGNNE# is an input from the system that tells the processor to ignore numeric errors.

INIT# Pin

INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0_FFFF_FFF0h.

INTR Pin

INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.

JTAG Pins

TCK, TMS, TDI, TRST#, and TDO are the JTAG interface. Connect these pins directly to the motherboard debug connector. Pull TDI, TCK, TMS, and TRST# up to V_{CC_CORE} with pullup resistors.

K7CLKOUT and K7CLKOUT# Pins

K7CLKOUT and K7CLKOUT# are each run for two to three inches and then terminated with a resistor pair: 100 ohms to V_{CC_CORE} and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and V_{CC_CORE} /2.

Key Pins

These 16 locations are for processor type keying for forwards and backwards compatibility (G7, G9, G15, G17, G23, G25, N7, Q7, Y7, AA7, AG7, AG9, AG15, AG17, AG27, and AG29). Motherboard designers should treat key pins like NC (No Connect) pins. A socket designer has the option of creating a top mold piece that allows PGA key pins only where designated. However, sockets that populate all 16 key pins must be allowed, so the motherboard must always provide for pins at all key pin locations.

See “NC Pins“ for more information.

NC Pins

The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.

NMI Pin

NMI is an input from the system that causes a non-maskable interrupt.

PGA Orientation Pins

No pin is present at pin locations A1 and AN1. Motherboard designers should not allow for a PGA socket pin at these locations.

For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

PLL Bypass and Test Pins

PLLTEST#, PLLBYPASS#, PLLMON1, PLLMON2, PLLBYPASSCLK, and PLLBYPASSCLK# are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to V_{CC_CORE} with pullup resistors.

PWROK Pin

The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification.

For more information, Chapter 8, “Signal and Power-Up Requirements” on page 39.

SADDIN[1:0]# and SADDOUT[1:0]# Pins	The AMD Athlon XP processor model 10 does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to VCC with pullup resistors, if this bit is not supported by the Northbridge (future models can support SADDIN[1]#). SADDOUT[1:0]# are tied to VCC with pullup resistors if these pins are supported by the Northbridge. For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.
Scan Pins	SCANSHIFTEN, SCANCLK1, SCANINTEVAL, and SCANCLK2 are the scan interface. This interface is AMD internal and is tied disabled with pulldown resistors to ground on the motherboard.
SMI# Pin	SMI# is an input that causes the processor to enter the system management mode.
STPCLK# Pin	STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.
SYSCLK and SYSCLK#	SYSCLK and SYSCLK# are differential input clock signals provided to the PLL of the processor from a system-clock generator. See “CLKIN, RSTCLK (SYSCLK) Pins” on page 65 for more information.
THERMDA and THERMDC Pins	Thermal Diode anode and cathode pins are used to monitor the actual temperature of the processor die, providing more accurate temperature control to the system. See Table 13, “Thermal Diode Electrical Characteristics,” on page 36 for more information.
VCCA Pin	VCCA is the processor PLL supply. For information about the VCCA pin, see Table 5, “VCCA AC and DC Characteristics,” on page 35 and the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.
VID[4:0] Pins	The VID[4:0] (Voltage Identification) outputs are used to dictate the V_{CC_CORE} voltage level. The VID[4:0] pins are strapped to ground or left unconnected on the processor package. The VID[4:0] pins are pulled-up on the motherboard and used by the V_{CC_CORE} DC/DC converter. For more information, see Table 22, “VID[4:0] Code to Voltage Definition,” on page 71.

Table 22. VID[4:0] Code to Voltage Definition

VID[4:0]	V_{CC_CORE} (V)	VID[4:0]	V_{CC_CORE} (V)
00000	1.850	10000	1.450
00001	1.825	10001	1.425
00010	1.800	10010	1.400
00011	1.775	10011	1.375
00100	1.750	10100	1.350
00101	1.725	10101	1.325
00111	1.675	10111	1.275
01000	1.650	11000	1.250
01001	1.625	11001	1.225
01010	1.600	11010	1.200
01011	1.575	11011	1.175
01100	1.550	11100	1.150
01101	1.525	11101	1.125
01110	1.500	11110	1.100
01111	1.475	11111	No CPU

For more information, see the “Required Circuits” chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

VREFSYS Pin

VREFSYS (W5) drives the threshold voltage for the system bus input receivers. The value of VREFSYS is system specific. In addition, to minimize V_{CC_CORE} noise rejection from VREFSYS, include decoupling capacitors. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

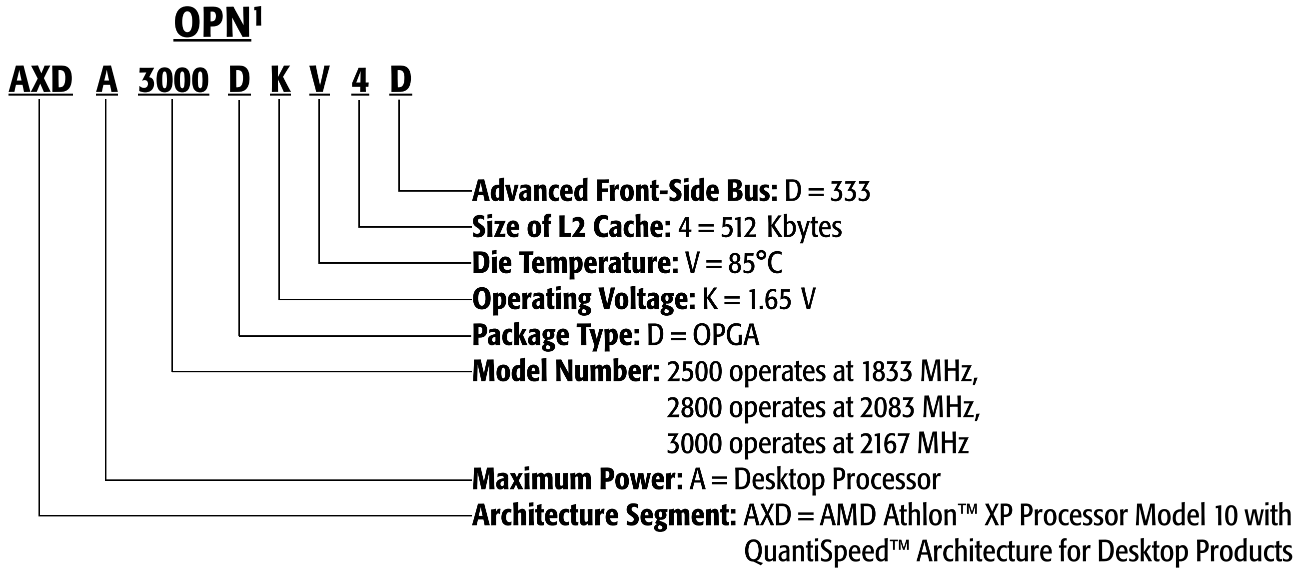
ZN and ZP Pins

ZN (AC5) and ZP (AE5) are the push-pull compensation circuit pins. In Push-Pull mode (selected by the SIP parameter SysPushPull asserted), ZN is tied to V_{CC_CORE} with a resistor that has a resistance matching the impedance Z_0 of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance Z_0 of the transmission line.

11 Ordering Information

Standard AMD Athlon™ XP Processor Model 10 Products

AMD standard products are available in several operating ranges. The ordering part numbers (OPN) are formed by a combination of the elements, as shown in Figure 16.



OPN[1]

AXD A 3000 D K V 4 D

Advanced Front-Side Bus: D = 333
Size of L2 Cache: 4 = 512 Kbytes
Die Temperature: V = 85°C
Operating Voltage: K = 1.65 V
Package Type: D = OPGA
Model Number: 2500 operates at 1833 MHz,
2800 operates at 2083 MHz,
3000 operates at 2167 MHz
Maximum Power: A = Desktop Processor
Architecture Segment: AXD = AMD Athlon™ XP Processor Model 10 with QuantiSpeed™ Architecture for Desktop Products

Note:

1. Spaces are added to the number shown above for viewing clarity only.

Figure 16. OPN Example for the AMD Athlon™ XP Processor Model 10

Appendix A

Thermal Diode Calculations

This section contains information about the calculations for the on-die thermal diode of the AMD Athlon™ XP processor model 10. For electrical information about this thermal diode, see Table 13, “Thermal Diode Electrical Characteristics,” on page 36.

Ideal Diode Equation

The ideal diode equation uses the variables and constants defined in Table 23.

Table 23. Constants and Variables for the Ideal Diode Equation

Equation Symbol	Variable, Constant Description
$n_{f,\ \text{lumped}}$	Lumped ideality factor
k	Boltzmann constant
q	Electron charge constant
T	Diode temperature (Kelvin)
V_{BE}	Voltage from base to emitter
I_C	Collector current
I_S	Saturation current

Equation (1) shows the ideal diode calculation.

$$V_{BE} = n_{f,\,lumped} \cdot \frac{k}{q} \cdot T \cdot \ln\left(\frac{I_C}{I_S}\right) \qquad \textbf{(1)}$$

Sourcing two currents and using Equation (1) derives the difference in the base-to-emitter voltage that leads to finding the diode temperature as shown in Equation (2). The use of dual sourcing currents allows the measurement of the thermal diode temperature to be more accurate and less susceptible to die and process revisions. Temperature sensors that utilize series resistance cancellation can use more than two sourcing currents and are suitable to be used with the AMD thermal diode. Equation (2) is the formula for calculating the temperature of a thermal diode.

$$T = \frac{V_{BE,\,high} - V_{BE,\,low}}{n_{f,\,lumped} \cdot \frac{k}{q} \cdot \ln\left(\frac{I_{high}}{I_{low}}\right)} \qquad \textbf{(2)}$$

Temperature Offset Correction

A temperature offset may be required to correct the value measured by a temperature sensor. An offset is necessary if a difference exists between the lumped ideality factor of the processor and the ideality factor assumed by the temperature sensor. The lumped ideality factor can be calculated using the equations in this section to find the temperature offset that should be used with the temperature sensor.

Table 24 shows the constants and variables used to calculate the temperature offset correction.

Table 24. Constants and Variables Used in Temperature Offset Equations

Equation Symbol	Variable, Constant Description
$n_{f,\,actual}$	Actual ideality factor
$n_{f,\,lumped}$	Lumped ideality factor
$n_{f,\,TS}$	Ideality factor assumed by temperature sensor
I_{high}	High sourcing current
I_{low}	Low sourcing current
$T_{die,\,spec}$	Die temperature specification
T_{offset}	Temperature offset

The formulas in Equation (3) and Equation (4) can be used to calculate the temperature offset for temperature sensors that do not employ series resistance cancellation. The result is added to the value measured by the temperature sensor. Contact the vendor of the temperature sensor being used for the value of $n_{f,TS}$. Refer to the document, *On-Die Thermal Diode Characterization*, order# 25443, for further details.

Equation (3) shows the equation for calculating the lumped ideality factor ($n_{f,\ lumped}$) in sensors that do not employ series resistance cancellation.

$$n_{f,\,lumped} = n_{f,\,actual} + \frac{R_T \cdot (I_{high} - I_{low})}{\frac{k}{q}(T_{die,\,spec} + 273.15) \cdot \ln\left(\frac{I_{high}}{I_{low}}\right)} \qquad \textbf{(3)}$$

Equation (4) shows the equation for calculating temperature offset (T_{offset}) in sensors that do not employ series resistance cancellation.

$$T_{offset} = (T_{die,\,spec} + 273.15) \cdot \left(1 - \frac{n_{f,\,lumped}}{n_{f,\,TS}}\right) \qquad \textbf{(4)}$$

Equation (5) is the temperature offset for temperature sensors that utilize series resistance cancellation. Add the result to the value measured by the temperature sensor. Note that the value of $n_{f,TS}$ in Equation (5) may not equal the value used in Equation (4).

$$T_{offset} = (T_{die,\,spec} + 273.15) \cdot \left(1 - \frac{n_{f,\,actual}}{n_{f,\,TS}}\right) \qquad \textbf{(5)}$$

Appendix B

Conventions and Abbreviations

This section contains information about the conventions and abbreviations used in this document.

Signals and Bits

- Active-Low Signals—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- Three-State—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.

- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

  See Table 25 on page 81 for more abbreviations.
- Little-Endian Convention—The byte with the address xx...xx00 is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

Abbreviations and Acronyms

Table 25 contains the definitions of abbreviations used in this document.

Table 25. Abbreviations

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga-
Gbit	Gigabit
Gbyte	Gigabyte
GHz	Gigahertz
H	Henry
h	Hexadecimal
K	Kilo-
Kbyte	Kilobyte
lbf	Foot-pound
M	Mega-
Mbit	Megabit
Mbyte	Megabyte
MHz	Megahertz
m	Milli-
ms	Millisecond
mW	Milliwatt
µ	Micro-
µA	Microampere
µF	Microfarad
µH	Microhenry
µs	Microsecond
µV	Microvolt
n	nano-
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond
ohm	Ohm

Table 25. Abbreviations (continued)

Abbreviation	Meaning
p	pico-
pA	picoampere
pF	picofarad
pH	picohenry
ps	picosecond
s	Second
V	Volt
W	Watt

Table 26 contains the definitions of acronyms used in this document.

Table 26. Acronyms

Abbreviation	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
CPGA	Ceramic Pin Grid Array
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
FIFO	First In, First Out
GART	Graphics Address Remapping Table
HSTL	High-Speed Transistor Logic
IDE	Integrated Device Electronics

Table 26. Acronyms (continued)

Abbreviation	Meaning
ISA	Industry Standard Architecture
IPC	Instructions Per Cycle
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LAN	Large Area Network
LRU	Least-Recently Used
LVTTL	Low Voltage Transistor Transistor Logic
MSB	Most Significant Bit
MTRR	Memory Type and Range Registers
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OD	Open-Drain
OPGA	Organic Pin Grid Array
PA	Physical Address
PBGA	Plastic Ball Grid Array
PCI	Peripheral Component Interconnect
PDE	Page Directory Entry
PDT	Page Directory Table
PGA	Pin Grid Array
PLL	Phase Locked Loop
PMSM	Power Management State Machine
POS	Power-On Suspend
POST	Power-On Self-Test
PP	Push-Pull
RAM	Random Access Memory
ROM	Read Only Memory
RXA	Read Acknowledge Queue
SCSI	Small Computer System Interface
SDI	System DRAM Interface
SDRAM	Synchronous Direct Random Access Memory
SIMD	Single Instruction Multiple Data
SIP	Serial Initialization Packet
SMbus	System Management Bus
SPD	Serial Presence Detect

Table 26. Acronyms (continued)

Abbreviation	Meaning
SRAM	Synchronous Random Access Memory
SROM	Serial Read Only Memory
TLB	Translation Lookaside Buffer
TOM	Top of Memory
TTL	Transistor Transistor Logic
VAS	Virtual Address Space
VPA	Virtual Page Address
VGA	Video Graphics Adapter
USB	Universal Serial Bus
ZDB	Zero Delay Buffer

Related Publications

These documents provide helpful information about the AMD Athlon™ XP processor model 10, and can be found with other related documents at the AMD Web site, *http://www.amd.com*.

- *AMD Athlon™ Processor x86 Code Optimization Guide,* order# 22007
- *AMD Processor Recognition Application Note,* order# 20734
- *Methodologies for Measuring Temperature on AMD Athlon™ and AMD Duron™ Processors,* order# 24228
- *AMD Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794
- *Builders Guide for Desktop/Tower Systems*, order# 26003

Other Web sites of interest include the following:

- JEDEC home page—www.jedec.org
- IEEE home page—www.computer.org
- AGP Forum—www.agpforum.or