August 2000 • NREL/SR-520-28783

Subcontractor Report

Optimization of Processing and Modeling Issues for Thin Film Solar Cell Devices Including Concepts for the Development of Polycrystalline Multijunctions

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24 August 1998—23 August 1999

R.W. Birkmire, J.E. Phillips, W.N. Shafarman, E. Eser, S.S. Hegedus, B.E. McCandless
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Newark, Delaware

National Renewable Energy Laboratory

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Contract No. DE-AC36-99-GO10337

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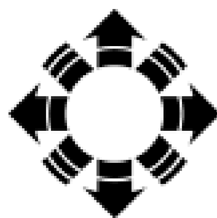
Prepared under Subcontract No. ZAK-8-17619-33



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SUMMARY

The overall mission of the Institute of Energy Conversion is the development of thin film photovoltaic cells, modules, and related manufacturing technology and the education of students and professionals in photovoltaic technology. The objectives of this 12 month NREL subcontract are to advance the state of the art and the acceptance of thin film PV solar cells in the areas of improved technology for thin film deposition, device fabrication, and material and device characterization and modeling, relating to solar cells based on $CuInSe_2$ and its alloys, on a-Si and its alloys, and on CdTe.

$CuInSe_2$-BASED SOLAR CELLS

CIS-based Solar Cells with Improved Manufacturability

For solar cells based on thin film $Cu(InGa)Se_2$ to become a commercially viable technology, manufacturing costs must be reduced. One means to accomplish this is by reducing the substrate temperature at which the $Cu(InGa)Se_2$ layer is deposited

This report addresses material and device issues related to reducing T_{ss} from 550˚C to 400˚C for the deposition of $Cu(InGa)Se_2$ by physical vapor deposition using multisource elemental evaporation. The $CuInGaSe_2$ deposition sequence was varied to determine the effect of a Cu-rich growth step, i.e., deposition with the Cu molar flux greater than the sum of the In and Ga fluxes. The connection between grain size, morphology, compositional uniformity, and device performance, as they are affected by substrate temperature and growth process, was investigated. The objective was to develop a process for improved device performance with T_{ss} = 400˚C.

Device results with T_{ss} = 400˚C show that a Cu-rich growth step during the $Cu(InGa)Se_2$ deposition is needed for improved device performance. However, the film and device results are the same whether the Cu-rich growth occurs during the initial nucleation or later in the process. This indicates tolerance to different process sequences, which allows flexibility in deposition process design.

Films grown at 550˚C have larger grains and give better performance than films deposited at 400˚C. But, with a given substrate temperature there is no simple correlation between grain size and device performance. At the lower temperature the improved cell results with Cu-rich growth cannot be explained by increased lateral grain size at the surface. Conversely, at the higher temperature, the increased grain size with the Cu-rich growth does not provide improved device performance.

At T_{ss} = 550˚C, the device performance is insensitive to the use of Cu-rich growth. A simple process with constant fluxes throughout the deposition gives as high a device efficiency as processes incorporating graded fluxes to give Cu-rich growth. At 400˚C, the uniform process gives more columnar grains but the same lateral grain size as the graded, Cu-rich processes. However, the best devices result from Cu-rich growth although not necessarily during the initial film nucleation.

In-line Evaporation of $Cu(InGa)Se_2$

In-line evaporation is a potentially effective means to achieve the high rate uniform deposition necessary for commercial-scale manufacture of CIGS modules. In this process, the substrate is linearly translated over thermal sources from which the elemental materials are evaporated.

The Institute of Energy Conversion has co-developed and installed an in-line deposition system for CIGS processing. The IEC system is configured to handle a rigid substrate with uniform deposition of Cu, In, Ga and Se. The sequencing and spacing of the sources can be varied to allow different relative flux profiles to be investigated. To date, the in-line system has been installed at IEC. Cu, In and Ga effusion sources have been developed, demonstrated and calibrated. Software for vacuum system and substrate drive control has been developed.

High Bandgap Alloys of $Cu(In,Ga)(S,Se)_2$

It has been demonstrated previously at IEC that the loss in efficiency of $Cu(In,Ga)Se_2$ solar cells with increasing Ga content is due to a decrease in fill factor, and to a lesser extent V_{oc} which is caused by a drop in the light generated current with increasing forward voltage.

Devices were fabricated with semi-transparent (0.04 μm) Mo contacts. Bi-facial spectral response measurements were made as a function of bias voltage and analyzed in order to determine the changes in collection efficiency as a function of changing Ga composition and applied voltage.

Analysis of these measurements on devices with increasing Ga content made as a function of light intensity have shown that the main cause of the decrease is a voltage dependent light generated current. Bi-facial spectral response measurements have shown that the minority carrier diffusion length decreases with increasing E_G, thereby making the minority carrier collection from the voltage dependent space charge region more important.

Sulfurization of Cu, In, and Cu/In Precursors

The incorporation of sulfur into $CuInSe_2$ thin films was quantitatively investigated to establish a scientific and engineering basis for the fabrication of homogeneous and compositionally graded $CuIn(Se,S)_2$ thin films. The approach taken was the reaction of thin-film Cu/In layers and $CuInSe_2$ thin films in H_2S and/or H_2Se gases at atmospheric pressure. This work was largely performed as the Ph.D. dissertation research of Michael Engelmann.

$CuIn(SeS)_2$ polycrystalline thin films were fabricated by reaction of layered Cu/In metal precursors in an H_2S:H_2Se:O_2:Ar atmosphere. The $H_2S/(H_2Se+H_2S)$ fraction was controlled and varied from 0.5 to 0.99 and temperature was maintained at 450˚C for all treatments. The solid phase composition of the $CuIn(Se,S)_2$ films after reaction for 120 minutes was found to correspond to the compositional dependence predicted by an equilibrium replacement reaction between H_2S-H_2Se and $CuInSe_2$-$CuInS_2$, including ideal and non-ideal mixing effects. This reaction was shown to strongly favor the presence of $CuInSe_2$ at 450˚C.

Based on these results, prediction and control of the bandgap in the fabrication of homogeneous films is possible. However, the use of hydride gases results in a high degree of compositional

sensitivity in the solid phase to the gas phase composition in the range of interest. Control of the flow rates becomes critical in this situation. With improved control of the gas phase composition, this method is feasible for the engineering of $CuIn(Se,S)_2$ to optimize the band gap for the solar spectrum.

$CuInSe_2$ Team Participation

IEC is an active member of four sub-teams under the National CIS Team for the NREL Thin Film Partnership program. The CIS team was restructured into sub-teams designed to directly support the industrial partners. IEC is active with the following:

Global Solar Energy. This team is focusing on helping GSE develop a low temperature process for the roll-to-roll deposition of $Cu(InGa)Se_2$. IEC is providing direct support through materials characterization and device fabrication and characterization.

ISET. IEC is assisting in the development of improved performance of ISET's CIS-based materials by investigating the use of sulfur incorporation to increase the voltages in the devices and modules.

Siemens Solar Industries. This sub-team is addressing reliability and transient effects in SSI's cells and modules. Specifically, IEC is completing device measurements and analysis of cells and mini-modules subjected to light exposure, thermal stress, and voltage bias.

UNISUN. IEC is providing detailed materials characterization, device fabrication and characterization to support UNISUN's development of particle-based processes for deposition of $Cu(InGa)Se_2$. This lead to IEC fabricating a 11.7% device on UNISUN's CIGS layer.

a-Si-BASED SOLAR CELLS

Micro-crystalline p-layers

The focus of the a-Si research was on deposition of more conductive μc-Si based p-layers and characterizing properties of TCO layers following plasma exposure. The Si:C:H and Si:O:H p-layers were deposited by RF CVD. The effect of H_2, SiH_4, CH_4 and CO_2 flow rates, boron dopant source gas, and RF power on microcrystallinity and conductivity was studied. This work is motivated by the need for a wide bandgap highly conductive p-layer material to simultaneously increase V_{oc} and blue response of superstrate p-i-n solar cells.

The investigation of glow discharge deposited crystalline p-layers was conducted in two stages. First, we investigated the deposition and characterization of these types of films having high level of CH_4 in the feed gas, which completed the investigation of carbon containing p-layers. The goal was to determine the feasibility of obtaining crystalline SiC phases in the films. Second, we investigated the deposition and characterization of films having CO_2 in the feed gas. The goal here was to obtain two phase films of crystalline Si imbedded in a matrix of a–Si:O:H:C. The idea is that such films incorporated in p-i-n type devices could give high currents due to the transparency of the amorphous phase and high voltages due to the highly conductive crystalline phase with a smaller junction surface. Also, the presence of CO_2 in the glow

discharge plasma would tend to decrease the reducing effects of the plasma on the thin conductive oxide used as the front contact in superstrate devices.

The p-layers were deposited on 7059 glass and on SnO_2 substrates, and their crystallinity was determined by Raman spectroscopy. In-plane conductivity and activation energy measurements were also performed on most of the films deposited on glass substrates.

The main experimental variables were the hydrogen dilution and CH_4 or CO_2 content in the feed gases. The secondary parameters were discharge power density and doping gas (B_2H_6) level. Increasing hydrogen dilution reduces deposition rate even though silane partial pressure and gas residence time stay the same. This observation supports hydrogen etching of the film during growth. The observed increase in deposition rate with gas phase diborane concentration is related to the known ability of diborane in cracking silane molecules. Results also show that while the CO_2 level in the discharge does not seem to have an effect on the c-Si content in the case of glass substrates, it does, however, control crystallinity of the films deposited on SnO_2 substrates.

In this study of crystallinity in glow discharge deposited boron-doped carbon and oxygen-containing films (CH_4 and CO_2 containing discharges, respectively), the only crystalline phase identified was silicon. Volume fraction of the crystalline phase was found to depend on hydrogen dilution but not on the discharge power. High silane partial pressures resulting in high deposition rates suppress the formation of the crystalline phase. On the other hand, discharge power does not control crystallinity in a significant way and high levels of crystallinity were obtained at very low power densities. Crystallinity in the films was found to decrease with increasing amounts of CH_4 or CO_2 in the discharge. The amount of crystalline phase in the films deposited on SnO_2 was consistently lower than in the films deposited on glass substrates.

Effect of H_2 Plasma and c-Si Deposition on SnO_2 and ZnO/SnO_2 Bilayers

It has been well known that exposure of SnO_2 films to H_2 plasma or deposition of a-Si by plasma CVD can lead to degradation in optical transmission. It has been reported that degradation can be minimized or even eliminated by using low substrate temperatures or by covering the SnO_2 with a thin protective sputtered ZnO:Al layer. However, there are conflicting results from different studies regarding plasma interaction with SnO_2 or ZnO.

Also, degradation of the SnO_2 due to interaction between the plasma is likely to get worse under conditions required for growth of μc-Si layers, i.e., higher H_2 dilution and slow growth rates. This could impact our ability to incorporate the μc-Si films into superstrate devices.

Therefore, we performed a study to determine the influence of four variables: substrate temperature during plasma exposure; the ZnO protective layer thickness; the SnO_2 supplier; and comparing H_2 plasma with deposition of μc-Si films at the same temperature. The goals were to identify if there were different sensitivities to H_2 plasma between two different commercially available SnO_2 products (Asahi and AFG textured SnO_2) used for superstrate a-Si device fabrication; to separate changes in carrier mobility from carrier density; and to investigate the ability of sputtered ZnO:Al to protect the underlying SnO_2 from damage. From the optical transmission, we conclude that the threshold for damage to bare SnO_2 is between 150 and 200˚C,

that 20 nm of ZnO is sufficient to protect the SnO_2 from plasma-induced damage even at 200˚C and that bare SnO_2 is unaffected by either a H_2 plasma or µc-Si deposition at 150˚C. Furthermore, there are beneficial effects to the electronic properties (i.e., mobility) with either H_2 or Si processing at 150˚C.

The sheet resistance, mobility and carrier concentration of the AFG SnO_2 is essentially unaffected by the treatments. In contrast, R_{sh} for Asahi SnO_2 decreases with H_2 plasma treatments. The decrease in R_{sh} occurs similarly for Asahi films with or without the protective ZnO layer. The Hall effect mobility increases with increasing substrate temperature during the plasma treatments, nearly doubling from 30-32 to 57-62 cm^2/V-sec with or without ZnO layer.

These results demonstrate that the 20 nm of ZnO is sufficient to protect the SnO_2 from plasma-induced damage resulting from either a H_2 plasma or µc-Si deposition, while at the same time allowing the beneficial improvement in bulk SnO_2 mobility. Compared to Asahi SnO_2, the AFG SnO_2 has greater optical losses and shows no improvement in electrical properties upon exposure to H_2 plasma or µc-Si film deposition.

Hot-wire Deposited Film

An experimental study was carried out to understand the relationship between hot wire chemical vapor deposition (HWCVD) processing parameters and deposited thin Si film properties. Thin silicon films were deposited from pure silane onto 7059 Corning glass and single-crystal (100) silicon substrates. The choice of pure silane as opposed to diluted silane in hydrogen was made to simplify the reaction system and provide a basic framework from which more complicated systems can be understood. The depositions were carried out in a multi-wire HWCVD reactor. The wire temperature was monitored with a dual-wavelength pyrometer focused through a viewport. A quadrupole mass spectrometer with a resolution of 1 amu and a range of 1-512 amu was used to measure the concentration of the gas phase species during deposition. At the wire temperatures used, the conversion of silane as measured by the mass spectrometer was approximately constant, ranging from 90 to 9 percent.

For both substrates used, the Si films had grain sizes between 10 to 50 nm and displayed a (220) preferred orientation. The crystalline fraction varied from 0 to 89 percent depending on the process conditions. These results demonstrate that crystalline films can be deposited from silane without hydrogen dilution.

Previously, several studies have concluded that high hydrogen dilution is essential in the deposition of crystalline Si films. However, high crystalline fractions can be obtained without hydrogen dilution by carefully choosing the other processing parameters without the penalty in growth rate, which typically occurs with hydrogen dilution.

a-Si Team Participation

IEC is a member of the National a-Si Team under the Thin Film Partnership Program. Steve Hegedus is the leader of the Multijunction Device sub-team. The work on characterization of the TCO/p contact resistance was performed as part of the Teaming activities in collaboration with Solarex. During this contract period, IEC collaborated with: Gautam Ganguly at Solarex by characterizing the TCO/p contact resistance on their sub-modules having different textured

SnO_2; Bhushan Sopori at NREL by fabricating back reflector structures on textured TCO/a-Si substrates from Solarex for analysis by PVOPTICS; and Eric Schiff at Syracuse University by providing him with special TCO/i-n device structures for electroabsorption measurements. These teaming collaborations lead to co-authoring three publications at the Spring 1999 Materials Research Society Conference.

CdTe/CdS-BASED SOLAR CELLS

Fabricating high efficiency CdTe/CdS *superstrate* devices when using ultra-thin CdS window layers presents a difficult technical challenge because of the coupled nature of the processing steps and of the interaction between CdS and CdTe films. We and others have shown that simply reducing CdS thickness to reduce parasitic absorption does not lead to the expected increase in performance, since the junction quality is found to progressively deteriorate (as measured by a loss in V_{oc} and FF) as final CdS thickness in the device is reduced below 100 nm. The extent of this phenomenon is: 1) process specific; 2) more serious for processes in which the CdTe layer is deposited at temperatures below 400˚C; and 3) related to consumption or even disappearance of a continuous CdS layer. In addition, reducing CdS thickness exposes the TCO/glass materials to interaction with the chemical treatment ambient, which can result in loss of adhesion or contamination. The loss of CdS due to diffusion into CdTe is dominated by the grain boundary diffusion. Incorporating S uniformly into the CdTe lattice at concentrations below the solubility limit does not have a deleterious effect on the junction quality. Improving the $CdTe_{(1-x)}S_x$/TCO junction quality for CdTe devices with ultra-thin CdS has been facilitated by use of a high resistance layer between the TCO and CdS films.

There are also serious problems to be solved at the other end of the device, namely the CdTe contact. Prior to forming a low resistance contact to CdTe, the surface must be modified to remove oxides and residues and produce a Te-enriched layer. Nearly-all contacting schemes follow this step with application of a copper-containing contact or copper layer and a heat treatment. Analysis of the resulting surface reveals that low resistance contact operation is facilitated by formation of a very thin Cu_2Te layer between CdTe and the current-carrying material. In stress-degraded devices, removing the current-carrying contact, re-etching the surface, and re-applying a contact removes the leaky diode "blocking" behavior. Thus, this behavior can be attributed to the CdTe/contact interface.

In this report, the critical issues are addressed for processing superstrate CdTe/CdS devices with ultra-thin CdS and in evaluating their stability-limiting mechanisms. Progress was achieved on several aspects of these problems.

CdS/CdTe Junction Processing and Interdiffusion Studies

We have quantified the chemical reactions and inter-diffusion of the CdS/$CdTe_{(1-x)}S_x$/CdTe junction including the polycrystalline nature of the materials. A physio-chemical basis for vapor $CdCl_2$:O_2 treatment was developed, micro-compositional S distribution measurements were made, and modeling of x-ray diffraction line profiles of $CdTe_{(1-x)}S_x$ alloys was continued.

Efforts to minimize CdS consumption during processing have been successful. We have found that increasing as-deposited CdTe grain size reduces CdS film loss during $CdCl_2$ post-deposition processing by reducing diffusion pathways (i.e., grain boundaries).

CdS/CdTe adhesion can be a problem during some post-deposition treatments. For cells with ITO, crystallization of the ITO layer prior to CdS growth improves CdS/CdTe adhesion and reduces reaction of different glasses with $CdCl_2$.

We have continued to study and optimize the device performance with thin CdS by incorporating a TCO with high resistance layer. Incorporating a high resistance layer between CdS and standard low resistance TCO layers allows V_{oc} and FF to be maintained as CdS thickness is reduced, resulting in physical vapor deposited cells with efficiency > 13%.

The CdS deposition method appears to be increasingly critical as the CdS thickness is reduced. A new chemical bath CdS deposition technique was developed that yields a low density of pinholes and particulates and has > 90% utilization of cadmium species.

CdTe Contact Processing and Stability Studies

We are now using electrical and chemical analysis of the contact to CdTe to relate processing variations to electrical behavior in as-deposited cells and stress-degraded cells. Analysis of the surface under the contact reveals that low resistance contact is formed with a very thin Cu_2Te layer between CdTe and the current-carrying material. To gain additional information about the nature of the CdTe contact surface, glancing incidence x-ray diffraction measurements were made at each processing stage. After some forms of stress, this Cu_2Te layer disappears.

A new stress testing system was assembled and became operational. The system has 4 vacuum-compatible chambers for exposing up to 16 devices to various controlled atmospheres (dry air, H_2/Ar, Ar, vacuum), temperature (25-120°C), illumination intensity and electrical bias (reverse to forward) while monitoring the electrical performance. Devices with a range of back contact processes were stressed, typically at 100°C at 1.2 suns, in dry air or H_2/Ar, at biases of –0.5V, 0V (J_{sc}), V_{mp}, and V_{oc}. A strong dependence on bias during stress has been observed for all devices studied. We find that the J_{sc} bias point has the least degradation for all parameters (V_{oc}, J_{sc}, and FF). The degradation for devices biased at V_{oc} is extremely rapid, and devices biased at V_{mp} or V_{oc} degrade at similar rates. Degradation in dry air, H_2/Ar or Ar is very similar, indicating that oxygen during stress is not a key ingredient for degradation. Stress at V_{oc} creates blocking contact in the dark and light diode in all three ambients. Stress at J_{sc} or –0.5V has a more dramatic effect on the forward bias characteristic of the dark diode than on the light diode.

CdTe Team Participation

IEC has actively participated in the National CdTe R&D Team by depositing CdTe films for analysis, fabricating contacts and stressing devices for the stability sub-team, and fabricating devices for the CdS sub-team using different high resistance transparent layers between CdS and the TCO. Brian McCandless and Steve Hegedus have reported these results through presentations and written reports at Team Meetings.

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1. INTRODUCTION

1.1 $CuInSe_2$-based Solar Cells

$CuInSe_2$ has a bandgap of 1 eV and the devices typically have V_{oc} less than 0.5 V. This bandgap is about 0.5 eV less than required for a single junction device to have optimal efficiency for terrestrial applications. Champion cells have been made with bandgaps of about 1.2 eV through the addition of Ga. It is desirable to further increase the bandgap from 1.4 to 1.6 eV for improved module performance.

Presently, most companies developing $CuInSe_2$ for modules form the $CuInSe_2$ films by either multisource evaporation selenization of Cu/In films in either an H_2Se or Se atmosphere. Progress has been made in characterizing the chemical pathways to film growth and estimating the reaction rate constants. As the process evolves to include the $CuInSe_2$ alloys, characterization of the reaction chemistry and kinetics needs to be extended to the alloys. While reaction pathways have been identified that lead to the formation of near stoichiometric $CuIn_{1-x}Ga_xSe_2$ when the processing temperatures are limited to below 400˚C, all cells with record-level efficiencies were produced by reacting the absorber layers at temperatures above 500˚C. Such high processing temperatures limit the choice of substrate materials (e.g., lightweight Kapton foil) and make processing and substrate handling in general more difficult. It is presently not well understood why the champion cells had to be processed at such high temperatures.

1.2 a-Si:H-based Solar Cells

Amorphous silicon (a-Si) PV modules were the first thin-film PV modules to be commercially produced and are presently the only thin-film technology that had an impact on the overall PV markets. However, the efficiencies of these modules have not yet reached the levels that were predicted in the 1980s. To a significant degree this is due to the intrinsic degradation of a-Si under illumination. The amount of light-induced degradation can be limited to 20 to 30% in modules operating under prevailing outdoor conditions. Both material processing schemes and device design schemes have been developed to improve the stabilized solar cell efficiency of a-Si solar cells. The use of multijunction devices (allowing the use of thinner absorber layers in the component cells) and the use of light-trapping appear to be the most powerful device design schemes to improve stabilized device performance.

The US industry is currently using these approaches to build a-Si-based modules. The substrate type devices are built on stainless steel foil. The superstrate devices are built on glass coated with transparent conductors (TCO). Presently, all superstrate devices use an a-SiC p-layer while substrate devices use a "μc-Si" p-layer, which is in fact a mixture of a-Si and μc-Si phases. Fabricating devices with p-layers having wider bandgaps and higher conductivity is expected to lead to higher V_{oc} and higher blue response, hence J_{sc}. Further, such highly conductive and transparent layers will reduce electrical and optical losses at the n/p interconnect junction of multijunction devices. Thus, improvements in p-layers would benefit both superstrate and substrate device technologies, in either single or multijunction configurations.

1.3 CdTe/CdS-based Solar Cells

Fabricating high efficiency CdTe/CdS *superstrate* devices when using ultra-thin CdS window layers presents a difficult technical challenge because of the coupled nature of the processing steps and of the interaction between CdS and CdTe films. We and others have shown that simply reducing CdS thickness to reduce parasitic absorption does not lead to the expected increase in performance, since the junction quality is found to progressively deteriorate (as measured by a loss in V_{oc} and FF) as final CdS thickness in the device is reduced below 100 nm. The extent of this phenomenon is: 1) process specific; 2) more serious for processes in which the CdTe layer is deposited at temperatures below 400˚C; and 3) related to consumption or even disappearance of a continuous CdS layer. In addition, reducing CdS thickness exposes the TCO/glass materials to interaction with the chemical treatment ambient, which can result in loss of adhesion or contamination. The loss of CdS due to diffusion into CdTe is dominated by the grain boundary diffusion. Incorporating S uniformly into the CdTe lattice at concentrations below the solubility limit does not have a deleterious effect on the junction quality. Improving the $CdTe_{(1-x)}S_x$/TCO junction quality for CdTe devices with ultra-thin CdS has been facilitated by use of a high resistance layer between the TCO and CdS films.

There are also serious problems to be solved at the other end of the device, namely the CdTe contact. Prior to forming a low resistance contact to CdTe, the surface must be modified to remove oxides and residues and produce a Te-enriched layer. Nearly-all contacting schemes follow this step with application of a copper-containing contact or copper layer and a heat treatment. Analysis of the resulting surface by glancing incidence XRD (GIXRD) reveals that low resistance contact operation is facilitated by formation of a very thin Cu_2Te layer between CdTe and the current-carrying material. In stress-degraded devices, removing the current-carrying contact, re-etching the surface, and re-applying a contact removes the leaky diode "blocking" behavior. Thus, this behavior can be attributed to the CdTe/contact interface.

In this report, the critical issues are addressed for processing superstrate CdTe/CdS devices with ultra-thin CdS and in evaluating their stability-limiting mechanisms. Progress was achieved on several aspects of these problems.

1.4 Training and Education

During the period of this subcontract (August 24, 1998 to August 23, 2999) IEC provided training and education for the following: two visiting professionals; five post-doctoral fellows; thirteen graduate students; and ten undergraduate students. One of our visiting professionals was a Fulbright scholar. Names are given in the list of contributors.

1.5 Publications

As a result of research performed under this subcontract, IEC published 11 papers.

1.6 Organization of the Report

This report is organized into three technical sections: $CuInSe_2$-based solar cells, a-Si:H-based solar cells, and CdTe-based solar cells. Each section describes the progress made at IEC in addressing the critical issues discussed above during the 12-month period of this subcontract.

2. $CuInSe_2$-BASED SOLAR CELLS

2.1 CIS-based Solar Cells with Improved Manufacturability

For solar cells based on thin film $Cu(InGa)Se_2$ to become a commercially viable technology, manufacturing costs must be reduced. One means to accomplish this is by reducing the substrate temperature at which the $Cu(InGa)Se_2$ layer is deposited. Soda lime glass is typically used as the substrate for high efficiency $Cu(InGa)Se_2$ solar cells, but it deforms at the temperatures used for the highest efficiency devices, 550 – 600°C. With lower substrate temperature (T_{ss}) there is less stress on the glass, or alternative substrate materials, like a flexible polymer, could be utilized. In addition, lower T_{ss} can allow faster heat-up and cool-down time and decrease the heat load and thermal stress on the entire deposition system.

Several companies are developing processes and equipment for in-line physical vapor deposition of CIGS onto a moving substrate as a means to achieve the high rate and spatial uniformity desired for cost-effective manufacturing. In this process, the substrate passes over thermal sources from which elemental or compound materials are evaporated in sequence. IEC with an equipment manufacturer has been designing, constructing, and implementing such a system to develop a manufacturable process for CIGS deposition.

The two primary objectives under this task are:

- To determine the effects of lowering the processing temperature from 550 to 400°C on CIGS films and devices.
- To make an in-line CIGS deposition system operational.

2.1.1 Reduced Deposition Temperature

This report will address material and device issues related to reducing T_{ss} from 550°C to 400°C for the deposition of $Cu(InGa)Se_2$ by physical vapor deposition using multisource elemental evaporation. Deposition of $Cu(InGa)Se_2$ by multisource evaporation typically is done with a process which incorporates a Cu-rich growth step, i.e., deposition with the Cu molar flux greater than the sum of the In and Ga fluxes [1]. With (Cu) > (In) + (Ga), the growing film contains a mixture of $Cu(InGa)Se_2$ and Cu_xSe_y, where the specific Cu_xSe_y phase may depend on the temperature [2]. This is then followed by a Cu-deficient growth step so that the final film has the desired composition range with Cu/(In+Ga) < 1. This process was found to have an effect on both the film morphology and device performance [1]. We have previously shown that, using a deposition with a Cu-rich growth step and varying T_{ss} from 600°C down to 350°C, the $Cu(InGa)Se_2$ grain size decreases over the entire range of T_{ss} and the device efficiency decreases slowly for $550 \geq T_{ss} \geq 400$°C [3].

The connection between grain size, morphology, compositional uniformity, and device performance, as they are affected by substrate temperature and growth process, is investigated. The objective is to develop a process for improved device performance with T_{ss} = 400°C. We will compare the grain size and morphology, as well as the solar cell device performance, for $Cu(InGa)Se_2$ films deposited at 550 or 400°C using different temporal flux profiles during the

deposition to examine the effect of the Cu-rich growth step. Specifically, we will compare depositions with a uniform flux, i.e., no Cu-rich growth to depositions with a Cu-rich flux at the beginning of the deposition or a Cu-rich flux in the middle of the deposition. This will distinguish if the effects of Cu-rich growth specifically require the presence of the Cu_xSe_y phase during the initial nucleation of the film on the glass/Mo substrate.

2.1.1.1 Experimental Procedures

$Cu(InGa)Se_2$ films were deposited by thermal evaporation from independently controlled elemental sources for the Cu, In, Ga, and Se. Three temporal deposition flux profiles were used to give depositions with: (1) uniform fluxes so that the films composition was never Cu-rich; (2) Cu-rich flux, Cu/(In+Ga) > 1, at the beginning of the run followed by only In, Ga, and Se fluxes to give the desired Cu-deficient final composition; and (3) Cu-rich flux in the middle of the run. These are shown schematically in Figure 2.1. The In, Ga, and Se fluxes were kept constant throughout each deposition, so there were no gradients in Ga content or bandgap, and were the same for each flux profile. The differences in the depositions, then, were only in the Cu fluxes. These three flux profiles were done at T_{ss} = 550°C and 400°C. The deposition time for all films was 44 min. and the final film thicknesses were 2.5 – 3 µm. In addition, separate depositions were done to determine the intermediate compositions when the films were Cu-rich, using the profiles with the fluxes Cu-rich in the beginning and the middle of the runs. In these runs, the profiles were the same for the first 32 minutes and then the runs were aborted with a shutter between the sources and substrates closed.

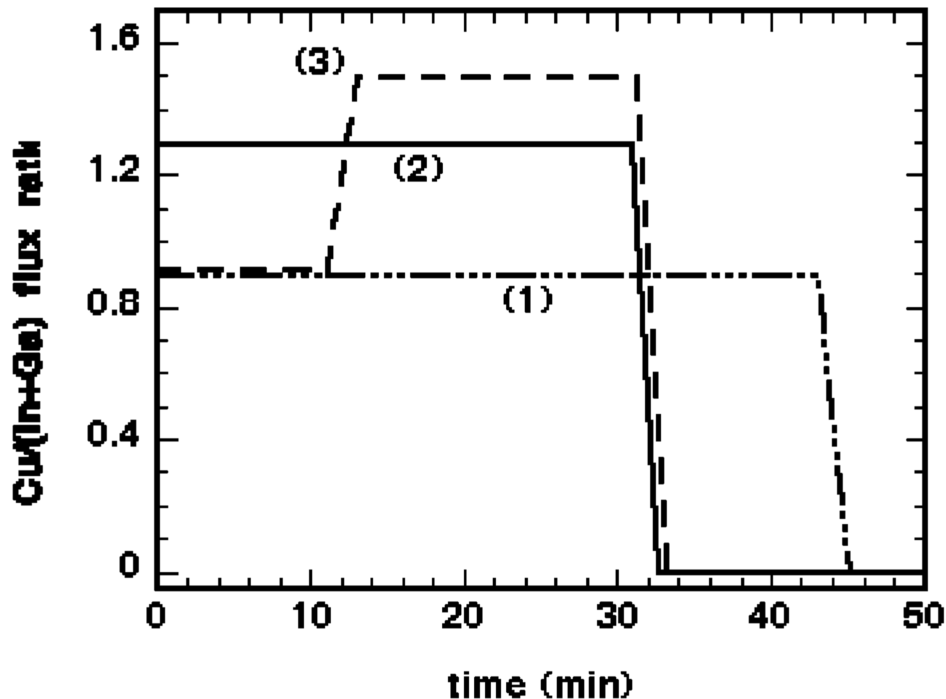


Figure 2.1 Schematic representation of three temporal flux profiles, as described in the text.

All films used for morphological characterization and devices had a final composition, measured by energy dispersive x-ray spectroscopy (EDS), with Cu/(In+Ga) = 0.8 – 0.9 and Cu/(In+Ga) ≈ 0.3. This gives a bandgap of E_G = 1.2 eV. The runs with the deposition aborted after 32 min. had Cu/(In+Ga) ≈ 2 and Cu/(In+Ga) ≈ 0.3.

In addition to EDS, films were characterized by scanning electron microscopy (SEM), Auger electron spectroscopy (AES) depth profiles, performed by Amy Swartzlander at NREL, and x-ray diffraction (XRD). Scanning electron microscopy (SEM) and atomic force microscopy (AFM) were used to characterize the $Cu(InGa)Se_2$ morphology and grain size. Tapping mode AFM images, taken on a Digital Instruments Dimension 3100 Scanning Probe Microscope, were specifically used to enable the lateral grain size distribution to be quantitatively determined. In some cases, the $Cu(InGa)Se_2$ films were first etched in a 2 wt% bromine in methanol solution for 15 sec. to reveal grain boundaries.

All $Cu(InGa)Se_2$ films were deposited on soda lime glass substrates with a 1 μm thick sputtered Mo layer. Devices were fabricated with the chemical bath deposition of 30-50 nm CdS. This was followed by an rf sputtered ZnO:Al bilayer. The first layer, deposited with ~1% oxygen in the sputter gas, had thickness ~50 nm with resistivity 10-100 Ω-cm. The second layer had thickness ~500 nm with resistivity $\sim 10^{-3}$ Ω-cm or sheet resistance ~20 Ω/sq. Finally, an evaporated Ni/Al grid was deposited and cell areas were delineated by mechanical scribing to give area = 0.47 cm^2. In a few cases, which will be specifically noted, an anti-reflection coating was applied by the electron beam evaporation of 125 nm MgF_2. Details of the deposition and cell fabrication are given in [4].

Devices were characterized by current-voltage (J-V) measurements with the sample at 25°C under 100 mW/cm^2 AM1.5 illumination and by quantum efficiency (QE) measurements with different light and voltage bias conditions.

2.1.1.2 Results: Grain Size and Composition

SEM cross-sectional micrographs of films grown with the three profiles and two temperatures are shown in Figure 2.2. The films grown at T_{ss} = 550°C all have larger grains than those grown at 400°C. At the lower temperature, the uniform flux process appears to give more columnar grains and a smoother surface. There are no apparent differences between films grown with the Cu-rich flux at either the beginning or middle of the deposition.

AFM images of the top surface were used to determine the lateral grain size. This is shown in Figure 2.3 for the films grown with a Cu-rich flux at the beginning at each temperature. Again, the higher T_{ss} clearly gives larger grains, while the lower T_{ss} gives more a more faceted morphology. To quantify the grain size, a map of the grain boundaries was made from these images as shown in Figure 2.4. This map was then digitized and National Institutes of Health (NIH) Image software was used to determine the grain sizes. The grain size statistics were collected for three randomly selected 10 μm x 10 μm areas on each sample. The resulting grain sizes were found to conform to a log-normal distribution which is described by:

$$f(\ln A) = \frac{1}{\sigma(\ln A)\sqrt{2\pi}} \exp\left[-\frac{(\ln A - \ln \overline{A})^2}{2\sigma(\ln A)^2} \right] \quad (2.1)$$

where A is the grain area, $\overline{A}$ is the mean area, and σ is the standard deviation. This log-normal distribution is commonly used to describe grain size in polycrystalline materials [5].

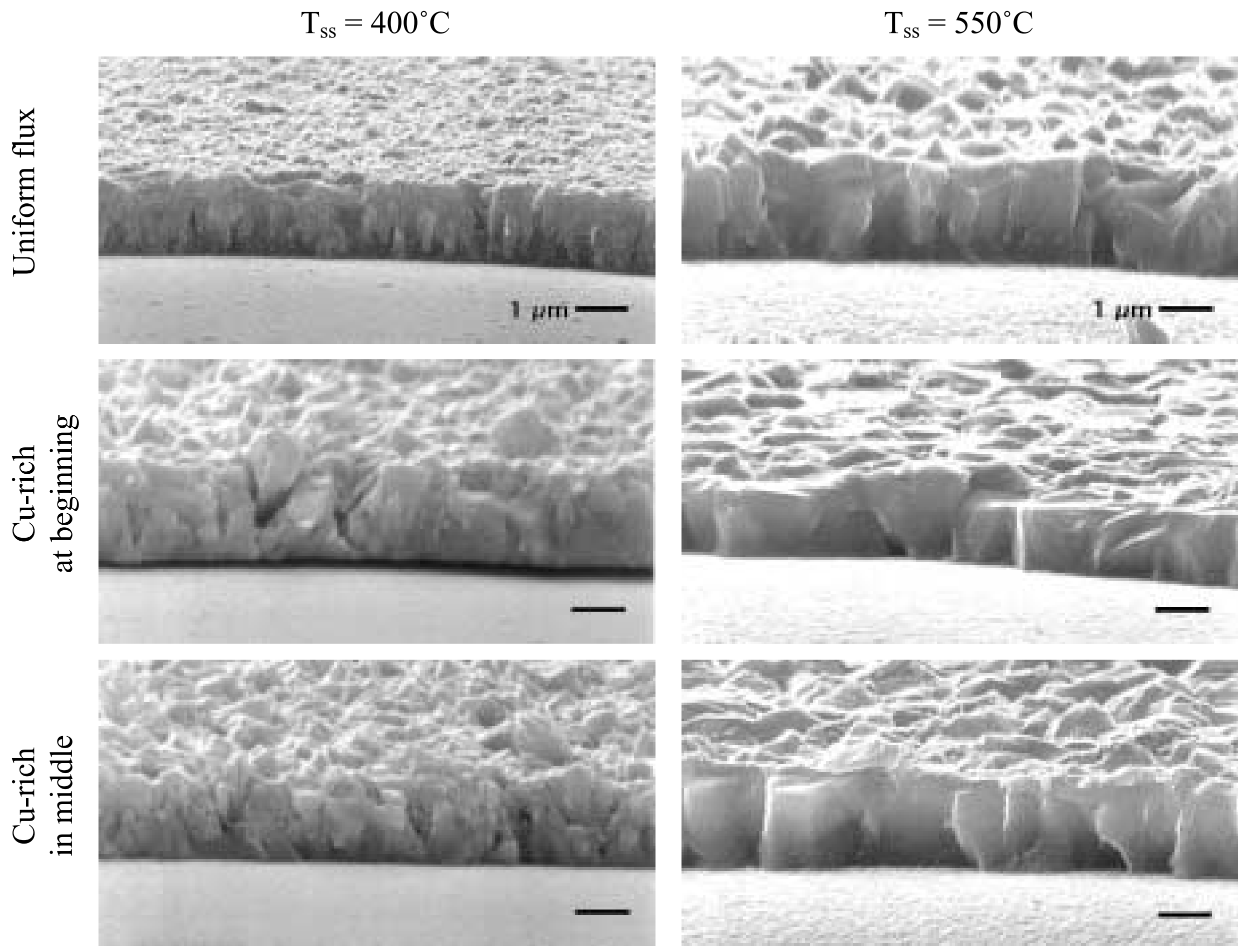
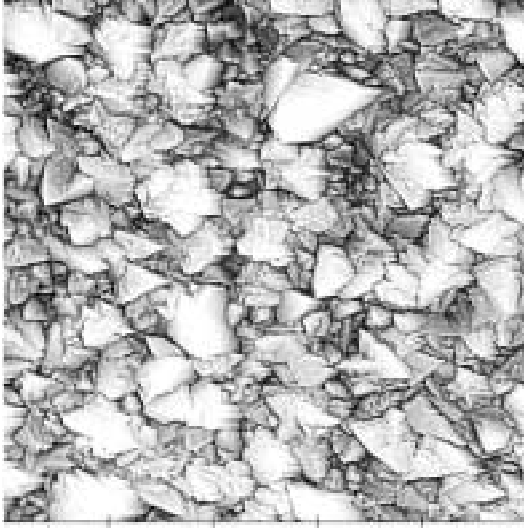


Figure 2.2 Cross-sectional SEM micrographs of $Cu(InGa)Se_2$ films deposited with different flux profiles and T_{ss}.

These distributions are shown in Figure 2.5 for the 6 different cases above. The number of grains in the 300 μm^2 total sampling area, the mean grain areas, $\overline{A}$, and the standard deviations, σ, are listed in Table 2.1. At 400°C, there is no significant difference in the distribution of lateral grain size at the surface. At 550°C, on the other hand, the mean area is smaller with the uniform flux process than for either Cu-rich process.

T_{ss} = 400˚C



T_{ss} = 550˚C

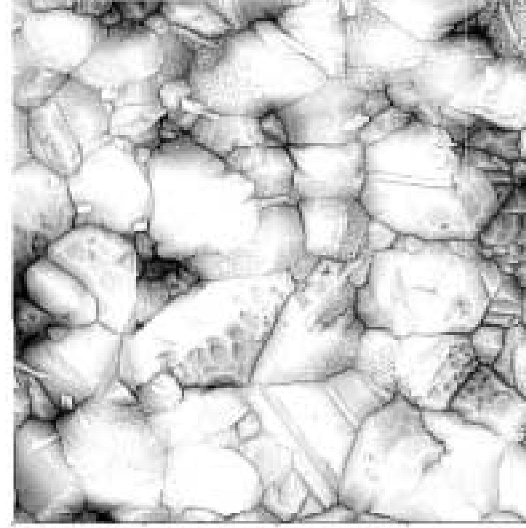
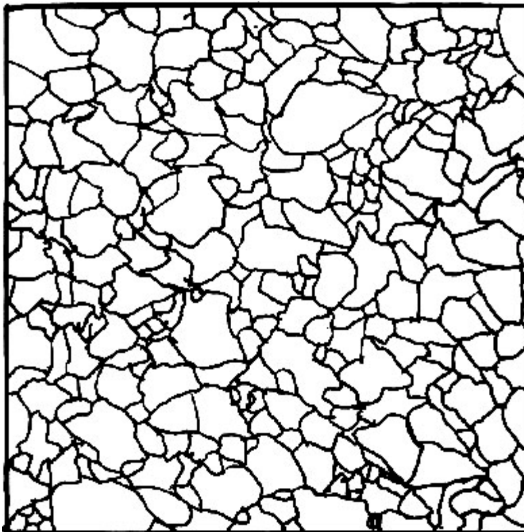


Figure 2.3 AFM images of the top surface of films deposited with a Cu-rich flux at the beginning of the deposition with T_{ss} = 400˚C and 550˚C. Each figure shows a 10 µm x 10 µm area.

T_{ss} = 400˚C



T_{ss} = 550˚C

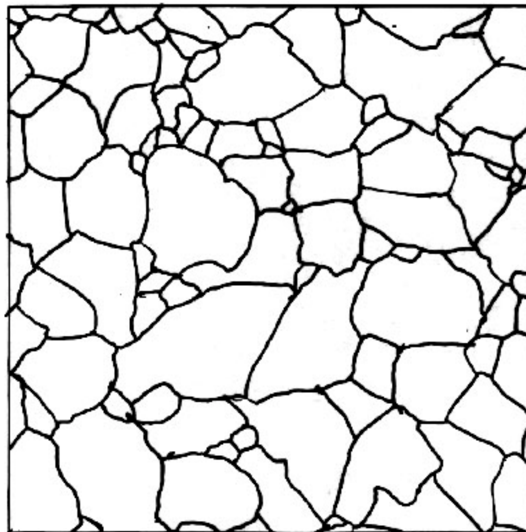


Figure 2.4 Grain boundary maps created from the AFM images in Figure 2.3.

Table 2.1 Number of grains and mean grain areas.

Process	T_{ss} = 400°C			T_{ss} = 550°C		
	# of grains	$\overline{A}$ (μm^2)	σ (ln(μm)^2)	# of grains	$\overline{A}$ (μm^2)	σ (ln(μm)^2)
Uniform	973	0.074	1.2	510	0.38	1.1
Cu-rich in beginning	952	0.080	1.1	316	0.54	1.5
Cu-rich in middle	984	0.066	1.1	325	0.57	1.2

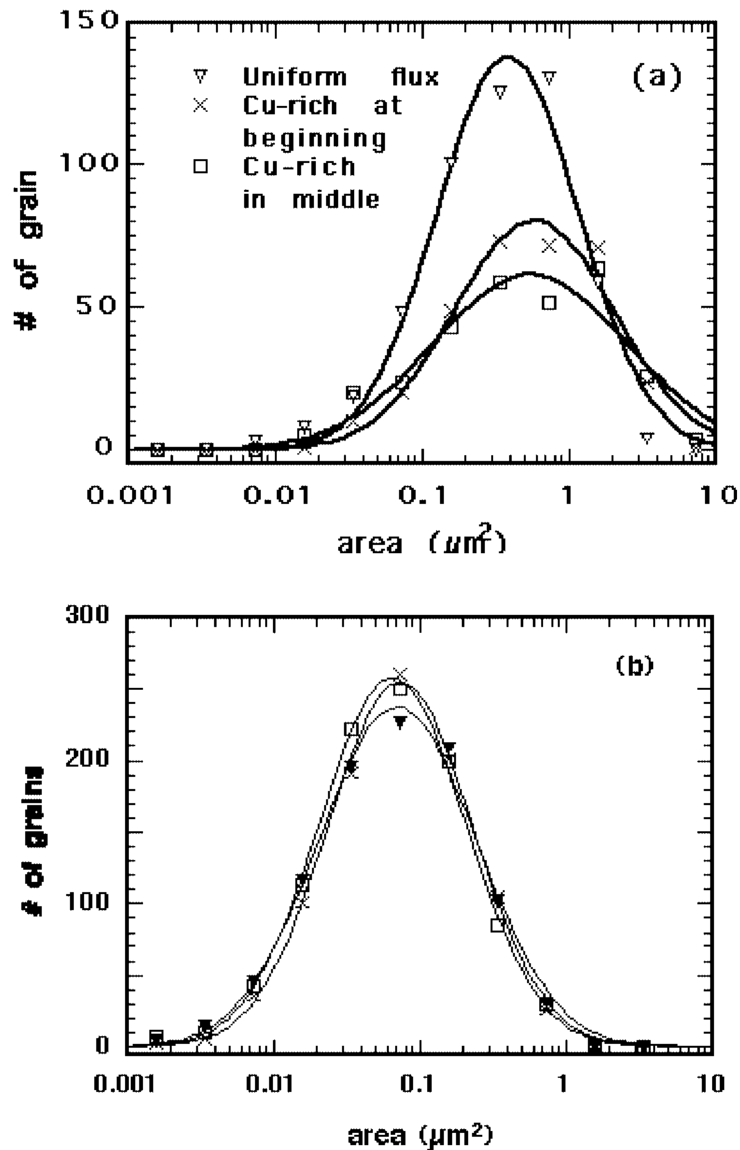


Figure 2.5 Grain sizes showing log-normal distributions for films deposited at (a) 550˚C and (b) 400˚C.

The films were further characterized by Auger depth profiles and XRD measurements. AES depth profiles were measured to determine the compositional uniformity through the thickness of the films deposited at T_{ss} = 400˚C for the depositions with the uniform fluxes, with the Cu-rich flux in the beginning of the deposition profiles, and with the deposition aborted when the film was Cu-rich after 32 min. The compositional ratios Cu/(In+Ga) and Ga/(In+Ga) are shown in Figure 2.6 along with the Mo signal to indicate the back of the film. The films deposited with the three flux profiles all showed uniform distribution of the Cu, In, and Ga through all the films with no compositional gradients despite the Cu flux gradient. The Cu-rich films have a uniform distribution of Ga/(In+Ga) but the Cu is non-uniform with increased relative composition at or near the front surface. This is consistent with the formation of Cu_xSe_y which resides at the surface. In addition, we previously showed that the amount of Na which diffused in the films from the soda lime glass substrate is comparable for films deposited at 400°C or 550°C with a flux profile Cu-rich at the beginning [3].

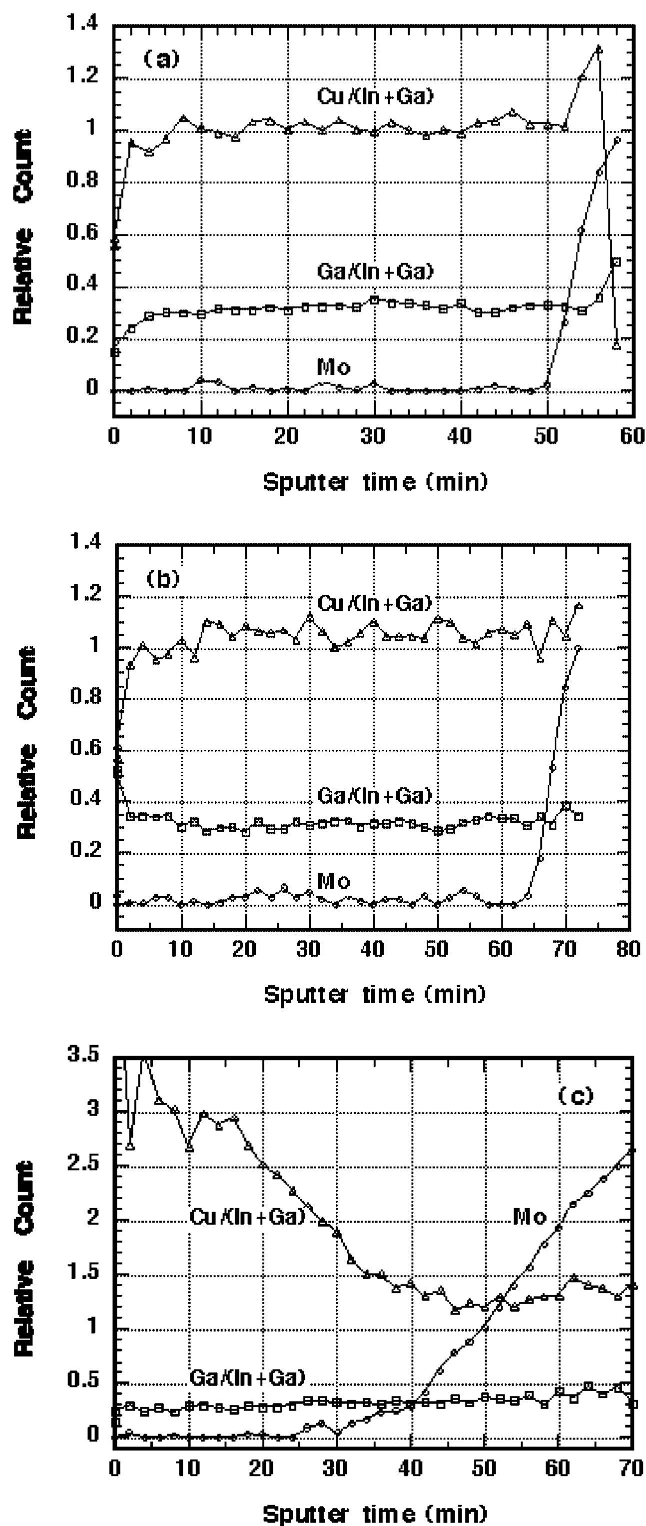


Figure 2.6 Auger depth profiles of Cu/(In+Ga), Ga/(In+GA) and Mo for (a) deposition with uniform flux, (b) deposition with Cu-rich flux in the beginning of the run followed by In, Ga, and Se, and (c) deposition with only Cu-rich flux. All samples were deposited at T_{ss} = 400˚C.

Finally, XRD measurements did not show any significant difference in the film orientation for any of the different processes or temperatures. All the films had nearly random orientation, as has been found for films deposited on (110) oriented Mo films [6].

2.1.1.3 Results: Devices

The device performance for the best cells achieved with each process and temperature are summarized in Table 2.2. With T_{ss} = 400°C, the Cu-rich flux, either in the beginning or the middle of the deposition, gives better device efficiency than the uniform flux. However, at 550°C there is no significant difference in the three processes. In repeated depositions the uniform process seems to be more reproducible in terms of producing high efficiency devices.

Table 2.2 Device performance with each process and temperature.

T_{ss} (˚C)	Process	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	η (%)
400	Uniform flux	0.56	29	69	11.3
	Cu-rich at beginning	0.59	33	71	13.7
	Cu-rich in middle	0.60	33	71	13.8
550	Uniform flux	0.65	33	74	15.9
	Cu-rich at beginning	0.65	32	76	16.0
	Cu-rich in middle	0.65	32	75	15.5

The J-V curves under illumination and in the dark are shown in Figure 2.7 for the two devices with the Cu-rich flux in the beginning of the deposition. The most significant difference is the increased voltage with higher T_{ss}. This cannot be attributed to the bandgap of the $Cu(InGa)Se_2$ absorber layer since the composition is the same and all films are compositionally uniform.

The J-V data is replotted with the current on a logarithmic scale, with the curves measured under illumination in Figure 2.8(a) and in the dark in Figure 2.8(b).light curves. In each case, there is no change in the slope with different T_{ss} but a shift in the curves indicating a higher forward diode current, J_O. There is a greater difference between the devices with different T_{ss} in the illuminated J-V results than in the dark, suggesting that the mechanism for increased J_O is light dependent. In addition, the J-V curves for all the 400°C samples show hysterisis between up and down traces where the data is measured with first increasing then decreasing voltage using a sweep time of ~ 1 min. This is more clearly seen in Figure 2.8(a) where the difference between the up and down sweeps is indicated by arrows on the plot.

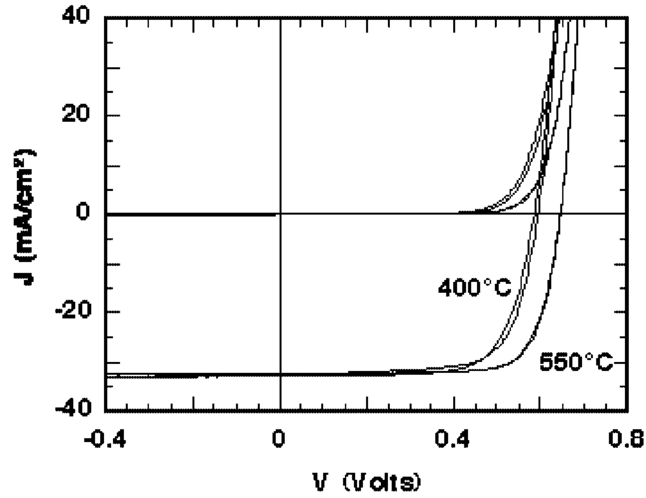


Figure 2.7 J-V curves for devices with $Cu(InGa)Se_2$ deposited at T_{ss} = 400 and 550˚C with a Cu-rich flux in the beginning.

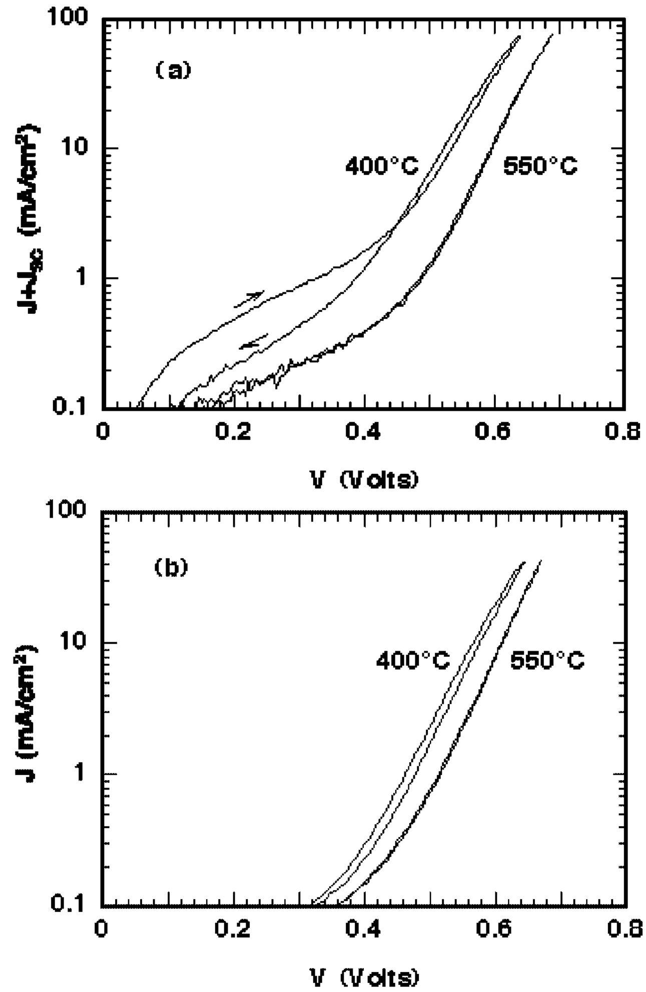


Figure 2.8 Logarithmic plot of $J+J_{sc}$ for the curves in Figure 2.7, (a) under illumination and (b) in the dark.

Finally, a 120 nm thick MgF_2 anti-reflection layer was deposited on the best cells above. This yielded cells with η = 16.4% for T_{ss} = 550°C and 14.1% with 400°C. These results are summarized in Table 2.3. The cell with η = 16.4% was tested at NREL along with several others. Test results comparing the measurement at IEC and NREL are included in Table 2.3.

Table 2.3 Device performance for the best cells after deposition of an anti-reflection layer. The cell with $Cu(InGa)Se_2$ deposited at 550˚C was measured at IEC and NREL.

Tss (˚C)	Measurement	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	η (%)
400	IEC	0.590	34.0	70.3	14.1
550	IEC	0.644	33.5	76.4	16.5
	NREL	0.648	32.9	76.9	16.4

2.1.1.4 Conclusions

Device results with T_{ss} = 400°C show that a Cu-rich growth step during the $Cu(InGa)Se_2$ deposition is needed for improved device performance. However, the film and device results are the same whether the Cu-rich growth occurs during the initial nucleation or later in the process. This indicates tolerance to different process sequences which allows flexibility in deposition process design.

The larger grain films grown at 550°C give better performance than the smaller grain films at 400°C, as expected. But, with a given substrate temperature there is no simple correlation between grain size and device performance. At the lower temperature the improved cell results with Cu-rich growth cannot be explained by increased lateral grain size at the surface. Conversely, at the higher temperature, the increased grain size with the Cu-rich growth does not provide improved device performance. Auger measurements show that device quality films, i.e., films with Cu/(In+Ga) < 1, have uniform profiles of Cu, In, and Ga whether or not they are deposited with a Cu-rich fluxes during the deposition. However, if the films remain Cu-rich, the Cu is not uniformly distributed.

In summary, the effects of T_{ss} on grain size and device performance have been investigated for $Cu(InGa)Se_2$ films deposited by elemental evaporation. At T_{ss} = 550°C, which has yielded the highest efficiency devices, the device performance is insensitive to the use of Cu-rich growth. A simple process with constant fluxes throughout the deposition gives as high a device efficiency as processes incorporating graded fluxes to give Cu-rich growth. At 400°C, the uniform process gives more columnar grains but the same lateral grain size as the graded, Cu-rich processes. However, the best devices result from Cu-rich growth although not necessarily during the initial film nucleation.

2.1.2 In-line Evaporation of $Cu(InGa)Se_2$

In-line evaporation is a potentially effective means to achieve the high rate uniform deposition necessary for commercial-scale manufacture of CIGS modules. In this process, the substrate is linearly translated over thermal sources from which the elemental materials are evaporated, as illustrated in Figure 2.9.

Deposition rate in the in-line process is determined by the translation speed of the substrate and the effusion rates from the sources. The growth of the $Cu(InGa)Se_2$ thin films will be different than in typical laboratory processes where the films are evaporated at low rates onto stationary substrates. The in-line process requires that the substrate passes sequentially over the sources so the incident flux composition changes and the films will have graded composition. The compositional profile of the film will depend on the sequence and spacing of the sources. This allows graded or "multi-stage" processes using steady-state source operation, whereas stationary-substrate systems require dynamic source operation.

IEC has co-developed and installed an in-line deposition system for CIGS processing. The IEC system is configured to handle a rigid substrate with uniform deposition of Cu, In, Ga, and Se over a 6" wide deposition zone. However, the system was designed to enable transition to a flexible substrate in a roll-to-roll configuration and a deposition zone up to 12" wide. The sequencing and spacing of the sources can be varied to allow different relative flux profiles to be investigated.

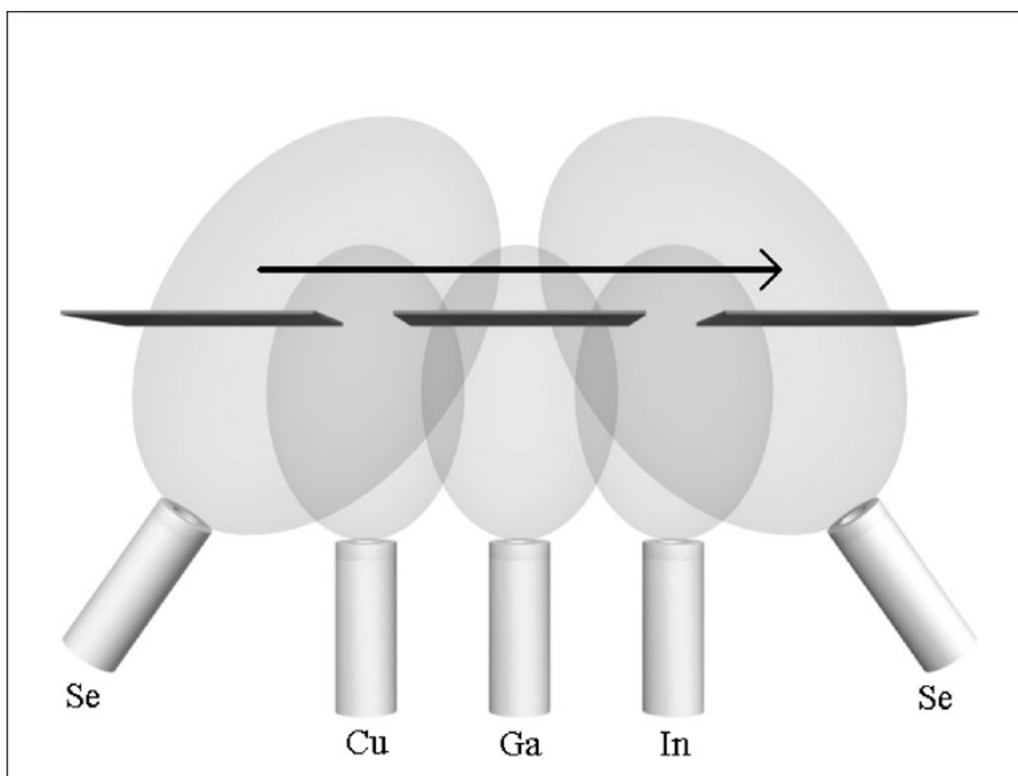


Figure 2.9 Schematic illustration of the in-line process for deposition of CIGS.

The IEC in-line system will be used to address the following issues:

- Develop a process to uniformly produce high quality $Cu(InGa)Se_2$ thin films in the in-line system, defined by the ability to fabricate high efficiency devices.
- Determine the limitations of high CIGS deposition rate and low substrate temperature, ~400˚C, in the in-line process on film and device properties.

- Determine the effects of the in-line process on film properties including composition gradients and the subsequent effect on device performance. This includes gradients in the Cu/(In+Ga) ratio as discussed above and in the Ga/(In+Ga) ratio which can produce bandgap gradients.

A critical issue for manufacturing is to develop process control strategies that are suitable for long-duration (~8 hr) deposition from high-rate effusion sources. The IEC system will incorporate the use of atomic absorption spectroscopy (AAS) to obtain a direct, element-specific measurement of effusion rate. A process control scheme utilizing detailed thermal modeling with source temperature measurements and the AAS measurement is being developed. In addition, a source effusion model has been developed and will allow the fluxes at the substrate to be incorporated into the process control strategy.

The IEC in-line evaporation system was built by MRG, LLC. A photograph is shown in Figure 2.10. The chamber measures 64" long × 33" wide × 28" high. The pumping stack consists of a Varian VHS-10 diffusion pump with a Leybold 65 cfm backing/roughing pump. An Opto22® distributed control system is used to execute the vacuum interlock logic. The system is capable of substrate travel velocities ranging from 0.25"/min to 20"/min. These velocities correlate to deposition times ranging from over one hour to just under one minute. The substrate heaters are designed to give a substrate temperature of up to 550ºC on a moving glass substrate.

Figure 2.10 In-line CIGS deposition system.

To date, the in-line system has been installed at IEC. Cu and In effusion sources have been developed, demonstrated and calibrated. Effusion source control using the AAS system has been demonstrated in a stationary laboratory system and a scheme has been developed to allow its implementation in the in-line system. Software for vacuum system and substrate drive control has been developed.

The IEC inline CIGS system offers a unique opportunity to contribute at both the laboratory and commercial scales. From the research standpoint, the system is well suited to studying the effects of varying incident flux composition and growth rate on CIGS film growth. From an engineering standpoint, the system allows a study of issues relevant to process scale-up, namely the implementation of in-situ flux measurement and the design and control of multiple effusion sources.

2.2 High Bandgap Alloys of Cu(In,Ga(S,Se)$_2$

The goal of this research was to develop an understanding of the functioning and processing requirements for high efficiency $Cu(In,Ga)(S,Se)_2$ solar cells with bandgaps from 1.3 to 1.7 eV leading to V_{OC} > 0.75 V & Eff. > 18%.

It has been demonstrated that the loss in efficiency of $Cu(In,Ga)Se_2$ solar cells with increasing Ga content is due to a decrease in fill factor, and to a lesser extent V_{OC} which is caused by a drop in the light generated current with increasing forward voltage [4,7].

Devices were fabricated with semi-transparent (0.04 µm) Mo contacts and bi-facial spectral response measurements were made and analyzed in order to determine the changes in collection efficiency as a function of changing Ga composition and applied voltage. The following analysis determines the amount of the decrease of light generated current with increasing voltage, $J_L(V)$, and whether it is primarily due to a reduction in minority carrier diffusion length (L) or a decrease in the width (w) of the space charge collection region near the $Cu(In,Ga)Se_2$/CdS junction [8].

2.2.1 $J_L(V)$ Determination in $Cu(In,Ga)Se_2$ Devices

To determine the magnitude of the $J_L(V)$ six samples with uniform $Cu(In,Ga)Se_2$ films with $E_G \approx 1.3$, 1.4 & 1.5 eV on standard "opaque" (1µm) and "slightly" transparent (0.04 µm) thick Mo were processed into 36 solar cells (0.47 cm^2) in order to quantify the voltage dependent minority carrier collection length and light generated current changes that occur with increasing E_G. The best solar cells fabricated from these uniform films have ~15% efficiency for $E_G \approx 1.3$ (Ga/(Ga+In) ≈ 0.5), but the device efficiency is less for the higher E_G's due to a decrease in fill factor and open circuit voltage (Table 2.4).

Table 2.4 J-V parameters for the best efficiency solar cells with both the standard 1µm thick and the "slightly" transparent 0.04µm thick Mo.

E_G (eV)	Mo thick (µm)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	η (%)	dV/dJ @V_{OC} (Ω-cm^2)	DJ/dV @J_{SC} (mS/cm^2)
1.3	1	0.703	29.4	70.7	14.6	1.9	3.
1.3	*0.04*	*0.701*	*28.5*	*65.7*	*13.1*	*3.8*	*2.*
1.4	1	0.752	22.9	71.6	12.3	2.5	1.
1.4	*0.04*	*0.746*	*23.3*	*65.7*	*11.4*	*4.4*	*2.*
1.5	1	0.833	16.5	66.5	9.2	3.5	2.
1.5	*0.04*	*0.789*	*16.8*	*65.5*	*8.7*	*6.0*	*1.*

At present the I-V measurements have been made at five different light intensities (full, 50%, 20%, 10% and Dark) on every solar cell. The results of these measurements for both thicknesses of Mo are shown in Table 2.5.

Table 2.5 J-V parameters as a function of light intensity for two solar cells with E_G = 1.5 eV and both Mo contacts.

Mo thick (µm)	Illumination	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	P_{out} (mw/cm^2)	dV/dJ @V_{OC} (Ω-cm^2)	DJ/dV @J_{SC} (mS/cm^2)
1	Full	0.820	18.02	66.8	9.86	3.7	1.7
	50%	0.770	9.34	66.8	4.80	6.7	0.5
	20%	0.729	3.63	65.8	1.74	17.6	0.4
	10%	0.710	1.93	65.1	0.89	31.8	0.3
	Dark						0.0
0.04	*Full*	*0.809*	*17.48*	*64.1*	*9.06*	*5.3*	*1.3*
	50%	*0.775*	*9.08*	*64.5*	*4.54*	*8.8*	*0.6*
	20%	*0.731*	*3.58*	*63.0*	*1.65*	*20.0*	*0.3*
	10%	*0.701*	*1.88*	*60.7*	*0.80*	*37.5*	*0.3*
	Dark						*0.0*

The J-V measurements made as a function of light intensity can be used to determine $J_L(V)$ as follows [7].

In most solar cells, it is possible to correct for parasitic resistive losses by determining (Equations 2.2 & 2.4) and subtracting (Equations 2.3 & 2.5) small shunt, R_{shunt}, and series resistance, R_{series}, terms from the measured J and V, respectively,

$$\frac{1}{R_{shunt}} = G_{shunt} \approx \left(\frac{dV}{dJ}\right)_{min}. \tag{2.2}$$

$$J' = J - \frac{V}{R_{shunt}} \tag{2.3}$$

$$R_{series} \approx \underset{\frac{1}{J}\to 0}{\text{Limit}}\left(\frac{dV}{dJ}\right) \tag{2.4}$$

$$V' = V - J R_{series}, \tag{2.5}$$

which then gives the junction current, $J_J(V')$, and the voltage dependent light generated current, $J_L(V')$, (Equation 2.5). If $J_J(V')$ is independent of light intensity and $J_L(V')$ is proportional to the light intensity, $J_L(V')$ can be found by subtracting the J-V data measured at two different light intensities (Equations 2.2 & 2.3) with the same spectral content (Equation 2.7).

$$J'(V') = J_J(V') - J_L(V') = J_J(V') - \eta(V')J_{L_{max}} \tag{2.6}$$

$$J_{21}(V') \equiv J_2'(V') - J_1'(V') = \eta(V')\left[J_{L_{1\,max}} - J_{L_{2\,max}}\right] \tag{2.7}$$

It is then possible to determine if the assumptions are correct by taking the difference between more than two light intensities and comparing the results, i.e.,

$$\eta(V') = \left[\frac{J_{21}(V')}{J_{21}(V')_{max}}\right]. \tag{2.8}$$

The results of this type of analysis for the five light intensities are shown in Figure 2.11.

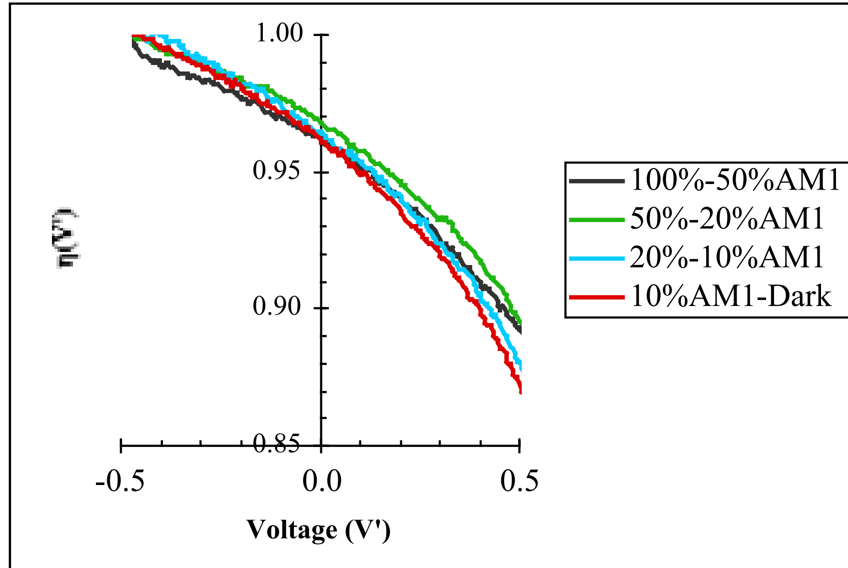


Figure 2.11 Normalized light generated current as a function of voltage η(V') for the device with an E_G of 1.5 eV and 1 µm Mo contact.

2.2.2 Collection Width Determination in $Cu(In,Ga)Se_2$ Devices

Electrical characterization of the devices included the total area current-voltage (J–V) response measured at 28˚C under AM1.5 illumination (Table 2.3) and quantum efficiency (QE) measured through both the ZnO/CdS (frontwall) and the Glass/semi-transparent Mo (backwall) as a function of voltage bias. Normalized transmission through the ZnO and Mo are shown in Figure 2.12 in the wavelength region of interest (750 - 1050 nm).

Table 2.6 Summary film and device parameters of the solar cells discussed Cu/(In+Ga) = 0.9 for all films.

Mo thk. (µm)	$Cu(In,Ga)Se_2$ thk. (µm)	Ga/(In+Ga)	E_G (eV)	Eff. (%)	FF (%)	V_{OC} (V)	J_{SC} (mA/cm^2)
1	3.0	0.30	1.2	14.9	73.5	0.627	32.4
1	2.3	0.65	1.4	10.1	68.1	0.755	19.6
.04	3.0	0.30	1.2	13.1	70.5	0.622	30.0
.04	2.3	0.65	1.4	10.0	68.7	0.734	19.9

From reference [9], the following internal quantum efficiency formulae apply to a uniform semiconductor under either frontwall (FW) or backwall (BW) illumination with: (1) minority carrier collection at a transparent front junction, (2) high or infinite surface recombination at the back, (3) thickness t, (4) diffusion length L, (5) optical absorption coefficient α and (6) total collection in a space charge width w, near the junction.

$$IQE_{FW} = 1 - e^{-\alpha w} + \frac{\alpha L e^{-\alpha w}}{(\alpha L)^2 - 1}\left[\alpha L - \frac{\left[\cosh\left(\frac{t-w}{L}\right) - e^{-\alpha(t-w)}\right]}{\sinh\left(\frac{t-w}{L}\right)}\right] \tag{2.9}$$

$$IQE_{BW} = \left(1 - e^{-\alpha w}\right)e^{-\alpha(t-w)} + \frac{\alpha L}{(\alpha L)^2 - 1}\left[\frac{1 - \cosh\left(\frac{t-w}{L}\right)e^{-\alpha(t-w)}}{\sinh\left(\frac{t-w}{L}\right)} - \alpha L e^{-\alpha(t-w)}\right] \tag{2.10}$$

These equations are used to represent the minority carrier collection in the $Cu(In,Ga)Se_2$ solar cells.

If the internal quantum efficiencies can be determined from the measured spectral responses of $Cu(In,Ga)Se_2$ devices Equations. 2.9 and 2.10 can be applied to find L, w and α. The calculated and measured QE's can then be compared for consistency. Because the optical absorption of the ZnO/CdS is fairly small and constant (Figure 2.12) in the wavelength region of interest (750 - 1050 nm), the measured QE_{FW} and IQE_{FW} will differ only by a constant. This constant can be determined to a good approximation by the maximum value of the measured QE_{FW}, by assuming 100% collection in the $Cu(In,Ga)Se_2$ at short wavelengths. Because of the absorption coefficient of $Cu(In,Ga)Se_2$ approaches 10^5 cm^{-1} at energies above the band gap, this is a reasonable assumption.

$$IQE_{FW}(\lambda) = \frac{QE_{FW}(\lambda)}{QE_{FW}(\max)} \tag{2.11}$$

By noting that IQE_{FW} and IQE_{BW} must be the same for uniform light absorption, the constant to correct QE_{BW} can be determined from QE measurements at longer wavelengths (this is in the wavelength region where the value of QE_{FW} is on the order of 10^{-2} to 10^{-3}).

$$IQE_{BW}(\lambda) = \left\{\frac{IQE_{FW}}{QE_{BW}}\left(\lambda_{long}\right)\right\} QE_{BW}(\lambda) \tag{2.12}$$

The measured bi-facial spectral responses at different voltage biases for the $Cu(In,Ga)Se_2$ solar cells with semi-transparent Mo contacts of Table 2.6 are shown in Figure 2.13. The bi-facial internal quantum efficiencies are shown in Figure 2.14. Also shown in Figure 2.14 are the internal quantum efficiencies calculated from fitting the measured data to Equations 2.9 and 2.10. Table 2.7 and Figure 2.15 give the parameters used for the calculated internal quantum efficiencies.

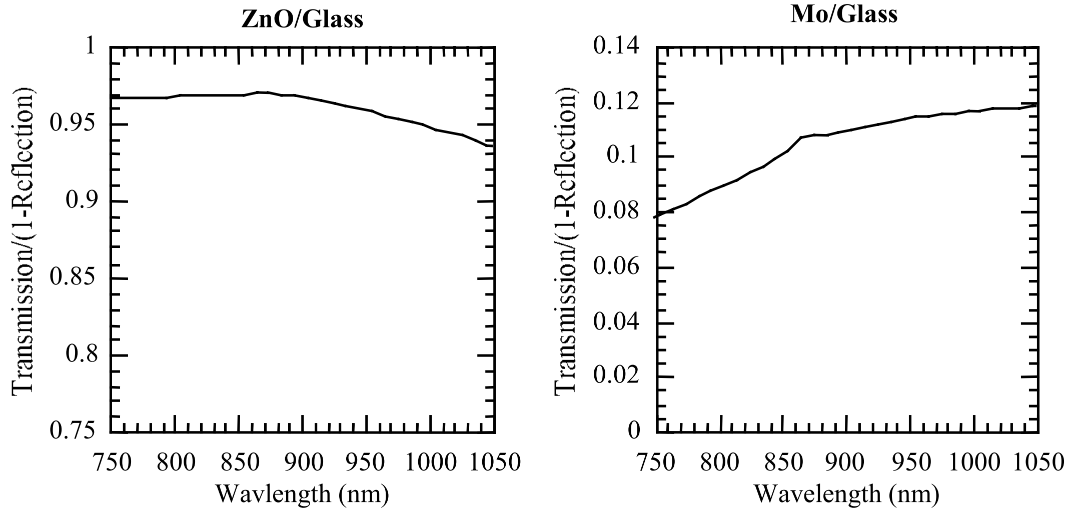


Figure 2.12 Optical absorption measured through both the ZnO and 0.04 μm thick semi-transparent Mo in the wavelength region of analysis.

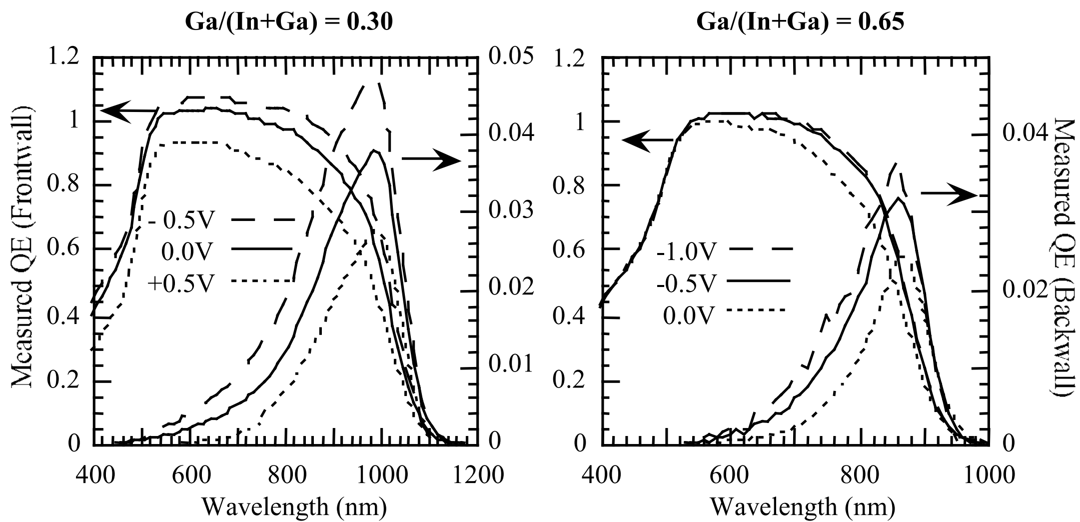


Figure 2.13 Spectral responses measured at different voltage biases through both the ZnO/CdS (frontwall) and semi-transparent Mo contact (backwall) for cells containing 30% and 65% Ga.

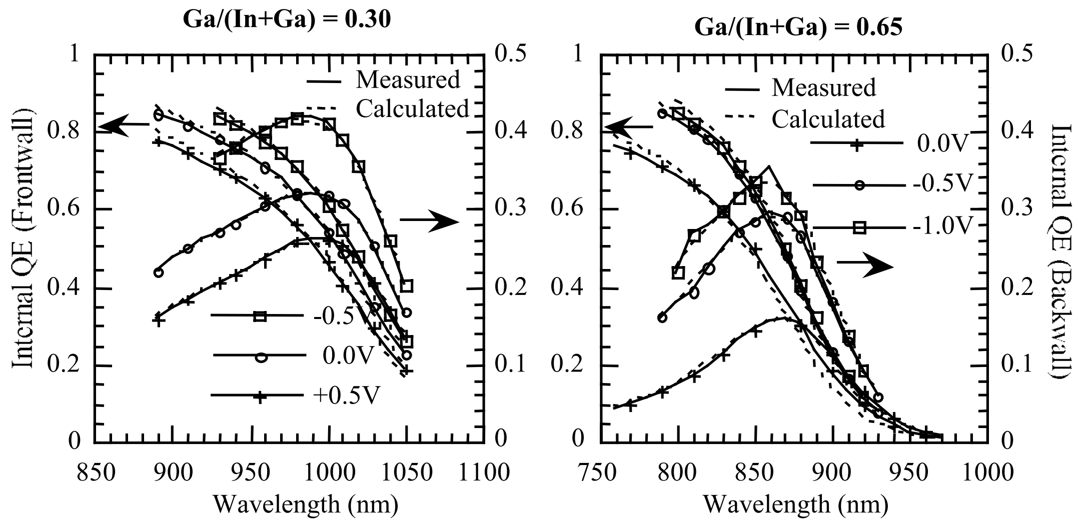


Figure 2.14 Calculated (from the parameters in Table 2.7) and measured internal quantum efficiencies at different voltage biases through both the ZnO/CdS (frontwall) and semi-transparent Mo contact (backwall) for cells containing 30% and 65% Ga.

Table 2.7 Diffusion lengths and collection widths from the calculated internal quantum efficiencies (Figure 2.14) and optical absorption coefficients (Figure 2.15).

		Collection Width: w (µm) Voltage Bias (Volts)			
Ga/(In+Ga)	**L (µm)**	**-1.0**	**-0.5**	**0.0**	**+0.5**
0.30	0.8		1.4	1.0	0.7
0.65	0.1	1.3	1.2	0.7	

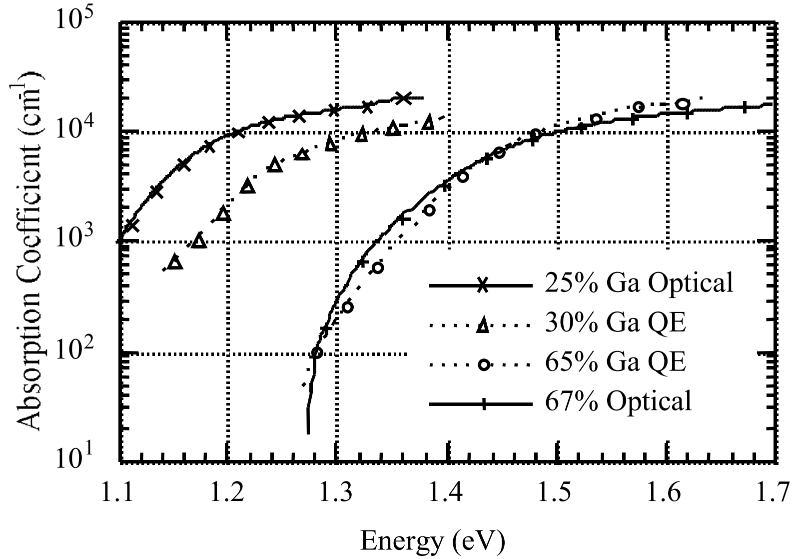


Figure 2.15 Optical absorption coefficients derived from measured optical data for films containing 25% and 67% Ga and from the internal quantum efficiency measurements for the cells containing 30% and 65% Ga.

The results of Table 2.7 show why there is a decrease in the light generated current with increasing voltage for samples with higher Ga content. If the total width for minority carrier collection is w + L (drift + diffusion), then this quantity is already less than 1 µm at J_{SC} (0.0V) for 65% Ga. Because this width is dominated by drift, it will continue to decrease with increasing forward bias, leading to a lowered FF and a substantial $J_L(V)$. This method also produces the optical absorption coefficient (α) of the samples as shown in Figure 2.15. The comparison with absorption coefficients derived from optical reflection and transmission measurements of Cu(In,Ga)Se_2 films made with comparable Ga concentrations is fairly good. Care must be used in the interpretation at small values of α derived from QE because of the of reflected light from the Mo back contact creating additional optical absorption and minority carrier generation in the Cu(In,Ga)Se_2 (this would increase the calculated α above its true value).

2.2.3 Conclusions

Analysis of these J-V measurements made as a function of light intensity has shown that the main cause of the decrease in performance is a voltage dependent light generated current [4,7]. Also, bi-facial spectral response measurements have shown that the minority carrier diffusion length decreases with increasing E_G, thereby making the minority carrier collection from the voltage dependent space charge region more important [9]. However, it has not been demonstrated that the voltage dependent light generated current can be explained solely by the reduction in minority carrier diffusion length.

In order to demonstrate this, bi-facial J-V measurements will be made as a function of light intensity, and bi-facial QE measurements will be made as a function of bias voltage on the same devices. The voltage dependent light generated current will be determined from analyzing the J-V measurements, and the voltage dependent collection length (diffusion + space charge) will be

determined from analyzing the bi-facial QE measurements done at various voltage biases. The voltage dependent light generated current predicted from the QE analysis (by integrating over the AM1.5 global spectra) will be compared to that obtained from the J-V measurements made as a function of light intensity.

2.3 Sulfurization of Cu, In, and Cu/In Precursors

The incorporation of sulfur into $CuInSe_2$ thin films was quantitatively investigated to establish a scientific and engineering basis for the fabrication of homogeneous and compositionally graded $CuIn(Se,S)_2$ thin films. The motivation for this work was to develop a means of controlling the band gap for this class of materials to achieve improved performance in photovoltaic devices. The approach taken was the reaction of thin-film Cu/In layers and $CuInSe_2$ thin films in H_2S and/or H_2Se gasses at atmospheric pressure. This work was the basis of a Ph.D. dissertation, *Growth and Characterization of Copper Indium Diselenide Polycrystalline Thin Films for Photovoltaic Applications*, by Michael G. Engelmann [10].

Cu, In and Cu/In precursors on both soda lime glass and Corning 7059 glass were reacted in $H_2S:O_2:Ar$ at temperatures ranging from 250°C to 550°C. The samples were then analyzed using XRD and SEM/EDS to determine phases and composition. For In samples on soda lime glass reacted at temperatures of 350°C or higher, the dominant phase was found to be $Na_2In_2S_4$. Indium films were also selenized at 550°C in an effort to identify an analogous phase. XRD analysis revealed the presence of an unknown phase, which is postulated to be '$NaInSe_2$' in analogy with the sulfide phase. The presence of the $Na_2In_2S_4$ and '$NaInSe_2$' phases was verified in $CuInS_2$ and $CuInSe_2$ films fabricated on soda lime glass.

On Corning 7059 glass, $Cu_{2-x}S$ was identified on sulfurized Cu films, In_6S_7 and In_2S_3 were identified in In films reacted at 250°C and higher temperatures, respectively. Cu/In layers were found to fully react only above 350°C, with $Cu_{11}In_9$ found at 350°C temperature reactions and lower. $CuInS_2$ was the only identifiable phase in the fully reacted films. Time progressive sulfurization treatments were completed, which showed that approximately 15 minutes is required for $CuInS_2$ to fully form for the reaction of Cu/In precursors at 450ºC. This was found to be comparable to the predicted rate of formation of $CuInSe_2$. Time-species profiles generated from the time progressive data correlated well with the published reaction model. A baseline sulfurization process was developed for the formation of $CuInS_2$ films and devices. Fabricated $CuInS_2$ films yielded efficiencies consistently above 7%.

With further optimization, the baseline sulfurization process may be improved to produce $CuInS_2$ devices with efficiency > 10%. This should be possible because devices with this efficiency have been reported using this process. Improvements could be achieved by using soda lime glass substrates to introduce Na into the films, which may have beneficial effects similar those observed in $Cu(In,Ga)Se_2$ based devices. Optimization of the Cu/In ratio before reaction could also be used to further improve device performance.

$CuIn(Se,S)_2$ polycrystalline thin films were fabricated by reaction of layered Cu/In metal precursors in an $H_2S:H_2Se:O_2:Ar$ atmosphere. The $H_2S/(H_2Se+H_2S)$ fraction was controlled and varied from 0.5 to 0.99 and temperature was maintained at 450°C for all treatments. The solid phase composition of the $CuIn(Se,S)_2$ films after reaction for 120 minutes was found to

correspond to the compositional dependence predicted by an equilibrium replacement reaction between H_2S-H_2Se and $CuInSe_2$-$CuInS_2$, including ideal and non-ideal mixing effects. This reaction was shown to strongly favor the presence of $CuInSe_2$ at 450°C.

The presence of O_2 during reaction was treated as an agent for the decomposition of H_2S and H_2Se in the gas phase, resulting in the liberation of Se_x and S_x polymers. For calculation of the upper limit of the contribution of the polymers, x was taken to be 2, since the dimers are the most reactive of the possible polymers. The interaction of the dimers with the $CuIn(Se,S)_2$ film was taken to be an alternate replacement reaction between Se_2-S_2 and $CuInSe_2$-$CuInS_2$, which favors the presence of $CuInS_2$. The result of this alternate reaction was the prediction of a minimum incorporation of sulfur into the films, dependent on the concentration of O_2 introduced to the system. This prediction was also supported by the experimental data.

Based on these results, prediction and control of the band gap in the fabrication homogeneous films is possible, however, the use of hydride gases results in a high degree of compositional sensitivity in the solid phase to the gas phase composition in the range of interest. Control of the flow rates becomes critical in this situation. The use of polymer Se_2 and S_2 in the gas phase instead of H_2Se and H_2S results in the preferred presence of $CuInS_2$. In this reaction the solid phase composition has less sensitivity to the gas phase composition and could result in better control. Polymers of Se_n and S_n with $n > 2$, would increase this sensitivity. With improved control of the gas phase composition, this method is feasible for the engineering of $CuIn(Se,S)_2$ to optimize the band gap for the solar spectrum.

Further verification of the validity of the proposed model is needed in two areas. First, varying the O_2 concentration should test the compositional dependence on the concentration of O_2 in the gas phase and the relative effect of S_2 and Se_2. The minimum sulfur incorporation in the $CuIn(Se,S)_2$ films should vary proportionally with the O_2 concentration. Second, the temperature dependence of the $CuIn(Se,S)_2$ film composition should be tested by repeating the experiment at multiple temperatures. The prediction of the model is that the incorporation of sulfur should be enhance with a decrease in reaction temperature and depressed with an increase in reaction temperature.

$CuInSe_2$ polycrystalline thin films were evaporated from the elements at a substrate temperature of 550°C, and a Cu/In ration of 1.05 to 1.2. The samples were subsequently annealed in an H_2S:Ar atmosphere. The time and temperature of treatment were systematically varied and samples were quenched at the end of the treatment time. XRD peak profiles of the (112) reflection were measured. The measured peak profiles were modeled applying the 2-D solution to the diffusion of a constant source into a finite medium with parallel grain boundaries and a reflecting back surface to a cylindrical grain geometry. The distribution of grain sizes were measured and found to be consistent over changes in Cu/In ratio from 0.9 to 1.2. Compositional maps of each grain size were weighted and mapped to XRD peak profiles in intensity versus 2θ. The modeled profiles were matched to the measured profiles for sulfurization treatments at 500°C using bulk and grain boundary diffusion coefficients of $3.0\text{x}10^{-12}$ and $3.0\text{x}10^{-10}$, respectively. Similarly, XRD peak profiles of sulfurization treatments at 450°C and 525°C were also modeled. An exponential fit was applied to the resulting diffusion coefficients. Activation energies of 1.0 eV and 0.4 eV were estimated for bulk and grain boundary diffusion,

respectively. Modeling Auger depth profiles near the film surface yielded estimates of the bulk diffusion coefficient at 450ºC and 500ºC that were in good agreement with the XRD analysis.

The enhancement of sulfur diffusion due to grain boundaries was found to be moderate for the films studied. This result suggests that graded structures fabricated by a reaction/diffusion process can not be adequately described by an average sulfur depth profile through the film. Any attempt to provide a detailed model of device behavior in graded band gap solar cells should account for this non-uniformity.

Expansion of data points over a broader temperature range is necessary to add confidence to the estimated values for the diffusion activation energies. Preliminary data suggests that there may be a dependence of diffusion on Cu/In ratio in the starting $CuInSe_2$ films. A systematic set of identical sulfurization treatments over a range of Cu/In ratios is necessary to establish the existence and functionality of this dependence. The validity of this analysis technique can be strengthened by application to the diffusion of S into a single crystal or epitaxial layer of $CuInSe_2$. This would eliminate the presence of grain boundaries. The measured broadening of the x-ray diffraction peak profiles would then be uniquely due to the bulk diffusion.

To summarize, both reaction chemistry and diffusion were employed to provide a fundamental basis of understanding for the fabrication of homogeneous and graded $CuIn(Se,S)_2$ thin films by reaction in a S or Se containing atmosphere. The reaction analysis showed that the film composition can be predicted and controlled based on the gas phase composition. Either hydride gasses or elemental Se and S can be used in the gas phase. The use of Se and S polymers results in the favored presence of $CuInS_2$ and the use of hydride gasses results in the favor of $CuInSe_2$. An important outcome of this analysis is if a mixture of both polymers and hydrides were used, the film composition could be fixed by control of their relative concentrations. This would move the process away from the compositional extremes where film composition varies rapidly with gas phase composition. The presence of oxygen during reaction in H_2S/H_2Se accomplishes this to a small degree. However a high concentration of oxygen would be necessary to achieve a high degree of sulfur incorporation in the film. This could pose a safety hazard, since H_2S and H_2Se are both flammable gasses. If the use of polymers were to be applied, the relative contributions of each existing polymer from S and Se to S_8 and Se_8 at the temperature of the treatment should be considered.

The analysis also suggests that the starting films are not required to be Cu/In layers, but could be $CuInSe_2$ or $CuInS_2$ films as well as many other types of precursors. This provides a possible means of incorporating a controlled degree of sulfur uniformly into $CuInSe_2$ films fabricated by other processes. This would make this technique convenient to add to existing fabrication processes for commercial use.

The diffusion of sulfur into $CuInSe_2$ films by reaction in a sulfur-containing atmosphere is closely related to the above discussion. The analysis of the diffusion process reveals the spatial distribution of sulfur in films that are not in an equilibrium or steady state. The same atmospheric conditions as described for the fabrication of uniform films can be used in this process. A mixed gas phase containing Se and S polymers and/or hydride gasses could be used to approximately fix the composition of the film surface. The sulfur diffusion could then be used to fabricate films with the desired steepness and penetration of grading by control of the time and

temperature of treatment. For the reduction of recombination current near the junction in graded devices, the grading should ideally be very steep and only extend through the space charge region. This type of profile can be nearly achieved, based on the results of this work, by a five-minute sulfurization treatment at 450ºC, but depends on film properties such as grain size distribution, film thickness, and grain geometry. The short time needed makes grading by this method desirable for commercial applications. This step could be added to existing processes without modification of other steps.

In effect, both the diffusion analysis and the steady state analysis describe the same process and the same system in two different regimes. The treatment always begins as a surface reaction / diffusion process and, if carried out long enough, results in a uniform film with composition determined by the gas phase composition. The diffusion analysis then gives an indication of how long it is necessary to wait to obtain a uniform film. This depends on the temperature of reaction and the thickness of the film.

The short time involved in obtaining the appropriate grading in films is desirable in a manufacturing process. The projected ability to effectively control the film composition using gas phase composition, temperature, and time make this process well defined and flexible. And lastly, the ability to add this treatment to existing processes without additional modifications suggests that this process would be relatively simple to add into an existing commercial production line. Therefore, this process has the potential of being a robust means of improving device and module performance in commercial applications.

3. a-Si-BASED SOLAR CELLS

3.1 Micro-crystalline p-layers

3.1.1 Introduction

During the present reporting year the investigation of glow discharge deposited crystalline p-layers was conducted in two parts. In the first part, we have investigated the deposition and characterization of these types of films having high level of CH_4 in the feed gas which completed the investigation of carbon containing p-layers. The goal was to determine the feasibility of obtaining crystalline SiC phases in the films. The second part of the work deals with investigation of the deposition and characterization of films having CO_2 in the feed gas. The goal here was to obtain two phase films of crystalline Si imbedded in a matrix of a-Si:O:H:C. The idea is that such films incorporated in p-i-n type devices could give high currents due to the transparency of the amorphous phase and high voltages due to the highly conductive crystalline phase with a smaller junction surface. Also, the presence of CO_2 in the glow discharge plasma would tend to decrease the reducing effects of the plasma on the thin conductive oxide used as the front contact in superstrate devices.

3.1.2 Experimental Approach

The p-layers were deposited on 7059 glass and on SnO_2 substrates, and their crystallinity and deposition rates were determined by Raman spectroscopy [11] and by profilometry. In-plane conductivity and activation energy measurements were also performed on most of the films deposited on glass substrates.

The main experimental variables were the hydrogen dilution and CH_4 or CO_2 content in the feed gases. The secondary parameters were discharge power density and doping gas (B_2H_6) level. In designing experiments and interpreting results, normalized flows rather than the actual gas flows were used. These normalized flows were defined as,

$$c = f(CH_4) / [f(SiH_4) + f(CH_4)]$$

$$h = f(H_2) / [f(SiH_4) + f(CH_4)]$$

$$b = 2 \times f(B_2H_6) / [f(SiH_4) + f(CH_4)]$$

for the deposition of carbon containing p-layers, and

$$o = f(CO_2) / [f(SiH_4) + f(CO_2)]$$

$$h = f(H_2) / [f(SiH_4) + f(CO_2)]$$

$$b = 2 \times f(B_2H_6) / [f(SiH_4) + f(CO_2)]$$

for the deposition of oxygen containing p-layers.

For all depositions substrate temperature was kept at 150°C. Except in few cases discharge pressure, SiH_4 partial pressure and residence times were also kept constant throughout the study by introducing He to the discharge as a buffer gas.

1.1.3 Results and Discussion

3.1.3.1 Films Deposited from CH_4 Containing Discharges

Here we investigated the flow ranges of $0.5 \leq c \leq 0.94$, $5 \leq h \leq 227$, and $b = 2 \times 10^{-3}$. SiH_4 partial pressure and total pressure were kept constant at 2.2 mT and 1 Torr levels, respectively. Table 3.1 gives the deposition parameters of a set of films deposited with c = 0.5.

Table 3.1 Deposition parameters of microcrystalline p-layers with c = 0.5 and discharge power density of 168 mW/cm^2. R is the deposition rate and c-Si is the amount of crystalline Si phase in the films as determined by Raman spectroscopy.

Gas Flows (sccm)					h	Glass Substrate		SnO_2 Substrate (1)	
SiH_4 (90% H_2)	CH_4	B_2H_6 (99.8% H_2)	H_2	He		R (Å/s)	c-Si (Vol%)	R (Å/s)	c-Si (Vol%)
10	1	1		445	5	0.38	0		NA
10	1	1	70	380	40	0.22	1		0
10	1	1	140	310	75	0.18	61		0
10	1	1	290	170	150	0.07	84		28
10	1	1	445		227	0.04	100		74

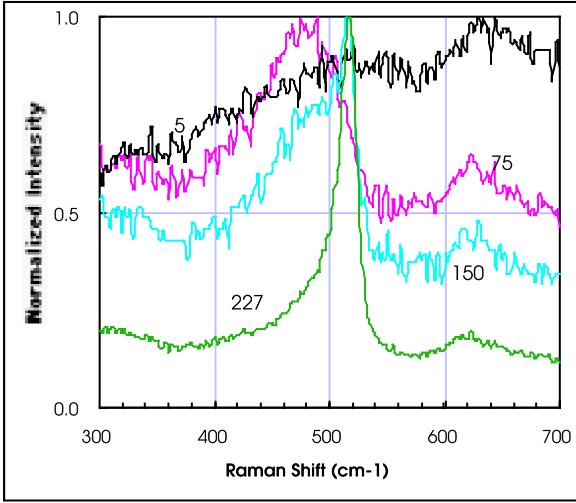
(1): Film thicknesses could not be measured due to textured surface

No crystalline SiC phase (peak at 800 cm^{-1}) was observed in the Raman spectra of these films.

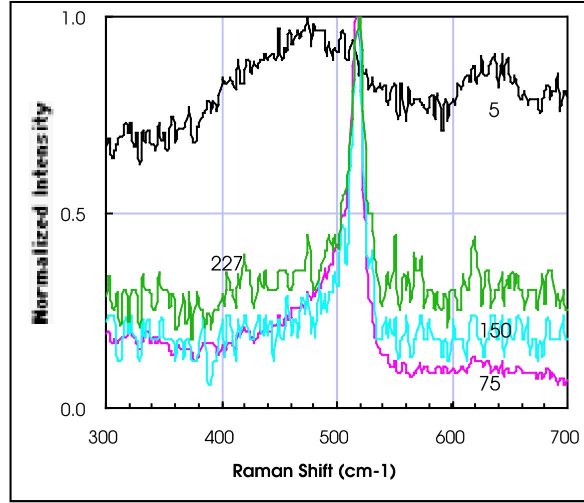
The spectra from 300 to 700 cm^{-1} are given in Figure 3.1. Films deposited on SnO_2 have no identifiable structure for h = 5 and, as h is increased, change gradually from a-Si:C:H (broad peak at 480 cm^{-1}) to a mixture of from a-Si:C:H and c-Si H (peak at 520 cm^{-1}). On glass, however, they start being a-Si:C:H at h = 5 but become entirely c-Si at hydrogen dilution of 227.

As can be seen from Table 3.1, while the onset of crystallinity on glass substrates is at hydrogen dilution of 40, on SnO_2 substrates it is between 75 and 150.

Table 3.1 also shows that the increase in hydrogen dilution h not only increases crystalline silicon volume fraction but also results in the decrease of deposition rate. Consequently, it is difficult to ascribe the change in crystallinity uniquely to changes in hydrogen dilution. However, at least for $40 \leq h \leq 75$ crystallinity is mainly controlled by hydrogen dilution since deposition rate shows a relatively small change within this range.



(a) Glass/SnO_2 substrate



(b) Glass substrate

Figure 3.1 Raman spectra of the films deposited c = 0.5 at a power density of 160 mW/cm^2. The labels give hydrogen dilution levels.

Analysis of films deposited under identical conditions but at 84 mW/cm^2 power density gave qualitatively similar results in terms of changes in crystallinity and deposition rate with hydrogen dilution. More quantitatively, however, deposition rates and crystalline Si volume fractions were found to be lower for the same hydrogen dilution. The results are shown in Table 3.2.

A number of films were also prepared at hydrogen dilution of 75 with c = 0.83 and 0.94 and with power densities from 168 to 420 mW/cm^2. Raman spectra of all these films were found to be featureless, lacking any of the characteristic peaks for crystalline or amorphous phases of interest.

Table 3.2 Deposition rate and crystallinity of the films deposited with power density of 84 mW/cm^2. All other parameters are the same as films of Table 3.1.

h	Glass Substrate		SnO_2 Substrate (1)	
	R (Å/s)	c-Si (Vol%)	R (Å/s)	c-Si (Vol%)
5	0.32	0		0
40	0.18	3		0
75	0.13	54		0
150	0.06	67		60
227	0.00 (2)	68 (2)		42

(1) Film thicknesses could not be measured due to textured surface
(2) No deposition at the center of the substrate, Raman spectrum taken at the edge.

3.1.3.2 Films Deposited from CO_2 Containing Discharges

In a first step, we have performed a deposition under conditions that favor crystallinity in films with CH_4 containing discharges for the purpose of evaluating crystallinity and carbon and oxygen incorporation into the film. The conditions chosen were:

SiH4 flow	20 sccm
Power Density	420 mW/cm^2
Pressure	1 Torr

h = 154

o = 0.23

b = $1.5x10^{-3}$

The films deposited simultaneously on 7059 glass and on smooth SnO_2 substrates were analyzed by Raman for their crystallinity and by SIMS for their composition. Figure 3.2 shows the Raman spectra of the films deposited on these two substrates. Data clearly shows the existence of a two-phase mixture consisting of c-Si and amorphous silicon phases. Also, the film deposited on glass seems to have a higher amount of c-Si phase. In fact, analysis of the data gives c-Si volume fraction of ≈ 45% for the film on glass, and of ≈ 35% for the film on SnO_2.

SIMS depth profile of the films is given in Figure 3.3. The data indicate that:

- the composition of the films are independent of the substrate,
- oxygen content of the films is more than two orders of magnitude higher than the carbon content,
- since the depth scale was calibrated by measuring the depth of the analysis crater, the profiles give a quite accurate difference of the film deposition rates on glass and on SnO_2 substrates: a factor of 1.7 higher on SnO_2.

It is important to note that since the films have a c-Si and an amorphous phase, the latter must contain, besides silicon and some boron, almost all the hydrogen, carbon and oxygen observed in the SIMS analysis. Thus, it can be concluded that the amorphous phase is essentially hydrogenated silicon oxide containing small amounts of carbon and boron.

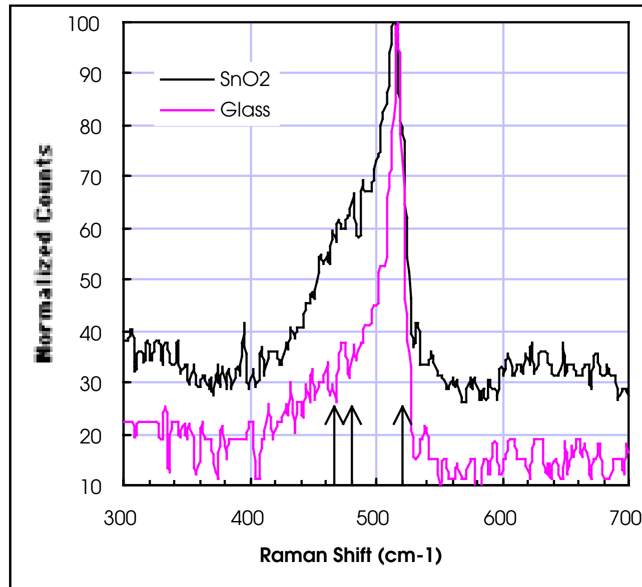


Figure 3.2 Raman spectra of the films deposited on 7059 glass and SnO_2 substrates from a CO_2 containing discharge. The arrows indicate the positions of c-Si at 520 cm_{-1}, the amorphous phase at 480 cm^{-1} and quartz at 465 cm^{-1}.

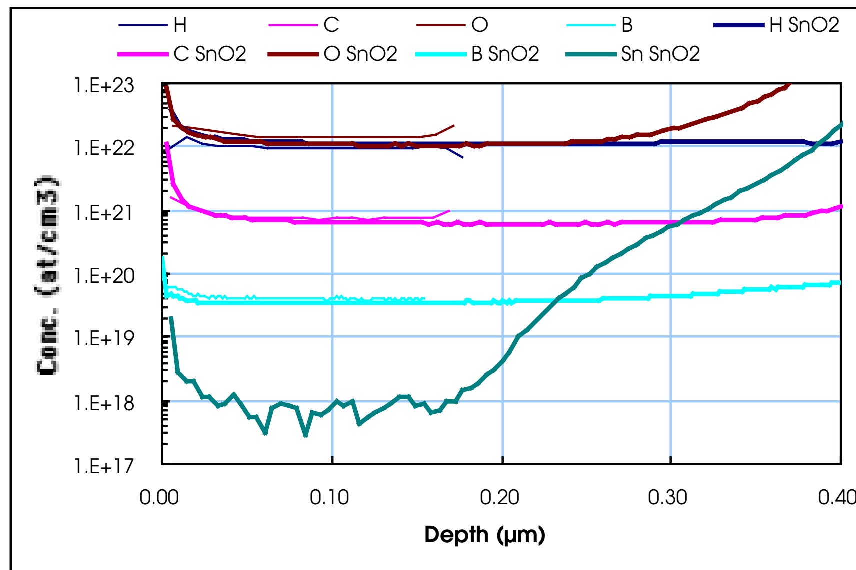


Figure 3.3 SIMS depth profiles of the films deposited on 7059 glass and SnO_2 substrates from a CO_2 containing discharge.

In the next step, films deposited at two different diborane dilutions "b" for a range of hydrogen dilution "h" were investigated. They were characterized for their crystallinity by Raman spectroscopy and their deposition rates determined by profilometric measurement of their thickness. Total pressure, silane partial pressure and discharge power density were, respectively, 5 mT, 1 Torr and 168 mW/cm^2. Table 3.3 summarizes deposition conditions and the measured film properties.

Table 3.3 Deposition conditions and measured characteristics of films deposited at two different diborane concentrations in the plasma for a range of hydrogen dilutions. Silane partial pressure 5 mT, discharge pressure 1 Torr, power density 168 mW/cm^2.

Gas Flows (sccm)							Glass Substrate				SnO_2 Substrate	
SiH_4 (90% H_2)	CO_2	B_2H_6 (99.8% H_2)	H_2	He	b	h	R (Å/s)	σ_d (S/cm)	E_a (eV)	c-Si (Vol%)	R (Å/s)	c-Si (Vol%)
20	0.6	10	0	370	$1.5x10^{-2}$	11	0.46	$3.8x10^{-08}$	0.54	1	0.63	0
20	0.6	10	75	295	$1.5x10^{-2}$	40	0.47	$4.7x10^{-08}$	0.54	5	0.63	0
20	0.6	10	145	225	$1.5x10^{-2}$	67	0.38	$1.3x10^{-04}$	0.15	13	0.63	0
20	0.6	10	232	138	$1.5x10^{-2}$	100	0.44	$1.2x10^{-03}$	0.10	13	0.49	0
20	0.6	10	368	0	$1.5x10^{-2}$	152	0.31	$1.7x10^{-01}$	0.06	42	0.47	16
20	0.6	1	0	380	$1.5x10^{-3}$	7	0.47	$5.0x10^{-11}$	0.70	0	0.76	0
20	0.6	1	40	338	$1.5x10^{-3}$	23	0.24	$1.8x10^{-05}$	0.23	10	0.49	0
20	0.6	1	72	305	$1.5x10^{-3}$	35	0.28	$7.2x10^{-03}$	0.11	36	0.44	0
20	0.6	1	110	270	$1.5x10^{-3}$	50	0.25	$1.3x10^{-01}$	0.07	58	0.42	22
20	0.6	1	150	230	$1.5x10^{-3}$	65	0.21	$1.5x10^{-01}$	0.07	62	0.33	25
20	0.6	1	190	187	$1.5x10^{-3}$	80	0.28	$1.4x10^{-01}$	0.07	67	0.35	43
20	0.6	1	240	138	$1.5x10^{-3}$	100	0.17	$3.1x10^{-01}$	0.06	74	0.28	47
20	0.6	1	381	0	$1.5x10^{-3}$	154	0.11	$2.3x10^{-01}$	0.07	71	0.22	50

First thing to note is that for the diborane concentration of b = 0.0015, the microcrystalline phase is observed at remarkably low hydrogen dilutions of h = 23 and 50, respectively, for 7059 glass and tin oxide substrates, even at such a low power density utilized here.

More generally, it is found that fraction of c-Si increases with increasing hydrogen dilution and decreases with increasing diborane level. Figure 3.4(A) displays this dependence. However, the degree of validity of this observation depends on the film deposition rates shown in Figure 3.4(B). This is because bonding rearrangement on the surface of the growing film that favors c-Si formation will be more extensive for low deposition rates. Consequently, dependence of crystallinity on hydrogen dilution is only clearly established for films deposited with low diborane levels with $23 \le h \le 100$ in the case of glass substrates and with $35 \le h \le 80$ in the case of tin oxide substrates. In the case of high diborane levels, the corresponding hydrogen dilution levels are $11 \le h \le 100$ and $11 \le h \le 67$, respectively. The deposition rate argument can also explain the difference in crystallinity between like substrates deposited at different diborane levels.

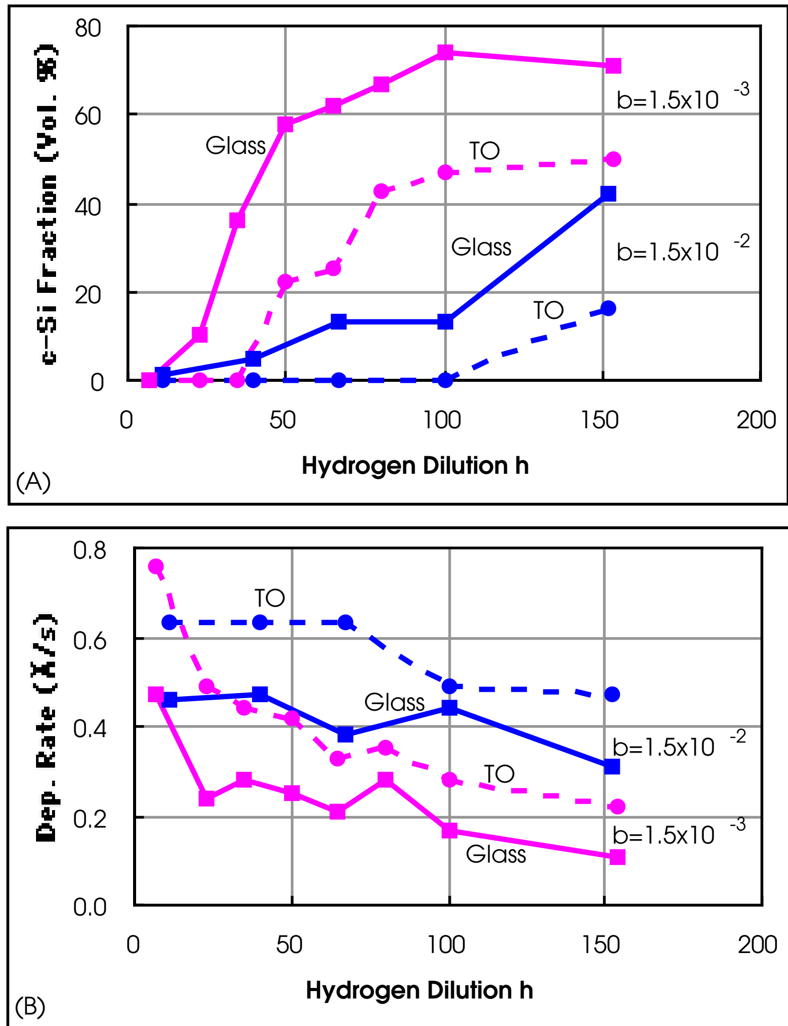


Figure 3.4 Crystalline fraction and deposition rate as a function of hydrogen dilution for two different gas phase diborane levels.

However, the difference in crystallinity between glass and tin oxide substrates for a given diborane level might also be controlled, in addition to deposition rate, by the possible difference in the initial nucleation rate of crystallites on glass and tin oxide surfaces.

Factors influencing the deposition rate are can be seen in Figure 3.4(B), most important being the conductivity of the substrate. This is most probably due to the voltage difference between the substrate and the plasma. In the case of a conductive substrate such as SnO_2, the surface is grounded and the potential difference between the substrate and the plasma is the plasma potential. In the case of the glass substrate, the potential difference is the floating potential which is, in general, substantially smaller than the plasma potential. Also affecting the deposition rate are hydrogen dilution and diborane levels in the discharge. Increasing hydrogen dilution reduces deposition even though silane partial pressure and gas residence time stay the same. This observation supports hydrogen etching of the film during growth. Finally, the

observed increase in deposition rate with gas phase diborane concentration is related to the known ability of diborane in cracking silane molecules.

As to the interpretation of the measured conductivities and activation energies, because of the two-phase nature of these films the in-plane measurements of these characteristics do not provide much useful information. However, it can be pointed out that measured activation energies of 0.07 eV are, within experimental errors, that of boron in silicon and, as such, confirm that in this respect silicon crystallites in the films behave like bulk silicon.

In the final step of the investigation a number of films were deposited at different CO_2 as a function of hydrogen dilution, with $b = 1.5x10^{-3}$ and keeping all other depositions the same as given in Table 3.3. c-Si content in these films is given in Figure 3.5 for glass and SnO_2 substrates. The data show that while the CO_2 level in the discharge does not seem to have an effect on the c-Si content in the case of glass substrates, it does, however, control crystallinity of the films deposited on SnO_2 substrates.

3.1.3.3 Conclusion

Evolution of crystallinity in glow discharge deposited boron doped carbon and oxygen containing films (CH_4 and CO_2 containing discharges respectively) has been investigated as a function of deposition parameters including hydrogen dilution. The only crystalline phase identified was silicon. Volume fraction of the crystalline phase was found to depend on hydrogen dilution but not on the discharge power. High silane partial pressures resulting in high deposition rates suppress the formation of crystalline phase. On the other hand discharge power does not control crystallinity in a significant way and high levels of crystallinity were obtained at very low power densities. Crystallinity in the films was found to decrease with an increasing amount of CH_4 or CO_2 in the discharge. The amount of crystalline phase in the films deposited on SnO_2 was consistently lower than in the films deposited on glass substrates.

During the next phase of the program, crystallinity of very thin films, in the order of 150 Å, deposited on SnO_2, ZnO and glass substrates will be investigated and based on these results we will proceed with the incorporation of these films into p-i-n type devices.

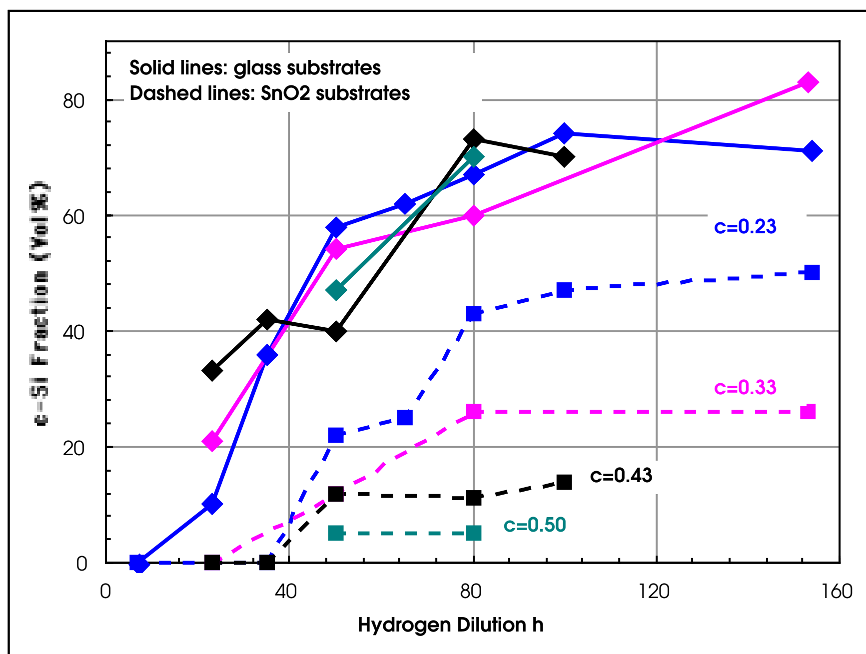


Figure 3.5 Volume fraction of c-Si as a function hydrogen dilution for different levels of CO_2 in the discharge.

3.2 Effect of H_2 Plasma and c-Si Deposition on SnO_2 and ZnO/SnO_2 Bilayers

It has been well known for over 15 years that exposure of SnO_2 films to H_2 plasma or deposition of a-Si by plasma CVD can lead to degradation in optical transmission. The SnO_2 is chemically reduced, leaving a thin but highly absorbing Sn-rich layer [12,13,14]. It has been reported that degradation can be minimized or even eliminated by using low substrate temperatures [14,15], at faster a-Si growth rates [15], or by covering the SnO_2 with a thin protective sputtered ZnO:Al layer [16,17,18]. The ZnO properties are relatively inert to H_2 plasma damage [14,15] although the H_2 penetrates several hundred Angstroms into the ZnO [15,19] and increases its bandgap (8). These conclusions also apply to growth of µc-Si from high H_2 dilution by hot wire CVD; ZnO is immune to damage while SnO_2 is not [20].

However, there are conflicting results from different studies regarding plasma interaction with SnO_2 or ZnO. One of the leading SnO_2 manufacturers, Asahi Glass, has shown that the optical transmission of their SnO_2 is not degraded by H_2 plasma over the range from 100 to 300°C [21], in direct contradiction to results from other groups, as well as their own later work [16]. Some groups find that a thin ZnO layer does not protect the SnO_2 [22,23]. Some groups observe a decrease in R_{sh} of the SnO_2 upon exposure to plasma [18,21] while others do not [24]. Some of these differences could be due to differences in SnO_2 structure, ZnO sputtering conditions [23], or differences in H_2 plasma conditions studied by different groups.

Degradation of the SnO_2 due to interaction between the plasma is likely to get worse under conditions required for growth of µc-Si layers, i.e., higher H_2 dilution and slow growth rates. This could impact our ability to incorporate the µc-Si films under development this past year into superstrate devices.

Therefore, we performed a study to determine the influence of four variables: substrate temperature during plasma exposure; the ZnO protective layer thickness; the SnO_2 supplier; and comparing H_2 plasma with deposition of μc-Si films at the same temperature. The goals were to identify if there were different sensitivities to H_2 plasma between two different commercially available SnO_2 products used for superstrate a-Si device fabrication; to separate changes in carrier mobility from carrier density; and to investigate the ability of sputtered ZnO:Al to protect the underlying SnO_2 from damage.

The textured SnO_2 substrates were from either Asahi (Type U) or AFG (provided by Dr. Ganguly of Solarex Thin film). Initial sheet resistances were ~13 and ~10 Ohm/sq, respectively. Some of Asahi SnO_2 substrates were coated with 20 and 60 nm sputtered ZnO layers before exposure to the plasma. The ZnO thicknesses were chosen to trade-off the optical losses with the protective abilities. A ZnO layer of 60 nm was thought to be sufficiently thick to prevent any plasma interaction with the SnO_2 but has 1-2% absorption beyond 500 nm: whereas a layer of 20 nm has negligible absorption losses but its ability to protect the SnO_2 was unknown since H can penetrate several hundred Angstroms through sputtered ZnO [16,20]. The sheet resistances of the 20 and 60 nm ZnO films were 900 and 250 Ohms/sq, respectively. They were RF sputtered onto unheated Asahi SnO_2 substrates at 3 mT in an Ar/O_2 atmosphere. Four substrates were placed in each H_2 plasma exposure or Si deposition: uncoated Asahi, uncoated AFG SnO_2, and Asahi SnO_2 pieces with 20 or 60 nm ZnO protective layers. The H_2 plasma conditions were 30 Watts, 100 sccm of H_2 at 1 Torr for 1 minute. The substrate temperatures were 100, 150 and 200°C. These conditions are similar to those used in the study by Asahi [21]. The Si deposition was under conditions which have yielded >80% crystallinity at similar thickness on glass: 50 Watts, SiH_4/H_2 = 20/200 sccm at 1 Torr, 150°C, for 2 minutes. The Si growth rate is ~ 0.2 Å/s. Optical transmission, sheet resistance and Hall effect measurements were made before and after plasma treatments.

Figure 3.6 and Figure 3.7 show the optical transmission of the Asahi and AFG samples, respectively. For both brands of SnO_2, H_2 plasma exposure at 100°C (not shown) or 150°C resulted in no change to the transmission while exposure at 200°C (shown) caused losses in the visible transmission. This is similar to what has been reported by others and attributed to increased absorption by the Sn-rich layer formed by chemical reduction of the SnO_2. Losses are much greater for the AFG SnO_2 compared to the Asahi SnO_2. However, Figure 3.6 shows that the transmission of the 20 nm ZnO coated piece is the same as the initial SnO_2 even with the 200°C plasma treatment. The transmission of all pieces with ZnO were unaffected by H_2 plasma at any temperature. Figure 3.8 shows the transmission of Asahi SnO_2 with and without the 20 nm ZnO layer following μc-Si film deposition or H_2 plasma, both at 150°C. They are essentially the same. From the optical transmission spectra in Figure 3.6, Figure 3.7, and Figure 3.8, we conclude that the threshold for damage to bare SnO_2 is between 150 and 200°C, that 20 nm of ZnO is sufficient to protect the SnO_2 from plasma-induced damage even at 200°C and that bare SnO_2 is unaffected by either a H_2 plasma or μc-Si deposition at 150°C. However, as discussed next, there are beneficial effects to the electronic properties with either H_2 or Si processing at 150°C.

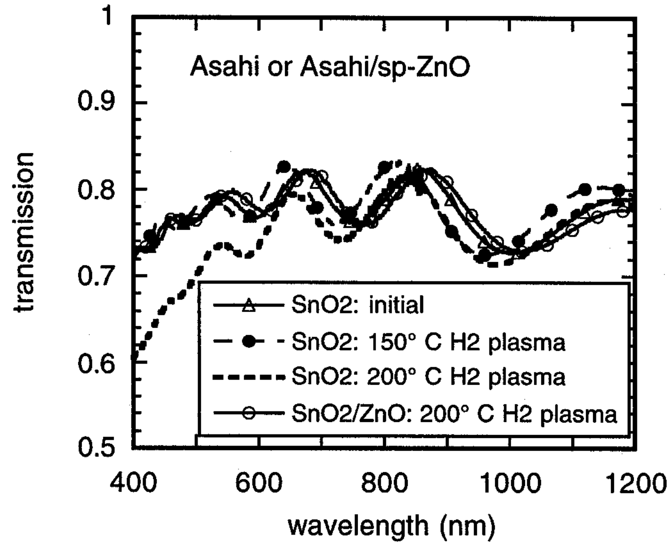


Figure 3.6 Transmission of as-received Asahi SnO_2 films, and after H_2 plasma treatments at 150 or 200˚C, and of Asahi SnO_2 coated with 20 nm ZnO after H_2 plasma treatments at 200˚C.

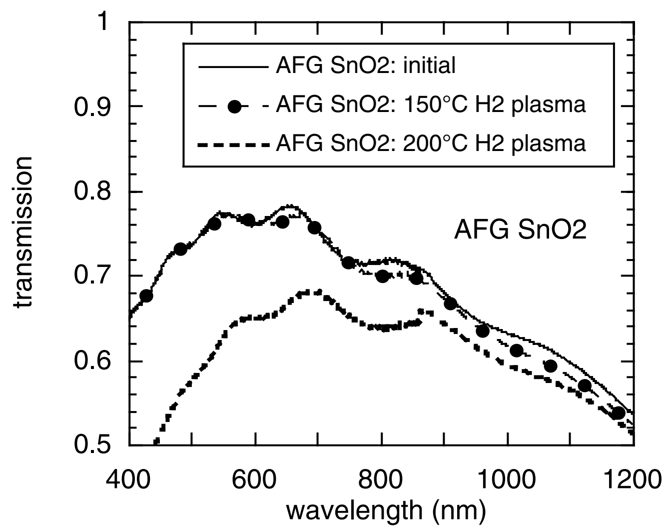


Figure 3.7 Transmission of as-received AFG SnO_2 films, and after H_2 plasma treatments at 150 or 200˚C.

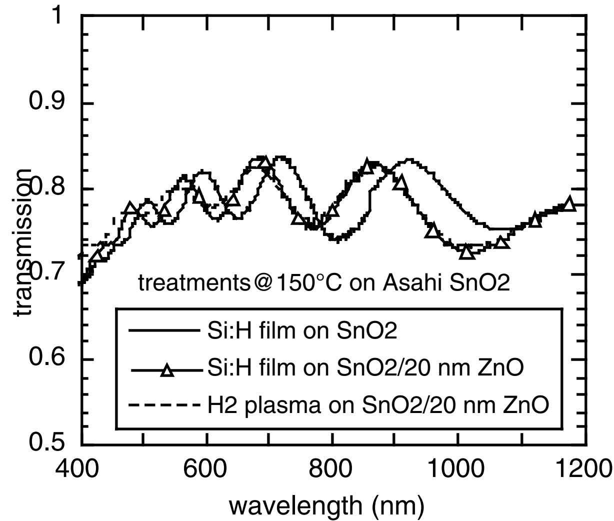


Figure 3.8 Transmission of Asahi SnO_2 treated at 150˚C, either Si:H deposition or H_2 plasma.

The effect of H_2 plasma substrate temperature or Si film growth on SnO_2 sheet resistance, mobility and carrier concentration are shown in Figure 3.9, Figure 3.10, and Figure 3.11, respectively. The sheet resistance, mobility and carrier concentration of the AFG SnO_2 is essentially unaffected by the treatments. In contrast, the Asahi SnO_2 improves. Figure 3.9 shows that R_{sh} for Asahi SnO_2 decreases from a nominal value of 12-13 down to 8-10 Ohms/sq with H_2 plasma treatments. The decrease in R_{sh} occurs similarly for Asahi films with or without the protective ZnO layer. Figure 3.10 shows that the Hall effect mobility increases with increasing substrate temperature during the plasma treatments, nearly doubling from 30-32 to 57-62 cm^2/V-sec with or without ZnO layer. This is a substantial increase. Similar increases in mobility following H_2 plasma treatments at similar temperatures were reported by Asahi and attributed to a reduction in grain boundary barrier height. Figure 3.11 shows that the carrier density is unaffected by the treatments for all samples. Also note that the AFG SnO_2 has twice the carrier density as the Asahi, consistent with its much lower transmission beyond 1000 nm (Figure 3.8 and Figure 3.9) resulting from higher free carrier absorption losses.

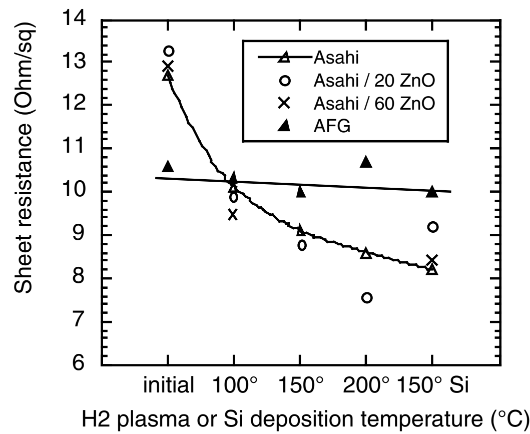


Figure 3.9 Sheet resistance of Asahi and AFG SnO_2: initial; after H_2 plasma exposure at 100, 150, and 200˚C; and after μc-Si film deposition at 150˚C. The lines are to guide the eye.

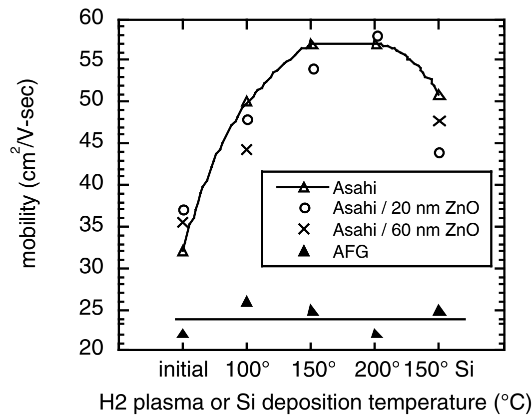


Figure 3.10 Mobility from Hall effect measurements of Asahi and AFG: initial; after H_2 plasma exposure at 100, 150, and 200˚C; and after μc-Si film deposition at 150˚C. The lines are to guide the eye.

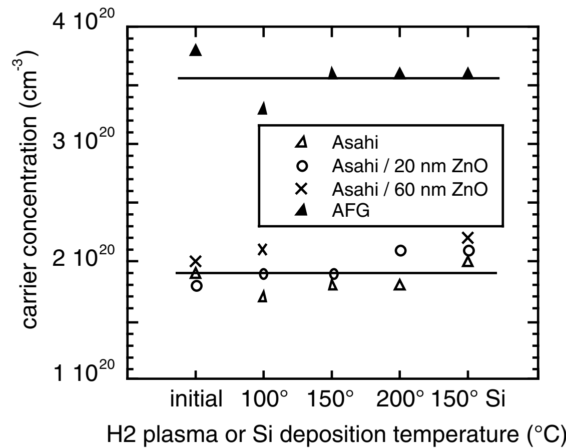


Figure 3.11 Carrier concentration from Hall effect measurements of Asahi and AFG: initial; after H_2 plasma exposure at 100, 150, and 200˚C; and after μc-Si film deposition at 150˚C. The lines are to guide the eye.

In summary, these results demonstrate that the 20 nm of ZnO is sufficient to protect the SnO_2 from plasma-induced damage resulting from either a H_2 plasma or μc-Si deposition, while at the same time allowing the beneficial improvement in bulk SnO_2 mobility. Degradation of transmission to bare SnO_2 films begins to occur for plasma exposure between 150 and 200°C, which is in the range of μc-Si film deposition for solar cells. Techniques such as this, which decrease SnO_2 R_{sh} by increasing the mobility, are preferable to those that increase carrier density, such as doping, since the gain in electrical properties is achieved without a loss in transmission due to free carrier absorption. Compared to Asahi SnO_2, the AFG SnO_2 has greater optical losses and shows no improvement in electrical properties upon exposure to H_2 plasma or μc-Si film deposition. These two commercially available brands of SnO_2 have very different sensitivity to H_2 plasmas.

3.3 Hot-wire Deposited Si Films

During this reporting period an experimental study was carried out to understand the relationship between hot wire chemical vapor deposition (HWCVD) processing parameters and deposited thin Si film properties. Thin silicon films were deposited from pure silane onto 1 in^2 7059 corning glass and single-crystal (100) silicon substrates. The native oxide was not removed from the silicon substrates. The choice of pure silane as opposed to diluted silane in hydrogen was made to simplify the reaction system and provide a basic framework from which more complicated systems can be understood. The depositions were carried out in a multi-wire HWCVD reactor which allows uniform deposition over a 6x6 $in.^2$ area. The wire material was high purity Ta and its temperature was monitored with a dual-wavelength pyrometer focused onto the wire through a viewport. A quadrupole mass spectrometer with a resolution of 1 amu and a range of 1-512 amu was used to measure the concentration of the gas phase species during deposition. This unit also featured a variable ionization potential which allowed the detection of individual radical species relative to their parent molecule. The depositions were performed at wire temperatures between 1500 to 1900°C and reactor pressures between 25 and 700 mTorr. Independent heating of the substrates allowed the substrate temperature to be varied from 200 to 500°C. The silane conversion, i.e., the silane utilization efficiency, was calculated from the known inlet silane pressure and the outlet silane pressure measured by the mass spectrometer. The film growth rate was obtained both by measuring the film thickness and the weight gain on the substrates. The silicon film crystalline fraction was determined from Raman spectroscopy. Measured spectra were deconvoluted into the characteristic crystalline (520 cm^{-1}) and amorphous (480 cm^{-1}) peaks and the ratio of their areas used to compute the ratio of crystalline to amorphous silicon [25,26]. The films were also characterized by XRD, to determine the grain size and preferred orientation.

For both substrates used, the Si films had grain sizes between 10 to 50 nm and displayed a (220) preferred orientation. The crystalline fraction varied from 0 to 89 percent depending on the process conditions. As reported by Dusane et al. [27], these results demonstrate that crystalline films can be deposited from silane without hydrogen dilution. At the wire temperatures used, the conversion of silane as measured by the mass spectrometer was approximately constant, ranging from 90 to 99 percent.

Film deposition in HWCVD proceeds through a series of reactions which occur simultaneously in the gas phase and at the wire and substrate surface. Understanding how this system of reactions is affected by process parameters is a prerequisite to determining the relationship between process conditions and film properties. Table 3.4 lists a proposed set of reactions leading to Si film formation [28,29]. Because of the high sticking probabilities of all the silane radicals, it is expected that all silane radical species, under the given reaction conditions, contribute to film deposition. The role of particular species in the formation of crystalline films is still unclear. While it has been accepted that SiH_3, having the lowest sticking probability [30], may promote ordered or crystalline films, there is also evidence of atomic hydrogen as the agent of crystalline film formation [31,32]. It is also possible that the factor determining crystalline fraction is not a single species, but the ratio of silane radicals to the atomic hydrogen flux to the growing film surface. The difficulty in separating these effects is clearly demonstrated by the second reaction in Table 3.4, where atomic hydrogen provides the major pathway for SiH_3 production, thus convoluting the role of either species.

With the exception SiH_4 flow rate and concentration (reactor pressure), the growth rate was found to be insensitive to other processing parameters. The growth rate was also insensitive to substrate choice. Figure 3.12 illustrates the effect of silane flowrate at two silane concentrations. The increase in growth rate with silane flowrate is the result of larger amounts of silane reacting to form larger amounts of radical precursors. As the pressure increases, the concentration of all radical species increases resulting in a higher growth rate. At the lower concentration, the growth rate becomes constant at the highest flowrates. This trend is attributed to a significant decrease in the residence time which leads to a decrease in the silane conversion. At higher pressures, this effect is balanced by the increase in concentration.

Table 3.4 Reaction system in the deposition of Si films from silane.

Silane cracking: $SiH_{4(g)} \rightarrow Si_{(g)} + 4H_{(g)}$
Hydrogen abstraction: $SiH_{4(g)} + H_{(g)} \rightarrow SiH_{3(g)} + H_{2(g)}$
Disproportionation: $2SiH_{3(g)} \rightarrow SiH_{2(g)} + SiH_{4(g)}$
Polymerization: $SiH_{2(g)} + SiuH_{4(g)} \rightarrow$ higher silanes
Film deposition: $SiH_{x(g)} \rightarrow$ film + $(x/2)H_{2(g)}$

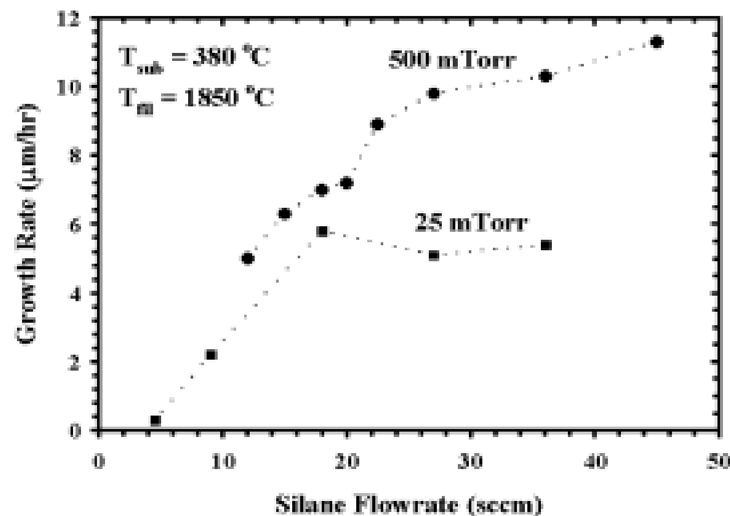


Figure 3.12 Effect of silane flowrate on the growth rate.

The crystalline fraction of the films was found to increase with increasing filament temperature, substrate temperature, and pressure, and also with decreasing total flow rate. The effect of wire temperature is shown in Figure 3.13. High crystalline fractions can be attained if the wire temperature is above a critical value, in this case 1800°C. The increase in crystalline fraction with wire temperature is related to the increase in atomic hydrogen concentration which results from the cracking of silane. Whether the atomic hydrogen effect is direct or indirect, through the production of SiH_3, is not yet known.

The effect of flowrate and pressure can be explained by means of a single parameter, namely the residence time. The residence time is a reactor independent parameter which represents the average time gas phase species spend in the reactor. It is proportional to the ratio of the silane pressure to the silane flowrate. In Figure 3.14, the effect of residence time on the crystalline fraction is shown. The growth rate was also included for comparison. It is clear that increasing the residence time by varying the silane flowrate or pressure leads to an increase in crystallinity. Because of their non-linear nature, the reactions in Table 3.4, while occurring simultaneously, are also affected serially by changes in residence time. As a result, the steady-state concentration of each product of reaction also varies with the residence time. This gives rise to the possibility that a given species (atomic hydrogen or SiH_3) is favored at high residence times and leads to high crystalline fractions.

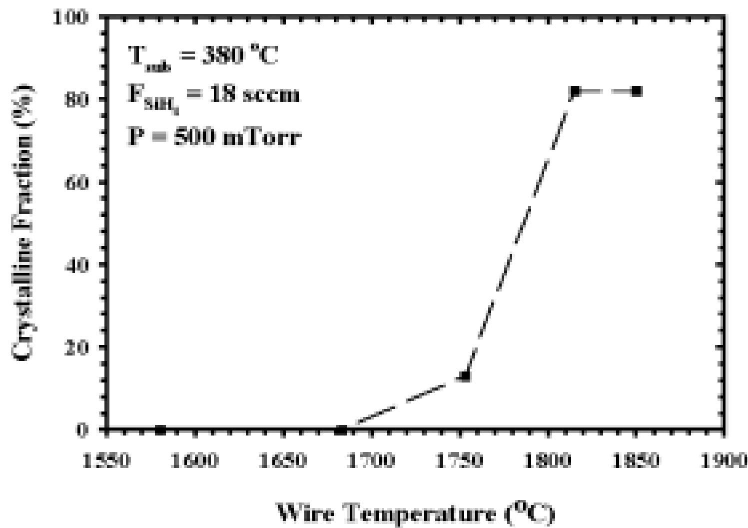


Figure 3.13 Effect of wire temperature on the crystalline fraction.

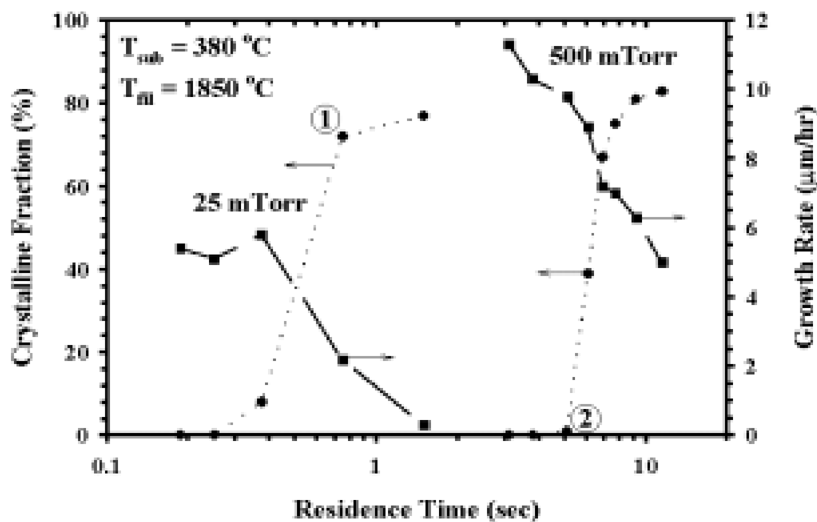


Figure 3.14 Effect of residence time on the crystalline fraction.

Figure 3.15 shows the dependence of crystalline fraction on the substrate temperature at two different conditions of residence time and concentration labeled 1 and 2 in Figure 3.14. These conditions were selected purposely to have starting points of high and low crystallinity, respectively. The effect of substrate temperature on the crystallinity is related to the mobility of the various species adsorbing onto the substrate surface and is independent of gas phase effects relating a given radical to high crystalline fractions. Therefore, the crystalline fraction is determined by gas phase effects relating the gas phase radical distribution to the wire temperature and residence time and by surface effects relating the mobility of adsorbates to the substrate temperature. By carefully selecting processing parameters, it is possible to isolate these effects. In the case of condition 1, for instance, gas phase conditions yield crystalline films irrespective of the substrate temperature. On the other hand, condition 2 illustrates a case where, gas phase conditions do not favor high crystallinity. Consequently, the crystallinity of the films can be improved by increasing the substrate temperature and thus the mobility of surface species.

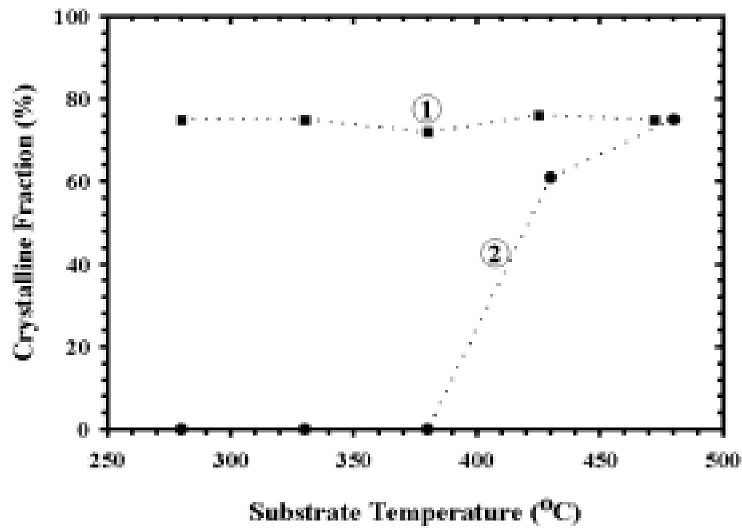


Figure 3.15 Effect of substrate temperature on the crystalline fraction.

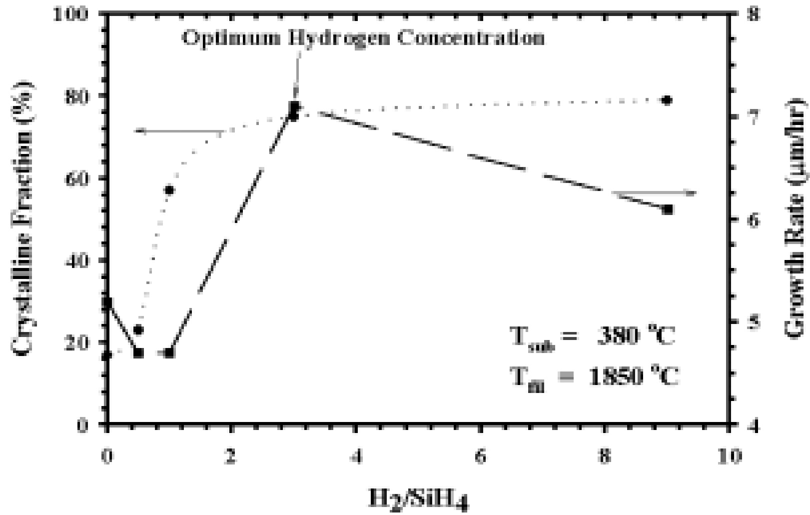


Figure 3.16 Effect of hydrogen dilution on the crystalline fraction.

Figure 3.16 shows the effect of hydrogen dilution. Previously, several studies have concluded that high hydrogen dilution is essential in the deposition of crystalline Si films [31,32]. This conclusion stems from the argument that higher hydrogen dilution leads to higher atomic hydrogen production at the wire. However, if atomic hydrogen is the desired end product, silane itself is a more prolific source of this species. It is evident from Figure 3.16 that the film crystallinity improves with increasing hydrogen content. However, crystalline fractions equivalent to those observed at the highest hydrogen dilution can also be obtained without hydrogen by carefully choosing the other processing parameters. Moreover, Figure 3.16 indicates that there is penalty in terms of growth rate when the hydrogen dilution exceeds a critical value. Nevertheless, hydrogen addition is still valuable in cases where high growth rates are desired and high crystalline fractions can not be delivered by pure silane (Figure 3.14). In such cases, there is a hydrogen to silane ratio (as in Figure 3.16) which optimizes the crystalline fraction and growth rate.

4. CdTe-BASED SOLAR CELLS

4.1 Background and Approach

In this report, the critical issues for processing superstrate CdTe/CdS devices with ultra-thin CdS are addressed. Fabricating high efficiency CdTe/CdS *superstrate* devices when using ultra-thin CdS window layers presents a difficult technical challenge because of the coupled nature of the processing steps and of the interaction between CdS and CdTe films. Detailed optical analysis of CdS/CdTe thin-film cells show that the CdS layer is inactive for photocurrent generations and thus constitutes a parasitic optical loss element in the device. Simply reducing CdS thickness to reduce parasitic absorption does not lead to the expected increase in performance, since the junction quality is found to progressively deteriorate as final CdS thickness in the device is reduced [33]. Cells having final CdS thickness greater than ~100 nm, are tolerant to film deposition and post-deposition processing and can readily yield small area conversion efficiencies in the 10 to 12% range. Cells having less than this final CdS thickness exhibit a fall-off in junction quality, measured as a loss in V_{oc} and FF. The extent of this phenomenon is: 1) process specific; 2) more serious for processes in which the CdTe layer is deposited at temperatures below 400˚C; and 3) related to consumption of the CdS layer, resulting in non-uniform or CdS-free junction area, with formation of junctions between the $CdTe_{(1-x)}S_x$ absorber layer and the transparent conductive oxide (TCO). In addition, reducing CdS thickness exposes the TCO/glass materials to interaction with the chemical treatment ambient, which can result in loss of adhesion or contamination.

Without resorting to a *substrate* device configuration, and treating the CdS layer as only a parasitic optical element, various approaches have been developed to minimize the combined effects of non-uniform, ultra-thin CdS, relying on control of CdS diffusion into the absorber layer and on improving the $CdTe_{(1-x)}S_x$/TCO junction quality.

CdS diffusion into CdTe occurs in the presence of $CdCl_2$ and O_2 via bulk and grain boundary diffusion and is dominated by the grain boundary diffusion. In the absence of $CdCl_2$ and O_2 species, the grain boundary diffusion is several orders of magnitude lower. Thus, CdTe films can be vapor-deposited on ultra-thin CdS films at high temperature, from 500 to 600˚C, with negligible inter-diffusion, yielding CdTe films with low concentration of crystallographic defects and grain boundaries. Such a film structure is more resistant to the diffusive effects of the $CdCl_2$:O_2 treatment. However, for CdTe films deposited at lower temperatures, <500˚C, the diffusion-resistant property of high-temperature deposited films can be attained by using a brief annealing step to reduce crystallographic defects [34] and by utilizing $CdTe_{(1-x)}S_x$ absorber layers with S content near the solubility for the post-deposition processing temperature [35,36,37]. Further, incorporating S uniformly into the CdTe lattice at concentrations below the solubility limit does not have a deleterious effect on the junction quality [38]. Finally, improving the $CdTe_{(1-x)}S_x$/TCO junction quality for CdTe devices with ultra-thin CdS has been facilitated by use of a high resistance layer between the TCO and CdS films [33].

The $CdCl_2$ treatment used to optimize the properties of the CdS and CdTe films for solar cell operation chemically modifies the CdTe surface. For wet $CdCl_2$ processes, the surface contains substantial quantities of chlorides, chlorates, and oxides, while vapor $CdCl_2$ processes leave very

thin oxide layers with surface chlorine concentration less than 0.1%. Prior to forming a low resistance contact to CdTe, the surface must be modified to remove oxides and residues and produce a Te-enriched layer. Nearly all contacting schemes follow this step with application of a copper-containing contact or copper layer and a heat treatment. The degree of post-deposition processing needed to attain the desired conductivity depends in part on the technique used to form the CdTe layer, but all cell making processes rely on formation of a p+ layer on the CdTe surface to form the primary contact to CdTe. Typically, Cu, excess Te, or a combination of these and other materials are used to facilitate contact formation. Analysis of the resulting surface reveals that low resistance contact operation is facilitated by formation of a very thin Cu_2Te layer between CdTe and the current-carrying material. Electrical analysis suggests that the contact can be represented as a leaky diode in series with the primary CdS/CdTe junction. The resulting CdTe contact can exhibit various degrees of leaky diode "blocking" behavior under different conditions: 1) at room temperature if insufficient Cu is used; 2) at lower temperatures; and 3) after stressing devices at V_{OC} and T ~ 100C. In stress-degraded devices, removing the current-carrying contact, re-etching the surface, and re-applying a contact removes the leaky diode "blocking" behavior. Thus, this behavior can be attributed to the CdTe/contact interface. To gain additional information about the nature of the CdTe contact surface, glancing incidence x–ray diffraction measurements were made at each processing stage.

It has been well established in recent years that some CdTe devices and modules often degrade when exposed to elevated temperatures (60-100°C) under illumination. Changes to cell performance include loss in V_{oc}, due to an increase in diode recombination current J_o, and decrease in FF, due to an increase in series resistance and/or formation of current limiting blocking contact. While the 60°C conditions might represent module exposure in the field, the higher temperatures are commonly used for life-testing by accelerating the appearance of any failure mechanisms. This shortens the testing interval to realistic periods of days or weeks instead of years. Several groups have reported that the degree of degradation in CdTe devices depends strongly on the electrical bias during stressing. Meyers and Phillips [39] found that stressing in reverse bias causes greater degradation than stressing at forward bias, and each bias ($V<0$ or $V>V_{oc}$) had a unique degradation mode. The group at Solar Cells Inc (SCI), now First Solar (FS), reported [40] that devices stressed under resistive load near maximum power degraded less than those at V_{oc} or J_{sc}, that encapsulated modules were more stable than unencapsulated ones, and that stressing at reverse bias in the dark at 100°C was the most strenuous stress condition. The largest degradation they reported for stressing at V_{oc} was 4% (relative) after 1000 hours. Hiltner and Sites [41] also reported devices stressed at J_{sc} or V_{mp} were more stable (about 10% degradation in efficiency) than those stressed at V_{oc} or reverse bias (50% and 20% degradation, respectively). They also found that devices stressed in the dark at the same bias as V_{oc} degraded less than those stressed in the light at V_{oc}, and that cells stressed at V_{oc} without Cu layers in their back contact were very stable, although with poorer performance. Analysis of the temperature dependence of the efficiency changes indicated an activation energy of about 1 eV. They also showed significant differences in bias dependence for different proprietary SCI contact processes. The group at Colorado School of Mines [42] stressed devices in air and vacuum at 100°C with different bias conditions. They found that devices stressed in air degraded more than did those in vacuum. They identified the possible effect of bias polarity on Cu electromigration. In our past reports [43], we have shown that there are at least two different degradation mechanisms, one affecting the junction (reducing V_{oc}) and one affecting the back contact (reducing FF and creating a blocking contact). More recently, IEC demonstrated

that removing the contact from a degraded device and re-applying the contact restored the Ohmic back contact and FF but did not improve the V_{oc}, thus separating the junction and contact degradation. We also found that devices only degraded when the completed cell structure is exposed to stress conditions. Stressing partially completed device structures, such as $CdCl_2$ treated CdS/CdTe layers without contacts, caused no change in initial performance when the contact was applied after stressing.

It is interesting to note that all four of these groups [39,40,41,42,43] studied devices in which the CdS/CdTe semiconductor layers were deposited at SCI, although there were likely to have been process changes over the 3 year period. Some groups applied their own contacts, others used devices completed at SCI with their contacts. Clearly, the bias condition, the ambient, and the contact have a critical influence on the degradation of CdS/CdTe devices. It is the goal of the IEC program to identify the degradation mechanisms in CdS/CdTe devices and to develop processing which minimizes or reduces the losses.

4.2 Window Layer Development for Superstrate CdTe Cells

4.2.1 Film Deposition and Treatment

4.2.1.1 Glass Preparation

Corning type 7059 borosilicate and Glaverbel soda-lime glasses were used as superstrates. Whereas Corning 7059 glass has served as the superstrate of research devices and has been the superstrate used in the most efficient CdTe devices, soda-lime glass is more economically suited to the needs of low cost photovoltaic modules. The optical transmission of these glasses are compared to that of quartz in Figure 4.1. For 7059, the loss in light-generated current for AM1.5 global spectrum from 300 nm to ~375 nm compared to quartz is only ~0.4 mA/cm^2. For soda-lime glass, the total absorption loss from 300 nm to 900 nm compared to quartz is slightly greater, ~ 0.6 mA/cm^2. Thus, based on glass absorption alone, the maximum light-generated current expected with a CdTe absorber is 30.6 mA/cm^2 on quartz, 30.2 mA/cm^2 on Corning 7059, and 30.0 mA/cm^2 on Glaverbel soda-lime glass.

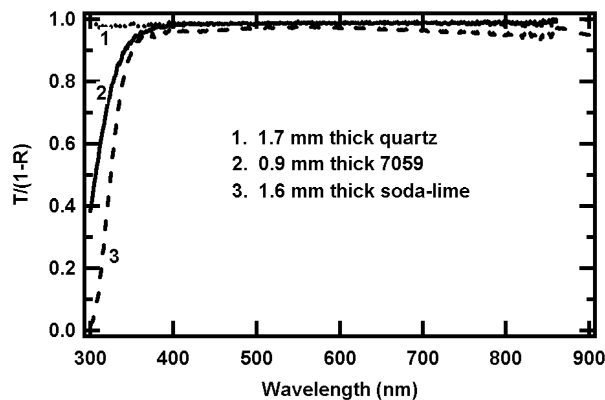


Figure 4.1 Optical transmission, normalized for reflection, of Corning 7059 and Glaverbel soda-lime glass compared to quartz.

Immediately prior to use, 1 inch square pieces of glass were mechanically cleaned with warm dilute detergent, rinsed in flowing deionized water, final-rinsed under a jet of deionized water, and dried in a stream of filtered argon.

4.2.1.2 ITO Deposition

Indium-tin oxide films, ITO, were sputter deposited onto selected cleaned glass in a CVC rf sputter deposition system. The glass samples were pumped overnight to achieve a base pressure of 1×10^{-7} Torr. Deposition of 200 nm thick ITO films is carried out on unheated substrates in flowing argon/oxygen at 5 mTorr and rf power of 700W. The as-deposited ITO films generally exhibit microcrystalline granular features less than 100 nm in diameter (Figure 4.2) and exhibit no x-ray diffraction peaks. The as-deposited sheet resistance is 20Ω/sq, and the optical transmission is poor in the ultraviolet as shown in Figure 4.3. After heat treatment in 4% H_2/Ar at 550˚C for 5 minutes, the films crystallize, exhibiting grain-like features ~300 nm (Figure 4.2) and x-ray diffraction peaks that index to In_2O_3. The treatment reduces the sheet resistance to 15Ω/sq and improves the ultraviolet optical transmission (Figure 4.3).

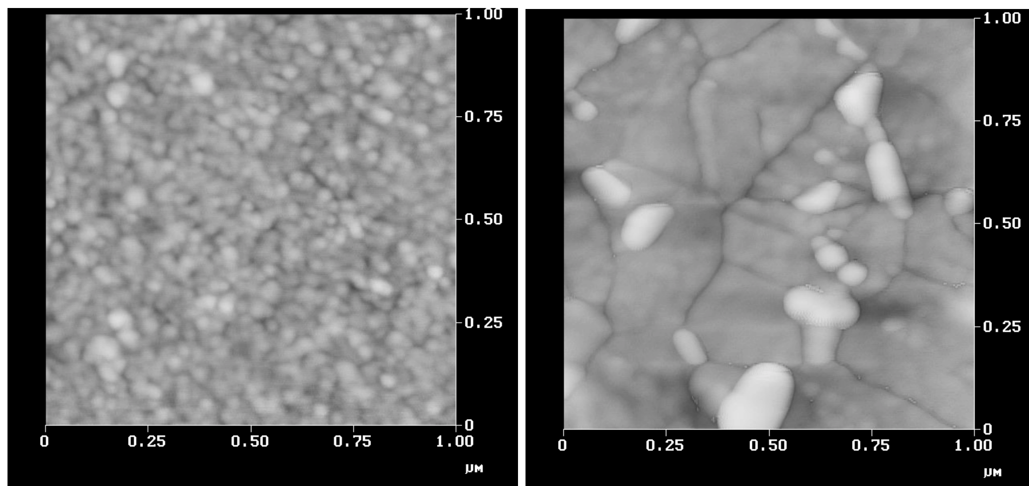


Figure 4.2 AFM images of 200 nm ITO/soda-lime glass before (left) and after (right) treatment in 4% H_2/Ar. The total grayscale range for these images is 100 nm.

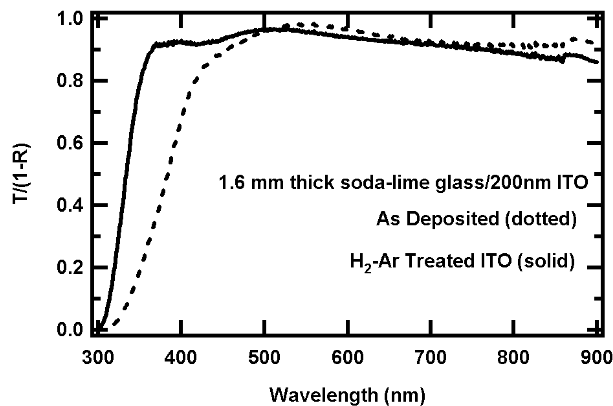


Figure 4.3 Optical transmission, normalized for reflection, of 200 nm ITO/soda-lime glass before and after treatment in 4% H_2/Ar at 550˚C for 5 minutes.

Using the transmission curves of Figure 4.3 as filters, the maximum light-generated current obtainable with 0.2 um ITO/soda-lime glass for AM1.5 global irradiation is estimated to be 27.6 mA/cm^2 for hydrogen-treated ITO and 27.0 mA/cm^2 for as-deposited ITO.

4.2.1.3 Evaporated CdS Deposition

CdS films were deposited by thermal evaporation of 6N purity CdS powder from Knudsen-type effusion cells made of boron nitride onto ITO/glass at 220˚C. The substrate temperature of the 3-by-3 sample array was controlled by a micro-thermocouple embedded in a witness superstrate. Film thickness was determined by optical absorption in the high-absorption region, from 400 to 450 nm. Pinholes in the CdS layer were by transmission optical microscopy assessed in the same way described in the previous annual report and were converted to a fractional area [44]. Table 4.1 below lists CdS effusion rate, film thickness, and fractional pinhole area for the central piece of the substrate array from ten sequential depositions targeting 80 nm film thickness. For these depositions, the same CdS charge was employed and yielded moderately constant effusion rate; variations in rate were compensated by altering the deposition time. The fractional pinhole areas measured for these samples are low enough to produce a negligible effect on open-circuit current of a device.

Table 4.1 Deposition and pinhole data for central witness piece of ten consecutive CdS depositions.

Run #	Effusion Rate (+/- 2mg/min)	Avg Thk (+/- 2 nm)	Pinhole Area Frac (E-6)
12311	20	74	-
12310	20	70	1.9
12309	16	80	4.9
12308	24	82	-
12307	20	82	2.5
12306	16	82	2.1
12305	18	80	-
12304	24	82	1.9
12303	22	80	3.0
12302	24	80	4.2
12301	20	76	2.1

The as-deposited CdS surface morphology consists of close-packed grains < 50 nm in diameter superposed on the crystallized ITO morphology (Figure 4.4). Symmetrical x-ray diffraction patterns of as-deposited films only exhibit a broad peak corresponding to the wurtzite CdS (002) reflection. After $CdCl_2$ vapor treatment at 420˚C for 20 minutes, the morphology exhibits evidence of grain coalescence to final grain size on the order of 100 nm. Diffraction patterns of the heat-treated films indicates a sharpening of the (002) reflection, which is consistent with the observed grain size increase. The optical transmission of a 60 nm thick CdS film on ITO/soda-lime glass is slightly increased near the band edge by $CdCl_2$ vapor treatment at 420˚C for 20 minutes as shown in Figure 4.5.

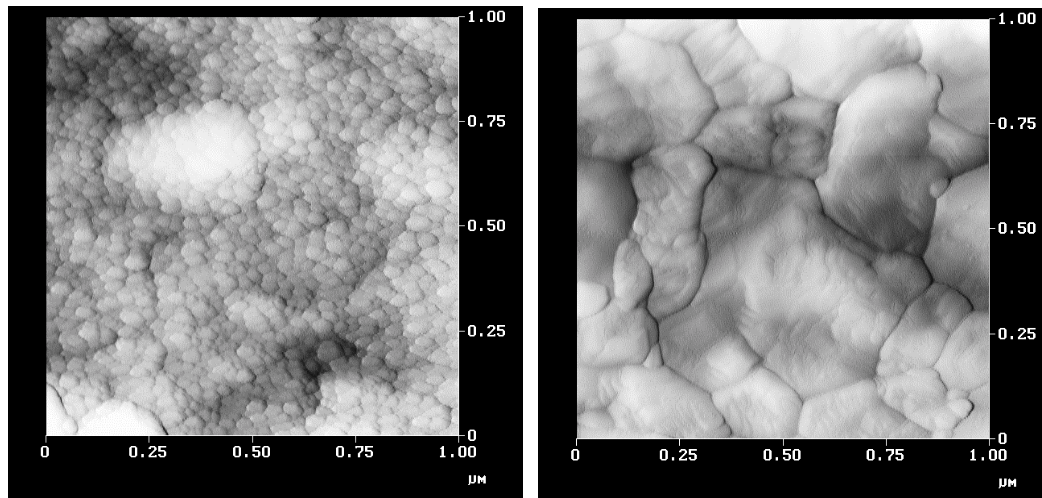


Figure 4.4 AFM images of evaporated 80 nm thick CdS before and after $CdCl_2$ vapor heat treatment. The total grayscale range for these images is 100 nm.

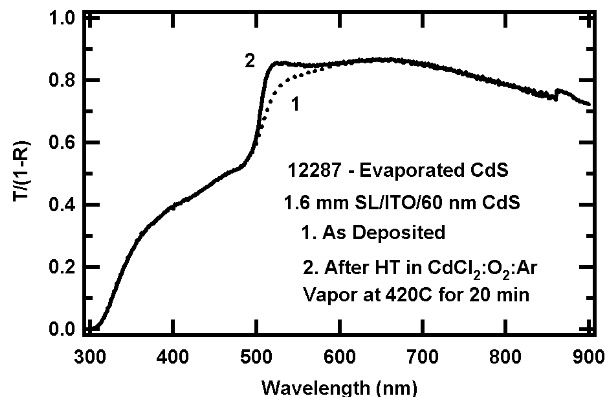


Figure 4.5 Optical transmission, normalized for reflection, of 60 nm thick evaporated CdS on ITO/soda-lime glass before and after $CdCl_2$ vapor treatment. Prior to CdS deposition, the ITO/glass was treated in 4% H_2/Ar.

In Figure 4.5, the CdS transmission after $CdCl_2$ treatment corresponds to a maximum light generated current of ~25 mA/cm^2. Consumption of CdS during post-CdTe $CdCl_2$ heat treatment increases transmission in the 350 nm to 500 nm wavelength range, yielding a possible range of light-generated current from 25 to 27 mA/cm^2 depending on the degree of CdS film loss.

4.2.1.4 Chemical Bath CdS Deposition

A new chemical bath technique for depositing ultra-thin CdS films was developed. The method yields particulate-free CdS films at ~3A/s with 99% utilization of cadmium species. A primary drawback of typical CdS chemical bath methods is the comparatively large solution volume, or bath. Generally, the bath is vigorously stirred to ensure uniform thermal and chemical mixing and to minimize adhesion of homogeneous-nucleated CdS particulates to the growing film surface. In such a scheme, the heat required to promote reaction at the TCO surface is delivered from the bath to the surface, which necessarily implies that conditions are favorable for heterogeneous CdS nucleation at the heating source and homogeneous CdS formation in the bath. If a heating jacket or water bath is used, significant CdS deposition occurs on the beaker; if an immersion heater is used, significant CdS deposition occurs on the heating element. Minimizing homogeneous-nucleated CdS particulate formation in the bath involves a delicate balance between species concentrations and heating rate. Ideally, the TCO surface itself should be the reaction heat source so that the bath serves only as a replenishment source of reaction species.

The new CdS deposition technique consists of application of metered quantities of cadmium and sulfur-containing solutions onto pre-heated TCO/glass slides. By mixing the solutions immediately prior to application, good thickness uniformity and reproducibility were obtained. For the present work, Table 4.2 summarizes the solutions and concentrations employed. Prior to deposition, superstrates were pre-heated on a hot plate at the deposition temperatures from 50˚C to 95˚C for 10 minutes.

Table 4.2 Solutions used for CdS chemical bath deposition.

Solution Name	Concentration (M)
cadmium sulfate	0.015
thiourea	0.35
ammonium hydroxide	4

Depositions were timed from the moment of solution application. No change was observed on the TCO until 1 minute, after which yellow CdS deposit was visible on the TCO/glass. After a total time of 2 minutes, no additional changes were observed. For these 2 minute depositions, the CdS film thickness obtained was 350 nm ± 50 nm, corresponding to >95% utilization of available cadmium species. Thus, for depositions longer than 2 minutes, the film thickness was found to be linearly dependent on the quantity of applied solution and independent of time and temperature over the range from 50˚C to 95˚C. The upper limit to film thickness for a single deposition was limited by the surface tension of the solution on the TCO, which determined how much solution could be applied without overflowing the sample edge. To deposit thicker films, multiple applications were employed. Figure 4.6 shows AFM images of the CdS morphology for single-coat and triple-coated CdS, corresponding to film thickness of 30 nm and 100 nm, respectively. There is a significant increase in the as-deposited grain size with the total film thickness, and $CdCl_2$ vapor treatment at 420˚C for 5 minutes clearly tightens the grain size distribution in both cases. The change in grain size with the number of applied coatings shows that the growth mechanism for this chemical bath technique is by heterogeneous nucleation at the surface, not by agglomeration of homogeneously nucleated particles. As with evaporated CdS films, the $CdCl_2$ vapor treatment improves the transmission of the CdS film, as shown in Figure 4.7.

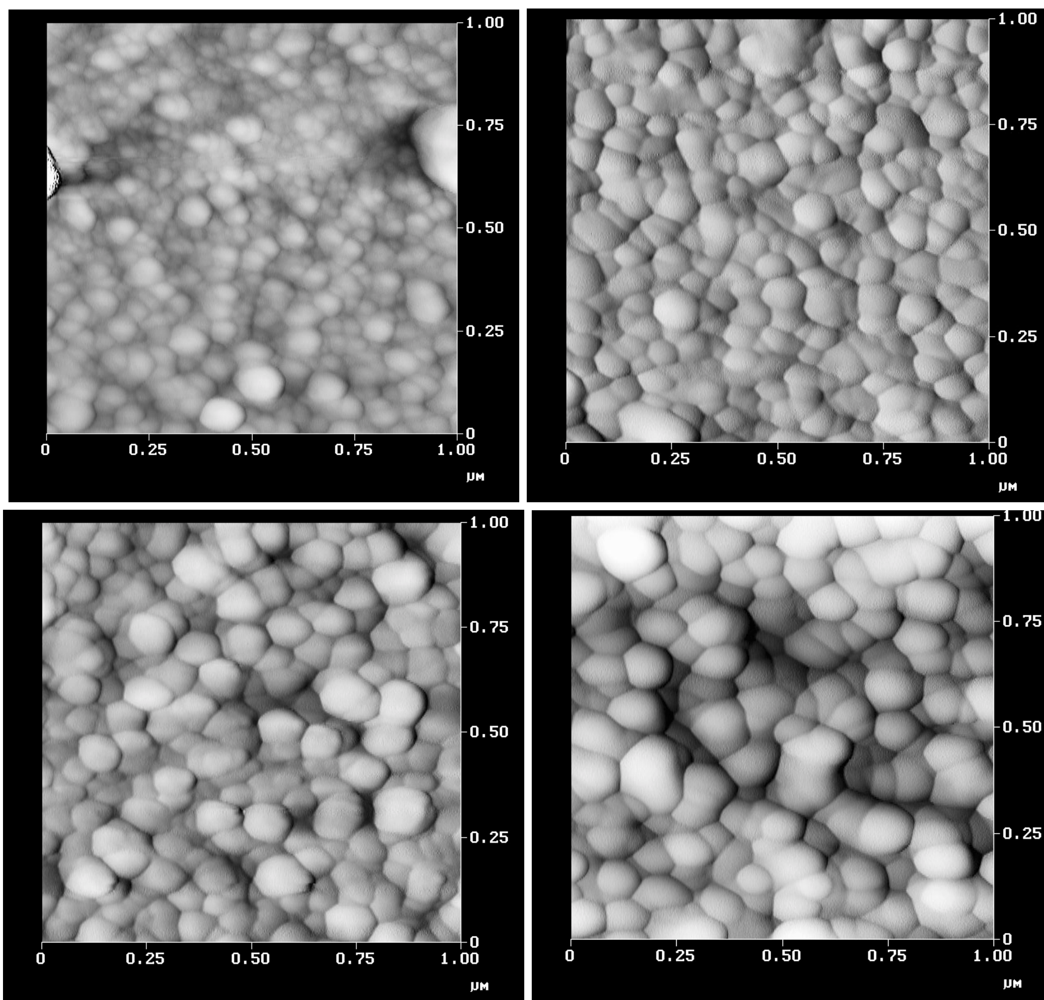


Figure 4.6 AFM images of CBD CdS before (left) and after (right) $CdCl_2$ vapor heat treatment for 30 nm (top) and 100 nm (bottom) film thickness. The total grayscale range for these images is 100 nm.

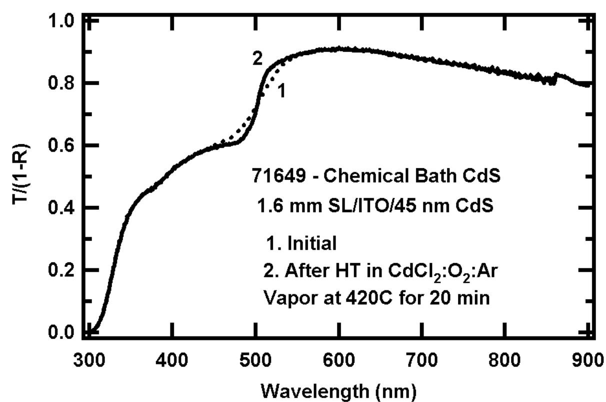


Figure 4.7 Optical transmission, normalized for reflection, of chemical bath deposited 45 nm thick CdS on ITO/soda-lime glass. Prior to CdS deposition, the ITO/glass was treated in 4% H_2/Ar.

4.2.1.5 Evaporated CdTe Deposition and $CdCl_2$ Vapor Treatment

CdTe films were deposited by thermal evaporation of 6N purity CdTe lumps 0.1 to 1 mm diameter from Knudsen-type effusion cells made of boron nitride onto CdS/ITO/glass. The substrate temperature of the 3-by-3 sample array was controlled by a micro-thermocouple embedded in a witness superstrate. Film thickness was determined by mass gain of the superstrates and was verified in selected cases by stylus step profilometry.

$CdCl_2$:O_2:Ar vapor treatments were performed by heating CdTe/CdS/ITO structures in a vapor mixture generated from a powder $CdCl_2$ source and flowing oxygen and argon. Samples were heated in a quartz reactor fitted with graphite susceptors heated externally by FCM quartz lamps in linear housings. The $CdCl_2$ source powder was evenly distributed in graphite susceptor supported on a quartz frame with a milled central cavity. A mica mask was used as both a separator and radiative/thermal insulator between the source susceptor and the thin film sample. Treatments were carried out at 1 atmosphere in a flowing mixture of oxygen and argon, at relative flow rates of 20:80. Temperature transients were characterized using a CdTe/CdS/ITO/glass sample with an embedded micro-thermocouple; the time needed to heat the sample to ~400˚C was measured to be 40 seconds. The time to heat the $CdCl_2$ susceptor to ~400˚C was measured to be 20 seconds. Thus, the heat-up rate of the susceptors, not the characteristic diffusion times for $CdCl_2$ vapor (~2 sec), controls the time to reach equilibrium conditions in the reaction zone.

Treatment in $CdCl_2$:O_2 vapor promotes numerous changes in the evaporated CdTe/CdS materials:

- inter-diffusion of CdS and CdTe;
- relaxes strain in CdTe film;
- increases grain size;
- decreases CdTe film texture;
- increases CdTe film conductivity;
- increases effective carrier lifetime in CdTe.

With respect to grain size, the action of the treatment has been inferred from SEM photographs of randomly sampled regions of CdTe samples. Now, using AFM, the grains in a *fixed* region of a CdTe film have been measured for time-progressive treatments in the short time domain and show that the large features seen after 20 minutes are the result of coalescence of adjacent small grains. Figure 4.8 shows AFM images for a CdTe film on CdS/ITO/soda-lime glass deposited at 300˚C and heat treated in $CdCl_2$:O_2:Ar vapor at 400˚C for 30 seconds and then again for 1 minute. Between the as-deposited case and the 30-second treatment, dominant grains are retained, and smaller grains coalesce to form new grains. In the next minute of treatment, this process continues, and some of the original, as-deposited, grain boundary lines persist as boundaries of singular grains. This data shows that the early phase of the treatment is very dynamical, as has been asserted in previous reports [45]. In the next paragraph we examine the extent of recrystallization and grain growth as a function of the CdTe film deposition temperature. In Section 4.2.2 we will propose a chemical pathway for this process that brings

together the chemical activity of species and the surface nature of the grain boundary mobility and diffusion processes.

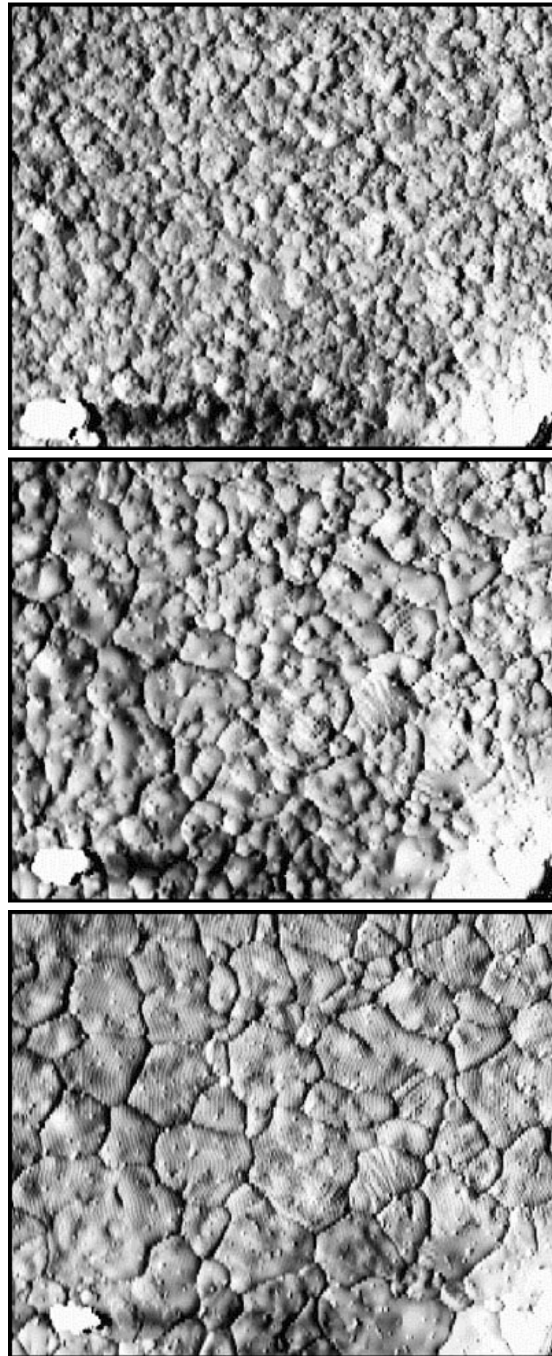


Figure 4.8 AFM images of the same area on a CdTe film surface: as deposited (top); HT for 30 sec (middle); and HT for additional 1 min (bottom). The width of each frame is 15 microns and the grayscale was 200 nm. SEM/EDS of this region showed that the particle in the lower left of each image is a CdTe spit, which is decreasing in size during each treatment.

In the previous annual report, CdS-CdTe inter-diffusion measurements by both x-ray diffraction and comparison of starting to final CdS film thickness showed that the extent of CdS film consumption during post-deposition $CdCl_2$ treatment is least for CdTe films with the largest possible grain size and fewest crystallographic defects [46]. For a given CdTe film, the other parameters of the treatment, such as $CdCl_2$ partial pressure, oxygen partial pressure and reaction temperature determine the extent of CdS diffusion. This is discussed below in Section 4.2.3. For a given set of treatment conditions, the CdTe film properties such as the density of defect and grain boundary diffusion paths offer an explanation for the observation that CdS consumption is greatest for the low-temperature CdTe deposition processes such as electro-deposition and evaporation.

For evaporated CdTe at a fixed incident flux, substrate temperature controls grain size and crystallographic defect density. In the present deposition system, substrate temperatures exceeding 350˚C are achievable, at a growth rate of 0.2 um/min. CdTe films deposited at elevated temperatures exhibit progressively larger as-deposited grain size, as shown in Figure 4.9 for 4 micron thick CdTe films deposited on CdS/ITO/soda-lime glass; note that CdTe depositions below 300˚C exhibit mean grain size smaller than 0.3 micron. The texture coefficient [47], p(111), before and after $CdCl_2$ treatment at 420˚C for 20 minutes is listed in Table 4.3 for CdTe films deposited on CdS at 5 different substrate temperatures.

Table 4.3 Texture coefficient and mean grain size of 4 micron thick CdTe films deposited at different substrate temperatures on CdS/ITO/soda-lime glass before and after $CdCl_2$ vapor HT at 420˚C for 20 minutes.

T_{sub} (C)	As Dep p(111)	HT TC(111)	As Dep Grain Size (um)	HT Grain Size (um)
250	5.3	1.0	0.2	1.2
275	4.5	1.5	0.2	1.3
325	3.6	1.8	0.7	1.4
340	2.5	1.6	0.9	1.8
350	2.5	1.5	1.3	2.0

After $CdCl_2$ treatment, the texture coefficients are similar for films deposited at all substrate temperatures. However, the mean grain size doubled for films deposited above 300˚C and quadrupled for films deposited below 300˚C. From Table 4.3 it can be concluded that films deposited at higher temperature undergo significantly less structural change during $CdCl_2$ vapor treatment. Although quantitative analysis of grain size distributions for these films is not completed, the AFM images of Figure 4.9 show a tendency towards a bimodal grain size distribution after $CdCl_2$ vapor heat treatment.

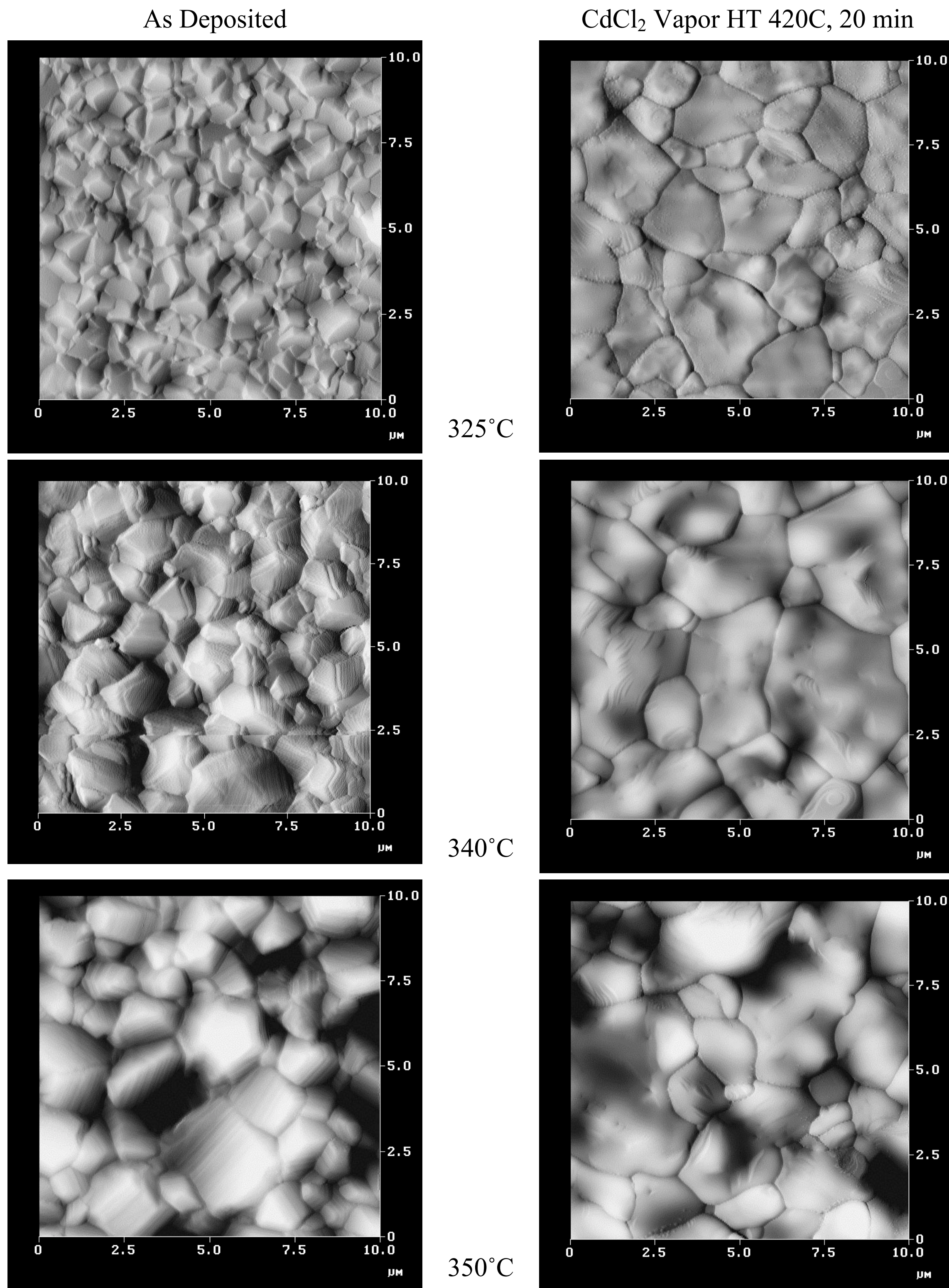
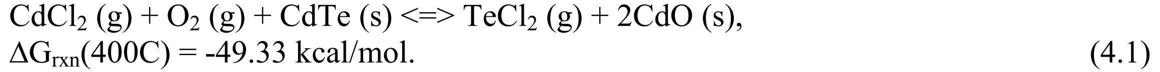


Figure 4.9 AFM images of evaporated CdTe deposited at different substrate temperatures >300˚C. Grayscale for all images is 200 nm.

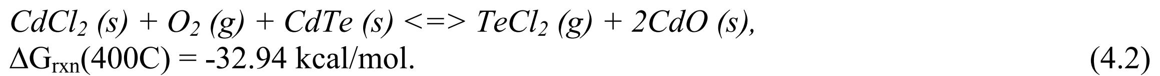
4.2.2 $CdCl_2:O_2:Ar$ Vapor Treatment Chemistry

Equilibrium estimates of free energy of reaction for possible reactions between vapor and solid species were made using data in reference [48]. For the typical isothermal vapor $CdCl_2:O_2$ treatments performed at ~400˚C, we consider the overall reaction between gas phase $CdCl_2$ and O_2 and solid CdTe:



$$CdCl_2\ (g) + O_2\ (g) + CdTe\ (s) <=> TeCl_2\ (g) + 2CdO\ (s),$$
$$\Delta G_{rxn}(400C) = -49.33\ \text{kcal/mol.} \quad (4.1)$$

For reactions where solid $CdCl_2$ is in physical contact with CdTe, we consider the solid phase reaction:



$$CdCl_2\ (s) + O_2\ (g) + CdTe\ (s) <=> TeCl_2\ (g) + 2CdO\ (s),$$
$$\Delta G_{rxn}(400C) = -32.94\ \text{kcal/mol.} \quad (4.2)$$

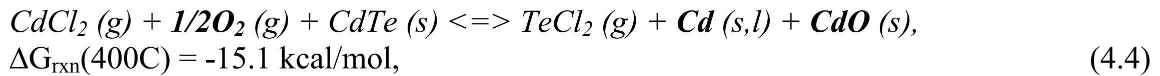
Both cases are thermodynamically favored; in the latter case, it is important to recognize the significant partial pressure of $CdCl_2$ obtained at the 400˚C reaction temperature = 10 mTorr.

This system leads to the Guldberg and Waage expression of overall equilibrium,

$$K_1 = [TeCl_2][CdO]^2/[CdCl_2][O_2][CdTe], \quad (4.3)$$

in which the quantity of CdO obtained will vary as the square root of O_2 concentration. This is pointed out because of data showing an enhancement in grain coalescence and inter-diffusion with oxygen partial pressure [49].

It is also useful to consider the intermediate reaction, which represents the balance between Cd and O_2:



$$CdCl_2\ (g) + \mathbf{1/2O_2}\ (g) + CdTe\ (s) <=> TeCl_2\ (g) + \mathbf{Cd}\ (s,l) + \mathbf{CdO}\ (s),$$
$$\Delta G_{rxn}(400C) = -15.1\ \text{kcal/mol,} \quad (4.4)$$

with equilibrium constant defined in terms of elemental Cd and molecular CdO:

$$K_2 = [TeCl_2][Cd][CdO]/[CdCl_2][O_2]^{0.5}[CdTe]. \quad (4.5)$$

This overall surface chemical basis was qualitatively and quantitatively tested by phase measurements of annealed powder samples (particle size < 150 µm) as shown in Table 4.4, Figure 4.10 and Figure 4.11. Powders were chosen to enhance diffracted x-ray signal from phases present at trace quantities. The powders were dehydrated in vacuum at 300˚C for 15 minutes prior to mixing and therewith were transferred to the heat treatment reactor, which was the same used to process CdTe/CdS thin-films.

Table 4.4 XRD phase results for closed-volume (batch) reaction of powder/gas mixtures at 400˚C for 60 minutes. The O_2 concentration was fixed at 20% by volume. Samples were quench-cooled after treatment.

System	Phases After Treatment
$CdTe + O_2 + Ar$	CdTe
$CdCl_2 + O_2 + Ar$	$CdCl_2$
$CdTe + CdCl_2 + O_2 + Ar$	CdTe, $CdCl_2$, CdO
$CdTe + CdCl_2 + Ar$	CdTe, $CdCl_2$

To minimize hydration of the $CdCl_2$ powder during the XRD measurement, the XRD pattern was acquired over a small angular range at a rate of 0.025 deg/sec. The angular range was selected to reveal the presence of major peaks of CdO, $CdCl_2$, and $CdCl_2$ hydrates . As Table 4.4 shows, CdO was detected in CdTe:$CdCl_2$ powders heated in O_2/Ar ambient at 400˚C for 1 hour. Figure 4.10 shows the XRD pattern containing the strongest CdO line (111) and a nearby $CdCl_2$ line for a CdTe:$CdCl_2$ powder treated in 20 vol% O_2 and Ar ambient at 400˚C for 1 hour. The Rachinger correction was applied to the raw data to remove Cu-kα_2 components. No $CdCl_2$ hydrate peaks were detected in any of the patterns.

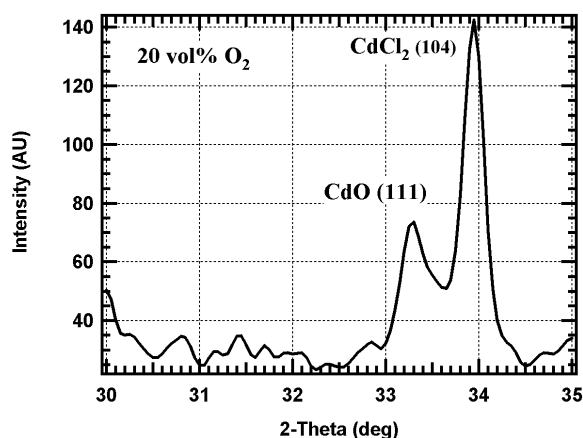


Figure 4.10 X-ray diffraction pattern of CdTe:$CdCl_2$ powder heated in 20 vol% O_2 in Ar ambient at 400˚C for 1 hour.

Figure 4.11 shows the intensity of the CdO (111) line, minus background, for powders treated at different O_2/Ar concentrations. In homogeneous powder mixtures, the intensity of a component phase is proportional to the volume fraction of that phase and inversely proportional to the mass absorption coefficient of the entire matrix, μ_m. For trace phases, μ_m varies negligibly and the intensity of the trace phase is proportional to its volume fraction. In this case, the volume fraction of CdO in the treated samples follows a square root dependence with [O_2], in accordance with Equation 4.3 above for the proposed chemical equilibrium of this system.

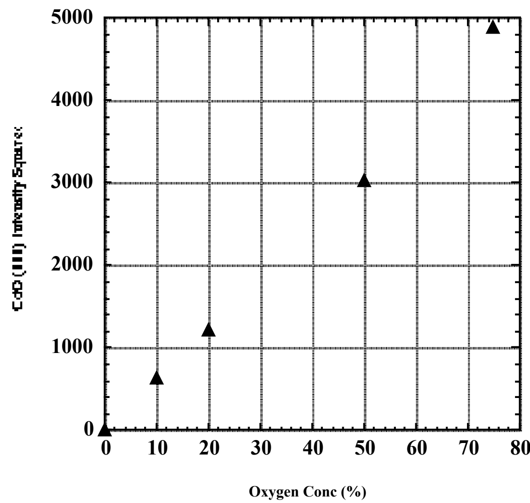


Figure 4.11 Square of intensity of the CdO (111) x-ray diffraction peak versus oxygen concentration during treatment of CdTe:$CdCl_2$ powders at 400˚C for 1 hour.

In thin-films, the grains of the film are analogous to the particulates of the powder. It is thus reasonable to assume that the quantity of CdO residue obtained on a *film* will depend on the O_2 concentration and on the quantity of $TeCl_2$ which can escape the heat treatment zone, since the CdTe and $CdCl_2$ reactants are in abundant supply. This latter condition represents a departure from equilibrium to which the system will react by generating additional products. In the limit, this process is diffusion-limited by the formation of the oxide layer. To examine the effect on film surfaces, glancing incidence x-ray diffraction was carried out on CdTe/CdS samples which were treated in $CdCl_2$:O_2:Ar vapor. The incident beam angle was 0.5º, which results in a depth penetration on the order of 100 nm. Figure 4.12 shows the GIXRD pattern of a sample treated at 420˚C for 20 minutes, revealing the presence of CdO and native oxides of CdTe.

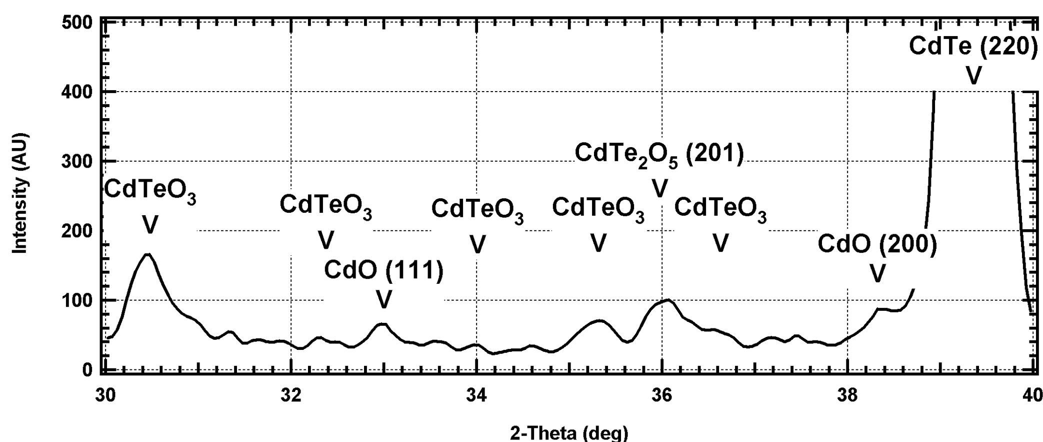
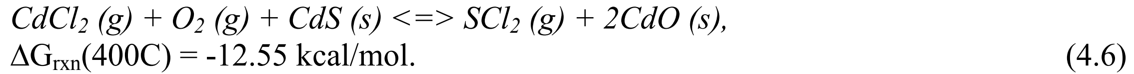


Figure 4.12 Glancing incidence x-ray diffraction pattern of CdTe surface after treatment at 420˚C for 20 minutes in $CdCl_2$:O_2:Ar vapor with $p(O_2)$ ~ 152 Torr and $p(CdCl_2)$ ~ 1×10^{-3} Torr at P_{total} = 760 Torr. The pattern was acquired at an incident beam angle of 0.5 degrees.

The presence of CdO in the films suggests the validity of the proposed chemical basis, with the additional observation of native oxide formation. Equations 4.1 and 4.4 above offer a phenomenological mechanism for grain growth and for CdTe-CdS intermixing. Given the observation that grain growth and CdTe-CdS intermixing depend strongly on O_2 and $CdCl_2$ concentration during the $CdCl_2$ treatment, and given that earlier XPS measurements of $CdCl_2$-treated films indicated Cd enrichment and the presence of CdO [50], and given that glancing-incidence XRD indicates the presence of CdO, we can postulate that the proposed chemistry of the treatment consists of conversion of the CdTe grain boundary surfaces to free Cd (liquid) and $TeCl_2$ gas, thereby increasing Cd and Te species mobility.

Similar chemistry can be shown to occur within the CdS film, resulting in highly mobile Cd, S, and Te species and a high degree of intermixing between CdS and CdTe. The disparity in rates of motion, CdS into CdTe versus CdTe into CdS, needs to be examined in detail and may be accounted for by differences in the steady state equilibria due to $CdCl_2$ and O_2 concentration profiles in the CdS and CdTe films and by the relative sizes of $TeCl_2$ molecules in the CdS matrix and SCl_2 molecules in CdTe matrix. Note that the formation of SCl_2 is favored:



$$CdCl_2\ (g) + O_2\ (g) + CdS\ (s) <=> SCl_2\ (g) + 2CdO\ (s),$$
$$\Delta G_{rxn}(400C) = -12.55 \text{ kcal/mol.} \qquad (4.6)$$

When the number of diffusion pathways are restricted by the action of high-temperature film growth or annealing, the degree of grain boundary motion and inter-diffusion are reduced. In this case, the beneficial electronic effects of the $CdCl_2$:O_2 treatment are obtained with minimal structural or chemical disturbance within the film. On the exposed surface of CdTe, however, the above chemistry always occurs, leaving a CdO-containing and Cd-enriched layer.

In summary, $CdCl_2$ and O_2 react with CdTe at grain surfaces, increasing the mobility of Cd and Te species. When the forces of grain surface motion are balanced, i.e., when equilibrium is achieved between adjacent grains, then the grain growth process ceases. The composition of the remaining grain boundaries and their surfaces then corresponds to the solid-state products of the equilibrium chemistry. The effect of $CdCl_2$ and O_2 concentrations on CdS diffusion and devices are presented in the next section.

4.2.3 CdS Diffusion into CdTe

The chemical affinity of CdS and CdTe, coupled with the isostructural nature of the CdS-CdTe system at each compositional end of the *T-x* equilibrium, lead to formation of zincblende $CdTe_{1-x}S_x$ and wurtzite $CdS_{1-y}Te_y$ alloys. In superstrate polycrystalline thin films of CdS/CdTe, in which a very thin, microcrystalline CdS film is sandwiched between an oxide film and the CdTe film, device processing conditions lead to formation of zincblende $CdTe_{1-x}S_x$ on the CdTe side and wurtzite $CdS_{1-y}Te_y$ on the CdS side. It has already been shown that thermal treatment in $CdCl_2$:O_2 ambient does not affect the miscibility limits of CdS-CdTe equilibrium but only increases the rate at which the end-points are reached [51,52]. If the CdS film is deposited at a high substrate temperature or is subjected to a thermal treatment prior to CdTe deposition, the formation of a $CdS_{1-y}Te_y$ alloy is minimized [53].

Formation of the $CdTe_{1-x}S_x$ alloy occurs during $CdCl_2:O_2:Ar$ heat treatment at the expense of the CdS film and is a critical phenomenon in structures where the starting CdS thickness is on the order of the quantity which can be consumed by the CdTe layer. Complete CdS consumption limits V_{oc} in devices by formation of parallel $CdTe_{1-x}S_x$/TCO junctions having higher J_o than $CdTe_{1-x}S_x$/CdS/TCO junctions [54]. We have identified processing methods that reduce CdS diffusion into the absorber layer, relying on a semi-quantitative understanding of the chemical and polycrystalline nature of the system. Figure 4.13 shows the sensitivity of CdS consumption, expressed as the equivalent CdS film thickness, d_{eq}(CdS), consumed as a function of time, for CdTe films deposited at 275˚C and treated at fixed $CdCl_2$ concentration. The triangles show the enhancement in CdS diffusion for fixed reaction temperature and increasing oxygen concentration. Circles show the enhancement in CdS diffusion obtained for fixed oxygen concentration and increasing reaction temperature. The hatched band shows the narrow range of CdS diffusion results obtained at 420˚C with either of two process modifications: 1) incorporation of a 600˚C treatment in argon prior to $CdCl_2:O_2:Ar$ treatment or 2) using a $CdTe_{0.95}S_{0.05}$ absorber layer in place of a pure CdTe layer.

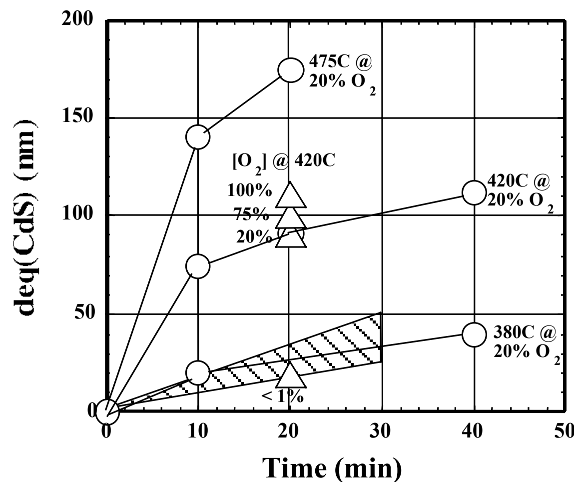


Figure 4.13 Equivalent CdS film thickness diffused into CdTe absorber layer versus $CdCl_2:O_2:Ar$ vapor treatment time at constant $CdCl_2$ concentration. Triangular points are for treatments at different O_2 concentration, in volume percent. Hatched band indicates range results for 420˚C treatment of films with either a 600˚C anneal prior to $CdCl_2$ treatment or use of a $CdTe_{0.95}S_{0.05}$ absorber layer.

Oxygen concentration in the post-deposition vapor ambient affects the final CdTe grain size, CdS diffusion, and device performance. Figure 4.13 (triangles) shows, for non-annealed CdTe/CdS films, a strong dependence of CdS diffusion for treatment at low oxygen concentration and a weak dependence for treatment at elevated oxygen concentration. Table 4.5 shows the mean CdTe grain size, equivalent CdS loss, and device data for cells with initially 180 nm CdS/4.5 µm CdTe treated at 420˚C for 20 minutes with different oxygen concentration. The CdTe was deposited at 275˚C.

Table 4.5 Mean grain size, change in CdS thickness, and device results for CdTe/CdS samples treated at different oxygen partial pressures.

$[O_2]$ (vol%)	Mean G.S. (um)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	R_{oc} (Ω-cm^2)	G_{sc} (mS/cm^2)	Eff (%)
<0.1	1.7	735	21.9	57	7	3	9.2
25	2.0	740	22.0	60	6	3	9.8
35	2.3	760	22.0	62	7	1	10.3
75	2.5	790	23.5	62	7	1	11.5

The grain size, equivalent CdS consumed, and device performance increase with oxygen concentration during treatment. The increase in efficiency is attributable to gains in current, voltage, and fill factor. The J_{sc} correlates with thinner CdS, which reduces parasitic absorption. The increases in V_{oc} and FF are not as easily explained and may be linked to oxygen doping and grain boundary passivation. At the typical oxygen concentration of 20-25% used to process cells, achieving V_{oc} > 750 mV and > 11% performance is obtained with a high temperature anneal prior to $CdCl_2$:O_2 processing. Thus, similar junction behavior may be obtained by treating at low oxygen concentration after a high temperature anneal or treating at high oxygen concentration without an anneal step. The first path offers improved control of CdS consumption when working with ultra-thin CdS layers.

A more quantitative assessment of CdS diffusion is now emerging. The chemical basis for the CdS-CdTe-$CdCl_2$-O_2 system presented above, dominated by surface oxide formation and CdS-CdTe equilibrium, was developed to reconcile thermodynamically favored reactions with measured phase compositions of bulk and surface region. A basis for the diffusive nature of the CdS-CdTe couple has now been considered in detail using a continuum model for grain boundary and bulk diffusion processes. Measured x-ray diffraction line profiles of CdS/CdTe couples in substrate and superstrate configurations were reasonably well modeled using only bulk and grain boundary diffusion coefficients as fitting parameters.

For this, CdTe/CdS diffusion couples were fabricated in the standard *superstrate* configuration and also in the *substrate* configuration using 200 nm thick CdS films and 2 µm thick CdTe films. For the *substrate* configuration, the CdTe film was deposited onto CuTe/Mo/7059 structures which resulted in uniform, micron-size CdTe grains which did not change appreciably after treatment. XRD data and model results for superstrate and substrate cases are shown in Figure 4.14. Since analysis of the *substrate* configuration case did not involve dynamical grain size considerations, i.e., the grain size remained constant throughout the treatment, the diffusion coefficients obtained are believed to be more representative: D_{bulk} (440°C) = 1 x 10^{-13} cm^2/sec and $D_{boundary}$(440˚C) = 1 x 10^{-8} cm^2/sec. Activation energies for the diffusion processes in the 380˚C to 480˚C range at fixed $CdCl_2$ and O_2 partial pressures were found to be: E_A(bulk) ≈ 2-2.5 eV and E_A (boundary) ≈ 3-3.5 eV.

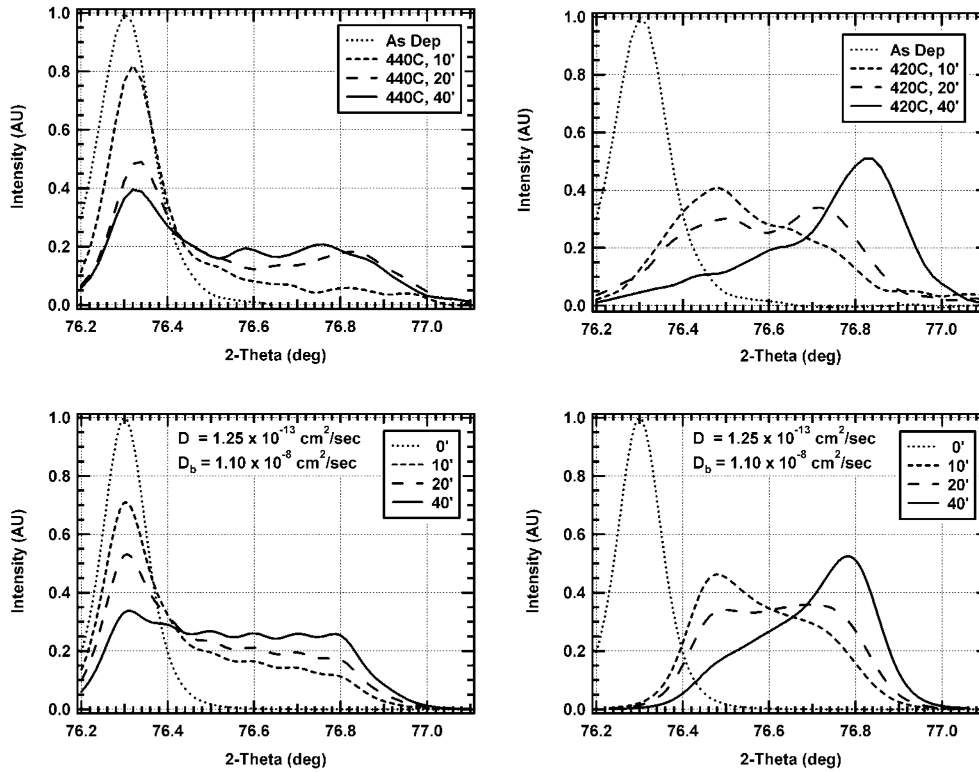


Figure 4.14 Measured (top) and modeled (bottom) x-ray diffraction (511)/(333) line profiles of CdTe/CdS couples for substrate configuration (left) and superstrate configuration (right).

Interpretation of these diffusion coefficients and activation energies with respect to chemical processes will be facilitated by repeating this analysis on samples treated with different vapor ambient compositions. The dependence of the diffusion coefficients and their activation energies on the $CdCl_2$ and O_2 concentration is thus under examination. Evaluation of the bulk diffusion coefficient is also being carried out by analysis of the diffusion of CdS films into (111)-oriented CdTe single crystals. In addition, sensitivity of the bulk diffusion coefficient to variations in crystallographic defect density are being examined by analyzing CdTe/CdS couples with evaporated CdTe films deposited at different substrate temperatures. CSS-deposited CdTe/CdS films made at First Solar, LLC and the Institute of Energy Conversion are being similarly analyzed before and after $CdCl_2$ treatment.

4.2.4 Modified TCO Structure

One problem associated with ultra-thin CdS films is penetration of the post-deposition treatment ambient to the TCO/glass materials, which can promote contamination from the glass, interfacial CdS-TCO strain, and delamination of the CdTe/CdS from the TCO surface [55,56]. With thinner CdS, the CdS-CdTe junction location approaches the contamination source, i.e., the TCO and glass. Contamination and delamination translate to poor device performance and low yield and may be related to the progressive drop in performance experienced for devices with starting CdS thickness less than about 100nm.

For physical vapor deposited CdTe/CdS devices using ITO, poor adherence after $CdCl_2$ treatment was found to be independent of the type of glass used (Glaverbel soda lime and Corning 7059) and variations in post-CdTe deposition processing, such as use of the high temperature anneal, or reduced $CdCl_2$:O_2 treatment time.

For baseline devices, with 200 nm thick CdS, optimal performance is obtained by heat treatment of the CdS/ITO/glass structure in the presence of $CdCl_2$:O_2 vapor at ~420˚C prior to the CdTe deposition. This treatment recrystallizes the CdS film, making it resistant to Te diffusion during subsequent processing of the entire device structure. The 200nm thick ITO film in these baseline devices is amorphous prior to the CdS deposition and partially crystallizes during the CdS deposition at 200-250˚C. ITO is further recrystallized during the $CdCl_2$ treatment of the CdS/ITO/glass structure. However, samples with thinner CdS films, from 30 to 100 nm thick, exhibited *no* evidence of ITO crystallization after the CdS deposition. Therefore, for samples with d(CdS) < 100 nm, the ITO is in an amorphous state when the $CdCl_2$ treatment is performed.

For CdS/ITO samples on 7059 glass, millimeter-size white spots frequently were observed to form in the structure during the $CdCl_2$ treatment, necessitating a reduction in treatment temperature and time. For samples on soda-lime glass, the spots frequently coalesced into broad translucent regions. Similar changes were found on bare 7059 and soda-lime glass, *without* an ITO layer. Microscopic and x-ray diffraction measurements of 7059 and soda-lime glass with and without ITO coating revealed that the $CdCl_2$ caused devitrification of the glass, resulting in formation of crystalline tridymite phase (7059 and soda-lime) and sodium silicates (soda-lime) as well as crystallization of the ITO film. Scanning electron micrographs revealed regions of varying morphology (Figure 4.15); EDS analysis at 10kV showed non-uniform lateral distribution of Na, In, and Si species. Figure 4.16 shows x-ray diffraction data for ITO/soda-lime glass. Finally, an increase in optical scattering and/or absorption of the glass is detected after $CdCl_2$ treatment (Figure 4.17). The devitrified phases were not detected on samples subjected to heat treatment alone, at temperatures up to 600˚C. The x-ray diffraction phases measured before and after different treatments for bare quartz, 7059 and soda-lime glass is summarized in Table 4.6.

Table 4.6 Phases detected by x-ray diffraction on three types of glass for the given treatments.

Condition	Quartz	Corning 7059	Glaverbel SL
Cleaned	Amorphous	Amorphous	Amorphous
HT 600C/Air	Amorphous	Amorphous	Amorphous
HT 600C/H_2	Amorphous	Amorphous	Amorphous
HT 420˚C/$CdCl_2$/Air	SiO_2	$BaSiO_2 + SiO_2$	$Na_2Si_2O_5 + SiO_2$

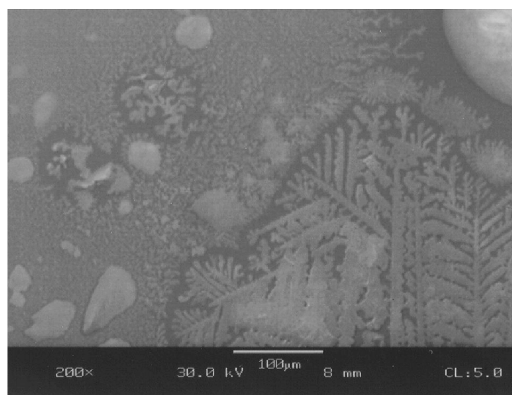


Figure 4.15 Scanning electron micrograph and EDS survey of ITO-coated soda-lime glass after $CdCl_2$:O_2:Ar vapor at 420˚C for 20 minutes.

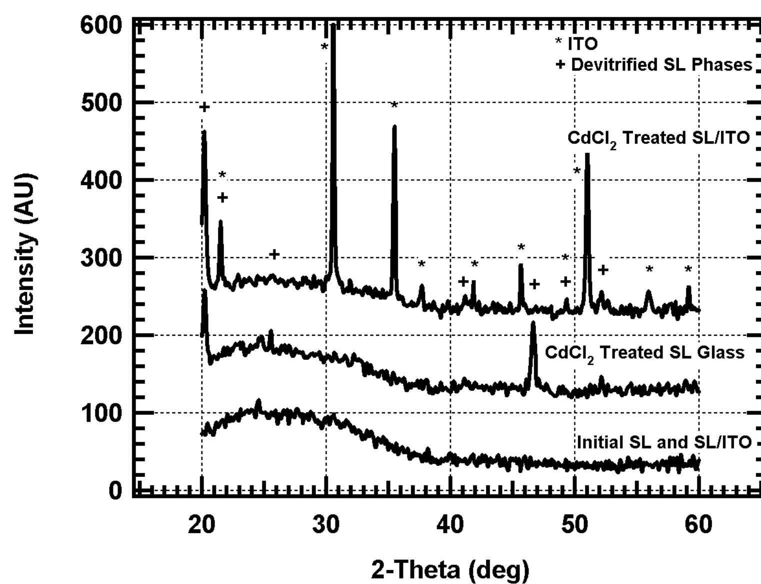


Figure 4.16 X-ray diffraction patterns of soda-lime glass (SL) and ITO-coated SL glass before and after treatment in $CdCl_2$:O_2:Ar vapor at 420˚C for 20 minutes.

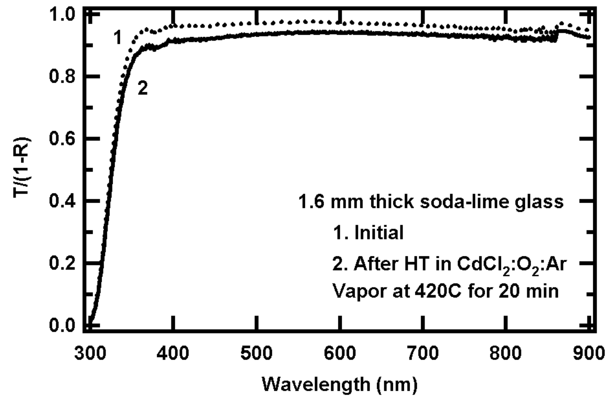


Figure 4.17 Normalized optical transmission, T/(1-R), of 1.6 nm thick Glaverbel soda-lime glass before and after heat treatment in $CdCl_2$:O_2:Ar vapor at 420˚C for 20 minutes.

Thus, amorphous ITO does not act as a barrier for the reaction and devitrification of glass in the presence of $CdCl_2$ vapor, resulting in delamination of CdS/CdTe from the ITO surface during processing. Furthermore, the sheet resistance of the ITO film in structures with d(CdS) < 100 nm was unstable with respect to the $CdCl_2$ treatment at 420˚C for 20 minutes, increasing from 25 to 150 Ω/sq after treatment. Three processing options were considered: 1) increase the ITO film thickness; 2) establish treatment conditions for ITO/glass prior to CdS deposition; or 3) rely on the CdS deposition temperature and subsequent $CdCl_2$ processing to set properties of all layers.

The first option, using thicker ITO films, was not fully explored, since the degree of crystallization would still be an issue. Also, thicker ITO layers translates to reduced optical transmission. The second option was evaluated for heat treatments in dry air, vacuum at 25 mTorr, and 4% hydrogen in argon at temperatures from 200 to 600˚C with subsequent $CdCl_2$ treatment at 420˚C for 20 minutes. Treatment in H_2/Ar at 550˚C for 5 minutes repeatedly produced crystallized ITO films with high transparency and 10 Ω/sq sheet resistance with no evidence of glass reaction or devitrification. Figure 4.18 shows the x-ray diffraction patterns of soda-lime glass with and without ITO after treatment in 4% H_2/Ar and $CdCl_2$ treatment, with only peaks attributable to ITO (In_2O_3). The integrity of the superstrate and adhesion of CdS and CdTe was good for evaporated and chemical bath-deposited CdS layers 20-80 nm thick. The third option was unsuccessful at completely eliminating adhesion problems associated with the $CdCl_2$ treatment of the CdTe/CdS/ITO/glass structure. Thus, well-crystallized ITO films produced from amorphous sputtered ITO films by brief heat treatment in H_2/Ar were found to be effective barriers for the reaction and devitrification of glass in the presence of $CdCl_2$ vapor, improving adhesion and performance.

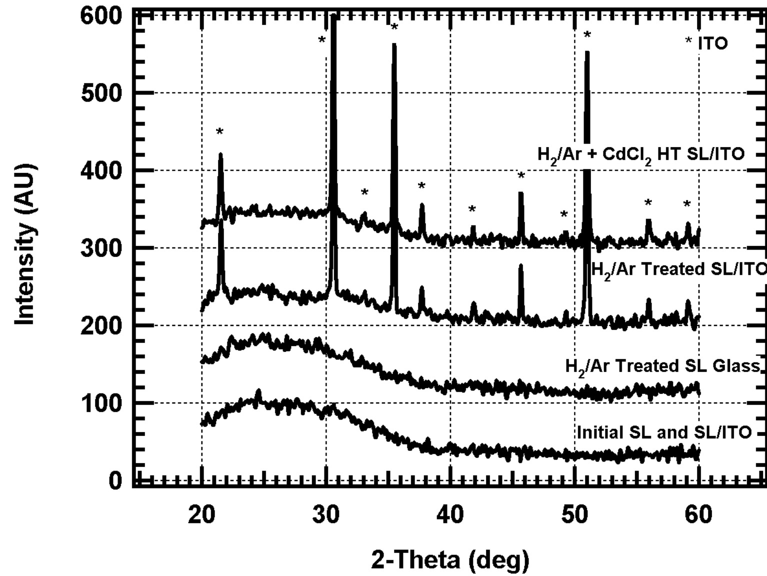


Figure 4.18 X-ray diffraction patterns of soda-lime glass (SL) and ITO-coated SL glass with heat treatment in H_2/Ar at 550˚C for 5 minutes before and after treatment in $CdCl_2$:O_2:Ar vapor at 420˚C for 20 minutes.

In evaporated CdTe/CdS solar cells, the decrease in device performance as d(CdS) is reduced has been reported elsewhere [33]. Figure 4.19 and Figure 4.20 depict this behavior for devices with different final CdS thickness using single-layer ITO/7059 and ITO/soda-lime glass. The expected gain in short circuit current is offset by a reduction in open circuit voltage. The work reported in previous sections was focused on limiting the diffusion of CdS into CdTe during treatments; the remainder of this section is focused on improving the junction characteristics when the final CdS thickness is below ~80 nm, which should yield J_{sc} values > 23 mA/cm^2.

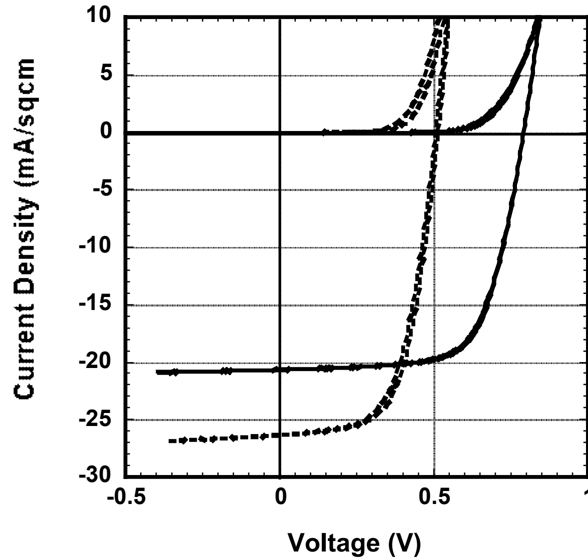


Figure 4.19 J-V curves in dark and at 100 mW/cm^2 for devices with final d(CdS) = 150 nm (solid) and 30 nm (dotted) on single-layer ITO/7059.

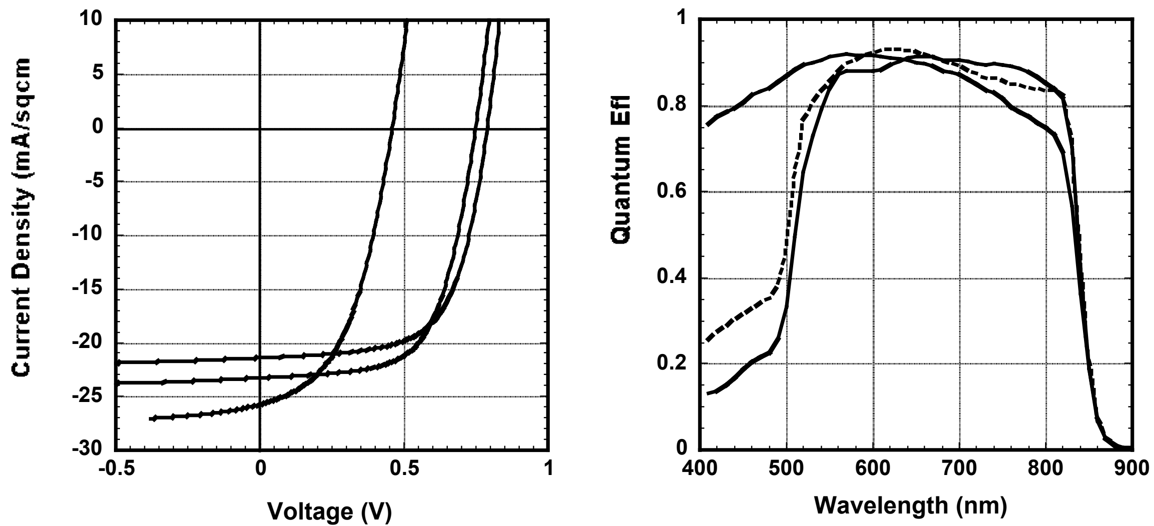


Figure 4.20 Light J-V and QE curves for devices with final d(CdS) = 20 nm, 95 nm, and 120 nm on ITO/soda-lime glass.

Cells employing ultra-thin CdS with improved junction characteristics and conversion efficiency approaching 14% were fabricated with evaporated CdTe by use of high resistance inter-layers (HR). Devices were thus fabricated on crystallized ITO on Glaverbel soda-lime glass (SL) or Corning 7059. The following TCO/HR configurations were used to evaluate high resistance inter-layers:

1) Sputtered indium-tin oxide prepared at IEC on ITO/SL and ITO/7059 prepared at IEC;
2) Oxidized indium, In_2O_3, prepared at IEC on ITO/SL and ITO/7059 prepared at IEC;
3) Oxidized tin, SnO_2, prepared at IEC on SnO_2/7059 prepared at Solarex;

4) Sputtered zinc stannate, Zn_2SnO_4, prepared by Xuanjing Wu at NREL on sputtered ITO/7059 prepared at IEC;
5) Sprayed Cd-doped SnO_2 prepared by Peter Meyers at ITN onto L.O.F. SnO_2/SL (TEC8).

In cases 1–4 above, the HR layer was approximately 100 nm thick with resistivity > 10 Ω-cm, but the sprayed SnO_2 layers were ~800 nm thick. The J-V behavior of the cell fabricated for each case, with evaporated CdTe films are shown in Figure 4.21, Figure 4.22, Figure 4.23, Figure 4.24, Figure 4.25, and Figure 4.26.

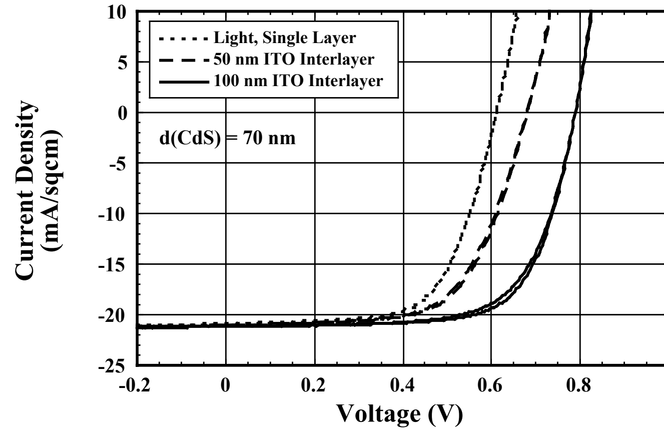


Figure 4.21 ITO HR layer on ITO TCO with evaporated CdS. Light J-V results for devices with final d(CdS) = 70 nm on single layer and bilayer ITO/7059 with 50 nm and 100 nm thick high-resistance ITO. The cell with 100 nm HR layer has V_{oc} = 785 mV; J_{sc} = 21.5 mA/cm^2; FF = 69%; Eff = 11.6%.

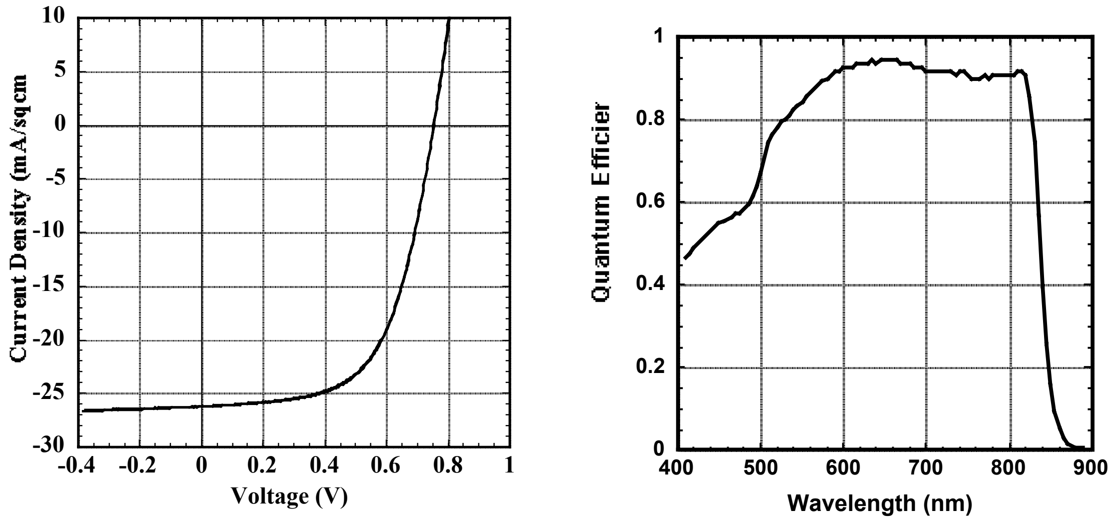


Figure 4.22 ITO HR layer on ITO TCO with chemical bath CdS. Light J-V results for devices with final d(CdS) = 40 nm on bilayer ITO/7059 with 100 nm thick high-resistance ITO. V_{oc} = 754 mV; J_{sc} = 26 mA/cm^2; FF = 60%; Eff = 11.7%.

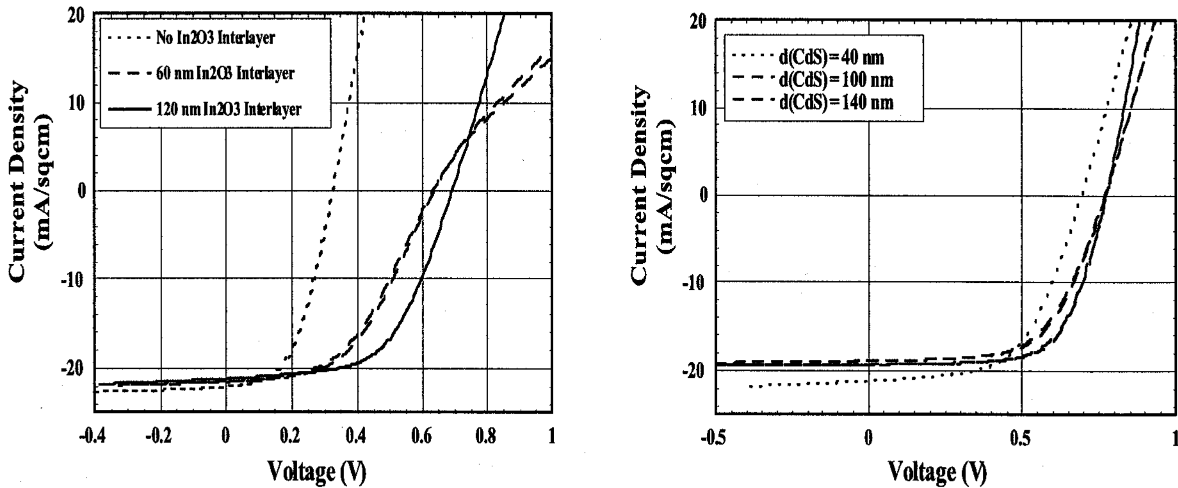


Figure 4.23 In_2O_3 HR layer on ITO TCO with evaporated CdS. Light J-V results for devices with varying HR In_2O_3 thickness (left) and CdS (right) on ITO/7059.

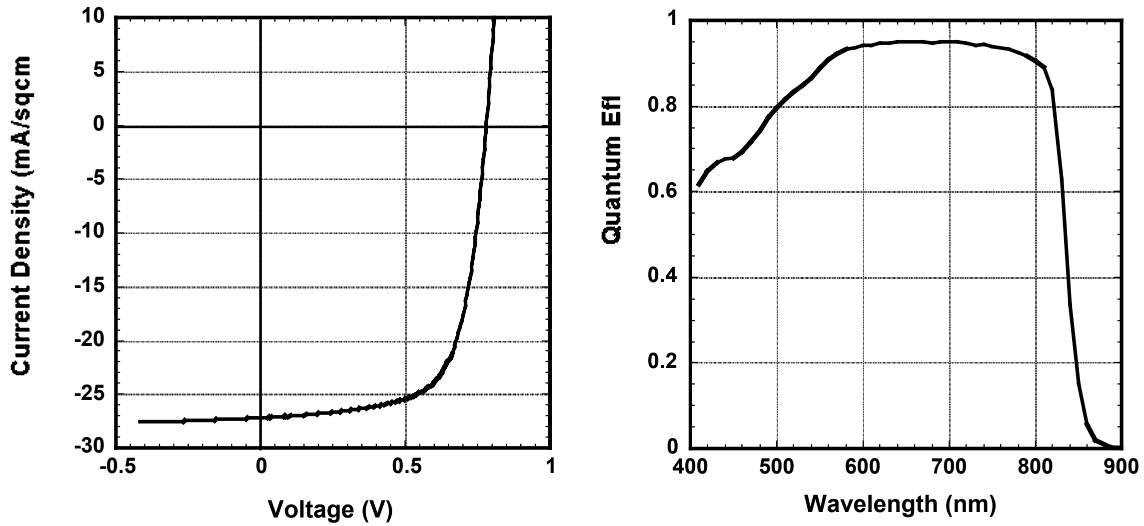


Figure 4.24 SnO_2 HR layer on SnO_2 TCO with evaporated CdS. Light J-V and QE results for device with final d(CdS) ~ 30 nm on 1000 nm SnO_2 HR layer on Solarex SnO_2/7059. V_{oc} = 790 mV; J_{sc} = 26 mA/cm^2; FF = 68%; Eff = 13.9%.

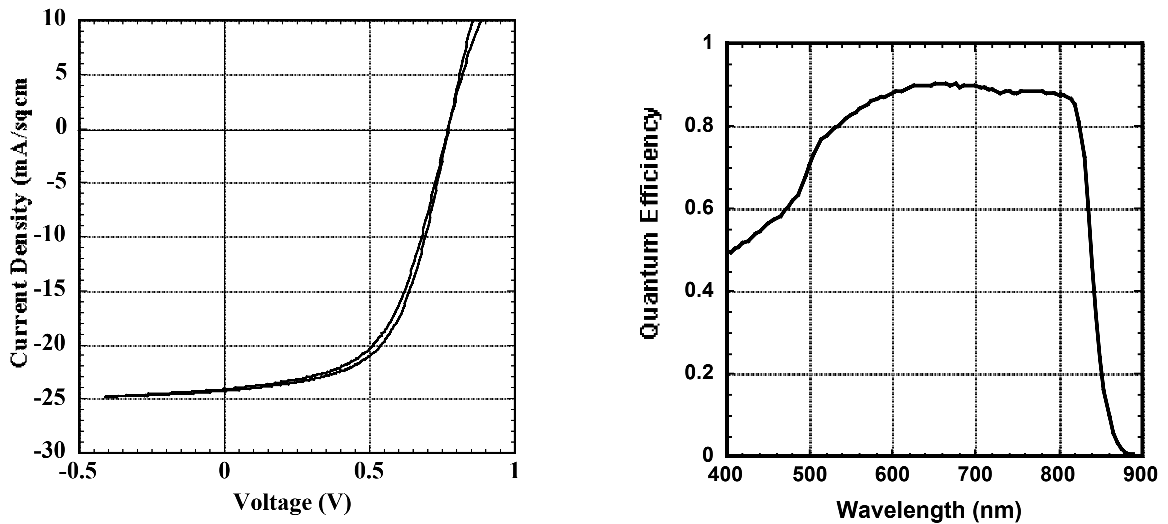


Figure 4.25 Zn_2SnO_4 HR layer on ITO TCO with evaporated CdS. Light J-V and QE results for device with final d(CdS) ~ 40 nm on 100 nm Zn_2SnO_4 HR layer on 200 nm ITO/7059. V_{oc} = 772 mV; J_{sc} = 24.3 mA/cm^2; FF = 58%; Eff = 10.9%.

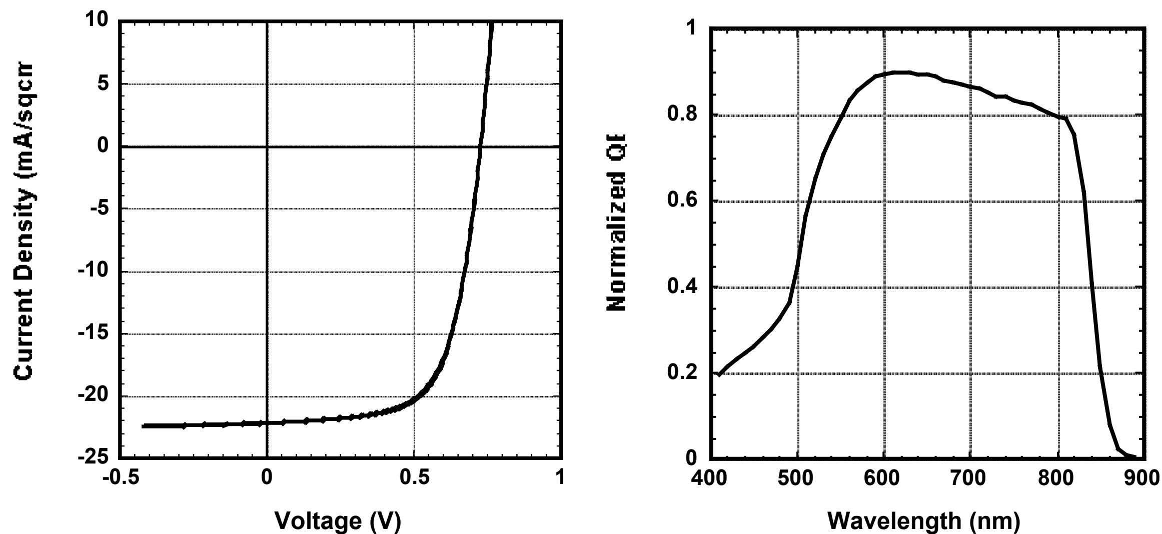


Figure 4.26 Cd-doped SnO_4 HR layer on SnO_2 TCO with evaporated CdS. Light J-V and QE results for device with final d(CdS_2) ~ 90 nm on 100 nm Zn_2SnO_4 HR layer on 200 nm ITO/7059. V_{oc} = 730 mV; J_{sc} = 22.1 mA/cm^2; FF = 65%; Eff = 10.5%.

The above data demonstrates that different HR layers can be employed to maintain junction characteristics for evaporated CdTe devices with final d(CdS) < 100 nm and processed with the same $CdCl_2$ vapor treatment. Further gains in efficiency are expected by optimizing both post-deposition and CdS processing for a given HR/TCO combination. Junctions between CdTe and the HR/TCO structure also need to be electrically analyzed.

Below, Table 4.7 summarizes the TCO layer structure and CdS thickness, measured J-V parameters, and extracted diode parameters for selected cells with different TCO configurations and CdS thickness. The J-V curves were analyzed by graphing dV/dJ vs ($1/J+J_{sc}$) to obtain R_s and A, and log ($J+J_{sc}$) vs ($V-JR_s$) to obtain diode parameters A and J_o. In general, good fits were obtained with the dark J-V, while poorer fits were obtained with the light J-V. The A-factors in the dark were near 2, except in the case of very low V_{oc}. The A-factor from the dark J-V curve was about half the value from the light, and J_o from the dark J-V is typically 3-5 orders of magnitude lower than from the light. This is commonly seen in cells with large voltage dependent collection (like a-Si). In this case, the apparent slope of log ($J+J_{sc}$) is not only due to the forward diode current but has other voltage dependent influences. Thus "J_o" and "A" obtained from the *light* should not be interpreted as diode parameters and are not included here. Values of R_s were always smaller in the light, typically less than 3 Ω-cm^2. The only devices with evidence of blocking contacts were the two from group E, having very thin (either 0 or 30 nm) final CdS, resulting in slight curvature in the light J-V, high R_s and large light-to-dark-crossover.

In Table 4.7, series A and B use ITO while series C, D, and E use SnO_2 as the TCO layer. Previously, with standard sputtered ITO of 200 nm thickness, the V_{oc} and FF would have been ~300 mV and 40%, respectively, for devices with initial CdS thickness of 100 nm (3). Series A shows the effect of CdS thickness on in-house ~0.5 μm ITO, which is 2X, the previously used

thickness. Note the decrease in V_{oc} as CdS is reduced from 140 to 80 nm but the improved performance compared to previous results. Piece 41082.12 represents a control since it has relatively thick ITO and thick bilayer CdS. Series B compares the effect of H_2-heat treatment and CdS thickness using in-house standard ITO. Comparing results from series A to series B shows that V_{oc} is strongly degraded by decreasing CdS thickness with thin ITO (200 nm) or by decreasing ITO thickness with thin CdS (60-80 nm). The FF is less affected than V_{oc}. Crystallizing the thin ITO with a H_2 heat treatment restores V_{oc} despite the thin CdS layer.

Series C shows the significant gain in V_{oc} and FF with the addition of a thin high resistance in-house SnO_2 layer obtained by oxidizing a tin film. In both C and D, the devices with the high resistance SnO_2 bilayer actually have much lower R_s but higher A and J_o. For example, 41082.13 having *undoped* ITN SnO_2 has poor FF not because of high R_s but very high A (~6) and J_o (2E-1 mA/cm^2). Pieces 41082.23 and .21 having Cd or Zn *doped* ITN SnO_2 have much lower A (~2) and J_o (~1E-5 mA/cm^2) but higher R_s. Thus, even though these pieces had 110 nm of starting CdS, the TCO resistivity affected the junction properties not the resistance. Series D compares ITN deposited SnO_2 layers (undoped and Zn and Cd doped) on LOF SnO_2. The Cd and Zn doped SnO_2 bilayers had equivalent device performance and diode parameters. Series E compares very thin CdS on the Zn-doped SnO_2 from ITN. These both represent improvements in V_{oc} over what has been obtained with such thin CdS on ITO indicating improved junction behavior with the new SnO_2 materials. However, the two cells in series E have low FF due to high R_s.

To separate effects of CdS processing from post-deposition processing, future work will repeat some of these device structures using as-deposited CdS with and without high-temperature annealing. In addition, devices will be fabricated and characterized using CdTe and $CdTe_{(1-x)}S_x$ absorber layers, deposited by PVD at substrate temperatures > 350˚C onto TCO bilayers with and without ultra-thin CdS coatings to characterize and compare $CdTe_{(1-x)}S_x$/TCO junctions made by 1) diffusing CdS into CdTe and 2) co-deposition of CdS and CdTe.

Table 4.7 Results from analysis of IEC CdTe pieces having different TCO materials and CdS thickness. Series resistance R_s, diode factor A, and recombination current J_o from analysis of dark J-V data. All CdS layers treated with $CdCl_2$ heat treatment prior to CdTe deposition.

Series	Piece #	Window Contact	Final CdS thick (nm)	R_s (Ohm/ sqcm)	A factor	J_o (mA/ sqcm)	V_{oc} (mV)	J_{sc} (mA/ sqcm)	FF (%)
A	41083.12	550 nm ITO	60	5.0	1.2	2.6e^-7	630	22.0	63
	41082.12	540 nm ITO	120 bilayer	2.5	2.2	1.2e^-5	790	21.4	64
B	41042.23	200 nm ITO	80	5.3	1.7	4.8e^-5	590	17.8	61
	41082.22	200 nm ITO with H_2 HT	90	3.8	2.1	2.4e^-5	750	23.3	63
	41078.21	200 nm ITO	40	2.36	1.6	1.1e^-3	400	24.0	55
C	41072.12a	Slx SnO_2	45	18	2.4	3.4e^-4	500	19.9	37
	41082.32	Slx SnO_2 +Sn layer	55	0.5	3.0	8.4e^-5	780	27.1	65
D	41082.13	Undoped SnO_2**	90	0.6	6.2	0.18	700	18.7	52
	41082.21	Cd doped SnO_2**	90	2.5	1.9	1.3e^-5	730	22.1	65
	41082.23	Zn doped SnO_2**	90	4.7	2.0	8.0e^-6	720	22.5	64
E	41077.23	Zn doped SnO_2**	0	28.3	hyst.	hyst.	520	23.8	50***
	41077.32	Zn doped SnO_2**	<10	17.8	1.9	7.2e^-6	700	22.3	49***

** SnO_2 bilayers deposited at ITN on LOF SnO_2

*** slight curvature in J-V beyond V_{oc}, large light-to-dark crossover

4.3 CdTe Contact Development

4.3.1 Wet Contact Process

This section describes the method and chemistry of the "wet" contact process. Table 4.8 shows the processing steps employed to fabricate solar cells from evaporated CdTe/CdS structures. We will focus on steps 4 to 9, from $CdCl_2$:O_2 treatment to final etch with Br_2:CH_3OH.

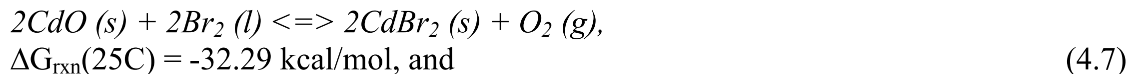
Table 4.8 Processing steps used for fabricating evaporated CdTe/CdS solar cells.

1	Deposit 10-100 nm CdS onto TCO/glass
2	HT CdS at 420C with $CdCl_2$:O_2
3	Deposit 2-4 μm CdTe
4	HT at 420C with $CdCl_2$:O_2:Ar
5	Etch/React with Br_2:CH_3OH
6	Etch/React with aqueous $K_2Cr_2O_7$:H_2SO_4
7	Etch/React with N_2H_4:H_2O
8	Deposit 10-40 nm Cu and HT at 200C
9	Etch/React with Br_2:CH_3OH
10	Apply Current-Carrying Conductor

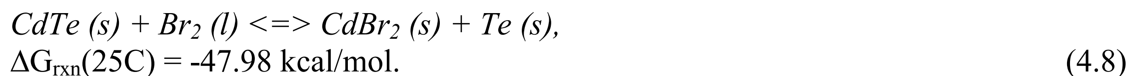
The oxide-containing and Cd-enriched surface produced on the CdTe after $CdCl_2$:O_2 treatment is detrimental in two ways: 1) p-type conductivity was shown by de Nobel [57] and others to depend inversely on *p*(Cd) and 2) CdO has high resistivity, may be variable in thickness, and is a potential diffusion barrier for p-dopants needed to compensate for the first detriment. To counter these effects, CdO must be removed, and the surface is chemically altered to a Te-rich condition. For its wet process, IEC utilizes a three-step reaction with Br_2:CH_3OH, aqueous $K_2Cr_2O_7$:H_2SO_4, and N_2H_4, collectively termed "BDH", after "bromine, dichromate, hydrazine". This process works by depleting the surface region of Cd followed by reduction of Te oxides. Each process step is considered below.

4.3.1.1 Reaction in Br_2:CH_3OH

Reaction of CdTe:CdO in Br_2:CH_3OH are shown to be thermodynamically favored according to:



$$2CdO\ (s) + 2Br_2\ (l) <=> 2CdBr_2\ (s) + O_2\ (g),$$
$$\Delta G_{rxn}(25C) = -32.29 \text{ kcal/mol, and} \quad (4.7)$$



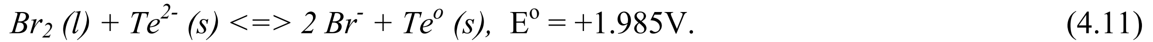
$$CdTe\ (s) + Br_2\ (l) <=> CdBr_2\ (s) + Te\ (s),$$
$$\Delta G_{rxn}(25C) = -47.98 \text{ kcal/mol.} \quad (4.8)$$

The product $CdBr_2$ is soluble in methanol and water and is removed from the surface by agitation and rinsing. The reaction to form elemental Te from lattice-bound Te^{2-} is further described by the room temperature half-cell reactions at the surface:

$$Br_2\,(l) + 2e^- <=> 2Br^-,\ E^o = +1.065V \qquad (4.9)$$

$$Te^{2-}\,(s) <=> Te^o\,(s) + 2\,e^-,\ E^o = +0.92V. \qquad (4.10)$$

Adding these reactions and potentials, the highly favored overall reaction is expected:



$$Br_2\,(l) + Te^{2-}\,(s) <=> 2\,Br^- + Te^o\,(s),\ E^o = +1.985V. \qquad (4.11)$$

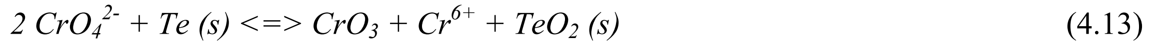
XPS studies by Danaher, et. al. [58] on single crystal CdTe reacted in 0.01% (vol) Br_2:CH_3OH show Cd-depletion at the surface, extending 3 nm into the surface. They determined an oxidation rate of free Te to be 0.02 nm/minute, according to the favored reaction:

$$Te\,(s) + O_2\,(g) <=> TeO_2\,(s),$$
$$\Delta G_{rxn}(25C) = -64.39\ \text{kcal/mol}. \qquad (4.12)$$

The thin Te coating produced by etching in Br_2:CH_3OH is not extensive and oxidizes rapidly, diminishing the benefits for doping or contacting; the step is primarily used therefore to eliminate CdO. SIMS measurements by the same group, on CdTe/CdS/ITO thin films, indicated residual Br through the film extending to the CdS/ITO interface.

4.3.1.2 Reaction in $K_2Cr_2O_7$:H_2SO_4

The reaction of CdTe in aqueous K_2CrO_4 produces TeO_2 according to:



$$2\,CrO_4^{2-} + Te\,(s) <=> CrO_3 + Cr^{6+} + TeO_2\,(s) \qquad (4.13)$$

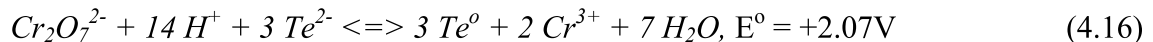
The addition of protons to the solution by adding acid complicates the ionic makeup of the solution. At low pH, the primary effect is the reduction of the chromate ion to dichromate:

$$2\,CrO_4^{=} + 2\,H^+ <=> Cr_2O_7^{2-} + H_2O \qquad (4.14)$$

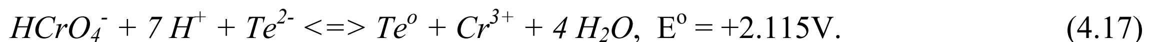
and the production of chromic acid:

$$CrO_4^{2-} + 2\,H^+ <=> H_2CrO_4. \qquad (4.15)$$

Elemental Te is readily liberated from the CdTe lattice by electrolytic reaction with the chromate or hypochromous ion. The overall favored reactions and room temperature potentials are:



$$Cr_2O_7^{2-} + 14\,H^+ + 3\,Te^{2-} <=> 3\,Te^o + 2\,Cr^{3+} + 7\,H_2O,\ E^o = +2.07V \qquad (4.16)$$

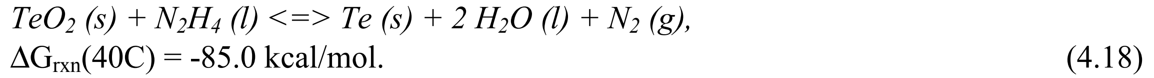


$$HCrO_4^- + 7\,H^+ + Te^{2-} <=> Te^o + Cr^{3+} + 4\,H_2O,\ E^o = +2.115V. \qquad (4.17)$$

XPS and studies by Danaher , et. al. on single crystal CdTe reacted in aqueous K_2CrO_4 and in $K_2Cr_2O_7$:H_2SO_4 solution confirm this chemistry, indicating Cd-depleted surface in all cases, with TeO_2 on the surface reacted with aqueous K_2CrO_4 and elemental Te on the surface reacted with 1:1 $K_2Cr_2O_7$:H_2SO_4. Mixed Te:TeO_2 was obtained on samples reacted with lower acid concentrations. SIMS measurements of reacted CdTe/CdS/ITO films indicated that Cr penetrated the CdTe film but did not accumulate in the CdS/ITO films.

4.3.1.3 Reaction in N_2H_4:H_2O

As a final step in producing a Te-enriched surface, reaction in hydrazine is carried out. Reactions with TeO_2 powder and 98:2 N_2H_4:H_2O solution at 25-40C release significant quantities of gas and change the solution color from clear to faint purple. Similar results are obtained when etching films after reaction with $K_2Cr_2O_7$:H_2SO_4. These observations are consistent with reduction of TeO_2:



$$TeO_2\ (s) + N_2H_4\ (l) <=> Te\ (s) + 2\ H_2O\ (l) + N_2\ (g),$$
$$\Delta G_{rxn}(40C) = -85.0\ \text{kcal/mol.} \quad (4.18)$$

Direct reaction of CdTe with N_2H_4:H_2O to release Cd or Te is not thermodynamically favored. GIXRD measurements at 1 degree incidence of CdTe/CdS/ITO thin films confirm the formation of elemental Te after the entire BDH process as shown in Figure 4.27.

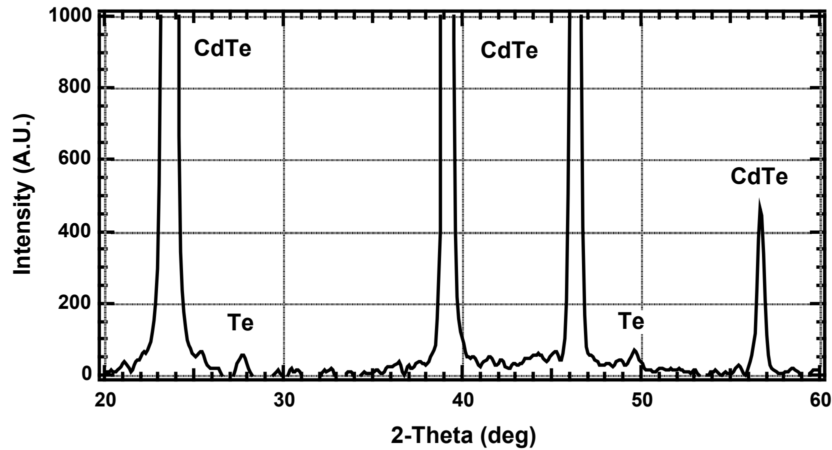


Figure 4.27 Glancing incidence x-ray diffraction pattern of the CdTe surface of a CdTe/CdS/ITO thin film after the entire BDH process, showing elemental Te. The pattern was acquired at an incident beam angle of 1.0 degree.

4.3.1.4 Copper Deposition and Reaction

Rapid transferal of the reacted CdTe samples to the Cu deposition system reduces the formation of TeO_2 after the N_2H_4:H_2O reaction. Deposition of Cu followed by *in situ* vacuum heat treatment at 200˚C produces copper tellurides:

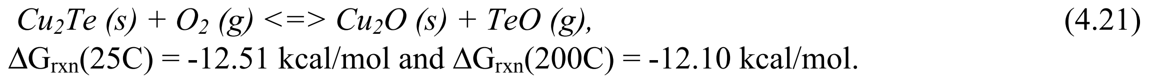
$$Te\ (s) + 2\ Cu\ (s) <=> Cu_2Te\ (s),$$
$$\Delta\ G_{rxn}(200C) = -12.13\ \text{kcal/mol,} \quad (4.19)$$

and

$$Te\ (s) + Cu\ (s) <=> CuTe\ (s),$$
$$\Delta G_{rxn}(200C) = -6.47\ \text{kcal/mol.} \quad (4.20)$$

The equilibrium T-x phase diagram for the Cu-Te system shows the possible phases obtained over the full range of relative quantities of Cu and Te. In the devices, we are primarily concerned with Cu_2Te; the possible equilibrium phase fields around this composition are Cu+ Cu_2Te, $Cu_{2-x}Te$, $Cu_{2-x}Te + Cu_3Te_2$, and Cu_3Te_2 + CuTe. Failure to provide sufficient Cu thus forces the system out of the Cu_2Te phase field and into the Te-rich phases.

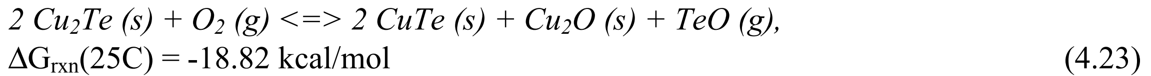
The formation of oxides by reaction in air with Cu_2Te or unreacted Cu is thermodynamically favored:



$Cu_2Te\ (s) + O_2\ (g) <=> Cu_2O\ (s) + TeO\ (g),$ (4.21)
$\Delta G_{rxn}(25C) = -12.51$ kcal/mol and $\Delta G_{rxn}(200C) = -12.10$ kcal/mol.

22) $2\ Cu\ (s) + O_2\ (g) <=> Cu_2O\ (s),$
$\Delta G_{rxn}(25C) = -28.02$ kcal/mol and $\Delta G_{rxn}(200C) = -20.38$ kcal/mol. (4.22)

GIXRD measurements at 1 degree incidence of 15 nm Cu/CdTe/CdS/ITO thin films confirm the presence of only elemental Cu and Cu_2Te (Weissite) phases after Cu deposition plus *in situ* vacuum heat treatment at 200C. After additional heat treatment at 200C in air, Cu_2Te, CuTe, and Cu_2O were detected as shown in Figure 4.28. Elemental Cu was reacted, and, as the figure shows, CuTe formed, suggesting that in the presence of O_2, Cu_2Te can act as a source of Cu, supplying the overall reaction:



$2\ Cu_2Te\ (s) + O_2\ (g) <=> 2\ CuTe\ (s) + Cu_2O\ (s) + TeO\ (g),$
$\Delta G_{rxn}(25C) = -18.82$ kcal/mol (4.23)

For this chemical system, if the component concentrations were fixed, then Gibb's equilibrium phase rule allows for the number of phases, P = (C+2)-F, where C is the number of components (= 3), and F is the number of degrees of freedom (= 0). In this case, P = 5, and the phase rule is not violated. If, however, the component concentrations are allowed to vary, which seems realistic for the Cu_2Te phase, then F = 1 and P = 4, leading to a violation of the phase rule, suggesting that the pattern at the top of Figure 4.28 could represent an intermediate condition between equilibrium states. Alternatively, multiple equilibria exist at different spatial locations, i.e., that the system is dominated by chemical kinetics at different points through or across the film surface.

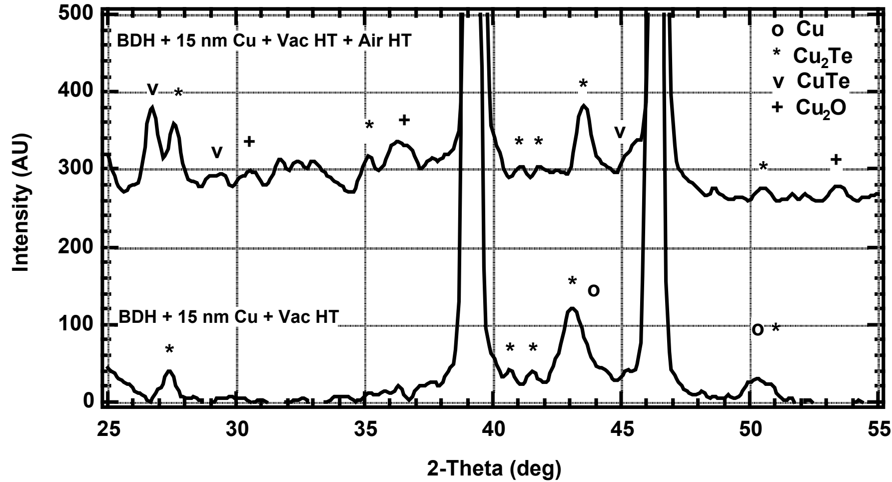
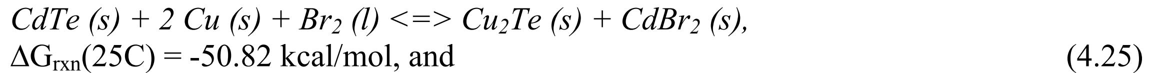


Figure 4.28 Glancing incidence x-ray diffractograms with 1 degree incident beam angle of 15 nm Cu/CdTe/CdS/ITO/glass structure: a) after Cu deposition and *in situ* vacuum heat treatment at 200˚C and b) after additional air heat treatment at 200˚C.

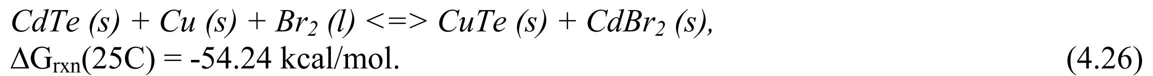
4.3.1.5 Etch/Chemical Treatment after Copper Deposition

To minimize formation of oxides in completed devices, reaction in Br_2:CH_3OH is used to remove surplus Cu. In the presence of CdTe, this reaction can produce additional Cu_2Te:

$$Cu\ (s) + Br_2\ (l) <=> CuBr\ (s),$$
$$\Delta G_{rxn}(25C) = -29.01 \text{ kcal/mol,} \quad (4.24)$$



$$CdTe\ (s) + 2\ Cu\ (s) + Br_2\ (l) <=> Cu_2Te\ (s) + CdBr_2\ (s),$$
$$\Delta G_{rxn}(25C) = -50.82 \text{ kcal/mol, and} \quad (4.25)$$



$$CdTe\ (s) + Cu\ (s) + Br_2\ (l) <=> CuTe\ (s) + CdBr_2\ (s),$$
$$\Delta G_{rxn}(25C) = -54.24 \text{ kcal/mol.} \quad (4.26)$$

In both reactions, the bromide products are soluble in methanol and water and are thus removed by agitation or rinsing. GIXRD measurements of etched surfaces indicate the presence of both Cu_2Te (Weissite) and CuTe (Vulcanite) phases.

4.3.2 Vapor Contact Process

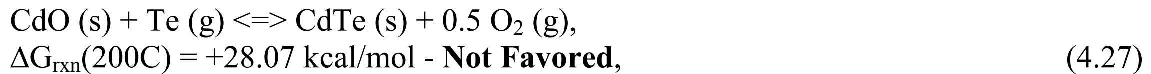
This section describes the method and chemistry of the all-vapor process used to fabricate solar cells from evaporated CdTe films. Table 4.9 shows the processing steps employed to fabricate solar cells from evaporated CdTe/CdS structures. For the chemical analysis, we will focus on steps 5 and 6, reaction of CdTe surface with Te/H_2 vapor and deposition/reaction of Cu.

Table 4.9 Processing steps used for fabricating evaporated CdTe/CdS solar cells.

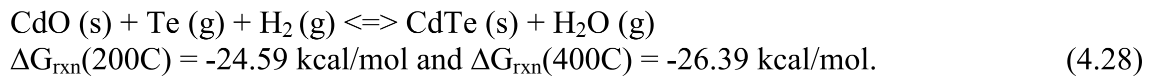
1	Deposit 10-100 nm CdS onto TCO/glass
2	HT CdS at 420C with $CdCl_2$:O_2
3	Deposit 2-6 μm CdTe
4	HT at 420C with $CdCl_2$:O_2
5	React with Te/H_2
6	Deposit 10-40 nm Cu and HT at 200C
7	Apply Current-Carrying Conductor

4.3.2.1 Heat Treatment in Te/H_2

As discussed in Section 4.2.2, the back surface of the CdTe film contains CdO and native oxides. The net result of the wet chemical process is removal of these oxides and production of a Te layer. This process can be forced to occur without wet chemistry by reacting the CdO-containing surface in an overpressure of Te and H_2. The H_2 component is essential to obtain oxidation of Cd by Te:



$$CdO\ (s) + Te\ (g) <=> CdTe\ (s) + 0.5\ O_2\ (g),$$
$$\Delta G_{rxn}(200C) = +28.07\ \text{kcal/mol - \textbf{Not Favored}}, \qquad (4.27)$$



$$CdO\ (s) + Te\ (g) + H_2\ (g) <=> CdTe\ (s) + H_2O\ (g)$$
$$\Delta G_{rxn}(200C) = -24.59\ \text{kcal/mol and}\ \Delta G_{rxn}(400C) = -26.39\ \text{kcal/mol}. \qquad (4.28)$$

Reaction 4.28 above shows that the entire chemical reaction to form CdTe and H_2O is highly favored in the 200-400˚C temperature range. The Te vapor can be generated from a sintered planar powder source at a distance of ~0.5 mm from the surface of the CdTe/CdS sample. At a source temperature of 400˚C, the Te partial pressure (as 1/2 Te_2 over solid Te) is ~100 mTorr. Generating excess surface Te is accomplished by maintaining Te supersaturation above the CdTe surface; a temperature differential of ~100˚C causes Te condensation, resulting in a net mass transfer from source to substrate. For the gas phase concentrations involved, steady state is rapidly achieved, and the accumulation of Te on the CdTe surface has been determined to be linear. At 1 atmosphere total pressure, T_{Te} = 400˚C and T_{CdTe} = 250˚C, the growth rate is ~10 nm/min.

Initially, experiments were conducted with CdO + Te powders (50-100 μm particle size) in an isothermal reactor at 400˚C in Ar with and without H_2 species. The powders were mixed in 1:1 molar ratio of CdO:Te and were heat treated at 400˚C for 30 minutes. Figure 4.29 shows powder XRD diffractograms for each case; the quantity CdO was reduced, and CdTe was obtained only when the reaction of the CdTe/CdS structure was carried out in H_2 ambient, as 4% H_2 in balance of Ar. Similar experiments conducted in close-space configuration with CdTe/CdS samples for devices and yielded Ohmic forward bias J-V contact behavior only in cases using H_2, indicating the necessity for removal of CdO.

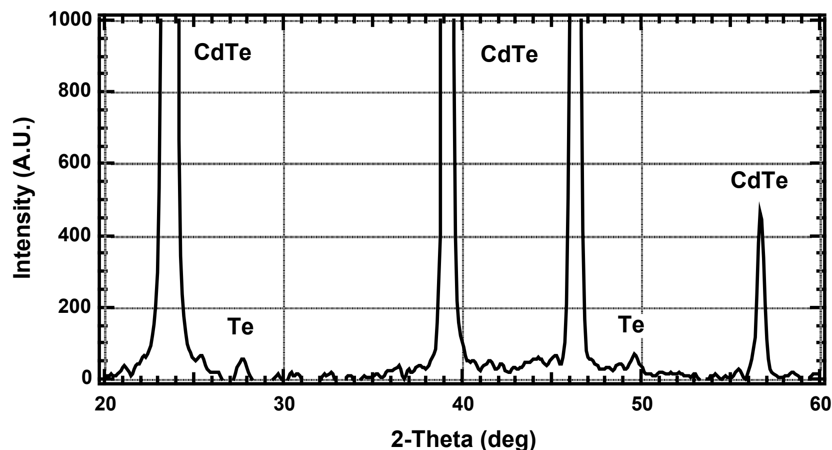


Figure 4.29 Powder x-ray diffraction patterns of CdO + Te before and after heat treatment in Ar with and without H_2 at 400˚C for 30 minutes.

4.3.2.2 Copper Deposition and Reaction

Rapid transferal of the reacted CdTe samples to the Cu deposition system reduces the formation of TeO_2, and deposition of Cu followed by in situ vacuum heat treatment at 200˚C produces copper tellurides as in the wet technique previously described.

Te (s) + 2 Cu (s) <=> Cu2Te (s),
$\Delta(G_{rxn}(200C) = -12.13$ kcal/mol, and (4.29)

Te (s) + Cu (s) <=> CuTe (s),
$\Delta(G_{rxn}(200C) = -6.47$ kcal/mol. (4.30)

The quantity of Cu deposited must be chosen to maintain the Cu_2Te stoichiometry as shown in Table 4.10.

Table 4.10 Thickness of Cu and Te required for Cu_2Te formation.

Cu_2Te Thickness Desired (nm)	Te Thickness Required (nm)	Cu Thickness Required (nm)
1	0.58	0.41
5	2.9	2.0
10	5.8	4.1
20	11.6	8.1
50	29.1	20.3
100	58.2	40.7

Glancing incidence x-ray diffraction (GIXRD) measurements at 1 degree incidence of 5 nm Cu/>7 nm Te/ITO/glass and of 5 nm Cu/>7 nm Te/CdTe/CdS/ITO/glass thin films confirm the presence of only Cu_2Te (Weissite) phases after Cu deposition plus *in situ* vacuum heat treatment at 200˚C. The tolerable range of Cu excess in the device structure has not been determined, but it is expected that performance will be limited by shunting for d(Cu) > 40 nm and formation of oxides. Figure 4.30 shows GIXRD patterns of Cu/Te/CdTe/CdS structures with varying Cu/(Cu+Te) at the back surface. The phase composition varies in accordance with the equilibrium phase diagram for the Cu-Te system. The J-V behavior of devices made on these samples exhibited less Ohmic behavior as Cu/(Cu+Te) decreased.

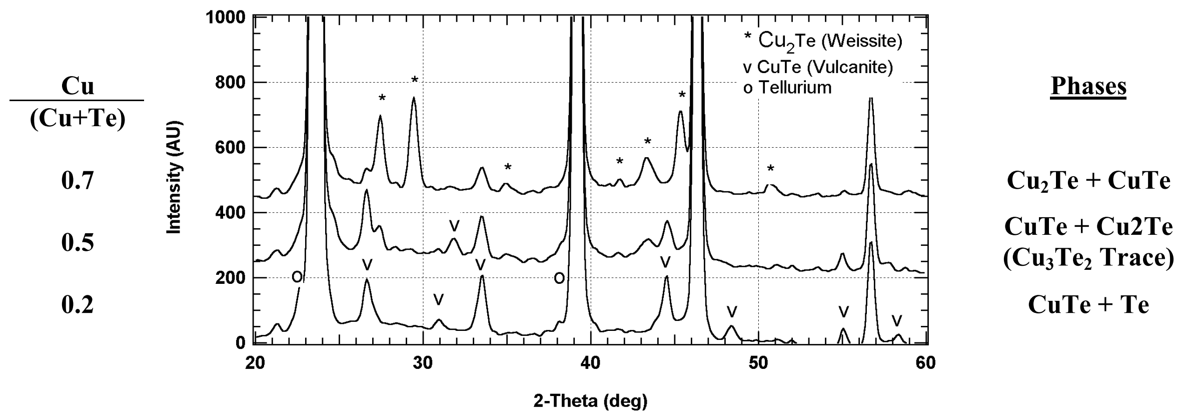
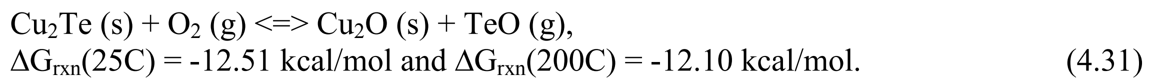


Figure 4.30 GIXRD of Cu/Te/CdTe surface after heat treatment in vacuum at 200˚C for 30 minutes.

As before, the formation of oxides by reaction in air with Cu_2Te or unreacted Cu is thermodynamically favored:



Cu_2Te (s) + O_2 (g) <=> Cu_2O (s) + TeO (g),
$\Delta G_{rxn}(25C) = -12.51$ kcal/mol and $\Delta G_{rxn}(200C) = -12.10$ kcal/mol. (4.31)

$$2\,Cu\,(s) + O_2\,(g) \Leftrightarrow Cu_2O\,(s),$$
$$\Delta G_{rxn}(25C) = -28.02\ \text{kcal/mol and}\ \Delta G_{rxn}(200C) = -20.38\ \text{kcal/mol.} \qquad (4.32)$$

4.3.3 Electrical Analysis of Contact

The chemical assessment of the contact in Sections 4.3.1 and 4.3.2 show that the amount of free Cu available to dope the CdTe layer, grain boundaries and bulk, depends on the relative amount of Te produced by the CdTe surface treatment. We have begun to examine the effects of the Cu/Te ratio on device performance and stress-induced degradation. Table 4.11 shows J-V results for devices made with First Solar CdTe/CdS and IEC vapor contact with a fixed Cu thickness but varying Te thickness. As with earlier experiments fixing Te treatment but varying the Cu thickness, the V_{oc} and FF were found to decrease with decreasing Cu/Te ratio. The R_{oc} for the light diode is essentially unaffected, suggesting that a similar p+ surface was formed at the CdTe-Cu-Te interface. The sensitivity of the device performance to small changes in Cu/Te ratio may bear on any field-type migration effects produced by optoelectrical stressing.

Table 4.11 First Solar CdTe/CdS with IEC vapor contact process for varying Te concentration.

Cell 2435	Te	P_{max} mW/ sqcm	V_{oc} (mV)	J_{sc} mA/ sqcm	FF (%)	Eff (%)	R_{oc} Ohm-sqcm	G_{sc} mS/ sqcm
I3.16-2	1X	11.2	810	20.0	69	11.1	4.9	0.8
I3.15-2	2X	10.1	792	18.9	67	10.0	4.6	0.6
I3.13-2	4X	9.7	776	19.2	65	9.7	5.3	1.3

Analysis of the electrical behavior of the contact produced was carried out for an IEC CdS/CdTe device made by physical vapor deposition with a carbon contact [59]. We have also found that for stress-degraded devices, the "blocking" behavior can be eliminated by removing the original contact, re-etching the surface, and applying a new contact. This suggests the existence of a junction in the interface between CdTe and the current-carrying conductor whose properties depend critically on sample preparation and subsequent treatment.

4.4 Stability of CdS/CdTe Solar Cells

4.4.1 Effect of Cu Thickness and Contact Processing on CdS/CdTe Stability

We have observed in the past that devices stressed without any Cu layer degrade differently than those stressed with a 150Å Cu layer, where both types of devices had a C contact as the primary current conductor. During this contract, we fabricated and stressed a series of CdS/CdTe devices having a systematic variation in Cu thickness (0, 20, 50, 150 Å). Two different contact processes were used at each thickness: one was our previous standard involving bromine-dichrol-hydrazine (BDH) etch and $CdCl_2$ heat treatment, a “wet” process; the other was a newly developed all-vapor treatment, a “dry” process. All CdS/CdTe devices were cut from a single plate of SCI material, #20632.H3, and all subsequent processing was performed at IEC. Devices

were stressed for 6 days at 100°C in room air at V_{oc}. We focus on V_{oc} and FF because they degrade the most.

Figure 4.31 and Figure 4.32 show the dependence of V_{oc} and FF on Cu layer thickness before and after stressing for the two different contact processes. Initial V_{oc} was 0.80 ± 0.02 V and FF was 69 ± 2% for all devices except the one without Cu, as expected. Note that the device without Cu having the wet contact has the highest V_{oc} *after* stressing, despite having the lowest V_{oc} *before* stressing. It degraded only 0.04 V compared to ~0.15 V for all the other devices. Figure 4.31 shows that the piece with the dry contact and thickest (150Å) Cu layer had the highest V_{oc} after stressing of any device with Cu. Conversely, the highest FF after stressing was on the piece with least Cu (20Å) and the wet contact. This suggests that there is an optimum Cu thickness depending on the surface properties of the CdTe following a given contact process. But these results also demonstrate significant degradation occurs independent of the amount of Cu for both of the contact processes.

Figure 4.33 and Figure 4.34 show light and dark JV curves at 25°C and at -30°C before and after stressing, respectively, for device H3.3 having 50Å Cu with the standard wet contact process. Even though this device had a FF of 71% at 25°C before stressing, the dark JV curve in Figure 4.33 shows curvature at forward bias and high resistance which is missing from the light JV curve. Both these effects are magnified at -30°C. The blocking contact behavior is readily apparent at -30°C even before stressing. After stressing, Figure 4.34 shows increased curvature and blocking behavior at both temperatures. Comparing Figure 4.33 and Figure 4.34, we conclude that lowering the temperature before stressing has qualitatively the same effect on the forward bias JV characteristic as stressing, perhaps relating to a decrease in conductivity of the CdTe layer at the back contact. It was observed that devices with the dry contact process tend to have less "roll over" (current limiting curvature in forward bias) after stressing. This suggests the wet contact enhanced the formation of the blocking contact.

Additional insight into degradation of V_{oc} was obtained from analysis of V_{oc} vs T. V_{oc} was measured at three intensities (100, 35, and 15% of one sun illumination) from 350 to 220 K before and after stressing. A linear relation between V_{oc} and T was found over this range for all devices except for the one without Cu. Figure 4.35 and Figure 4.36 show V_{oc} vs T before stressing for devices with the wet contact with 0Å Cu (H3.0) and with 20Å Cu (H3.1), respectively. Figure 4.35 shows that the V_{oc} values for the device without Cu lose both their intensity and temperature dependence with decreasing temperature, converging to a value around 0.84 V. This could be due to carrier freeze-out since the CdTe conductivity and carrier density is very low without Cu as a dopant. In contrast, the device with 20Å Cu in Figure 4.36 shows typical linear behavior with an intercept of ~1.45 eV at one sun, as expected for the bandgap of the CdTe absorber, indicating recombination occurs through the distribution of gap states in the space charge region in the CdTe [60].

Figure 4.37 and Figure 4.38 show V_{oc} vs T at one sun intensity before and after stressing for these same two devices with 0Å Cu (H3.0) and with 20 Å Cu (H3.1), respectively. Figure 4.39 shows data for a device with the dry contact with 20Å Cu (H3.2). Figure 4.38 and Figure 4.39 are qualitatively and quantitatively similar indicating the wet and dry contact process have the same influence on recombination and V_{oc} degradation. Extrapolation to T = 0 K in Figure 4.38 and Figure 4.39 gave intercepts which decreased by ~0.1 V after stressing which is slightly less

than the decrease in V_{oc} at 300 K. This suggests a decrease in barrier height. The slopes of V_{oc} vs T were relatively unchanged with stressing indicating no change in the fundamental recombination mechanism.

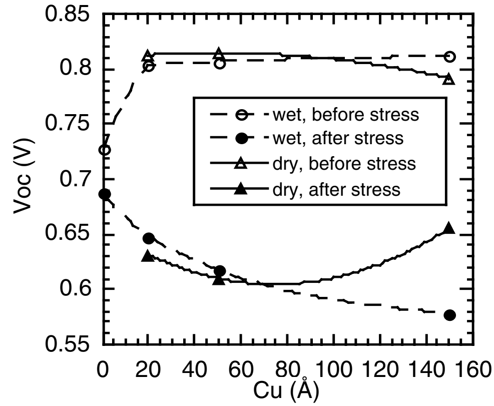


Figure 4.31 V_{oc} vs Cu thickness before and after stress for devices with wet or dry contacts.

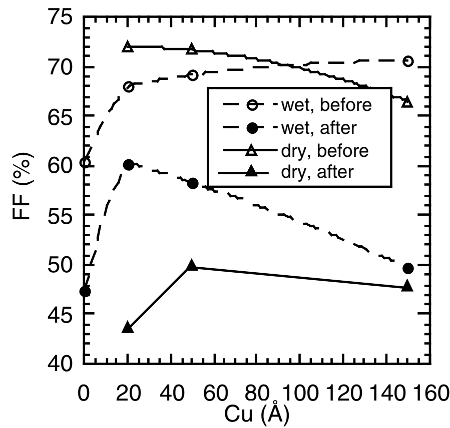


Figure 4.32 FF vs Cu thickness before and after stress for devices with wet or dry contacts.

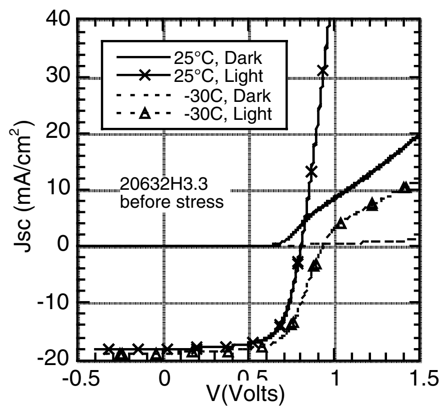


Figure 4.33 JV curves in light and dark at 25˚C and at -30˚C before stressing for device H3.3 with 50Å Cu and wet contact processing.

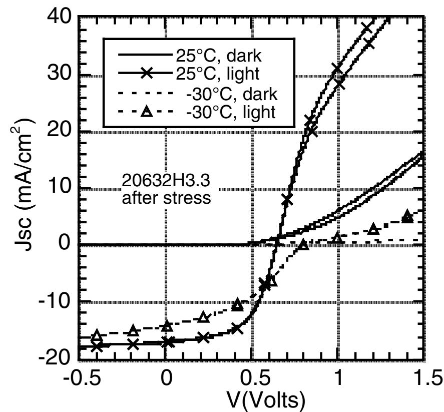


Figure 4.34 JV curves in light and dark at 25˚C and at -30˚C after stressing for same device as Figure 4.33

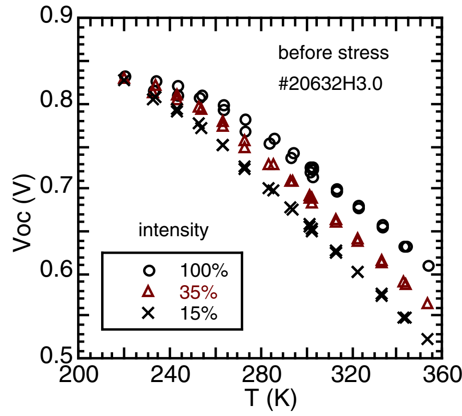


Figure 4.35 V_{oc} vs T at three intensities for device H3.0 with wet contact process and 0Å Cu, before stressing.

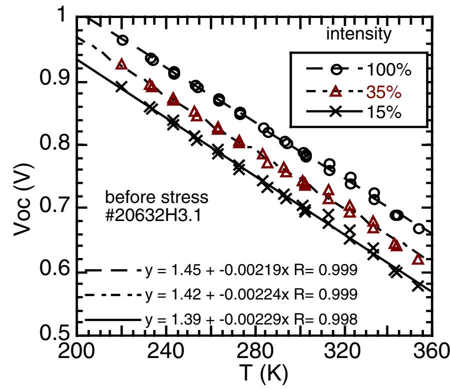


Figure 4.36 V_{oc} vs T at three intensities for device H3.1 with wet contact process 20Å Cu, before stressing.

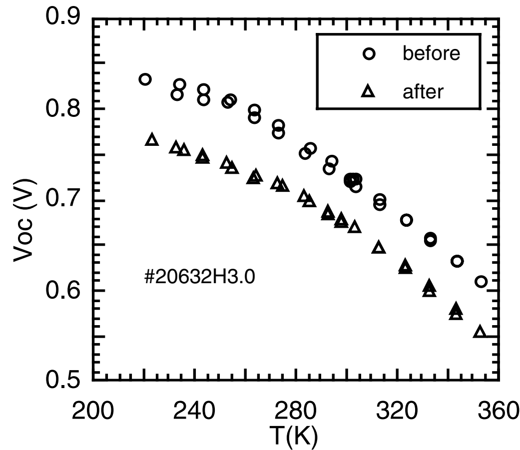


Figure 4.37 V_{oc} vs T for device H3.0 with wet contact process and 0Å Cu, before and after stressing.

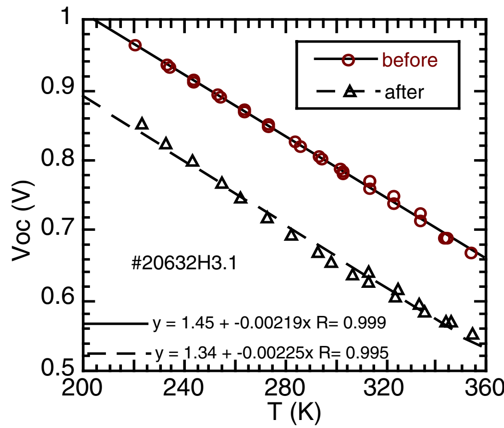


Figure 4.38 V_{oc} vs T for device H3.1 with wet contact process and 20Å Cu, before and after stressing.

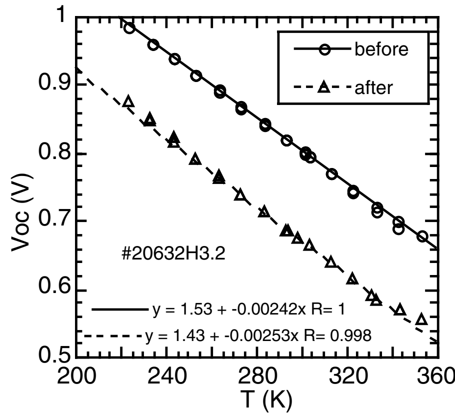


Figure 4.39 V_{oc} vs T for device H3.2 with dry contact process and 20Å Cu, before and after stressing.

Further stressing was performed to characterize the degradation of Cu-free devices. Devices from the same SCI plate were processed having the wet contact with and without the BDH etch, and having the dry contact without the BDH etch. The BDH etch leaves a Te layer >100 Å while without the BDH etch the Te layer is <100Å. Initial performance shown in Figure 4.40 of the devices with the standard wet contact process with or without BDH was comparable with V_{oc} ~0.74 V and FF ~58%. After stressing they had comparable V_{oc} ~0.68 V but very different FF (47% with BDH etch and 26% without BDH etch). Figure 4.41 shows that devices without the BDH etch develop extreme distortion of the JV curve. After stressing, the slope at open circuit, R_{oc}, was ~20 Ohm-cm^2 for the device with BDH etch but >200 Ohm-cm^2 for the devices without BDH etch, independent of whether they had wet or dry contact processing. Clearly, for devices without Cu, the surface preparation method does not significantly affect the initial light J-V performance. However, after stressing, the sample with BDH processing was less susceptible to blocking contact formation.

As before, degradation in V_{oc} for these three Cu-free devices is much less (~0.06 V) than typically found for devices with Cu layer (see Figure 4.31). The relatively smaller loss in V_{oc} after stressing is independent of the contact processing or surface etch. However, severe degradation in FF occurs even without Cu suggesting formation of a blocking contact is suppressed with sufficient Cu or Te, consistent with maintaining a p+ surface. The changes in J-V behavior due to stress seen in Figure 4.40 and Figure 4.41 suggest changes in non-copper doping sources such as oxygen, chlorine, and excess Te. Devices with insufficient Cu dopant will be more susceptible to presence of other doping species which may be less well controlled.

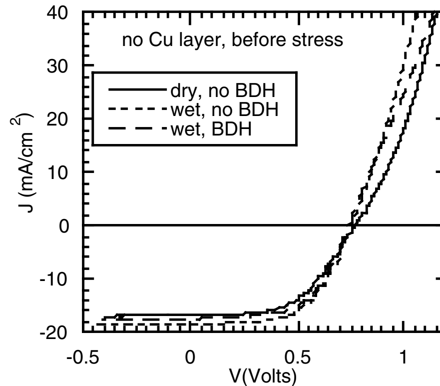


Figure 4.40 Illuminated JV curves before stressing for three devices without a Cu layer, having different back contact processing.

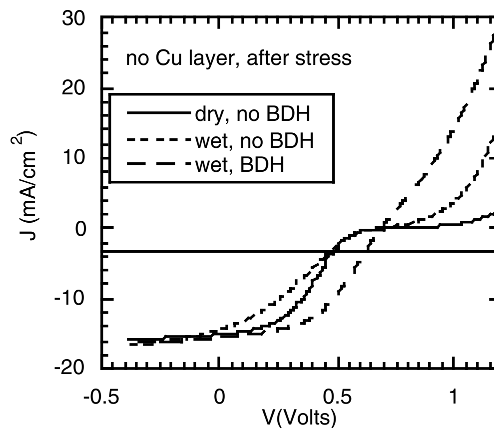


Figure 4.41 Illuminated JV curves after stressing fore three devices without a Cu layer, having different back contact processing.

4.4.2 IEC Stress Testing System

During this contract period a new stress testing system (Figure 4.42) was assembled and became operational. The system has 4 vacuum-compatible chambers for exposing devices to various controlled atmospheres, temperature, illumination intensity and electrical bias while monitoring the electrical performance. The chambers are pumpable down to 20 mT prior to stress. Then they are backfilled with the appropriate atmosphere. This is repeated several times to reduce moisture and O_2 before raising the temperature and beginning the stress study. Stressing can occur in an atmosphere of dry air, Ar, 2% H_2 in Ar, or vacuum. The chambers are 5 inches high and 6 inches in diameter and have two 6 inch diameter glass windows. Temperatures of 60-120°C are achieved with two 100 W halogen floodlamps mounted outside the chamber, one below providing solar cell illumination and one above providing additional heat if needed. Typically, we have adjusted the position of the bottom lamp to provide a J_{sc} of 1.2 suns for CdTe devices, which heats the devices to about 70-80°C. Accurate temperature control is obtained without affecting the solar cell illumination intensity by adjusting of the power to the top lamp. Devices can be electrically biased from reverse bias through the active power quadrant into forward bias. Bias in the power quadrant is provided using a bipolar source-sink power supply along with a variable series resistance (0-100 Ohms). Analysis of a large number of stressed and unstressed devices found that the ratio of V_{mp} to V_{oc} is ranges from 0.70 to 0.78. Therefore, we have selected to define "stressing at maximum power" as having an applied bias of 0.75 times $V_{oc.}$ This is adjusted during stress as V_{oc} degrades.

Each chamber can have up to four 1x1 inch pieces and four cells under bias. Unbiased cells are at V_{oc} by default. Thus, 16 cells can be biased and stressed at a time, with 4 each under 4 different conditions if desired. A computer controlled switching matrix has been interfaced to standard solar cell test hardware to allow in-situ JV sweeps during stress without removing the cells from the stress chamber. All subsequent stressing discussed here was performed in the new stress system.

Figure 4.42 The new IEC stress testing system showing the 4 chambers with glass windows and lamps, vacuum pump, gas handling system, and bias control panel.

4.4.3 Effect of Bias During Stress

Using the new stress test system, we have stressed several identically processed pieces of SCI glass/SnO_2/CdS/CdTe layers at 100°C, at 1.2 suns, in dry bottled air for up to 10 days. The layers were processed into cells with the IEC dry contact process with 50Å Cu and C paste contacts. One cell on each piece was biased, the other 3 cells were at V_{oc}. Applied biases were -0.5V, 0V (=J_{sc}), 0.75*V_{oc} (~V_{mp}), and J = -1.5*J_{sc} (V > V_{oc}). Initial values were typical, with V_{oc} = 0.79-0.81 V, J_{sc} = 18-20 mA/cm^2, and FF = 65 -71%. Figure 4.43 shows the light and dark JV curves after 10 days stress at several biases. The cell at forward bias of 1.5*J_{sc} had become unstable and shunted after 5 days and is not discussed further.

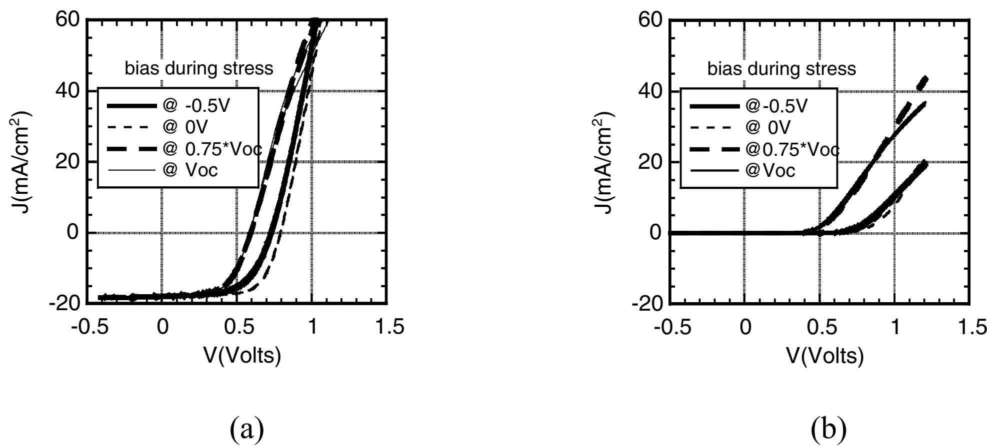


Figure 4.43 Light and dark JV of devices from pieces SCI#2435I3.5 through .8 after 10 days stressing at 100°C in light in air at biases of -0.5 V, 0 V, 0.75 V_{oc}, and V_{oc}. JV parameters before and after stress are given in Table 4.12.

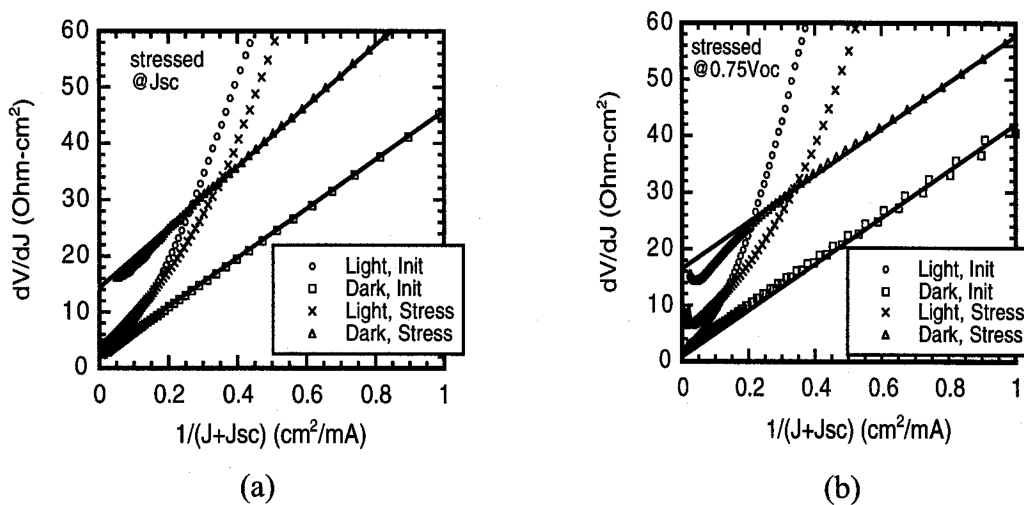


Figure 4.44 dV/dJ plots of JV data shown in Figure 4.43 for devices stressed at 0 V (I3.6-3) and at 0.75 V_{oc} (I3.7-3), respectively, before and after stressing.

Figure 4.43 indicates that the devices stressed at J_{sc} or -0.5 V degraded less than those at V_{mp} or V_{oc}. As Table 4.12 shows, the light JV performance of the device at stressed J_{sc} had *essentially no degradation*. Figure 4.44, however, shows that the dark diode properties changed significantly. The series resistance (from the intercept) in the dark increased from 2.0 to 14.4 Ohm-cm^2 and the A-factor (from the slope) increased from 1.7 to 2, but no curvature occurred. The curvature, or bending upward at low values of 1/J, is associated with the blocking contact. The devices stressed at V_{mp} or V_{oc} were essentially indistinguishable after stressing, with losses in V_{oc} of 0.20 V and losses in FF of ~6%. Figure 4.44(b) shows a similar increase in dark series resistance, from 1.9 to 17.0 Ohm-cm^2 as for the device stressed at J_{sc}, but the A-factor of 1.5 is unchanged with stress. Note the curvature in both the light and dark data after stressing. Figure 4.44 indicates that dark and light diodes change differently with stress, and that stressing at J_{sc}

may suppress formation of the blocking contact. These results differ from those of the CSU group [14] who also stressed devices on SCI material (with SCI's X3 contact). They found stressing at maximum power was more stable than at J_{sc}; we find it is significantly worse. But both groups find stressing at $V < 0$ is slightly worse than at $V = 0$. Our results should not be considered generally applicable to all CdTe since they were obtained on devices from only one contact process. But they clearly indicate a strong increase in degradation for cells biased between $V = 0$ and $V = Vmp$ (~0.75 V_{oc}). This is discussed further below.

Table 4.12 JV parameters for devices before (initial) and after stressing at 100˚C for 10 days at 4 bias conditions.

cell number	Bias condition	V_{oc} (Volts)	J_{sc} (mA/cm^2)	FF (%)	R_{oc} ($Ohm\text{-}cm^2$)	G_{sc} (mS/cm^2)
2435I3.5-1	initial	0.806	18.6	67	5	1
	-0.5V	0.731	18.1	59	7	2
2435I3.6-3	initial	0.793	19.2	67	5	1
	0V	0.792	18.1	67	6	1
2435I3.7-3	initial	0.795	19.0	66	5	2
	0.75 V_{oc}	0.594	17.8	60	7	1
2435I3.7-2	initial	0.787	19.0	65	5	1
	V_{oc}	0.588	18.0	60	7	1

4.4.4 V_{oc} Degradation and Recovery of CdTe Devices

Our previous studies [16] of stressing devices on SCI CdTe material with IEC's wet or dry contact process at V_{oc} (unbiased) indicated that V_{oc} degraded 0.1-0.2 V over 5-6 days. This was observed on devices which received a wide range of contact processing at IEC. The rate of this decrease and whether it saturated with time was unknown since at that time we could not monitor V_{oc} during stress. This is now possible with the new stress system. In order to help identify the mechanism of the V_{oc} degradation, devices biased at $V = V_{oc}$, V_{mp} and J_{sc} were closely monitored during a 10 day degradation study. The stress temperature was 100°C, light intensity was 1.2 suns, ambient was dry air, and V_{oc} was measured at the stress temperature. The devices were two identically processed pieces of SCI CdTe (2435I3.10 and .12) cut from a larger plate. They received a dry contact process at IEC with 50Å Cu and C paste. Initial performance was typical with $V_{oc} = 0.80$ V and FF = 68-70%.

Figure 4.45 shows the degradation behavior of V_{oc} at 100°C for three devices. The V_{oc} was monitored as the chamber was heating up to 100°C (~30 minutes). At the end of that time, the device biased at V_{oc} had already lost 0.05 V compared to the others. Figure 4.45 shows that the V_{oc} of the device biased at J_{sc} remained very stable at about 0.64 V. After 7 hours, it was biased briefly at Voc for 30 minutes, leading to a 30 mV decrease in V_{oc} during that short time. The device was then returned to bias at J_{sc}. Note that V_{oc} began to recover upwards towards the

original value of ~0.64 V. The V_{oc} for two forward biased devices, being held at V_{oc} and at 0.75 V_{oc}, degraded at essentially the same rate. Then at 10 hours, the device which had been biased at 0.75 V_{oc}, was switched to being biased at J_{sc} instead. Figure 4.45(b) is a plot of V_{oc} vs log time (stress time at 100°C) for these same three devices. Note the logarithmic decrease in V_{oc} followed by a similar increase after 10 hours when it was switched from V_{oc} to J_{sc} bias. This data suggests the loss of V_{oc} is metastable and may be partially recovered. The V_{oc} of the device biased at V_{oc} continues to degrade after 6 days, although at slower rate after the first several hours.

This data shows several important features regarding loss of V_{oc}. First, the degradation for devices biased at V_{oc} is extremely rapid. Second, devices biased at V_{mp} or V_{oc} degrade at similar rates, in contrast to results from others that find V_{mp} a much more stable condition. Finally, losses in V_{oc} are partially recoverable by biasing the device at J_{sc}, except recovery at J_{sc} requires at least an order of magnitude longer than the degradation at V_{oc}.

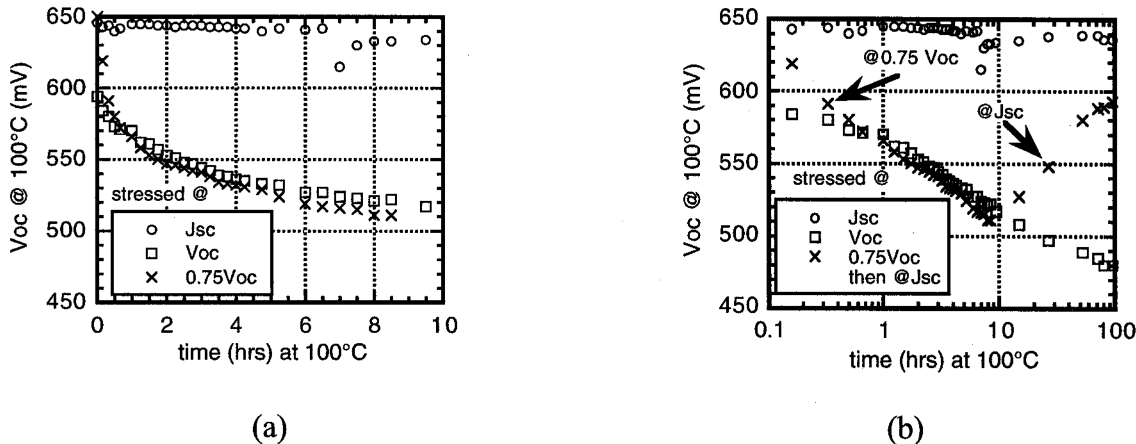


Figure 4.45 Linear and log time dependence of Voc measured at 100˚C for three CdTe devices. One device was biased at J_{sc} except for 30 minutes between 6.5 and 7 hours, one was at V_{oc} the entire time, and one was biased at 0.75 V_{oc} for 10 hours, then biased at J_{sc}.

Since it appeared that losses in V_{oc} could be partially recovered at 100°C in a few hours, many devices that were stressed in the past year were retested following 6-12 months of dark storage in air at room temperature. Typically, there was a 30-60 mV *increase* in V_{oc} and 2-4% *decrease* in FF, and no consistent change in J_{sc}. Often, the stress-induced JV curvature beyond V_{oc} was reduced and a more linear forward bias region was restored.

Further attempts were made to restore degraded devices. After stressing for 10 days, cooling to room temperature, and JV testing, some cells were returned to the stressing system and biased with reverse bias of 0V, -0.5 or -1 V in dark or light, at 25, 80 or 100°C for several days. We reasoned that if degradation occurred when forward biased in the light (at V_{oc} or V_{mp}), recovery might occur if reverse biased, either in presence of carrier photogeneration or not. All these attempts were unsuccessful. We conclude that once the devices are brought to room

temperature, the source of the degradation is “frozen in” and cannot be annealed under similar conditions over periods of days.

In conclusion, degradation in V_{oc} is very rapid for these devices when stressed at 100°C at or near V_{oc}, losing 15% of initial V_{oc} in a few hours, while V_{oc} is relatively stable for devices stressed at J_{sc}. Devices biased at J_{sc} show little change in the light JV characteristics but show degradation in their dark JV, with an increase in series resistance being the dominant loss. Devices biased at $V_{mp} \sim 0.75$ V_{oc} show a similar increase in dark series resistance but also evidence of blocking contact formation in the light and dark diode, resulting in lower FF. Switching the bias from V_{oc} to J_{sc} at 100°C after several hours recovers more than half of the initial V_{oc} loss, but requires several days. Storage in the dark at room temperature also helps recover losses in V_{oc} and in forward bias diode current due to stressing but takes many months. When cells have been degraded at forward bias, no recovery is seen from exposing them to reverse bias either at 25 or 100°C, at least for periods of days. Taken together, these results suggest that degradation in V_{oc} is partially a metastable process, perhaps related to capture at or emission from gap states created during stress, and that recovery occurs much more slowly than the degradation. It is unlikely that simple movement of Cu ions in the presence of a field at elevated temperatures can explain these changes.

4.4.5 Effect of Stress Ambient on Stability

Devices from all previous IEC stress studies were stressed in air, either room air (uncontrolled humidity) or bottled dry air (as in Sections 4.4.3 and 4.4.4). Section 4.3.3 discusses the chemical and structural changes occurring at the contact of devices stressed in air. In this section we describe results from stressing under bias in different atmospheres. This will provide crucial understanding of the chemical nature of the changes occurring in the device. It is possible to speculate about several possibilities. When stressed in air, the Cu or Te at the back contact could form oxides, or O_2 could diffuse down grain boundaries. When stressed in H_2, the Cu or Te oxides could be reduced, thus freeing more elemental Cu to diffuse down the grain boundaries. This would eventually shunt the junction and leave the back contact Cu-poor, leading to a highly resistive contact.

Devices were processed at IEC from a plate of FS CdS/CdTe material (746B3). They all received 6 nm of Cu and a C paste contact similar to devices described above. Efficiencies ranged from 10.5-11% before stress. Pieces were stressed at 100°C for 10 days in either Ar, H_2/Ar, or dry air. In each atmosphere, one cell each was at –0.5V, J_{sc}, V_{mp} and V_{oc}. No cells were biased beyond V_{oc} as we have found that to cause even greater degradation than bias at V_{oc} and often to cause shunting. The V_{oc} was monitored in-situ during the study.

Results before and after stress are shown in Table 4.13. Results from this new plate of FS CdTe are similar to other plates. The efficiency after stress ranges from 5.5 to 9%, excluding one obviously shunted cell (B3.2.3). Figure 4.1 shows the ratio of change in efficiency and V_{oc} for each bias condition. The largest degradation occurred at V_{oc} in all ambients. Interestingly, the next largest degradation was for –0.5V. Stress in H_2/Ar has the least bias dependence. It degrades more at J_{sc} but less at V_{oc} (i.e., changes appear flatter with respect to electrical bias). Figure 4.2 shows V_{oc} at stress (100°C) for each ambient vs log of time. Compared to other stress biases, degradation at V_{oc} is much more rapid and distinct for stressing in Ar or air. Cells

developed curvature in light and dark for stress at V_{oc} for all ambients. Cells in air became shunted in light and dark.

We make a potentially useful observation regarding the influence of bias , using the device stressed in Ar as an example. When stressed at V_{mp} (B3.1.3), the bias voltage was nearly the same voltage as for the cell at V_{oc} (B3.1.4) because B3.1.3 is biased at 75% of V_{oc}, while the V_{oc} for B3.1.4 has degraded to about 75% of the original value. For example, at 140 hours, B3.1.3 was biased at V_{mp} = 0.46V while B3.1.4 was at V_{oc} = 0.45V. Yet they had dramatically different degradation rates (Figure 4.2(a)). This suggests it is not the bias *per se* but the recombination or charged particle (current) flow that determines the degradation. The device at V_{oc} would have much greater recombination and majority carrier injection but no current flow through its contacts.

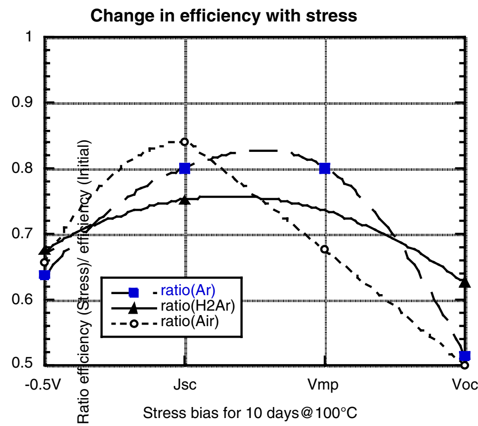
These results have shown that degradation occurs in three ambients of Ar, dry air, and H_2/Ar. Degradation for stress at V_{oc} is worst in all three ambients, leading to curvature beyond V_{oc} indicating formation of a blocking contact. Stress in Ar and air has common bias dependencies with stress at reverse bias or V_{oc} being worse than at J_{sc} or V_{mp}. This is confusing since V_{oc} has the maximum recombination and weakest field in direct opposition to –0.5V. Stress in H_2/Ar has least bias dependence. This result has been confirmed in two other IEC studies. Stress at V_{oc} creates blocking contact in all three ambients.

Table 4.13 JV test results from stressing in Ar, H_2/Ar, or dry air for 10 days at 100˚C at different bias. CdS/CdTe pieces were from First Solar plate 746B3 with IEC contacts.

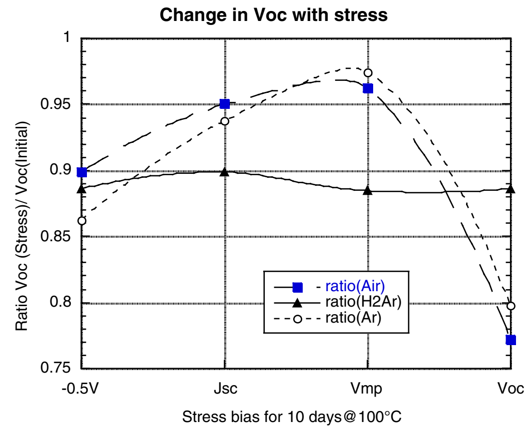
Device #	Stress Condition	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff	R_{oc} (Ω/cm^2)	G_{sc} (mS-cm^2)	Comment
B3.1.1	Initial	0.80	18.5	71.1	10.5	4.9	0.5	
	Ar, -0.5V	0.69	16.7	57.9	6.7	8.4	2	
B3.2.1	Initial	0.79	19.2	72.7	11.1	4.4	0.5	
	H_2/Ar, -0.5V	0.70	18.3	58.3	7.5	7.5	1.5	
B3.3.1	Initial	0.79	18.9	72.0	10.8	4.6	0	
	Dry air, -0.5V	0.71	17.5	57.3	7.1	7.9	2	
B3.1.2	Initial	0.80	19.5	71.1	11.1	4.7	0.5	
	Ar, J_{sc}	0.75	18.0	65.2	8.9	6.3	1	
B3.2.2	Initial	0.79	19.4	70.6	10.9	4.4	0.5	
	H_2/Ar, J_{sc}	0.71	18.7	61.3	8.2	6.0	1	
B3.3.2	Initial	0.80	19.5	69.2	10.7	4.6	0.5	
	Dry air, J_{sc}	0.76	18.5	64.0	9.0	6.5	1	
B3.1.3	Initial	0.79	19.5	69.0	10.6	5.0	0	
	Ar, V_{mp}	0.77	17.5	63.0	8.5	6.8	1	A
B3.2.3	Initial	0.78	18.6	71.3	10.4	4.7	0.5	
	H_2/Ar, V_{mp}	0.69	17.5	34	4.0	11	15	B
B3.3.3	Initial	0.79	18.5	71.7	10.5	4.6	0	
	Dry air, V_{mp}	0.76	17.4	53.8	7.1	7.7	6	B
B3.1.4	Initial	0.79	20.8	66.0	10.9	4.7	0.5	
	Ar, V_{oc}	0.63	16.3	54.5	5.6	9.7	2.5	A
B3.2.4	Initial	0.79	19.4	70.3	10.7	4.6	0	
	H_2/Ar, V_{oc}	0.70	17.9	54.1	6.7	8.9	2.5	A
B3.8.1	Initial	0.79	18.9	72.6	11.0	4.4	0	
	Dry air, V_{oc}	0.61	16.8	53.4	5.5	8.5	5.5	A,B

A = curvature in dark and light

B = dark and light very shunted (note larger value of Gsc)

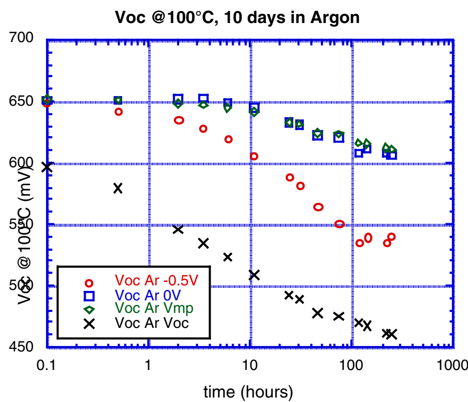


(a)

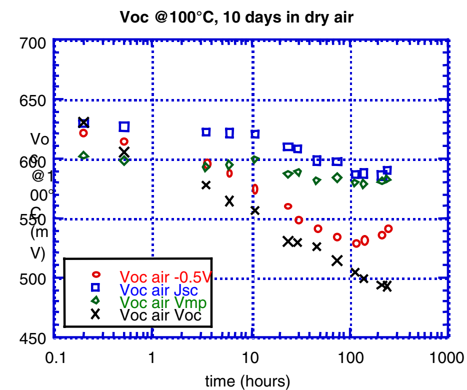


(b)

Figure 4.46 Relative change in V_{oc} and efficiency with electrical bias for devices stressed at 100˚C for 10 days in 3 different ambients.



(a)



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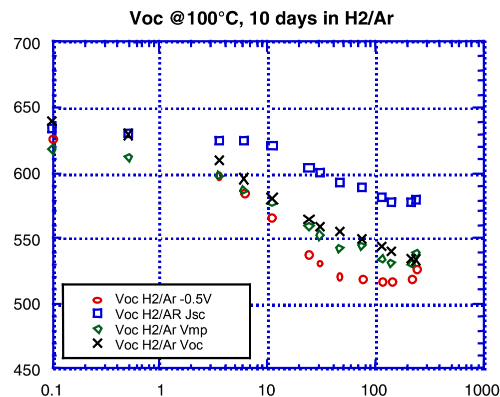

(c)

Figure 4.47 V_{oc} at 100˚C during stress for 10 days in dry air, Ar, or H_2/Ar. In each ambient, cells were at -0.5V, J_{sc}, V_{mp}, or V_{oc}.

We now discuss results from stressing devices with different Cu thickness under bias in H_2/Ar (4% H_2). Pieces of CdS/CdTe from First Solar plate 2435F2 were contacted at IEC, receiving Cu layers with thicknesses of either 30Å (F2.6) or 60Å (F2.10). They were stressed for 8 days at 100°C in H_2/Ar under illumination at biases of 0 Volts, V_{mp}, and V_{oc}.

The devices had initial efficiencies of 10 to 11% and degraded to 5.5 to 6.5% after stressing. Although there was no significant difference in degraded performance between cells with 30 or 60 Å of Cu, there was a dramatic increase in the linear dark shunt characteristic for devices with 60 Å Cu as seen in Figure 4.48. This suggests that exposure to a reducing atmosphere at 100°C allows free Cu to diffuse along grain boundaries creating shunt paths across the junction. This indicates the importance of understanding the chemistry of the back contact during stress.

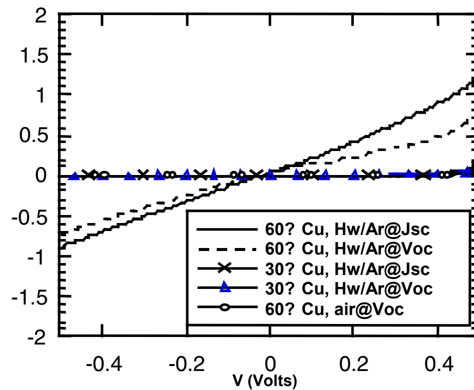

Figure 4.48 Dark JV behavior at low voltage for devices stressed in different atmospheres and biases with 30 or 60 Å Cu. Note large shunt develops only for devices stressed in H_2/Ar with thicker (60 Å) Cu layer.

5. ABSTRACT

This report describes results achieved during phase I of a three-phase subcontract to develop and understand thin film solar cell technology associated to $CuInSe_2$ and related alloys, a-Si and its alloys and CdTe. Modules based on all these thin films are promising candidates to meet DOE long-range efficiency, reliability and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for the development of viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development of improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to illumination, temperature and ambient and with respect to device structure and module encapsulation.

6. REFERENCES

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REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)

2. REPORT DATE
August 2000

3. REPORT TYPE AND DATES COVERED
Annual Report; 24 August 1998–23 August 1999

4. TITLE AND SUBTITLE
Optimization of Processing and Modeling Issues for Thin Film Solar Cell Devices Including Concepts for the Development of Polycrystalline Multijunctions; Annual Report; 24 August 1998–23 August 1999

5. FUNDING NUMBERS
C: ZAK-8-17619-33
TA: PV005001

6. AUTHOR(S)
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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Institute of Energy Conversion
University of Delaware
Newark, Delaware 19716-3820

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
NREL/ SR-520-28783

11. SUPPLEMENTARY NOTES
NREL Technical Monitor: B. von Roedern

12a. DISTRIBUTION/AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

This report describes results achieved during phase I of a three-phase subcontract to develop and understand thin-film solar cell technology associated to $CuInSe_2$ and related alloys, a-Si and its alloys, and CdTe. Modules based on all these thin films are promising candidates to meet DOE long-range efficiency, reliability, and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for the development of viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial-scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development of improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to illumination, temperature, and ambient and with respect to device structure and module encapsulation.

14. SUBJECT TERMS
photovoltaics ; thin film solar cell devices ; processing and modeling ; polycrystalline multijunctions ; $CuInSe_2$-based solar cells ; a-Si-based solar cells ; CdTe-based solar cells ; CdS/CdTe solar cells ; Thin Film Partnership Program

15. NUMBER OF PAGES

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL