Advanced Processing of CdTe- and CuIn$_x$Ga$_{1-x}$Se$_2$- Based Solar Cells

Phase I Report

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Subcontractor Report

NREL

National Renewable Energy Laboratory

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PART I: CDTE

1.0   INTRODUCTION

The main tasks of this project include the development of simplified processing for the fabrication of high efficiency CdTe solar cells, studies on the long term stability of CdTe devices, development of alternative transparent conducting oxides, window layers, and back contacts.

The development of simplified processing has been focusing on limiting the deposition temperatures for the fabrication of CdTe/CdS solar cells below 550°C. To this end the CSS of CdTe and CdS are being optimized to meet these requirements. In the case of CdTe the deposition temperature has been lowered below 500°C while maintaining respectable performance. Another process being studied/developed is $CdCl_2$ treatment using vapors of $CdCl_2$ instead of the typical solution (wet) based process. Near state-of the art solar cell performance has been achieved using this process. Reproducible and robust vacuum deposited back contacts are also being developed and devices with V_{OC}'s in excess of 830 mV and ff's greater than 70% have been fabricated.

Long term stability and the identification of degradation mechanisms is another major task for this project. To address this issue CdTe solar cells are being stressed at several temperatures and their performance is being monitored. Several devices have already been stressed for over 1400 hours. Light soaking experiments have also been initiated during this phase. Although the back contact has been associated with most degradation observed in CdTe devices to date, the early results obtained at USF suggest that changes are taking place at the CdTe junction while the back contacts exhibit minimal degradation (if any).

Work on alternative TCO's and window layers has included materials such as ZnO, ZnSe, and CdO. Transparent conductors are primarily investigated to determine whether their electro-optical properties can be improved over commonly used SnO_2 and ITO films.

All solar cells are characterized by standard techniques that include light and dark J-V, C-V, C-f, and spectral response measurements. The basic junction parameters such as diode factor (A) and reverse saturation current (J_O), are measured when appropriate and are used to explain solar cell behavior and optimize processing conditions. The optical, electrical, and structural properties of thin films are characterized using resistivity, optical transmission, SEM, XRD, and PL measurements.

The University of South Florida continues to participate in the CdTe National Team's activities, by addressing some of the common Team Tasks and often processing devices and films for other universities or industrial partners. USF also often collaborates with professor Roy Gordon of Harvard University on issues related to transparent conductors.

2.0 SOLAR CELL FABRICATION PROCEDURES/OPTIONS

Several processes are being utilized for the fabrication of CdTe junctions and solar cells. The table shown below outlines the various materials/processes currently being studied under this program. The "Baseline Process" refers to processes that have already been optimized and are being used as a benchmark for new processes and materials.

TABLE 1: Outline of solar cell processes and materials.

	Baseline Process	Alternative Materials/Processes		
Substrate	Borosilicate or Soda Lime (LOF)			
TCO	SnO_2 (bilayer)	ZnO rf sputtering	CdO CVD	
Window	CdS (CBD or CSS)	ZnSe CSS	CdO CVD	
CdTe	High Temperature: (>580°C) (HT)	Intermediate Temp.: (~550°C) (IT)	Low Temp.: <500°C (LT)	
CdCl₂ Heat Treatment	Wet Process	$CdCl_2$ Vapors	Evaporation	
Back Contact	Doped Graphite: HgTe:Cu	Cu_xTe rf sputtering	Sb_2Te_3 rf sputtering	$ZnTe/Cu_xTe$ rf sputtering

3.0 TCO's AND WINDOW LAYERS

3.1 CSS CdS

It has been previously reported that the performance of solar cells fabricated entirely by the close spaced sublimation has exceeded the 15.0% level for cells fabricated on borosilicate glass, and the 14.0% level for cells fabricated on soda lime glass (1). The utilization of the same technology for the deposition of both semiconductors is very attractive for large area manufacturing applications. Two of the key process parameters in achieving state of the art performance for all-CSS devices were the ambient used for the deposition of the CSS CdS films and in some cases the post deposition heat treatment of these films.

Since the properties of the CSS-CdS films appear to have considerable influence on device performance, several CSS-CdS films were deposited on glass substrates in order to study their electrical properties. The as-deposited CdS films are typically very

resistive and four point probe resistivity measurements cannot be carried out. Instead, the resistivity of these films was measured by applying four indium contacts (typically 3 cm wide). A power supply was used to pass current through the two outer contacts and the voltage was measured across the inner two. All measurements were carried out in a copper screened enclosure to minimize noise. The resistivity was also measured under AM1.5 conditions using an ELH lamp.

3.11   Resistivity of As-deposited CSS-CdS
Table 2 shows the dark and light resistivity for several films deposited in inert or O_2 ambient. Although run to run variations exist the data suggests that the resistivity (dark and light) of CdS films deposited in the presence of oxygen is consistently 2-3 times higher than that of films deposited in inert ambient. A simple explanation for this could be the fact that films deposited in a He/O_2 ambient consisted of smaller grains and therefore a larger number of grain boundaries present increased the lateral resistivity of the films (1). However, it is speculated that in addition to the effect of the grain boundaries, that the bulk resistivity of the films deposited in O_2 is also higher. Photoluminescence measurements indicated that the use of O_2 leads to a reduction in S vacancies, which are responsible for the n-type conductivity of the CdS films (2).

TABLE 2. Dark and light resistivity of CSS CdS films.

Run #	Ambient	Dark ρ, (Ω-cm)	Light (AM1.5) ρ, (Ω-cm)
4	He	3.2×10^8	5.5×10^3
5	He	2.1×10^8	7.1×10^3
6	He	1.4×10^8	4.7×10^3
31	He/O_2	4.8×10^8	1.1×10^4
32	He/O_2	4.1×10^8	1.3×10^4
33	He/O_2	4.5×10^8	1.0×10^4

3.1.2   Resistivity of CSS-CdS Heat treated in H_2
Some of the samples listed in table 2 were heat treated in H_2 in the temperature range from 200 to 450°C. The dark and light resistivity for these films is shown in figure 1 (the values corresponding to T=25°C are for as-deposited films). In all cases the resistivity (dark and light) is higher for films deposited in O_2. For annealing temperatures in the range of 200-350°C the resistivity decreases but appears to level off beyond 350°C.

Since the conductivity (resistivity) is given by

$$\sigma = \frac{1}{\rho} = nq\mu$$

the observed decrease in resistivity could be attributed to an increase in the carrier concentration or the mobility of the CdS. For example, the heat treatment could cause an increase in the carrier concentration as a result of an increase in the sulfur vacancies. In

this case the conductivity activation energy should remain constant (3). It is also possible that the intergrain barrier height can decrease, as a result of the heat treatment, leading to an increase in the effective mobility. In this case the activation energy should decrease (3). In order to determine which mechanism is responsible for the observed changes in the resistivity of the CSS-CdS films, the resistivity (conductivity) activation energy was approximated

Figure 1. Dark and light resitivity for CSS-CdS films deposited in He and O₂ ambient.

from a plot of *Ln(ρ) vs. 1/T*. The resistivity as a function of temperature for several CSS-CdS films annealed in H₂ is shown in fig. 2. The activation energy for the as-deposited films and those annealed at 250°C is found to be approximately 0.82 eV. For films annealed at higher temperatures the activation energy decreases to 0.63 and 0.49 eV for 300 and 350°C respectively. This behavior favors a mobility activated resistivity (conductivity) model. For this model to be valid, the intercept of the plots shown in fig. 2 must be constant. Calculation of the intercept for several as-deposited films indicated that this was essentially constant, however, the intercept for H₂ annealed films exhibited some scattering. The conductivity for grain barrier controlled mobility is given by:

$$\sigma = (\frac{nq^2 d_g v}{kT})\exp(-q\varphi_b / kT)$$

where

d_g is the grain width,
$q\varphi_b$ is the barrier height, and
v is the thermal velocity.

The effective mobility $\mu*$ is given by:

Figure 2. Temperature dependence of resistivity for as-deposited and H₂ annealed CdS films.

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$$\mu^* = (\frac{qd_g v}{kT})\exp(-q\varphi_b / kT)$$

Since adsorbed oxygen is a common source of negative charge at the CdS surface, and H_2 annealing is an effective way of removing it, it is suggested based on the above discussion that the effect of H_2 annealing is removal of adsorbed oxygen and the lowering of the intergrain barrier.

The above model is based on the assumption that the average grain size is less than the mean free path in the grain, and therefore grain boundary scattering dominates. However, if this assumption is not valid then the effective mobility has its own characteristic temperature dependence as given by:

$$\mu^* = \mu_g(T)\exp(-q\varphi_b / kT)$$

where
μ_g is the mobility of the bulk CdS.

This may explain some of the observed variations in the intercept of the H_2 annealed samples, and suggests that additional scattering mechanisms are present. It should also be noted that although the above results provide some insights on the changes in the CdS films *prior* to the CdTe deposition, it is still critical to understand and study their properties *after* the entire solar cell structure is complete.

3.1.3   CdS Carrier Concentration
The low limit of the uncompensated donor concentration in CSS-CdS was estimated assuming full grain depletion. Figure 3 shows a fully depleted grain structure. The relationship between the space charge region and barrier height is given by:

$$W = \left(\frac{2\varepsilon V_{bi}}{q(N_D - N_A)}\right)^{1/2}$$

which can be rewritten in terms of the barrier height E_a and the grain size d_g:

$$(d_g / 2) = \left(\frac{2\varepsilon E_a}{q(N_D - N_A)}\right)^{1/2}$$

Using the above expression the low limits for the donor concentration in CdS films have been calculated and are shown in table 3.

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TABLE 3. **Calculated donor concentration vs. barrier height.**

E_a; (eV)	$(N_D - N_A)$; (cm^{-3})
0.82	1.3×10^{14}
0.49	7.7×10^{13}
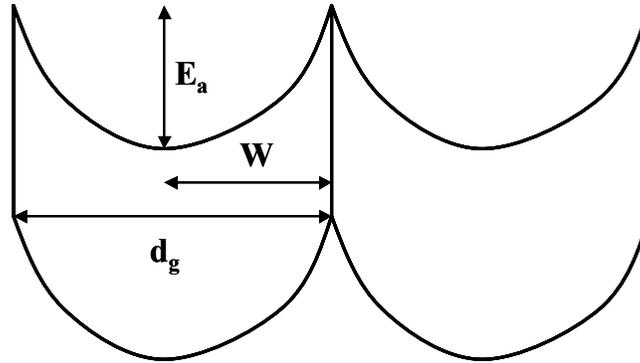
Figure 3. Energy band diagram for fully depleted grains.

3.2   All-CSS CdTe/CdS Solar Cells

All CSS devices are being fabricated on borosilicate and soda lime glass. Recent work on soda lime glass has become very challenging. Problems affecting film uniformity and believed to be associated with the glass substrates have been encountered. The samples after the deposition of SnO_2 and/or CdS appear spotty with large areas of non-uniformities. This problem has persisted regardless of the various cleaning procedures tried in an effort to determine whether the observed non-uniformities were related to substrate cleaning. The focus for all-CSS devices has shifted to 7059 glass substrates until the non-uniformities observed in films on soda lime substrates are eliminated.

3.2.1   The role of Oxygen

As discussed previously the use of oxygen for the deposition of CSS CdS films resulted in improved device performance (higher V_{CO}'s and ff's). The impact of oxygen on device performance is obvious but not fully understood yet. It has been previously speculated that the improved performance was a result of the smaller grain size of the $CSS\text{-}CdS(O_2)$ films, which leads to more interdiffusion as indicated by the behavior of the spectral response near the CdS absorption edge. Based on measurements of film properties carried out to date the following have been concluded on the effect of oxygen:

- it affects film composition; in some cases CdO was detected; the presence of CdO did not degrade cell performance.

- it affects gap states in CdS (based on PL measurements); PL transitions associated with sulfur vacancies have been found to decrease as a result of O_2 incorporation. These may influence among others the current transport at the CdTe/CdS interface.
- it affects the grain size of the films; modifies the nucleation process resulting in smaller grains.
- it yields films with higher resistivity (presumably due to the smaller grain size and a reduction in the S vacancies)

To further investigate the influence of O_2 on device performance, a series of devices were fabricated using CSS CdS films deposited in inert ambient, but annealed in O_2 ambient prior to the CdTe deposition. Figure 4 shows the V_{OC} and ff as a function of the CdS thickness (the CdS thickness is estimated based on transmission measurements; the error associated with these measurements is ±50Å). As these results suggest, the solar cell characteristics of devices fabricated with CdS deposited in inert ambient and subsequently annealed in O_2 are very similar to those obtained for films deposited in the presence of oxygen. Spectral response measurement of these cells exhibited a very soft roll over at 600 nm suggesting that some intermixing between the CdTe and CdS takes place. However, it should be mentioned that no apparent change in the grain size of the films was noticed, therefore the smaller grain size associated with CSS-CdS films deposited in oxygen is not the only reason intermixing takes place. It is possible that oxygen annealing modifies the surface of the CdS films prior to the CdTe deposition resulting in an improved CdTe/CdS interface. Only small CdS thicknesses were used in these experiments since emphasis is placed on increasing the blue response of CdTe/CdS solar cells. Similar experiments using different annealing conditions are underway to determine a set of "optimum" process conditions and further address the role of O_2 and other agents that may affect device performance.

Figure 4. V_{OC} and ff vs. the thickness of CSS CdS.

3.3 Zinc Oxide

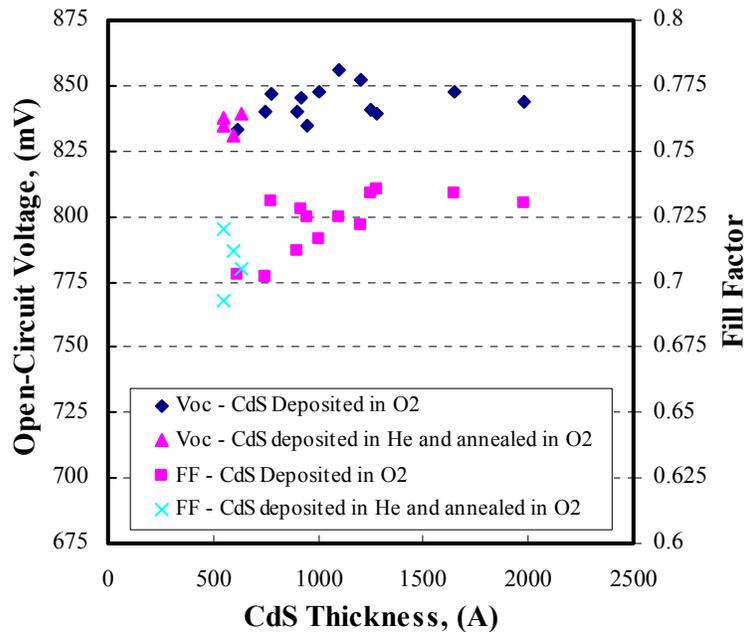It was reported in a previous report that ZnO:Al films prepared by rf-sputtering were being investigated as a candidate to replace SnO_2 (1). The difficulty in using ZnO:Al was

the thermal instability of this material at elevated temperatures and in particular in the presence of O_2. As previously reported the resistivity of ZnO increased considerably during the solar cell fabrication process, especially when O_2 was used during a particular processing step (i.e. CSS of CdS). As already mentioned above solar cell performance is enhanced if CSS-CdS films are deposited in the presence of oxygen. As a result of the increase in the ZnO resistivity the fill factors of CdTe/CdS/ZnO solar cells degrade due to high series resistance. Therefore, the instability of ZnO under these processing conditions appears to be incompatible with the currently optimized USF baseline process. One way to overcome this problem is to improve the performance of solar cells fabricated with CSS CdS that has been deposited at relatively low temperatures in inert ambient, and CSS CdTe also deposited at low temperatures.

All solar cell results (CdTe/CdS/ZnO) previously discussed were for devices fabricated on doped ZnO (i.e. ZnO:Al). Another set of experiments carried out during this phase dealt with the utilization of bi-layer ZnO films, since the use of a resistive layer on top of the conductive TCO has been found to enhance solar cell performance. Table 4 shows the performance of solar cells fabricated on bi-layer ZnO (the CdS for these devices was deposited in a 10% O_2 ambient). Typical solar cell parameters for devices fanbricated on ZnO:Al were: V_{OC}'s in the range of 780-820 mV and ff's up to 67%. As the results suggest the open-circuit voltages obtained for these devices are higher than all devices previously fabricated on ZnO by 15-25 mV. However, the ff's and J_{SC}'s of these devices are considerably lower than those of cells fabricated on ZnO:Al films. The low ff's and J_{SC}'s are due to significantly high series resistances in these devices. It therefore appears that the resitivity of the bi-layer ZnO films increases more than that of the single ZnO:Al layer. These results point to the significance of the bilayer TCO structure, but also the difficulties associated with incorporating ZnO in CdTe devices.

TABLE 4. Solar cell parameters for CdTe/CdS/bi-layer ZnO devices.

V_{OC}, (mV)	FF, (%)	J_{SC}, (mA/cm^2)
838	30.5	15.7
826	30.1	14.5
838	29.9	12.6
835	30.6	13.5

A summary of the performance of CdTe/CdS solar cells fabricated on ZnO is shown in fig. 5 where the open-circuit voltage and fill factor are plotted vs. processing conditions (the bars indicate high, low, and average values). As the data in these figures suggest the open-circuit voltage improves from left to right while the ff degrades. Typically, the performance of solar cells fabricated on conventional SnO_2 bi-layer TCO's using the processing variations shown in fig. 5 improves from left to right. Although this is true for the V_{OC} of CdTe/CdS/ZnO solar cells their ff's clearly degrade as a result of the increase in the resitivity of ZnO. It can therefore be concluded that ZnO films are incompatible with the currently optimized USF processing schemes. However, it is suggested that these films could be utilized with other processes that do not utilize high temperatures ($\geq 600°C$) and/or oxygen during subsequent fabrication steps.
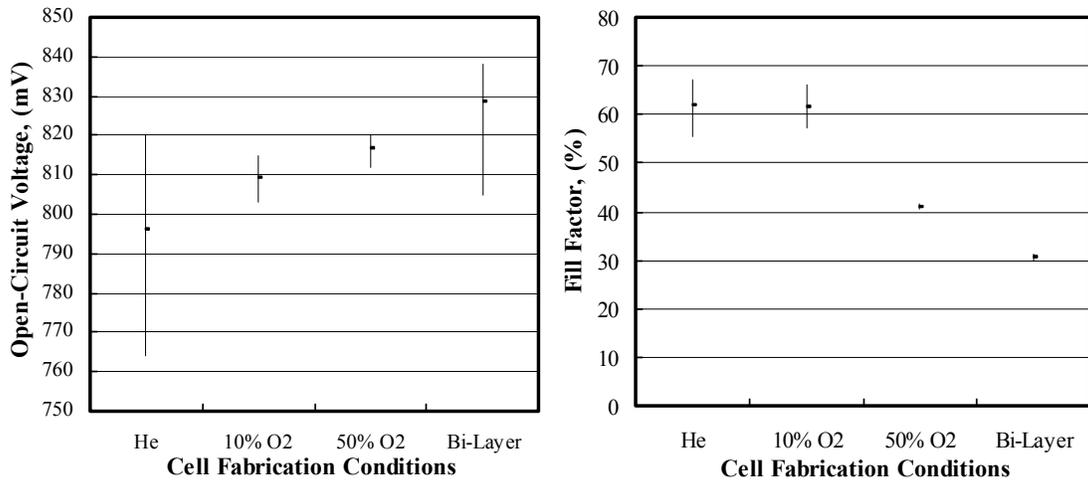
Figure 5. The effect of cell fabrication conditions on the V_{OC} and ff of CdTe/CdS/ZnO cells. The first three conditions refer to the ambient of the CSS-CdS process, and the fourth refers to the properties of the ZnO.

3.4 Zinc Selenide

An effort to utilize ZnSe as a window layer has been previously described (4). The performance of CdTe/ZnSe solar cells exceeded 11.0% efficiencies but results were difficult to reproduce. The difficulty reproducing the performance of CdTe/ZnSe junctions was attributed to the fact that both Zn and Se seem to diffuse extensively into the CdTe and form alloys. Controlling the formation of these alloys proved to be difficult. The main reason for this extensive interdiffusion is believed to be the rather high temperatures used for the CdTe deposition (near or above 600ºC). In order to minimize the diffusion problem described above a series of cells were fabricated at lower temperatures (CSS CdTe). The SR of one such a device (best cell in the batch) is shown in fig. 6 along with that of a CdTe/CdS cell processed under similar conditions for comparison.
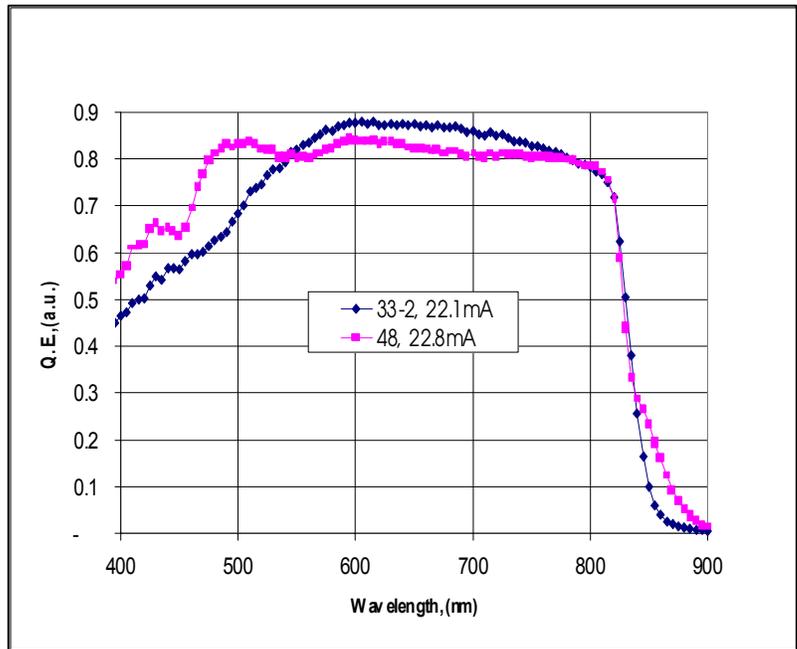
Figure 6. The SR of a CdTe(LT)/ZnSe junction.

Unlike high temperature devices this SR clearly shows the absorption edge of ZnSe at approximately 470 nm, suggesting that ZnSe can indeed lead to higher J_{SC}'s for CdTe solar cells. It is also clear that the SR of the CdTe/ZnSe device near the CdTe absorption

edge exhibits a shift toward longer wavelengths suggesting that selenium has diffused into CdTe (small amounts of Se in CdTe lead to a decrease in the energy gap (5). The solar cell characteristics of the two devices shown in fig. 6 are listed in table 5 along with the best cell parameters obtained on different CdTe/ZnSe cells. Based on these results it is suggested that the potential for higher J_{SC}'s exists, however, both the V_{OC} and ff of CdTe/ZnSe junctions are to date about 15% lower than those of CdTe/CdS cells.

TABLE 5. Solar cell parameters for CdTe/ZnSe devices.

	V_{OC}, (mV)	J_{SC}, (mA/cm^2)	ff, (%)
CdTe/CdS	836	22.1	64.0
CdTe/ZnSe	700	22.8	63.0
Best CdTe/ZnSe parameters obtained on different cells	728	22.8	63.0

3.5 Cadmium Oxide

Cadmium oxide has been previously used as a window layer for CdTe (6). During phase I work on CdO was initiated in order to determine the potential of this material as a window layer or TCO in CdTe solar cells. CdO films were deposited by MOCVD. The process was initially studied in an effort to optimize the electro-optical properties of CdO. The films were deposited in a commercial CVD reactor using Dimethylcadmium and oxygen as precursors. Helium was used as the carrier gas. The glass substrates were placed on a graphite susceptor (susceptor size 10 x 10 cm^2), which was heated using tungsten halogen lamps. Although most work to date focused on intrinsic films (i.e. no intentional doping), preliminary work on extrinsic doping has suggested that tin is an n-type dopant in CdO and is currently being evaluated. Table 6 lists the range of processing conditions used to-date.

TABLE 6. MOCVD CdO deposition conditions.

Precursor	
DMCd, (partial pressure)	$1.5 - 3.0 \times 10^{-4}$
O_2, (partial pressure)	$0.3 - 0.4$
T_{SUB}, (°C)	200-300

3.5.1 Deposition Rate

The deposition conditions (flow rates) were initially adjusted to result in uniform thickness over the entire susceptor area. A thickness uniformity of ±5% was obtained. Figures 7 and 8 show the deposition rate for the CdO films as a function of the deposition temperature and the DMCd partial pressure. As the temperature is increased from 200 to 275°C the deposition rate increases suggesting that in this range the process is reaction rate limited. As the temperature is further increased the deposition rate decreases. This was attributed to increased gas phase reactions that resulted in depletion of the precursors

prior to reaching the substrate surface; this conclusion was substantiated by the increased deposits on the reactor walls at the highest temperature. Having selected 275C as the "optimum" temperature the effect of DMCd partial pressure on the deposition rate was investigated and is shown in fig 8. The deposition rate increases with increasing DMCd partial pressure, as one would expect since the process is carried out in an environment of excess O_2.
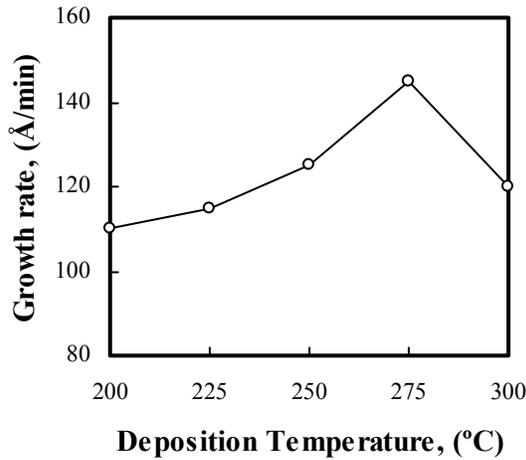
Figure 7. CdO growth rate vs. T_{SUB}
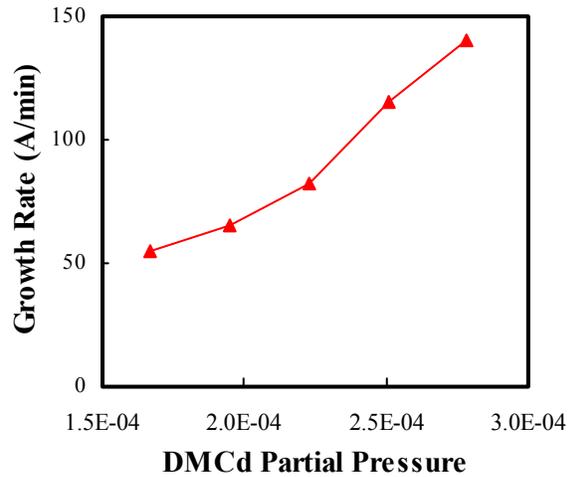
Figure 8. CdO growth rate vs. DMCd partial pressure

3.5.2   Structural Properties

All CdO films exhibited good adhesion to the glass substrates. Figure 9 shows the XRD for CdO films deposited at different temperatures. It appears that in the 200-275ºC range the films exhibit preferential orientation along the (111) direction, while for temperatures above 275ºC they exhibit preferential orientation along the (200) direction (see also fig. 10 for dependence of ratio of (200)/(111) directions on temperature)
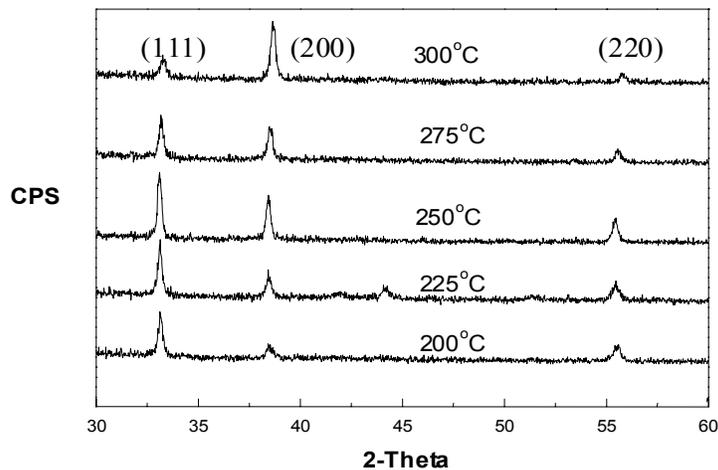
Figure 9. XRD spectra for CdO films.
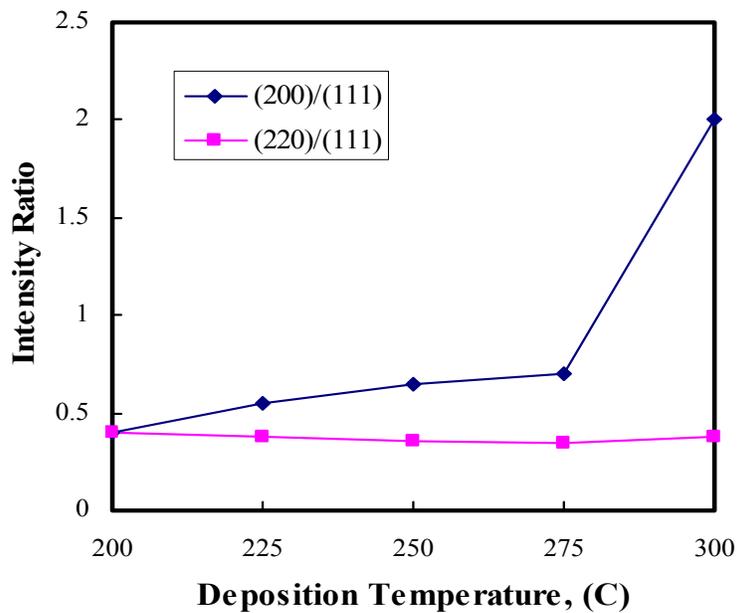
Figure 10. (200)/(111) and (220)/(111) ratios.

The SEM micrographs for the same series of films are shown in fig. 11. The grain size appears to decrease as the temperature is raised from 200 to 275ºC where it reaches a minimum value and then appears to increase at 300ºC.
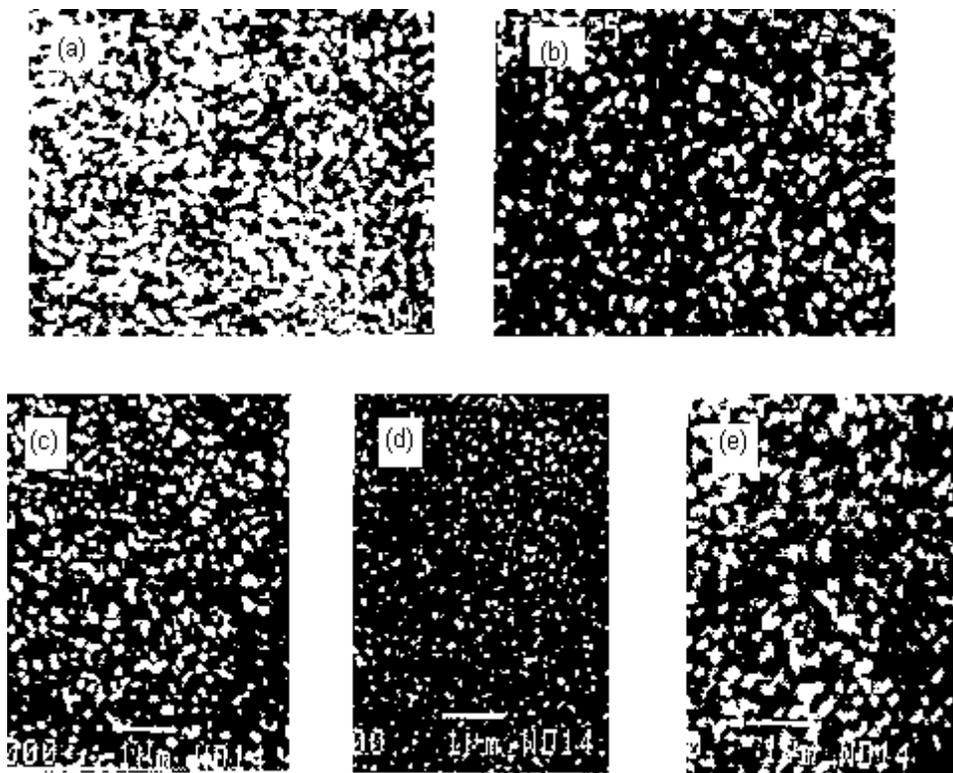
Figure 11. SEM micorgraphs of CdO films deposited at (a) 200, (b) 225, (c) 250, (d) 275, and (e) 300ºC.

Work on CdO films continues and as previously mentioned emphasis is now being shifted toward extrinsically doped films since these appear to exhibit improved electrical properties.

4.0   LOW PROCESSING TEMPERATURES - VAPOR CDCL₂ TREATMENT

One of the primary objectives of this project is the development of simplified processing that can lead to lower manufacturing costs. The original target temperature was set at 550ºC. State of the art performance was obtained at this temperatures (1). However, since it became apparent that the temperature could be reduced work in this area continued emphasizing temperatures below 500ºC. Open-circuit voltages in excess of excess of 800 mV were reported previously for a substrate temperature of 480ºC(1).

Figure 12 shows SEM micrographs of three CSS CdTe films deposited at 420, 440, and 460ºC respectively. As indicated the grain size increases with increasing substrate temperature. Since at higher temperatures the surface mobility of the depositing species increases the number of nucleation sites decreases leading to larger grains. Based on these results subsequent work on devices focused on temperatures above 440C since the film deposited at 420ºC exhibited a large distribution in grain sizes (this film also exhibited pinholes visible to the naked eye). The characteristics of a series of devices prepared at temperatures in the 440-480ºC range are shown in table 7. The best performance is obtained at a substrate temperature of 480ºC. The similarity in performance between the two lower temperatures, suggests that variations in grain size do not impact device performance. Based on the lower V_{OC}'s it is suggested that the CdTe/CdS interface properties are negatively affected by the lower temperature. Based on these results 480ºC remains the lowest "optimum" temperature for the CSS-CdTe process.
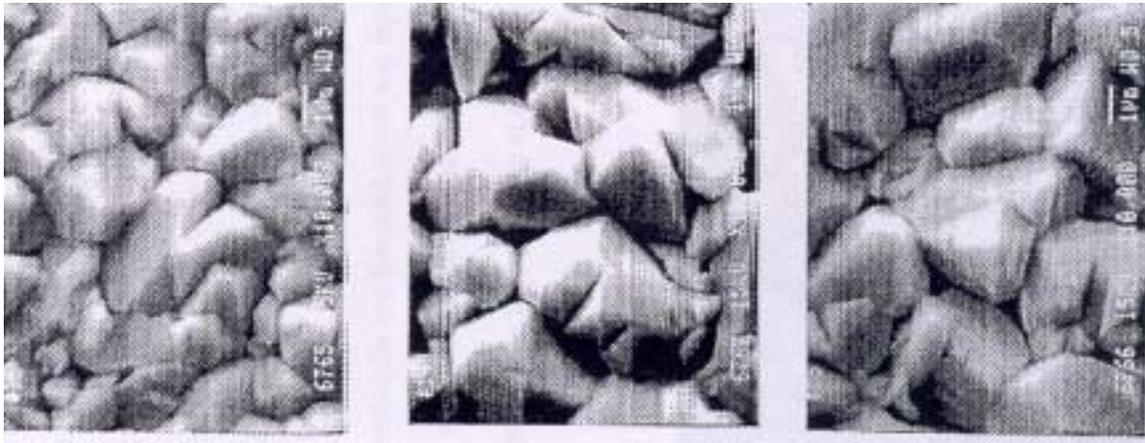
Figure 12. SEM micrographs of CSS CdTe deposited at substrate temperatures of 420, 440, 460 (left to right).

TABLE 7. Solar cell parameters for low temperature devices.

T_{SUB}, (°C)	V_{OC}, (mV)	ff, (%)	J_{SC}, (mA/cm^2)
440	805	60.0	20.1
460	807	65.0	19.5
480	834	64.5	20.64

In all cases where CdTe solar cells exhibit high efficiencies the devices are subjected to what has become a standard among all CdTe groups, CdCl$_2$ treatment. This process is rather simple but it also presents manufacturing challenges since in its simplest form involves solutions of CdCl$_2$ that result to large amounts of liquid. It would be preferred if this could be avoided. A vapor CdCl$_2$ treatment would be beneficial in improving the manufacturability of this processing step and it has been the subject of other investigations (7). At USF a two-zone reactor is used where the CdCl$_2$ powder and the CdTe/CdS structures are heated independently and the vapors of CdCl$_2$ are transported to the CdTe/CdS zone using a carrier gas. In this section the results from series of experiments performed to determine the effectiveness of this process are described.

Table 8 lists the performance of CdTe cells fabricated at high temperatures and exposed to the vapor CdCl$_2$ treatment. A device exposed to the baseline CdCl$_2$ treatment process is also included for comparison. The devices represent two batches (A and B) of four substrates. The first batch demonstrates that the vapor CdCl$_2$ treatment can indeed produce very similar results to the standard CdCl$_2$ process. The ff's of these devices are rather low, but this was attributed to the back contact. The second batch was carried out in order to establish the reproducibility of this process, since at the early stages of this work samples treated with vapor CdCl$_2$ exhibited significant variations in performance. However, as the results in table 8 suggest the process is rather reproducible (the four samples were exposed to the vapor CdCl$_2$ treatment one at a time).

TABLE 8. Solar cell parameters for CdTe devices treated with CdCl$_2$ vapor.

Batch	CdCl$_2$ Treatment	V_{OC}, (mV)	ff, (%)	J_{SC}, (mA/cm^2)
A	"baseline"	859	66.2	21.85
A	Vapor	847	62.1	21.65
A	Vapor	842	66.3	21.57
A	Vapor	849	63.3	21.54
B	Vapor	837	66.4	20.6
B	Vapor	843	63.0	21.0
B	Vapor	830	64.0	22.1
B	Vapor	831	63.3	22.3

Work on low temperature devices and the vapor CdCl2 treatment continues. The best device performance obtained to date for the vapor CdCl2 treatment is:

- CdTe – HT: V_{OC} = 851 mV   ff = 73.0 J_{SC} = 21.67 mA/cm^2
- CdTe – LT: V_{OC} = 820 mV   ff = 69.4 J_{SC} = 21.75 mA/cm^2

5.0   BACK CONTACTS

The baseline back contact currently used at USF is HgTe:Cu doped graphite paste. Although this contact has produced state of the art performance and it appears to be easily scalable for large area applications (it can be easily screen printed or sprayed), it is also rather bulky and this may prove to be a disadvantage when scribing and interconnects is considered. Another apparent shortcoming of the doped graphite paste approach is the use of copper, which has a high diffusion coefficient and its presence in these devices may be a source of possible degradation mechanisms. Therefore, a considerable effort has been dedicated in developing alternative back contact schemes. Some approaches emphasize ease of manufacture and some are based on copper free materials. The following discussion describes work carried on contacts based on the following materials: (a) Cu_xTe, (b) ZnTe, and (c) Sb_2Te_3

5.1   Copper Telluride

The use of copper during the formation of the back contact has proven to be a critical element in achieving effective low resistance back contacts. Several contacting approaches typically include the use copper during the back contact formation process. It has also been reported that the presence of Cu_2Te leads to ohmic contacts while poor contact performance was correlated to the presence of CuTe (8). The objective of this approach was to develop a simplified contacting process by directly depositing onto CdTe a Cu_xTe compound of the correct stoichiometry. The Cu_xTe films were deposited by rf sputtering of a 5N Cu_xTe target; the composition of the target was x=2 as indicated by the supplier. The Cu_xTe deposition was followed by graphite paste (undoped) application or molybdenum deposition by rf-sputtering. During the early stages of this work the samples were exposed to air between the Cu_xTe and molybdenum depositions. After the installation of a second sputtering source in the vacuum system used for this work, the Cu_xTe and molybdenum depositions can now be carried out sequentially in-situ. A summary of the process parameters studied and the corresponding ranges are given in table 9.

TABLE 9. Summary of Cu_xTe deposition conditions.

Power Density, (W/in^2)	8.5
Base Pressure, (torr)	10^{-6}
Sputtering Pressure, (mTorr)	5
Cu_xTe Thickness, (Å)	25-300
Substrate Temperature, (ºC)	25-350

The basic processing steps taken for the formation of the back contact were:
  (a) CdTe surface etch in Br_2/methanol (in a few cases a HNO_3/H_3PO_4 solution was also used)
  (b) deposition of Cu_xTe
  (c) deposition of molybdenum (or graphite paste application.)

5.1.1 Film Composition

Prior to the directly depositing Cu_xTe onto CdTe and studying solar cell performance, several Cu_xTe films were deposited on glass substrates at various temperatures and their composition was analyzed using EDS. These results are shown in table 10. It appears that as the temperature is increased the amount of copper in the films increases. The Cu/Te ratio approaches 2 when the temperature is over 200°C and appears to exceed 2 when the temperature is 250°C. This result may prove to be critical since the as mentioned earlier Cu2Te is favored for ohimc contact behavior.

TABLE 10. Cu_xTe composition as a function of deposition temperature.

Substrate Temperature, (°C)	Film Composition, (%)		Cu/Te Ratio
	Copper	Tellurium	
100	62.92	37.08	1.70
150	64.20	35.80	1.79
200	64.94	35.06	1.85
250	68.19	31.81	2.14

5.1.2 Cu_xTe Thickness

The amount of copper present during the back contact formation process is critical. There appears to be an optimum amount necessary to dope the CdTe surface (and the CdTe bulk) to facilitate the contact formation. However, an excessive amount of copper could also diffuse along the grain boundaries and develop shunting paths. It was anticipated that a certain amount of free copper could be present during the deposition of the Cu_xTe films, and it would therefore be necessary to control it in order to avoid shunting of the devices. In order to address the issue of controlling free copper, the thickness of Cu_xTe used for the back contact formation was varied and the properties of the solar cells studied. Figure 13 shows the dependence of ff and V_{OC} on the thickness of Cu_xTe for several CdS/CdTe/Cu_xTe/Mo solar cells. The Cu_xTe films were deposited at room temperature. It is clear that there exists an optimum range of thicknesses (approximately 30-80 Å), for which the CdTe solar cells exhibit respectable V_{OC}'s and ff's (over 800 mV and 65% respectively). Both the V_{OC} and ff degrade for small and large thicknesses. At large thicknesses the reason for the reduced V_{OC} and ff is low light shunt resistance as indicated by the light J-V data shown in figure 14 (triangles). At smaller thicknesses the V_{OC} remains high (near 800 mV) but the ff decreases drastically to nearly 50%. From the J-V data of the small Cu_xTe thickness device, shown in fig. 14, the slope at V_{OC} suggests that the series resistance of this device is of the same magnitude as the cell prepared with 50Å Cu_xTe. One would expect that as the amount of Cu_xTe decreases the back contact would degrade due to a high series resistance or no-linear i.e. rectifying behavior, none of which are present. However, the behavior of the J-V between 0 volts and V_{OC} seems to suggest that collection may be responsible for the lower ff.
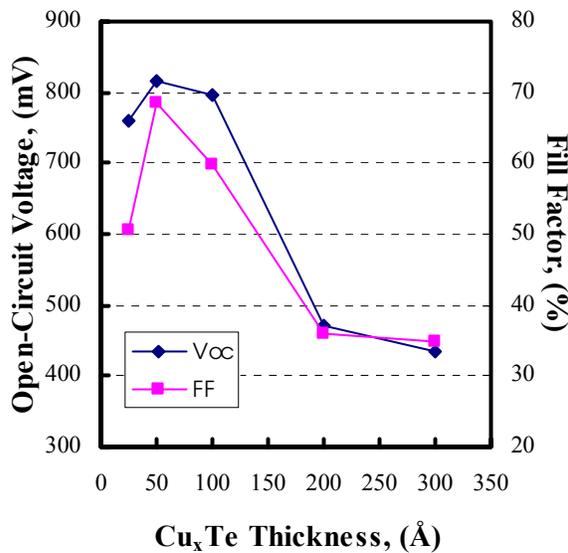
Figure 13. The effect of Cu$_x$Te thickness on the V$_{OC}$ of CdTe/CdS solar cells.
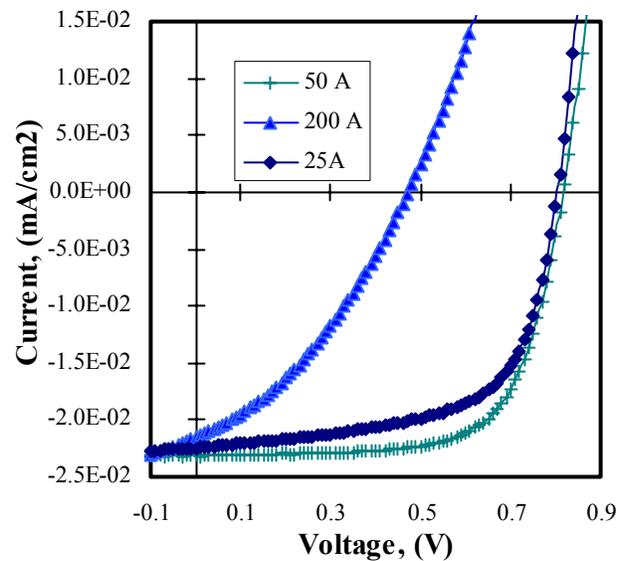
Figure 14. Light J-V data for CdTe solar cells fabricated with Cu$_x$Te contacts of different thicknesses.

5.1.3 Deposition Temperature

The Cu$_x$Te films for all cell results discussed in the previous section were deposited at room temperature. Based on the fact that the composition of the Cu$_x$Te exhibited a dependence on the substrate temperature a series of devices were fabricated for which the Cu$_x$Te films were deposited at elevated temperatures. Molybdenum was used as the back metal electrode for all these cells. Figure 14 shows the dependence of the ff and V$_{OC}$ on the Cu$_x$Te deposition temperature. Optimum performance is obtained in the range of 200-250ºC. As discussed in a previous section the Cu$_x$Te ratio in this range is close to 2.0. It is therefore suggested that the composition and the amount of Cu$_x$Te (which most likely determines the amount of free copper) are the most important parameters in optimizing the performance of this type of back contact.

A typical light J-V curve is shown in fig. 15. Based on the first quadrant characteristics it is reasonable to speculate that the Cu$_x$Te back contact is not ohmic. The J-V suggests that a back barrier exists, which however, does not affect the important fourth quadrant performance. The Cu$_x$Te contact process was found to be extremely robust and reproducible. The cells listed in table 11 are from consecutive batches and they indicate the reproducibility and robustness of this particular process.

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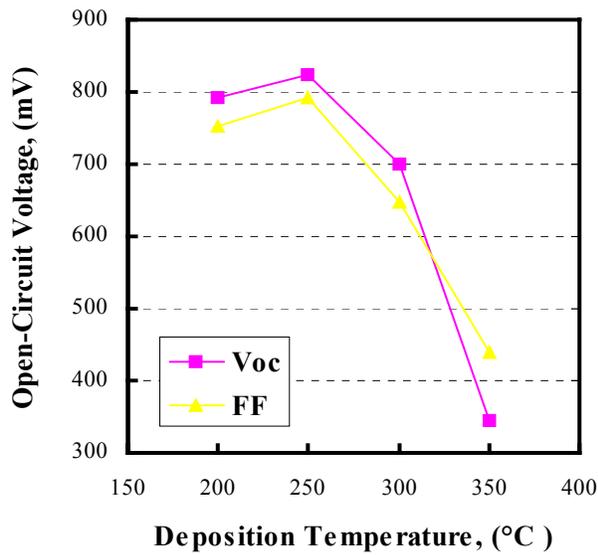
Figure 15. The effect of the Cu$_x$Te deposition temperature on V$_{OC}$.
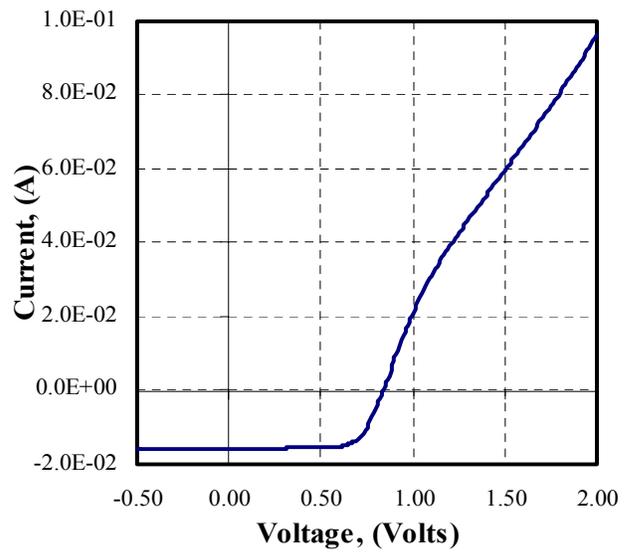
Figure 16. Light J-V data for a Mo/Cu$_x$Te/CdTe/CdS device.

TABLE 11. A series of devices processed to demonstrate the reproducibility of the Cu$_x$Te contact.

V$_{OC}$, (mV)	J$_{SC}$, (mA/cm^2)	ff, (%)
834	22.5	73.5
844	22.3	74.6
839	22.3	74.7
837	22.5	74.3
838	22.2	75.2

5.2   Zinc Telluride

Copper doped zinc telluride-based contacts have been used by various groups. During this phase, this contacting approach was briefly investigated and optimized for USF solar cells, in order to include this type of structures in stability studies. The overall objective is to eventually evaluate the stability of two types of back contacts; those based on copper and copper free.

Zinc telluride films were deposited onto the CdTe surface by rf sputtering from a 5N ZnTe target. Since the work on Cu$_x$Te back contacts seemed to suggest that there was free copper present during that process, a thin film of Cu$_x$Te was deposited onto ZnTe to provide copper for doping the ZnTe films. The fabrication procedure consisted of the following sequence:
(a) CdTe surface etch with Br$_2$/methanol
(b) ZnTe deposition

(c) Cu_xTe deposition
(d) Molybdenum deposition
(e) Post contact deposition anneal

The key parameter in optimizing the ZnTe:Cu back contact proved to be the Cu_xTe thickness i.e. the amount of copper introduced into the ZnTe. Table 12 shows the effect of the Cu_xTe thickness on cell performance. As the data suggests the performance is improved with increasing Cu_xTe thickness form 75 to 150Å approaching state of the art performance.

TABLE 12.   The effect of the Cu_xTe thickness on devices contacted with ZnTe/Cu_xTe.

Sample #	Cu_xTe Thickness, (Å)	V_{OC}, (mV)	FF, (%)
3-12B-4	75	778	56.6
5-20A-2	100	837	65.2
5-20A-3	150	846	71.5

The light J-V for the three cells shown in table 12 are shown in figure 17. All three devices exhibit shunt resistances (dV/dJ @ V_{OC}) well above 1.5 kΩ-cm^2 indicating that no significant shunting is present. In all three cases, and in particular for the two smallest Cu_xTe thicknesses there is evidence of a back junction as indicated by the J-V behavior in the first quadrant. Improvements in the ff with increasing Cu_xTe thickness are a result of a smaller R_S at V_{OC}. The device with the smallest amount of Cu_xTe also exhibits considerably lower V_{OC} presumably due to a larger back contact barrier.
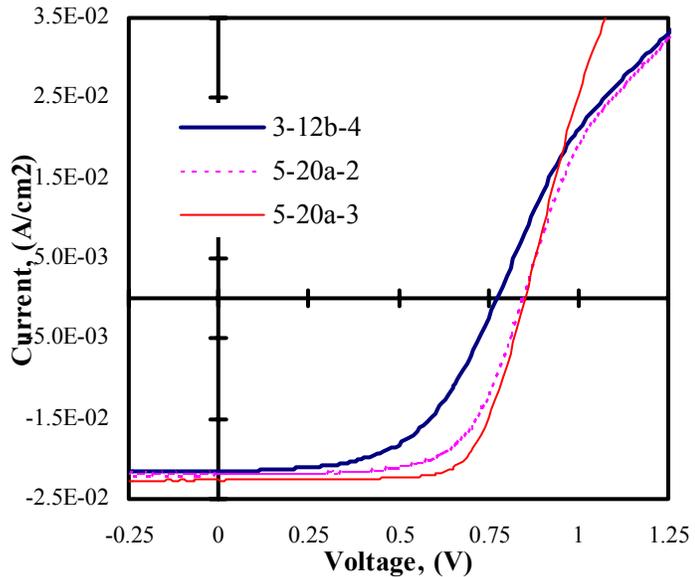
Figure 17. Light J-V data for several CdTe solar cells contacted with the ZnTe:Cu.

The Cu_xTe deposition temperature was also found to be critical. Based on a limited number of experiments it has been found that the optimum Cu_xTe deposition temperature is 250°C; it should be noted that this was also the optimum temperature for Cu_xTe contacts described in the previous section. The carrier concentration in CdTe was estimated from capacitance measurements and the results are tabulated in table 13. At high deposition temperatures (350°C) the CdTe doping concentration was 3-4 times

higher regardless of the total amount of Cu$_x$Te deposited on the samples. This seems to suggest that at the highest deposition temperature there is more free Cu available to be incorporated and become electrically active in CdTe. As described in a previous section the Cu/Te ratio increased above 2 for temperatures higher than 250°C which suggests the presence of free copper.

TABLE 13. Carrier concentration in CdTe as a function of the Cu$_x$Te deposition conditions.

Cu$_x$Te Thickness, (Å)	Cu$_x$Te Deposition Temperature	
	250ºC	350ºC
100	1.38 x 10^{14}/cm^3	6.9 x 10^{14}/cm^3
150	2.3 x 10^{14}/cm^3	6.9 x 10^{14}/cm^3

5.3   Antimony Telluride

Recently, Sb$_2$Te$_3$ has been successfully utilized as a back contact material. This approach produced devices with efficiencies over 15.0% but most importantly these devices exhibited remarkable stability at 20 suns for 48 hours (9)   Based on this report Sb$_2$Te$_3$ was chosen as a potential candidate for copper free based back contacts. The material was deposited by rf sputtering from a Sb$_2$Te$_3$ target 5N purity. Following the Sb$_2$Te$_3$ deposition, molybdenum was deposited to a thickness of about 1 μm. Based on to date results the performance of Mo/Sb$_2$Te$_3$/CdTe/CdS solar cells is limited due to a poor back contact characteristics. In nearly all cases the back contact appears to be rectifying limiting both the ff and V$_{OC}$. A number of processing parameters have been varied in search of optimum process conditions for better solar cell performance, but no clear trend has been observed and reproducible results are difficult to obtain. The performance of CdTe solar cells contacted with Sb$_2$Te$_3$ remains poor, with maximum VOC's in the range and ff's.

In an effort to determine what limits the performance of these devices, a number of Sb$_2$Te$_3$ films were deposited on glass or glass/SnO$_2$ substrates for additional characterization. XRD analysis was performed at the Institute of Energy Conversion (by Brian McCandless). Figure 17 shows the XRD spectra for three Sb$_2$Te$_3$ films: (a) deposited at 275°C on glass, (b) deposited at 275°C on SnO$_2$/Glass, and (c) deposited at room temperature. These results showed that the films deposited at room temperature contained non-equilibrium SbTe phases identified with x's. The SnO$_2$ peaks are also marked. The remaining peaks are associated with the Sb$_2$Te$_3$ compound. The films deposited at 275°C (which is the temperature used for the deposition of most Sb$_2$Te$_3$ contacts) contained only Sb$_2$Te$_3$. No Sb or Te was found in any of the films. These results seem to suggest that single phase Sb$_2$Te$_3$ may not be a good candidate for a back contact for CdTe solar cells.

The recent addition of a second sputtering source for in-situ Mo deposition, seems to have improved reproducibility for Sb_2Te_3 contacted cells, but not the performance. Additional work to better understand and optimize this process is underway.
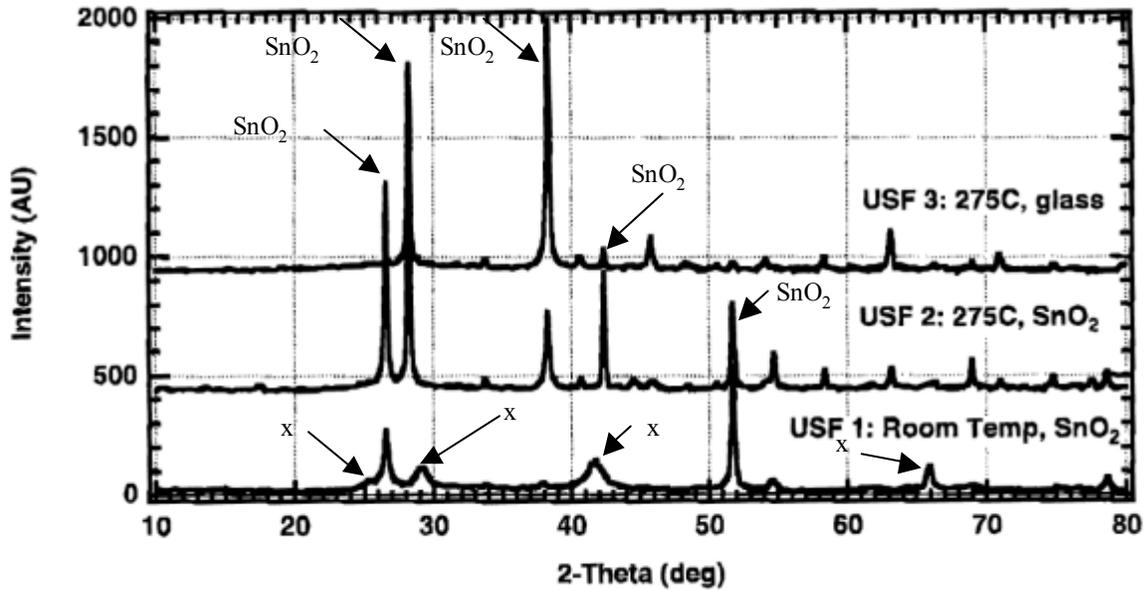
Figure 18. **XRD spectra for Sb₂Te₃ films (performed by Brian McCandless of IEC).**

6.0   STABILITY STUDIES

Since there has been some evidence on the presence of degradation mechanisms in CdTe solar cells part of the effort of this work is to try to identify the source(s) of such mechanisms, develop predicting models and seek solutions to achieve long-term stability (10).

6.1   Temperature Stress - Set "A"

During this phase of the project a series of baseline devices i.e. doped graphite /CSS-CdTe/CBD-CdS/bi-layer SnO_2/ borosilicate glass were selected for temperature stress experiments. A set of three cells (identified as set "A") was used for a pilot study, in order to understand and select the best suited stress conditions. The three devices were stressed at 70, 80 and 90ºC in inert ambient. After each stress cycle the light and dark J-V were measured. Initially the devices were stressed for 1 hour at a time, but as a general trend of their behavior evolved, the stress time was increased to 2, 4, 8, and eventually 24 hours at a time. The V_{OC}, ff, J_{SC}, efficiency, diode factor A, and J_O over the first 1000 hours of stressing are shown in appendix A. Table 13 shown below summarizes the observed changes in solar cell characteristics.

TABLE 13. Summary of observed changes for devices stressed at 70, 80, and 90ºC.

	70ºC	80ºC	90ºC
ΔV_{OC}, (mV)	~ -10	~ -20	~ -30
Δff, (%)	~ -5	~ - 5	~ -5
ΔJ_{SC}, (mA/cm^2)	~ -0.5	~ -0.0	~ -0.0
$\Delta \eta$, (%)	~ -1.0	~ -1.0	~ -1.3

6.1.1 *Short Circuit Current*

No significant change is observed in the short circuit current. After 1000 hours, it appears to have decreased by approximately 0.5 mA/cm^2 for the sample stressed at 70ºC, while it remains essentially constant for the other two samples stressed at higher temperatures. The slight drop observed in the 70ºC sample may be related to structural damage of the contact; due to excessive handling (the samples were stressed and measured more than 100 times) the edges of the contacts show signs of cracking and peeling.

6.1.2 *Open-Circuit Voltage*

The open-circuit voltage exhibited a small drop in all three cases. It is noteworthy that this change has taken place approximately in the first 200 hrs. After the first 200 hrs the V_{OC} appears to have leveled off up until the 800 hrs point at which it appears to be decreasing once again. The decrease in V_{OC} for the sample being stressed at 90°C is more significant than the other two samples as one should reasonably expect. It should however be noted that this particular sample has also been damaged during the testing process and a small part of this device has peeled off. An indication of the damage is the excessive shunting which lead to calculations of the A factor above 2.0 (3-5). The early drop in V_{OC} (in all devices) is accompanied by a similar behavior in J_O (see appendix A). The reverse saturation current has increased by approximately one order of magnitude within the first 200 hours and it appears to be leveling off beyond that point. Using the measured J_O and A values and the simple relationship

$$V_{OC} = \frac{kT}{q} \ln(\frac{J_{SC}}{J_O} + 1)$$

the V_{OC} predicted from the dark J-V was calculated and is plotted in fig. 19 along with the measured V_{OC}. It is apparent that using a simple diode model the V_{OC} can be reasonably predicted from the dark diode characteristics. It is therefore suggested that based on the to-date results, that the most significant changes affecting V_{OC} appear to be taking place at the junction. It should be noted that the values of A and J_O are the best estimates that can be obtained from the linear portion of the dark Ln(J) vs. V plot. If this portion of the plot is distorted by excessive shunting and/or high series resistance A and J_O cannot be obtained, and other measurements such as J_{SC} vs. V_{OC} which remove the effect of the series resistance are necessary.
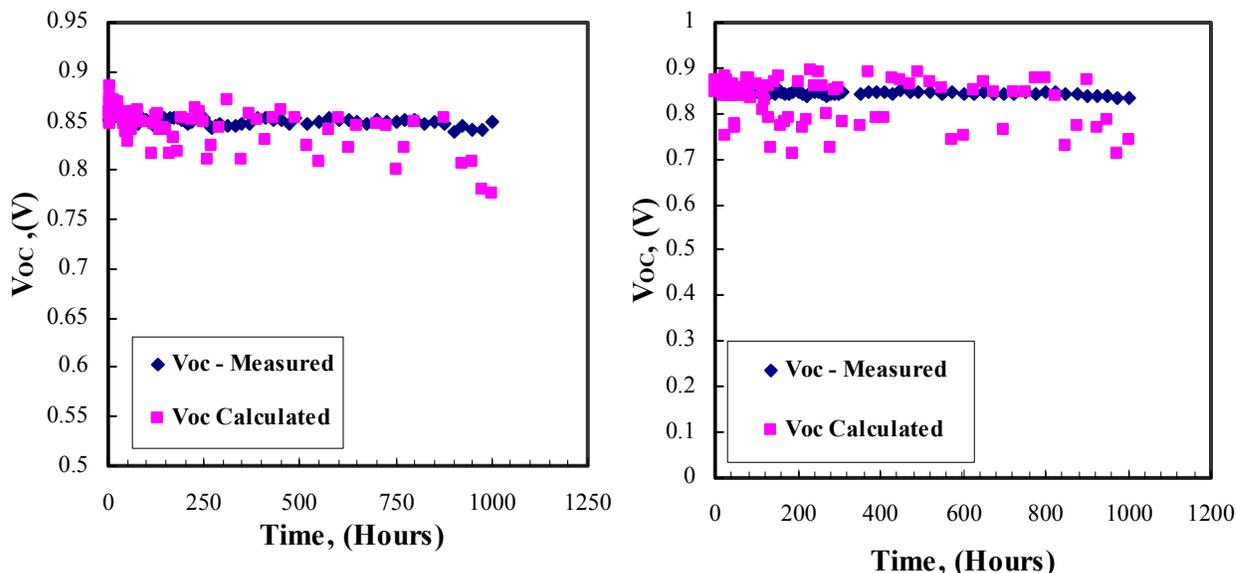
Figure 19. Measured and calculated V_{OC} for samples stressed at 70 (left) and 80°C (right).

6.1.3 Fill Factor

Similar to the V_{OC} behavior the ff also appears to decrease during the first 200 hours and then levels off. Measurement of the light shunt resistance indicated that this quantity remained above 2kΩ-cm^2 for all cells suggesting that light shunting is not the reason for the decrease in the ff. The light R_{SH} affects the ff significantly when its value drops below 800-1000 Ω-cm^2. Therefore the change in the ff could also be attributed at least partly to the observed increase in J_O. Another interesting observation is that the change in the ff appears to be independent of the temperature; it decreased approximately 5% in all three cases (70, 80, 90°C).

Based on the results obtained form the three samples described above another set of devices (Set "B") were selected and are being stressed at six different temperatures: 60, 70, 80, 90, 100, and 120°C. Three cells are being stressed at each temperature in inert ambient. Since results on these are still limited (up to 100 hours) they will be discussed in the next report.

6.2 Light Soaking – Set "C"

Another set of four cells (Set "C") is being light soaked at open-circuit voltage conditions for 8-10 hours daily. The samples are kept in a quartz container, which is continuously being purged with N_2 gas. The N_2 is also being used to maintain the temperature of the devices at 70°C. To-date, these devices have been light soaked for approximately 700 hours. The V_{OC}, ff, of one of these cells are shown in figs 20 and 21; (it should be noted that the light J-V are measured @ 70°C). All cells in this batch exhibit very similar behavior.

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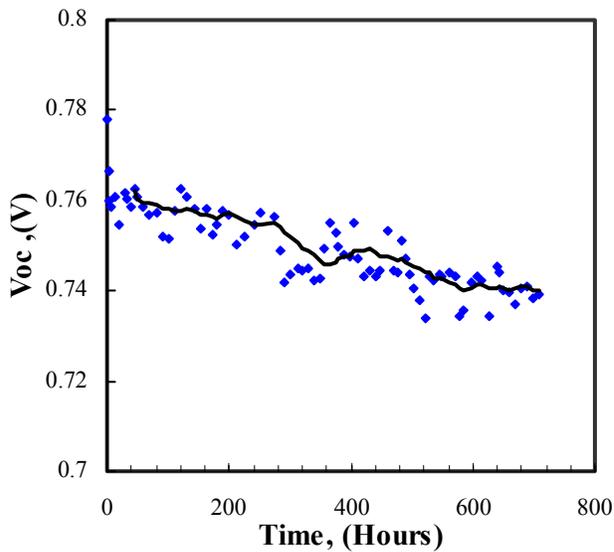
Figure 20. V_{OC} of light soaked solar cells.
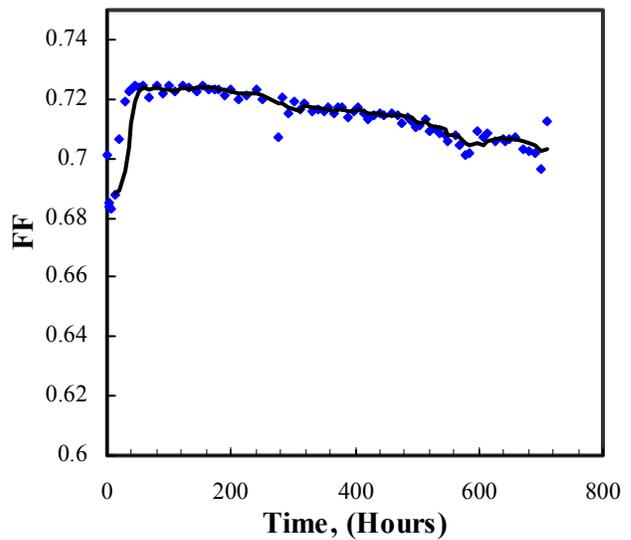
Figure 21. FF of light soaked solar cells.

Over this period of 700 hours the V_{OC} has exhibited what appears to be a linear decrease from about 760 to 740 mV (approximately a 3% loss). The ff has initially increased from 68 to over 72% within the first 30-50 hours of light soaking. After this initial increase the ff also shows an apparent linear decrease. To date the ff is still at a value higher than the starting one (nearly 3% higher). The combined effect of the changes shown in these two figures and the fact that J_{SC} has remained constant resulted in a nearly constant efficiency over these first 700 hours of light soaking. The mechanisms for this type of behavior appear to be quite different than the ones taking place for set "A" (temperature stress).

Figure 22 shows the light shunt resistance for the sample of figs 20 and 21 for the first 700 hours. As the data suggests the shunt resistance exhibits a rather "fast" increase from about 500 to 1500 Ω-cm^2 in the first 30-50 hours and then appears to steadily decrease (the data scattering observed in fig 22 is due to noise in the light J-V data near J_{SC}). This change appears to "mirror" the improvement observed in the ff. However, J_O (see appendix B) is increasing suggesting that the ff should actually decrease. This appears to be a case where two processes are simultaneously taking place each
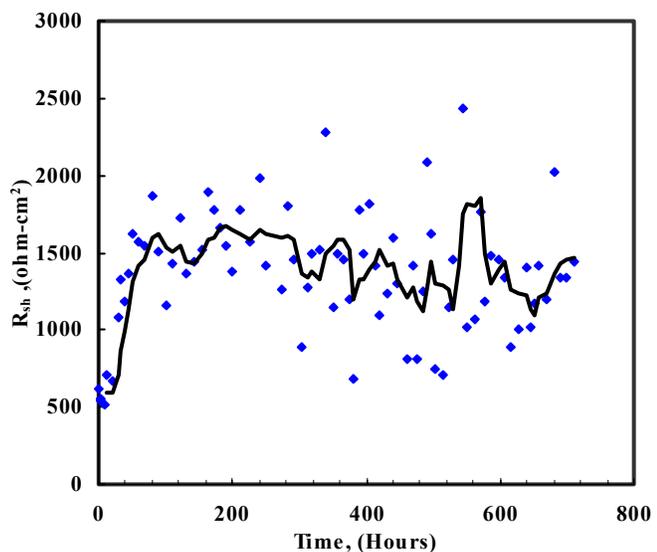
Figure 22. R_{SH} of the cell of figs 20 and 21.

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dominating the characteristics of these devices at different times. It should also be noted that using the values of the measured R_{SH}, A and J_O the simple diode model fails to predict the V_{OC} and ff for these devices. It is therefore suggested that a more complex model is used to predict the observed behavior.   It will also be necessary that additional device information must be collected in addition to the standard J-V measurements in order to better understand these changes. An effort to obtain information on the gap states in CdTe using deep level transient spectroscopy is underway. Although this has been complicated by the fact that cell performance is often affected by the measurement conditions, the methodology of carrying out this technique has been modified and meaningful results are currently being obtained.   Several stressed devices have also been sent to NREL for SIMS analysis in an effort to obtain information on impurity profiles at various stages of stressing.
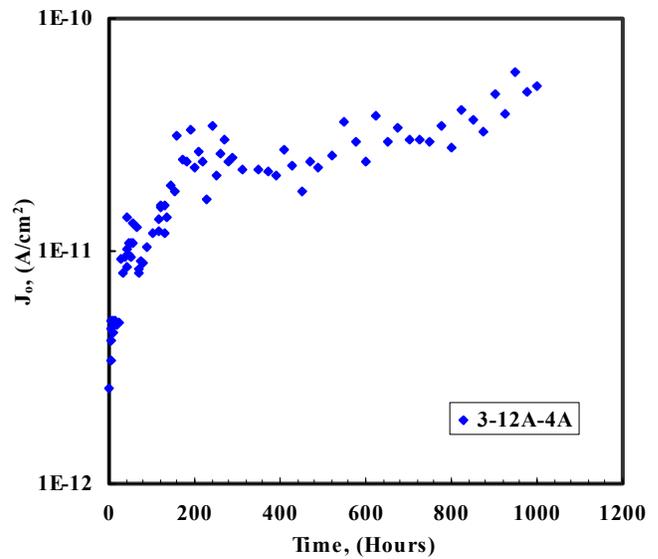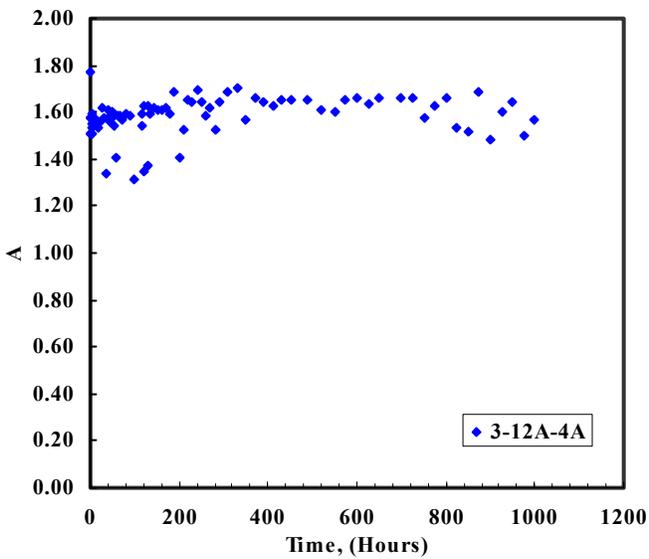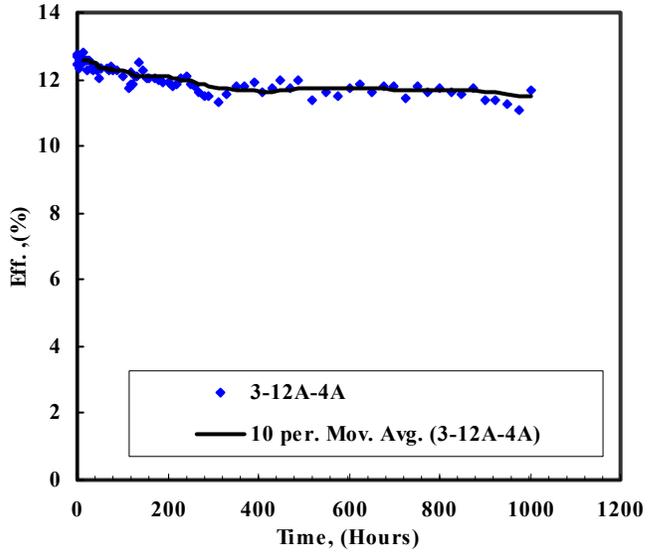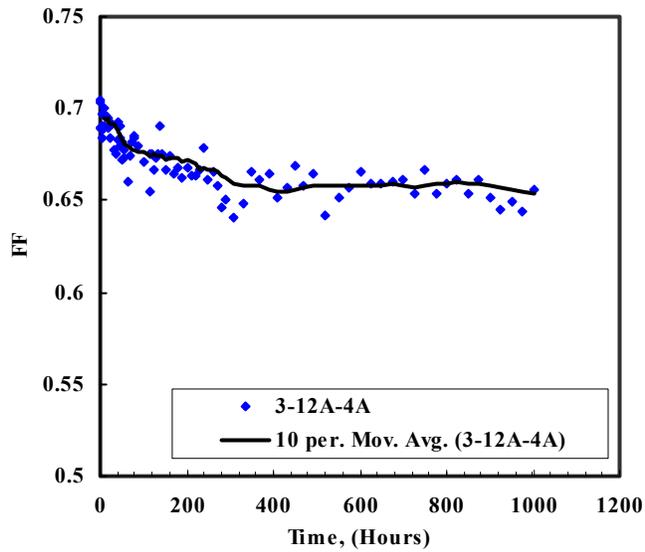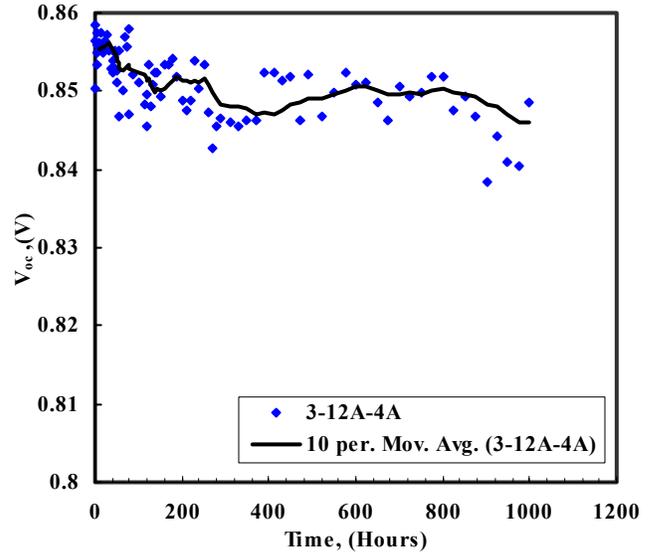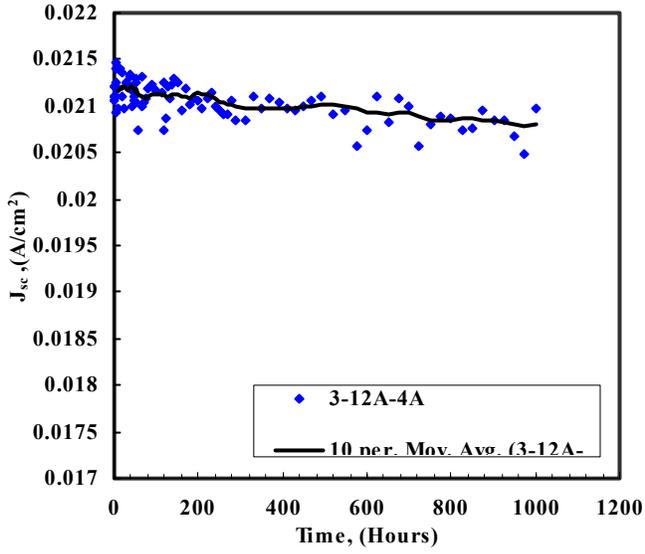
APPENDIX A – SET "A" TEMPERATURE STRESS STUDIES; T_{STRESS}=70ºC
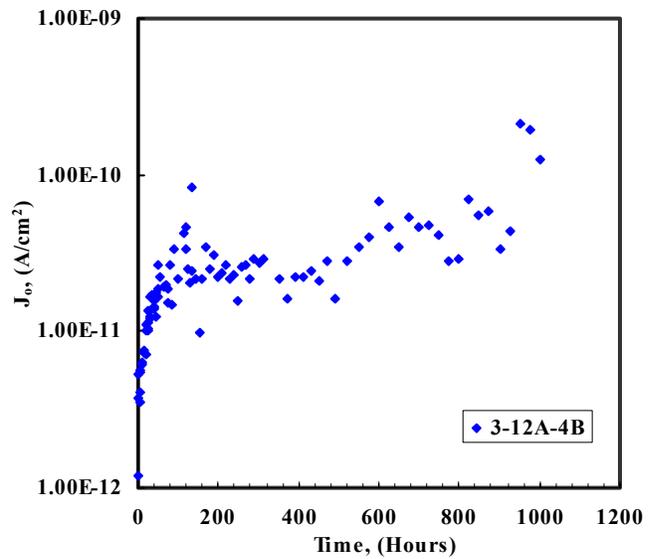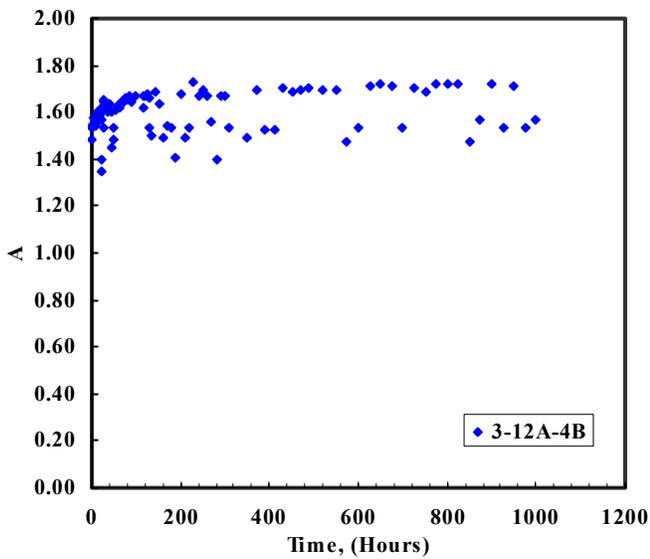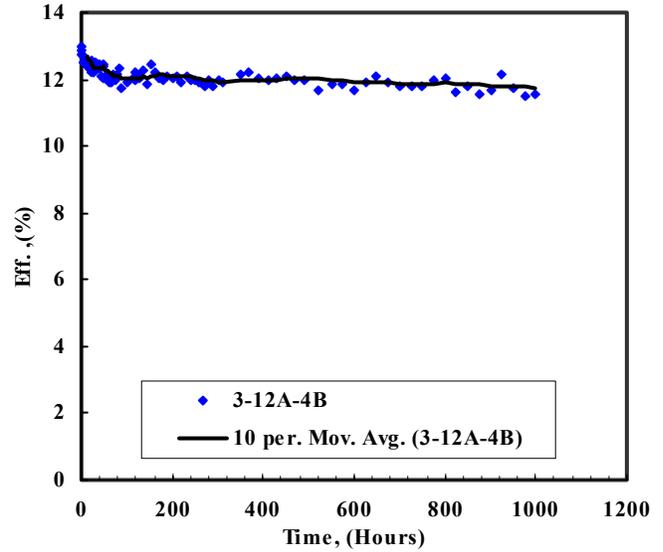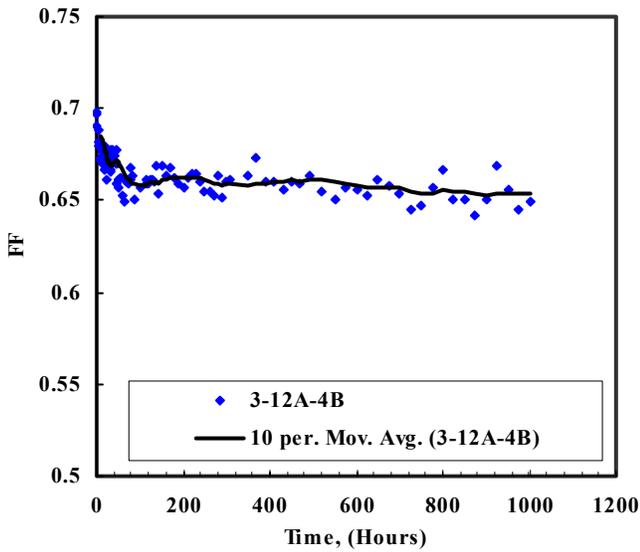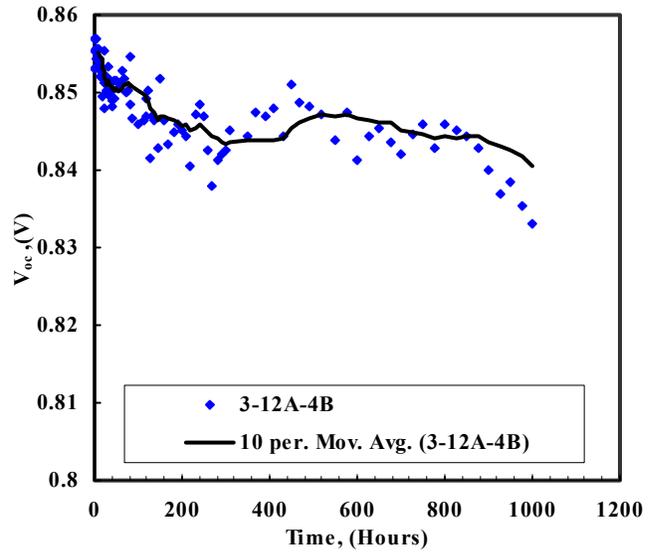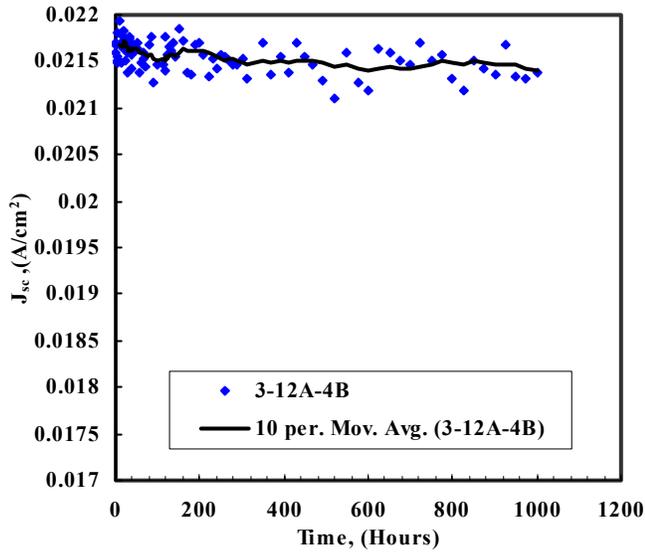
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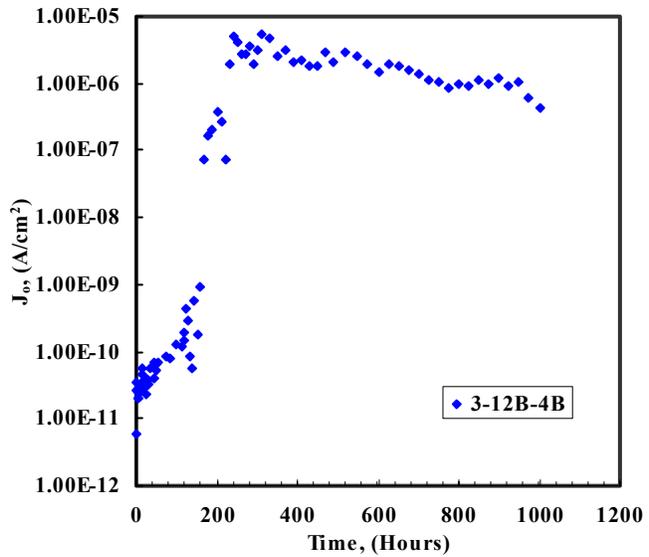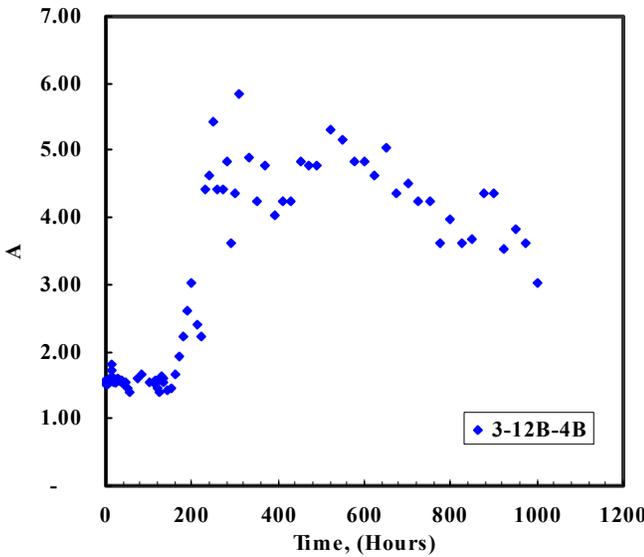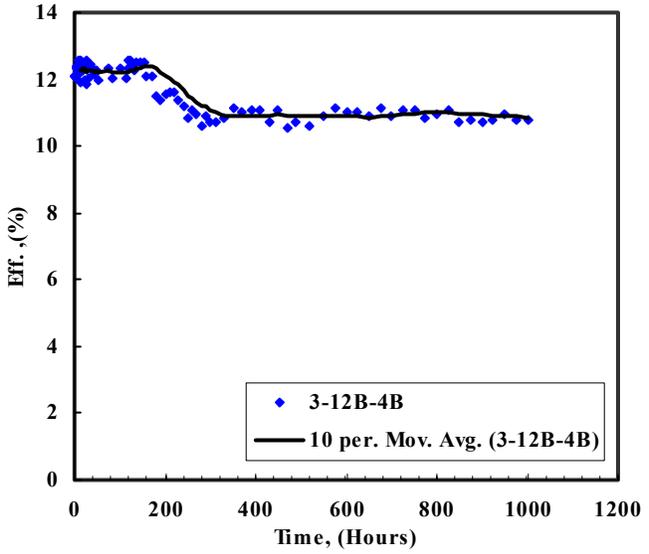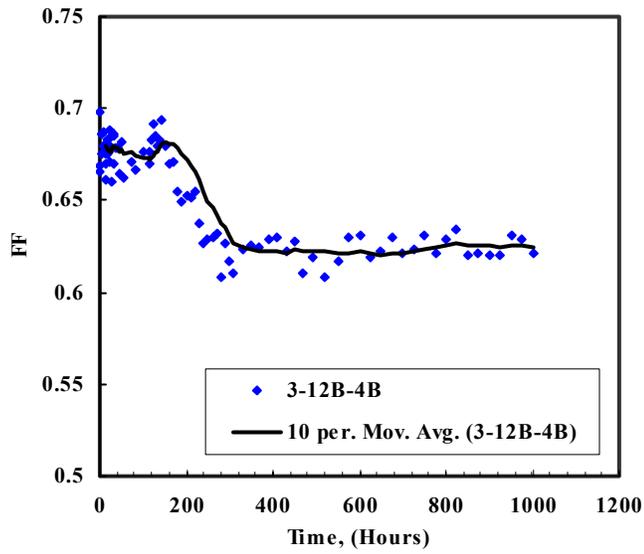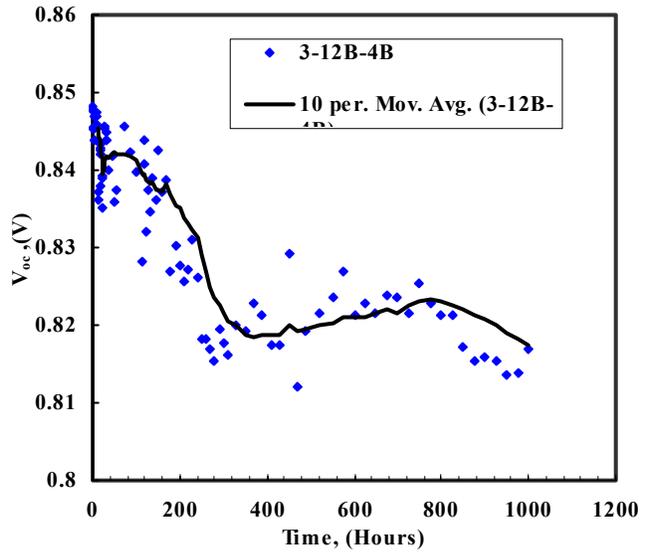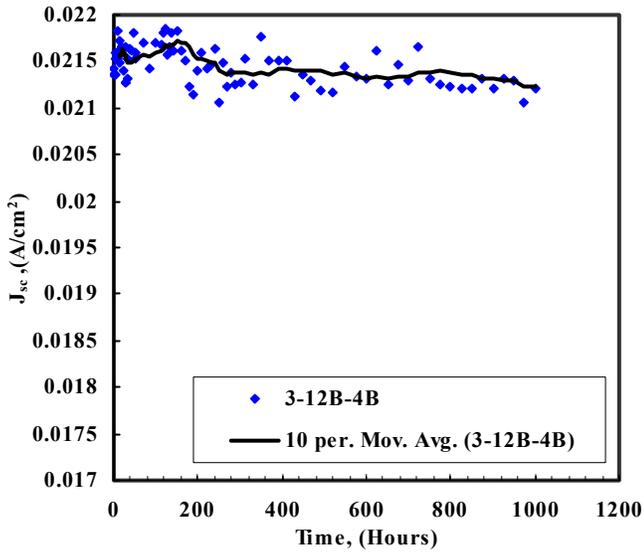
APPENDIX B – SET "C" LIGHT SOAKED AT T_{STRESS}=70ºC

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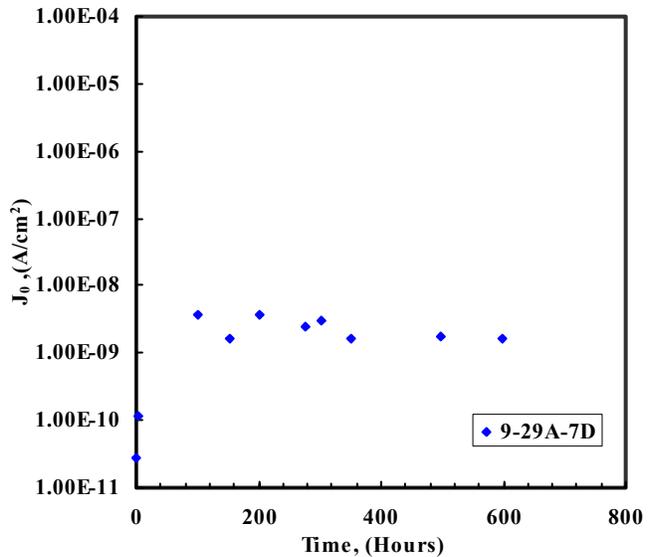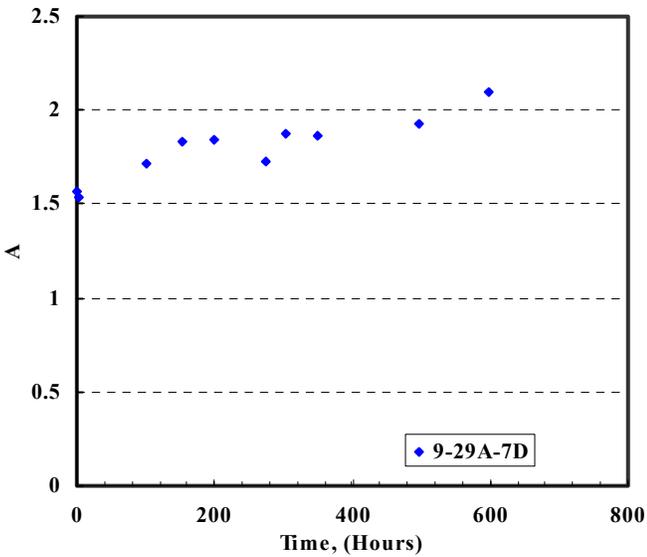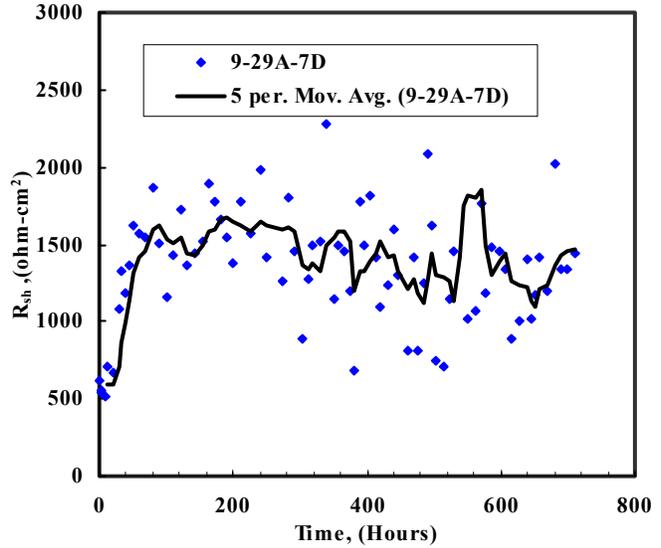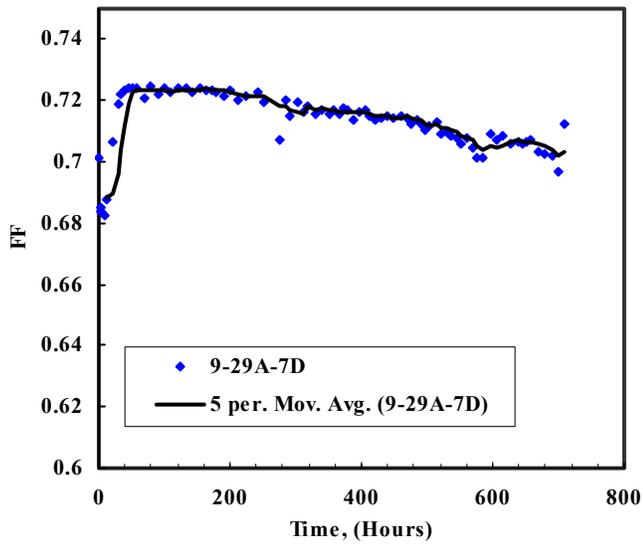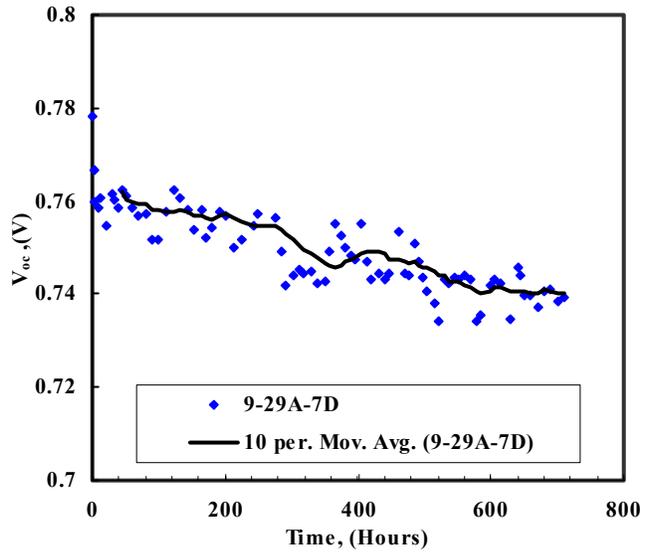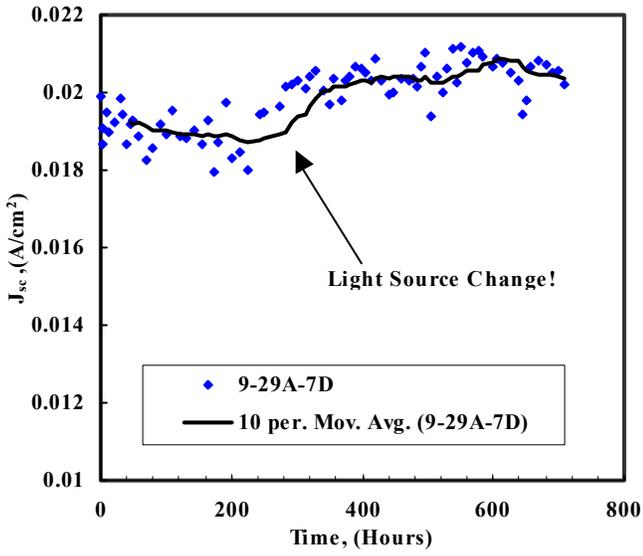
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PART II - CIGS

1.0   INTRODUCTION

This project has as its primary objectives the development of a manufacturable process for CIGS devices and the development of high band gap alloys for use in tandem structures. Additional objectives include development of improved junction formation processing and contributing to the overall understanding of these materials and devices. Because our processing is manufacturing driven, we use an all solid-state, simplified two-step process that relaxes the level of deposition control required. Our charter is to approach the levels of performance demonstrated by coevaporation with a more manufacturable process. Further details about our processing approach are provided below.

The high band gap alloys that we are developing are all based upon Ga. We have also worked with sulfur-based devices in the past(1), but feel that we can best proceed and contribute by focusing on Ga at this time.

With regard to junction formation we have had under development junctions formed directly with ZnO. This completely avoids Cd as well as an additional processing step. Since we have developed reactively sputtered ZnO for the conducting segment of the window layer, we have chosen to further develop its application to the resistive ZnO layer as well.

We process and analyze all of our devices within our own facilities. Material and device performance is primarily through device measurements and analysis. We perform the usual collection of standard measurements and augment these with advanced measurements as needed. This is also the case for material compositional and structural properties. Device and materials analysis is also guided by the use of several in-house models as well as the Penn State AMPS model.

Interactions with industrial partners of the national team are also under way. Results from these will typically not be discussed to protect the interests of the industrial partners.

1.1   Device Fabrication

Details of our deposition process have been described previously (2). We provide a brief description here for convenience. Our substrate is soda lime glass, which we purchase from the local hardware store. A standard glass cleaning procedure is used, and the glass substrate is heated in vacuum prior to Mo deposition by sputtering. Varying combinations of metal or metal selenide layers are deposited by sputtering or evaporation. These precursor layers are then annealed in a selenium flux through a temperature profile with a maximum temperature of 550 °C. Several process recipes are presently under development, and each involves specific precursor layers and anneal profiles. Much of what is presented in the following discussion is for our baseline process. In this process the order of deposition of the precursors is Cu/Ga/(In + Se). Deviations from this

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procedure will be presented as they arise in the ensuing discussion. Formation of the semiconductor layer takes about one-half hour. The substrate is finally turned into a device using standard procedures for CBD CdS followed by high ρ/ low ρ ZnO.

Because of the very complex nature of these materials we have found it useful to intentionally grade compositions. The relative location of the sources relative to the 2" x 2" substrate is shown in figure 1. Each source can be made to vary in deposition rate to result in a thickness difference of 5 to 10% from the near edge to the far edge of the substrate. The resulting compositional gradients allow for a richer data base and avoid issues associated with run to run variables when precise comparisons are necessary. By adjusting our run parameters we can operate in regimes which have both high and low sensitivity to the compositional profiles. This is also useful for avoiding high sensitivity processes that would be unacceptable at a manufacturing level.
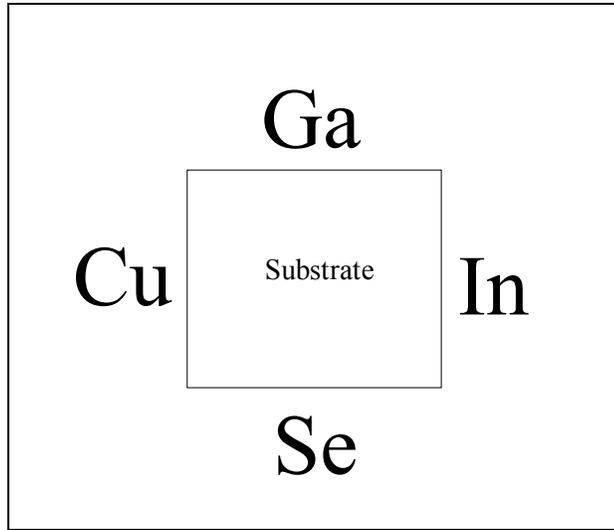
Figure 1. Arrangement of sources around the 2" x 2" substrate.

2.0   INCORPORATION OF GA IN LOW BAND GAP DEVICES

In previous reports we presented results relating to the incorporation of Ga in our devices. This is one of the key challenges of our two-step approach to processing. Basically we have to deposit the Ga in a layer and then use subsequent processing steps to get it to go where we want it to go and then to bond effectively. On the basis of a small number of runs our previous results indicated that there were sweet spots in deposition space which resulted in highly efficient Ga incorporation which led to improved performance. We have subsequently more fully
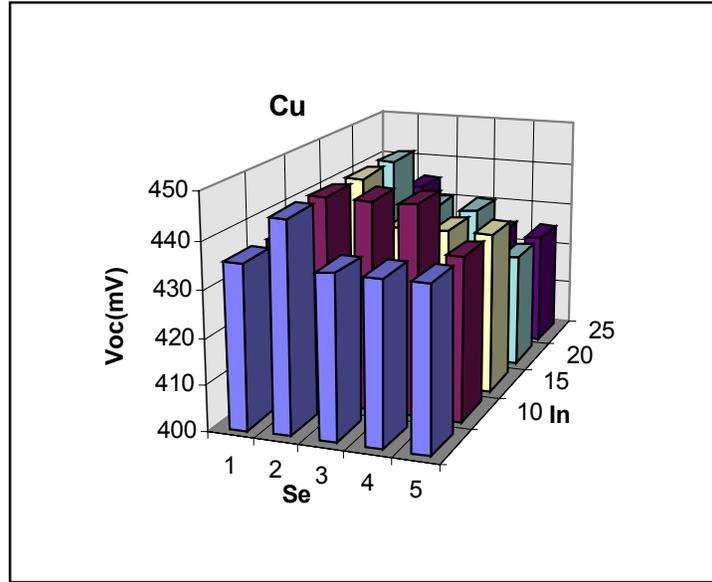
Figure 2. Voc profile for run 155.

explored these areas and have new results and insights to report. In the discussion which follows we will refer to our previous results in terms of what will be called our "standard run". Deviations from this run will be presented and discussed.

One of the important observations from our previous results was that small increases in band gap, presumably due to small quantities of Ga entering the space charge region, resulted in improvements in Jsc due to increases in both depletion width, W, and diffusion length, L. The amount of Ga that enters the SC region is due to a combination of factors including the Cu/In ratio. In run 155 we decreased the Cu/In ratio by 7% relative to the standard run (and lowered the Ga to compensate) to try to tune the amount of Ga in the SC region. The Voc profile for the 5 x 5 array of devices is shown in Fig 2. Spectral response data is shown in Fig. 3. The devices are numbered from 1 to 25 along the columns and rows as indicated in Fig. 2. The location of the sources, Cu, In and Se are as indicated. Ga is opposite Se though not indicated in the figure. Devices in the center have the highest Voc's. As we shall see, this is the result of a complex interplay of contributing factors.

The spectral responses in Fig. 3 reveal trends associated with compositional variations. In the standard run devices in the Cu-Se quadrant are observed to have typical band gaps of 0.95 eV, while those in the Ga-In quadrant have higher gaps - up to 1.07 eV. Devices on the Cu-Se side of the device 5 to 21 diagonal and near it exhibit the small increases in Eg and improved collection properties. By increasing the In level in this run we have moved the expected location of these devices toward the Cu. The spectrum exhibited by device 1 in Fig. 3 with a band gap of 0.97 eV is typical of the devices from the standard run
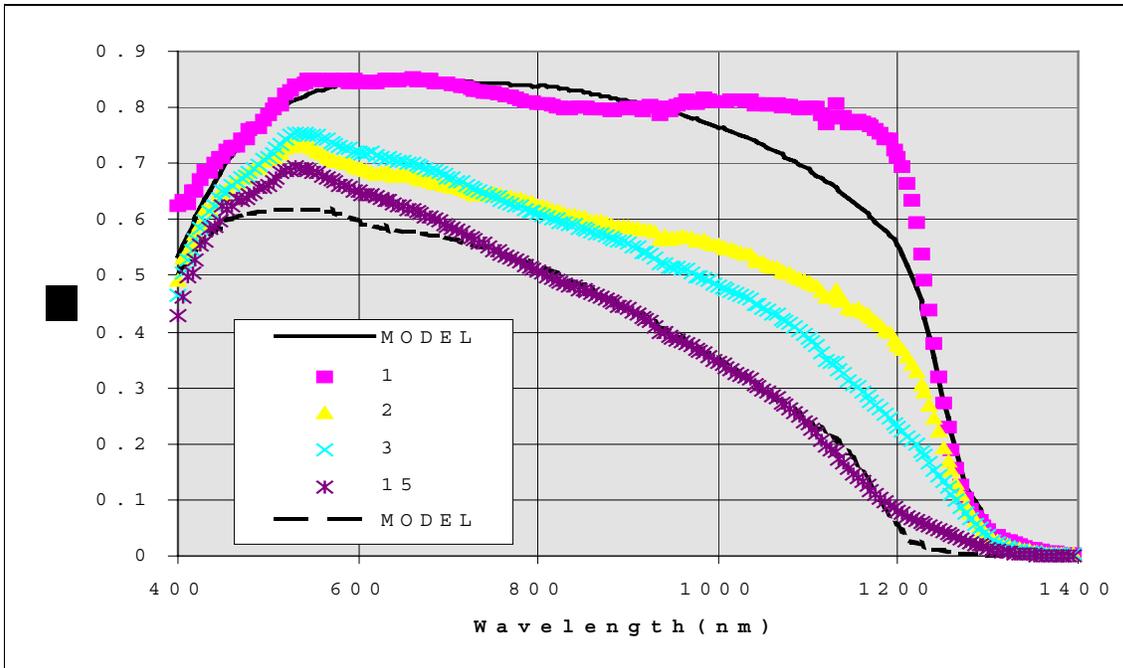
Figure 3. Spectral response for several devices from run 155. Modeled curves use the data in Table 1.

 verifying that the region has been shifted up as expected. As we go down column 1, however, starting at device 2 there is already evidence of the negative effects of too much

Group III entering the SC layer. At this point we note that since the Ga level should be the same for devices in column 1, we must blame this negative effect on In. This is not unexpected since we have increased the In level, but it is surprising that the downturn takes place between two adjacent devices that are spaced only a few mm apart. This occurrence due to Ga is not unlike that seen in standard devices in which the band gap and collection properties change abruptly between adjacent devices. Taken together these results imply (tentatively) that these devices are very sensitive to the Cu/Group III ratio. The good news is that Ga itself is not the problem. The bad news is that since Ga is nevertheless a member of Group III, we can't constructively add it to the space charge layer in this way.

Forcing more Ga into the mix further complicates things as seen in the spectrum for device 15. This device which is closer to the Ga source indicates a much stronger drop off in QE with increasing wavelength. In fact, in order to model the spectrum a change in band gap to 1.02 eV is necessary. Band gaps are determined by fitting QE spectra to a standard current collection model. The model is primarily directed toward band edge, diffusion length and space charge width determination and does not have refinements relating to interference phenomena and the like. It nevertheless allows useful comparisons among the key parameters. The parameters used to fit the data in Fig. 3 are listed in Table I. As can be seen, devices 1,2 and 3 were fit with an Eg of 0.97 eV, while device 15 required a shift to 1.02 eV. The effect of increasing Group III on the collection properties can also be seen. Increasing In causes significant deterioration of diffusion

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length by nearly an order of magnitude between device 1 and 3. Adding Ga causes an additional loss of a factor of three. A noteworthy aspect of the spectrum for device 15 is

Device	Eg	W(microns)	L(microns)
1	0.97	0.15	1
2	0.97	0.1	0.3
3	0.97	0.15	0.15
15	1.02	0.1	0.05

Table 1. Modeled parameters for devices from run 155.

the tail starting at 1200 nm. This is interpreted in terms of the presence of a residual 0.95 eV gap layer in the SC region. This layer is likely to be near the CdS, and if so, it would largely determine Voc. As can be seen in Fig. 2, the highest Voc's are not on the Ga side where the highest band gaps are expected. The small range in Voc's in fact suggests that they are likely more driven by lifetime fluctuations than by band gap. The drop off in transport properties in going toward the Ga-In quadrant could indicate a corresponding decrease in recombination lifetime in that region which would cause a drop in Voc to compensate for any increases in Eg that might occur.

Another complicating factor in this analysis is the interplay between Se and the Group III components. This is evidenced by the fact that the QE spectrum for device 25 (not shown) is similar to that of device 3, that is, the shift in band gap exhibited by device 15 is not present in device 25. Although device 25 is closest to the Ga source, the Se flux is also lowest there which favors the formation and removal of volatile Group III - Se species. We have observed these effects on other occasions and are still trying to characterize their behavior. More data is required.
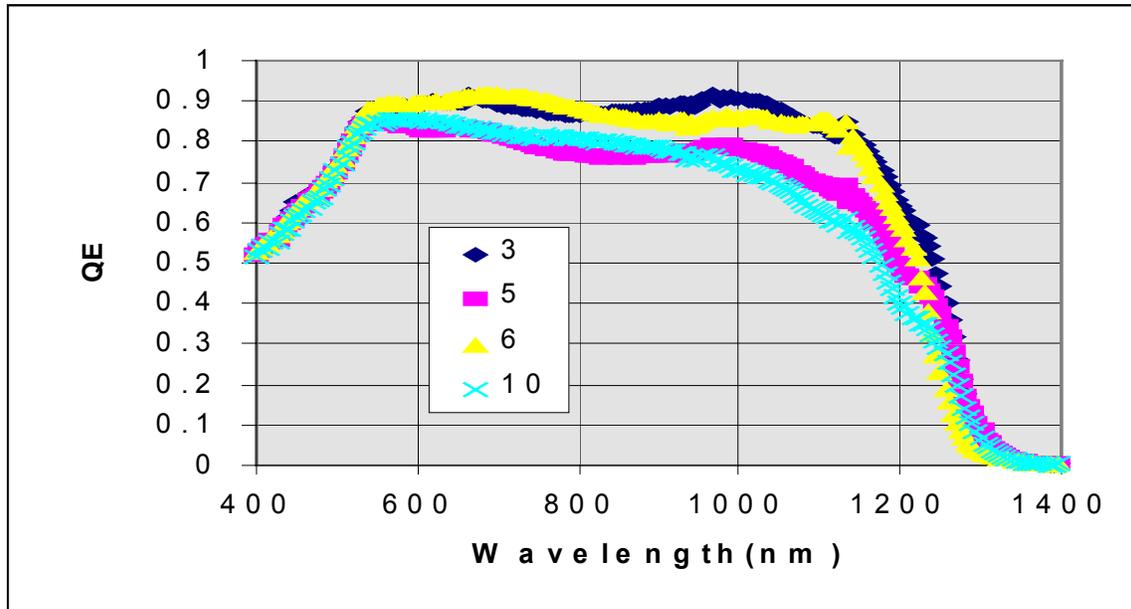
Figure 4. Spectral response for run with Ga introduced in a different precursor location.

In another run we examined the effect of changing the location of the Ga in the precursor layers relative to the other components. The run is the same as the others except that Ga was added earlier in the run. The representative spectral responses in Fig. 4 indicate no notable shift in band gap. The band gaps are 0.95 eV with devices 5 and 10 indicating some deterioration in collection for the In-rich devices. Device 6 does indicate a slight upward shift in Eg. However, the bottom line seems to be that the Ga does not make it into the SC charge region unless it is added later in the run. This is in keeping with its known tendency to migrate toward the rear of
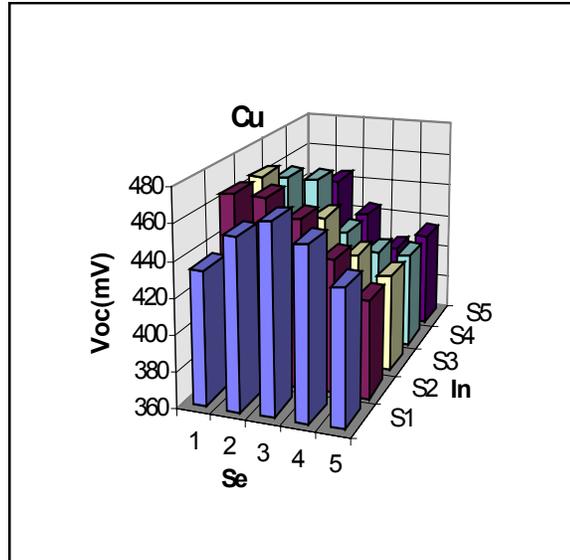
Figure 5. Voc profile for run with Ga introduced in a different precursor location.

the device. The Voc behavior for the array is shown in Fig. 5. Voc's in this case are about 20 mV higher than the previous run and favor the Cu-Se quadrant. This is again suggestive of a reduced adverse effect of excess Group III on recombination lifetime.

From the above runs we are learning that understanding the incorporation of Ga is not straightforward, but we are beginning to zero in on a few recurring themes. One in particular that attracts our attention is that there is a regime in deposition phase space in which small quantities of Ga can be incorporated in the space charge layer in a constructive manner. There is a small upward shift in band gap to the 0.97 - 0.99 range with an accompanying improvement in collection properties. This is the desired effect, which we are seeking. What we need to do next is realize the expected improvement in Voc that should accompany the upward shift in band gap. While much of our thinking regarding Voc centers on the behavior of the recombination lifetime, we are also confronted with the possible presence of a low gap region next to the CdS as discussed above. This would have the effect of "pinning" the Voc while the band gap of the bulk of the space charge layer is increased. One way to attack this issue is to increase the amount of Ga to increase its chances for competing with In in the important interface region. To test this idea in the next run the amount of Ga made available to the SC charge layer was increased by 50%. The spectral responses for representative devices on column S3 are shown in Fig. 6. The band gap shift is in the range 0.15 - 0.2 eV indicating significant encroachment of Ga into the space charge layer. The drop in carrier collection, however, is dramatic. In fitting the data with the spectral response model as shown, the resulting parameters were a depletion width of 0.15 microns and negligible diffusion length. The collapse of the diffusion length raises concerns that an inverted band profile might be hurting carrier collection. That is, the tails out to 1300 nm in the devices discussed above were interpreted as a low gap region near the CdS interface. If the low gap region were instead behind a higher gap region, which was at the CdS interface, this would hurt the
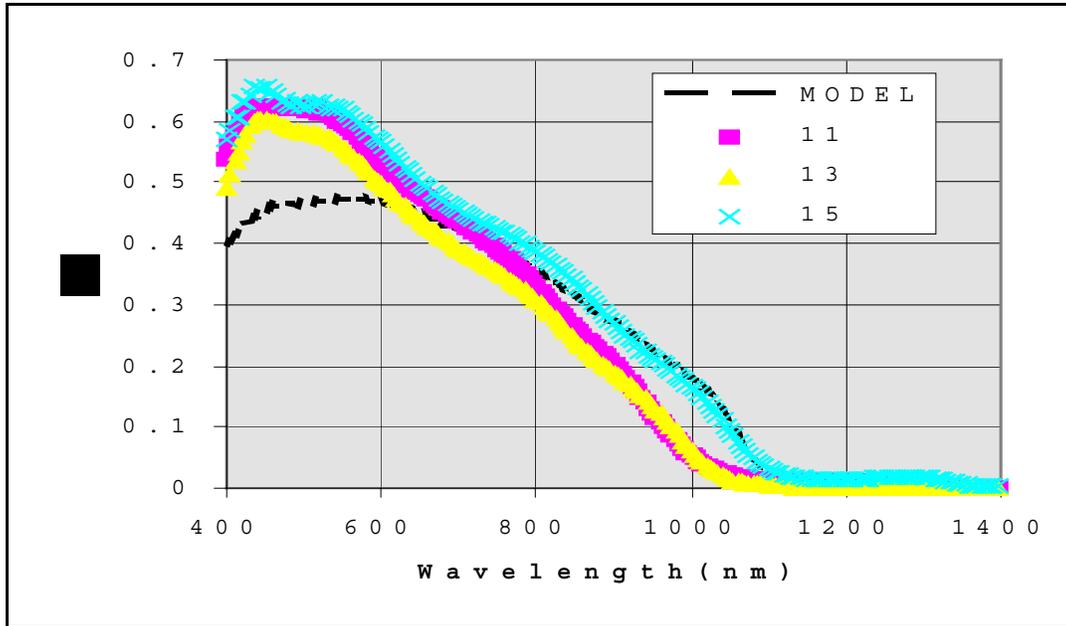
Figure 6. Spectral response for a run with increased Ga in the SC layer.

collection of minority carriers. Such a situation would also be expected to result in a poor FF, however, the FF for these devices is in the range 0.6 to 0.63 which is reasonable and not indicative of an inverted band profile. Another puzzling factor is the observation that the modeled curve falls below the data at short wavelengths in Fig. 6. Taken together the only tentative explanation that can be offered at this point is that these devices have a bilayer structure and a complex field distribution profile. This might explain the improved collection at shorter wavelengths, but further work is required to sort this through.

The Voc profile for the run is shown in Fig. 7. Voc's up to 575 mV are observed which is a 100 mV increase over devices with the standard Ga level. This still represents only about half of the voltage increase expected from the band gap shift. Since the evidence suggests that more Ga is near the CdS interface, which is thought to be the main recombination region, suspicion must be cast on Ga as the lifetime reducing agent. The bilayer structure hypothesized above, however, could provide a different perspective on voltage behavior. As seen in the figure, Voc favors the
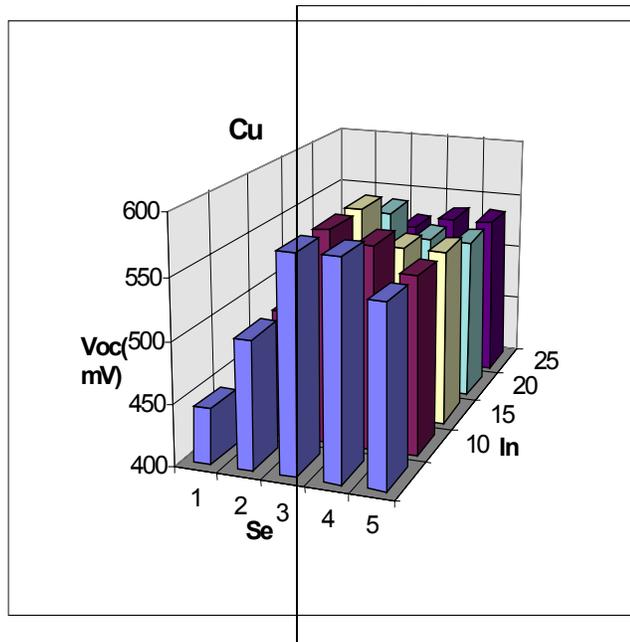
Figure 7. Voc profile for a run with increased Ga in the SC layer.

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central region, especially toward the Se source. This in part suggests a strong role by Se flux in forming the important interface region, but it equally can be interpreted as an aversion to Ga at these high Ga levels. This issue can be resolved by keeping Cu, In and Ga constant while varying Se flux, especially near the end of the run where the interface is formed. Such experiments are being planned and the findings will be reported in future reports.

3.0   HIGH BAND GAP DEVICES

3.1   Background

Much of our work on high band gap devices prior to this project focused on CGS. As with CIGS we used a two step approach to processing. While we were able to achieve absorbers and devices with reasonable electronic properties, they were not on a par with CIGS devices. There have been ongoing discussions in the literature suggesting that the high gap devices are expected to be more defective. Recently the theory group at NREL presented results suggesting that it is harder to form an n-type region in Ga rich compounds(3). This suggests a device format limitation as opposed to a fundamental limitation to performance. Given these expected shortcomings of high Eg compounds, it is important to develop a solid understanding of the dominating mechanisms, and given the complexity of these compounds we should not jump to conclusions too quickly or expect solid understanding to come easily.

In the above discussion of our standard CIGS devices we are at the other end of the spectrum. Our approach to optimization has centered on including only small amounts of Ga. This is a consequence of the constraints we have put on our processing approach based upon our concerns with manufacturability. In developing our CIGS process we varied the deposition conditions to include more Ga and effect larger band gaps. While some of these devices produced our best FF's to date, their overall performance was never quite as good as our low Eg devices, and so our pursuit of the underlying issues relating to these was shelved. Now that we have as an objective the development of high Eg devices we must go back and systematically explore the effects of significant Ga content on film and device performance. The approach that we follow is the same as that used for low gap devices, attempt to separate surface and bulk properties so that each can be independently optimized. To this end we start by trying to maintain Jsc while increasing Eg.

An issue of some importance to these activities is the relative reactivity of Ga and In. As discussed in previous reports our processing approach requires optimization of kinetics and thermodynamics, and these must be optimized within the context of device format. Thus because of the advantages of providing a favorable field profile by grading the band gap upward toward the rear of the device we set up deposition conditions to provide more Ga to the back region. In our baseline process we accomplish this by depositing the Ga layer before depositing In. This results in devices with an Eg of 0.95 eV in the SC region. By tuning the deposition conditions, however, we are able to coax small quantities of Ga forward as evidenced by increases in Eg in the SC region. Using this approach we have increased Eg up to 1.07 eV, however at the price of diminished electronic properties. Our best devices have an Eg just at 1.0 eV. We in fact observe an improvement of electronic

properties as we raise the gap from 0.95 to 1.0 eV. We have reported these effects previously(4) along with the observation that the properties can diminish abruptly with only a small incremental increase in Ga incorporation. To proceed with the development of high Eg devices it is important to understand these mechanisms, and thus we have changed our focus to studying the mechanisms of adding increasing levels of Ga to CIGS.

3.2   Effects of the Deposition Sequence on Material and Device Properties

In our baseline process the order of metal depositions and their relative thickness (in parentheses) is Cu(1500)/Ga(1500)/In(3600). The thickness is the reading in angstroms from the thickness monitor and corresponds relatively, but not exactly to the thickness on the substrate. Over the 2" x 2" substrate these values result in a Cu/(In + Ga) range of 0.85 − 1+. If we maintain this profile and increase the Ga (and Cu in proportion) we observe little change in performance. Basically all this does is to increase the thickness of the rear high Eg region. It also implies that the Ga and In do not intermix significantly, while the Cu finds it way through both. If the Ga level is increased much further, Se has difficulty penetrating to the bottom of the film and deterioration sets in.

Thus to have Ga bond in the SC region we can not depend on it migrating there, but must place it there by deposition. The first approach that was taken was to split the Ga deposition as follows: Cu(1500)/Ga(750)/In(3600)/Ga(750). A typical spectral response from this run is shown in figure 8. The band gap has not changed, but the electronic properties have diminished somewhat. Thus in spite of the fact that a significant amount of Ga was deposited on top of In, it basically all migrated to the rear of the device to leave In in control of the space charge region. Thus kinetics is not the issue here. It is thermodynamics. Our processing conditions favor formation of CIS over CIGS.
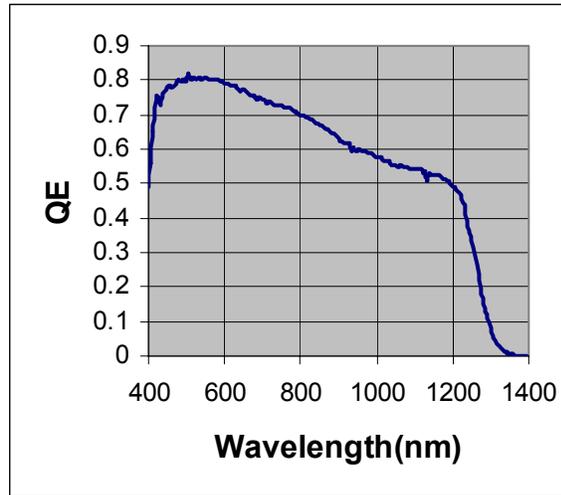

Figure 8. QE spectral response for a run with split Ga deposition.
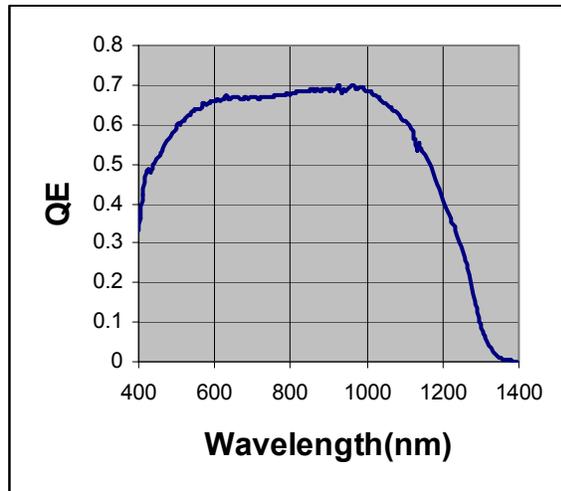

Figure 9. QE spectral response for a run with split Ga and favorable conditions for Ga

In another run in which the Ga split was as follows: Cu(1500)/Ga(1125)/In(3600)/Ga(375) and in which we made other modifications to the deposition conditions we achieved the response shown in figure 9. There are two pieces of positive information here. First, there is some erosion of dominance by the low band gap as evidenced by the roll off at 1000 rather than 1200 nm. This indicates that while part of the SC region has the typical 0.95 eV gap, a significant part has a higher gap. Second, although the overall spectrum has shifted down a bit, the curve remains flat out to the 1000 nm downturn. This suggests maintenance of good transport properties. We are presently under taking more extensive analysis of these results to better understand their implications.
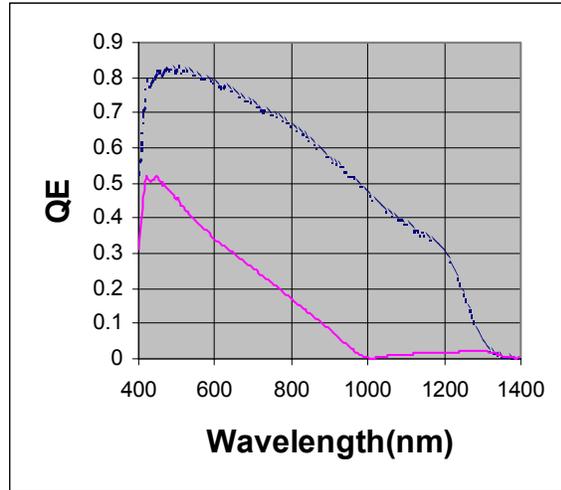
Figure 10. QE spectral response for run with 750/750 Ga split and lower In level. Upper curve is for device a. near the In source. The lower curve is device b.

To provide further insights to these mechanisms we reran the 750 Ga slit run with a lower In level. The profile was: Cu(1500)/Ga(750)/In(3300)/Ga(750). Two QE spectra from the run are shown in figure 10. Device a. was near the In source and indicates the typical low band gap/diminished transport properties profile as for the device of figure 8. Device b. is a bit further from the In source, and as can be seen there is a dramatic change in performance. Although it is not as apparent here as in the next figure, there is evidence of a dominant larger band gap, although accompanied by significant deterioration of transport properties. And there is evidence of a residual low band gap represented be the tail out to the 1300 nm region. In a subsequent run the conditions were identical but the In was further lowered to 3000. The QE spectrum for the device at the same position near In as the above is shown in figure 11. The dramatic shift in performance which occurred in moving across the substrate away from In in the previous run has now been created across the entire substrate. Also, the presence of the higher dominant band gap of about 1.3 eV is more easily observed here. These results are complex and will require ongoing study. However, they strongly suggest that a Cu rich environment improves the bonding competitiveness of Ga. This is an encouraging result that we are now pursuing. It gives us just the kind of opportunity we were seeking to differentially control the behavior of Ga.
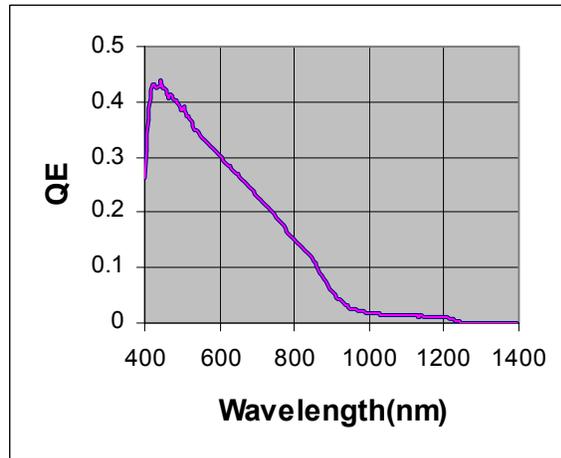
Figure 11. QE spectral response for a run similar to that for the run of figure 10 but with lower In.

3.3   Effects of Substrate Temperature on Material and Device Properties

One of the trademarks of our deposition process has been the use of sputtering to deposit metal layers because of its acceptability as a standard manufacturing tool. We have demonstrated that sputtering can be used effectively for metals, while Se is best deposited by evaporation. This is not a major issue in a manufacturing environment since accommodations for the incompatibilities of these processes can be handled be using separate chambers. However, in a University R&D environment in which a single chamber is used for all depositions, it is more convenient to use compatible deposition processes. Consequently we have systematically replaced sputtering with evaporation for metals. With the exception of Ga there seemed to be no notable differences in outcome. When we changed from sputtering to evaporation for Ga, however, we observed about a 50 mV drop in Voc values. This suggests that the details of the sputtering environment may be providing more favorable conditions for film growth. Since in our deposition sequence Ga is deposited on a predeposited Cu layer, these conditions involve the interaction of Cu and Ga. It is commonly known that sputtering is a more energetic process than evaporation. The arriving species, the sputtering gas and electrons all deliver energy to the growing film which is not available during standard evaporation. This excess energy can be very high at a local level and allow formation of species not accessible at the nominal substrate temperature. The excess energy can also be distributed and result in a higher substrate temperature. To understand the performance differences we were observing we conducted a series of experiments using thermal evaporation of Ga in which the substrate temperature was varied. We wished to learn if the excess energy provided by sputtering could be replicated by substrate thermal energy.

Figure 12 Voc profile for no heat during Ga deposition.

In figure 12 we show the Voc profile for a run which replicates our standard run process with the exception of deposition of Ga by evaporation rather than sputtering. (See figure 1 for orientation of sources.) In this process no heat is applied to the substrate during Ga deposition. Prior to Ga deposition the Cu layer is deposited at
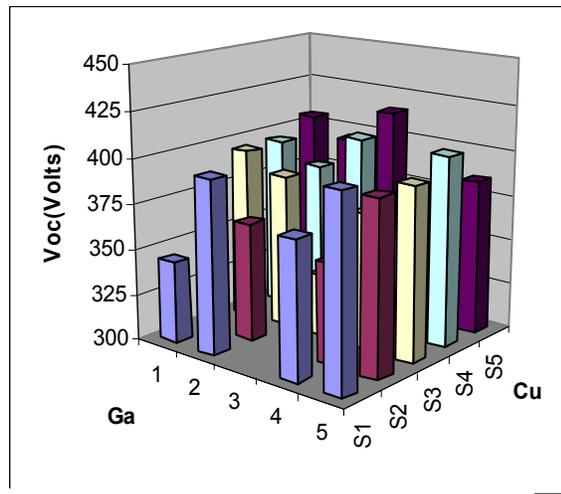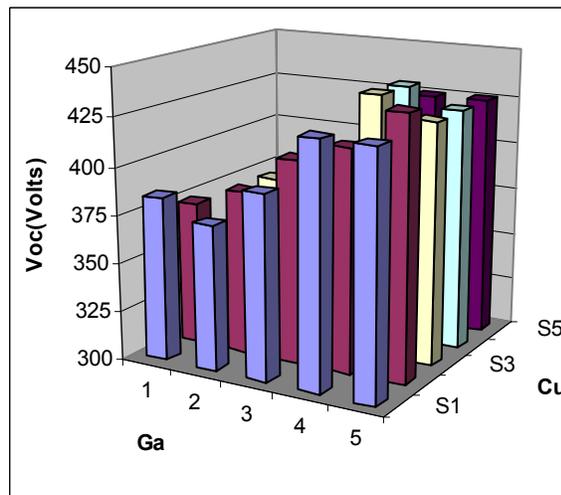

Figure 13. Voc profile for Ga deposition at a substrate temperature of 275 C.

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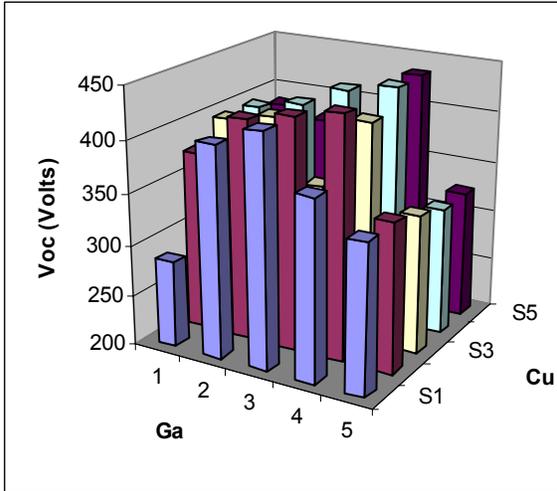
Figure 14. Voc profile for Ga deposition at a substrate temperature of 275 C and a higher Cu level.
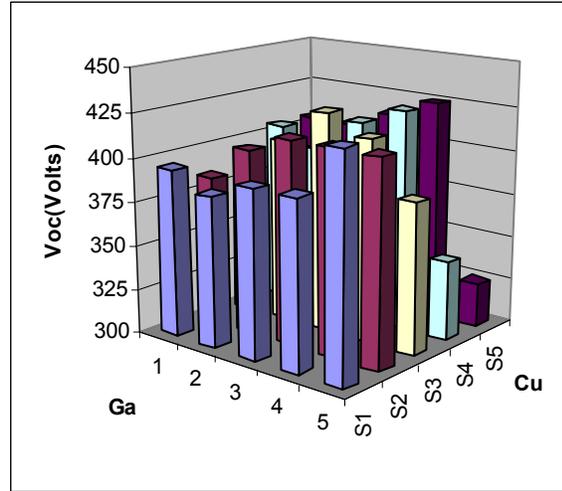
Figure 15. Voc profile for Ga deposition at a substrate temperature of 350 C.

275° C. During Ga deposition the substrate temperature falls to about 100° C. As can be seen, the performance is spotty with only a few devices above 400 mV and no clear trends. In figure 13 we show the profile for the same run conditions except that the substrate temperature during Ga deposition was held at 275° C. There is now a strong trend in rising Voc toward the Cu source. This indicates a much more favorable bonding environment that was not achieved with no substrate heating. Based upon our deposition thickness for the metals we know that the Cu/Group III ratio is near unity on the Cu side. In figure 14 we see the result of adjusting the metal ratios so that we see the edge where Cu/Group III exceeds 1. As we have observed and discussed previously there

Figure 16. Voc profile for Cu and Ga deposition at 350 C.

is a strong drop in Voc at this edge. The overall behavior observed here is not unlike that for sputtered Ga except for the lower magnitudes of Voc. There are also details regarding Ga bonding that we shall discuss further below. However, we first want to provide additional data on the effects relating to substrate temperature. In figure 15 we show the Voc profile for a higher substrate temperature of 350° C during Ga deposition. The Cu/Group III > 1 edge is still present, but there are additional stronger profiles relating to metal ratios that are not as apparent at lower temperatures.

One additional datum is the result of depositing both Cu and Ga at the elevated temperature of 350° C. As seen in figure 16 the Cu/Group III > 1 drop off has become more dramatic. While for the run of figure 15 higher Ga levels are favored, in this case the most pronounced
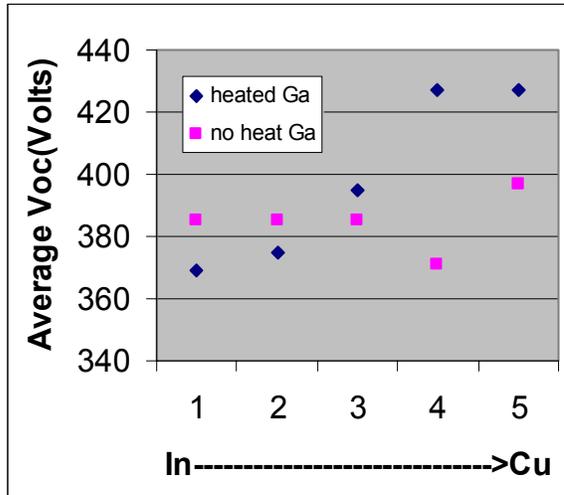
Figure 17. Average Voc vs. Cu/In ratio for Ga deposited with and without substrate heating.
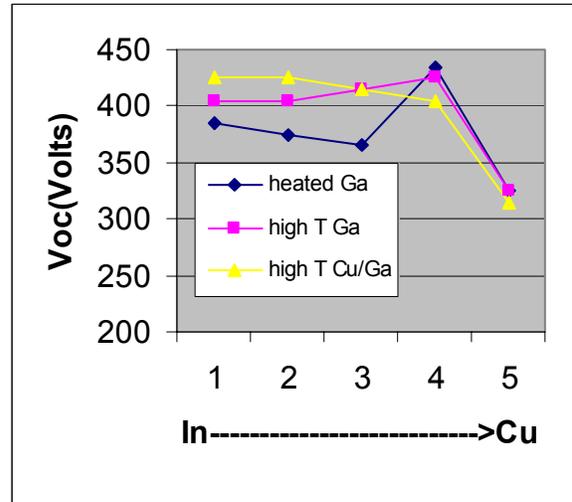
Figure 18. Voc vs. Cu/In for various Ga deposition temperatures for low Ga.

drop off is near Ga. This suggests very profound bonding and electronic property sensitivity to the energetics of the deposition.

To examine these mechanisms more carefully we will focus on the effect of Ga incorporation. To do this we first look at the dependence of performance on the Cu/In ratio. Using figure 15 as a reference, we look at the average performance in each row(1 to 5). In a given row the Cu/In ratio is constant, and, in going from column S1 to S5 within a row there is a diminishing Ga level. The Se source is opposite the Ga source, so we are also seeing the effect of an increasing Se flux level in going from S1 to S5. We tune our processing conditions to make Se flux a secondary effect, and generally once we have a defined process, we find Se flux not to be a major driver. We will assume this to be the case here, however, we do not yet have sufficient data in this new regime to claim this with certainty.

Proceeding under the assumption of ineffective Se we first look at the overall effect of heating the substrate during Ga deposition. To do this we take the average of the Voc's down each row for the data of figure 12. We do the same for the data of figure 13. We compare these because the Cu/Group III ratio is such that we have not pushed the ratio beyond the drop off edge. The results are shown in figure 17. For devices with no heat during Ga deposition there is a slow rise toward increasing Cu. For devices with heating during Ga deposition there is a much stronger rise toward Cu which is characteristic of devices made with sputtered Ga. Thus providing thermal energy during Ga deposition predisposes the Cu/Ga layer to more favorable bonding with In and improved electronic properties.

To understand the direct influence of Ga we look separately at the two regions farthest from and closest to the Ga source which are columns S5 and S1 respectively. These are shown in figures 18 and 19 for the various run temperatures discussed above. For the

region away from the Ga source(figure 18) additional thermal energy supplied either during Ga or Cu deposition improves uniformity. In the case of higher temperature for both Cu and Ga the usual rise in Voc as Cu/In = 1 is approached is eliminated. At higher Ga levels(figure 19) things are quite different. Firstly, there is more Group III material on this side, so the Cu/Group III > 1 edge should be shifted more toward Cu. As can be seen it appears to be shifted in the other direction. Since in this region the Cu/Group III ratio should not exceed 1, there should be no edge. The drop off on the Cu side is rather interpreted as inefficient incorporation of Ga. As the substrate temperature for Ga is
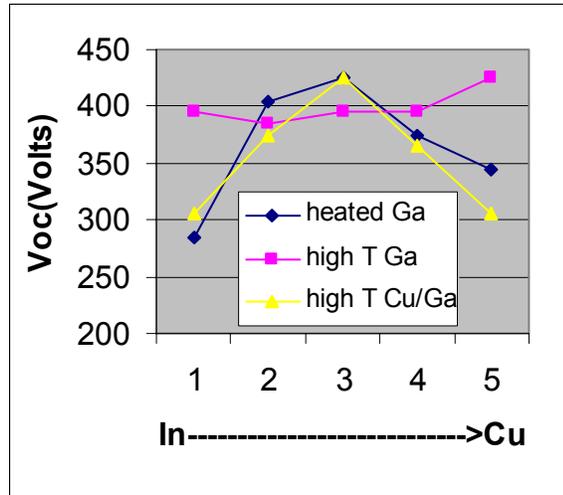
Figure 19. Voc vs. Cu/In for various Ga deposition temperatures for high Ga.

raised to the high T (350° C) level, there is no drop off or edge. There is only the typical rise toward Cu as the edge is approached. This is what is expected and suggests that higher substrate temperature during Ga deposition is perhaps able to mimic the energetics during sputtering. The profile for the high Ga temperature case suggests that the peak Voc will be higher than the results obtained to date. We will determine how much higher in future experiments.

A puzzling result in figure 19 is that for the case in which both Ga and Cu are deposited at high temperature. As can be seen, the behavior looks similar to the standard "heated Ga" case. The edge is again present and appears to be steeper than the standard case. This contrasts with the low Ga region in which the higher temperature had a smoothing effect on the profile. Needless to say, there are several complex mechanisms at play here that will require additional data to sort out. However, we are encouraged by both the insights provided by our growing database and our ability to reasonably understand and control these mechanisms. Out of these efforts have come several new paths to follow which promise improved performance.

4.0   ZNO/CIGS JUNCTIONS

Because of the interest in replacing CBD CdS with a more acceptable contact material/process we have extended our efforts with reactively sputtered ZnO. Initially we were just interested in developing a faster process for the doped ZnO layer. By using a Zn target we can deposit at very high rates and maintain good properties in doped ZnO. Recently we turned our attention to replacing the CdS layer with this same process. This was ambitious at the outset because of the supposed sensitivity of the CIGS interface to air/oxygen and the fact that the reactive atmosphere for ZnO contains excited oxygen species. We nevertheless persevered and reported results comparable to the best literature results at the last World PV conference(5). Meanwhile Larry Oleson at Washington State has demonstrated near state-of-the-art performance using CVD for ZnO deposition(6). We are thus encouraged that a ZnO/CIGS junction can work, and we hope to show that reactive ZnO can be used as the deposition process. It is also the case that this major modification to junction formation will add to our understanding of its operation. This can lead to further improvements with CdS junctions and perhaps to new junction alternatives.

There are two key issues that must be addressed for ZnO to succeed as a replacement for CdS. First, it must be demonstrated to work as well as CdS, i e, achieve equivalent device efficiency. Secondly, the deposition process must be acceptable. With regard to the latter it is apparent that physical vapor deposition would be acceptable if uniformity and throughput can be achieved. Sputtering has clearly demonstrated large area uniformity in a production environment. However, if a ceramic target is used, the deposition rate can be unacceptably low. We have chosen reactively sputtered ZnO for this reason. What remains then is to demonstrate acceptable device performance using this deposition technology.

We have undertaken extensive studies of the reactive sputtering environment and have developed techniques for depositing state-of-the-art films in terms of conductivity and transparency. Details of our deposition techniques and doped ZnO film properties have been previously reported(7). The specific issue we confront in this study is that of controlling the interface. It is commonly known that in standard CdS/CIGS devices the ZnO over layer is a double layer having a high resistivity layer next to the CdS. The dopant in the conducting top ZnO layer is commonly Al or B, and it is thought to be important to isolate this doped layer from the CdS. Ongoing studies suggest that this may not be necessary, but the requirements for this region are not yet known. In this case we are confronted with exposing the semiconductor surface to the reactive environment. Needless to say, deposition of the initial ZnO layer on the CIGS surface is the most critical step of the deposition process. It is also the case that the semiconductor surface can be tuned to the requirements needed for this environment. In the case of CIGS we have not yet changed its surface properties to address these special circumstances. The semiconductor substrates, which we use to form ZnO/CIGS devices, are the same as for our standard CBD CdS process. However, there are techniques, which we apply to mitigate the reactive environment during deposition of the ZnO layers. These techniques result from developing control and understanding of undoped reactively sputtered ZnO.
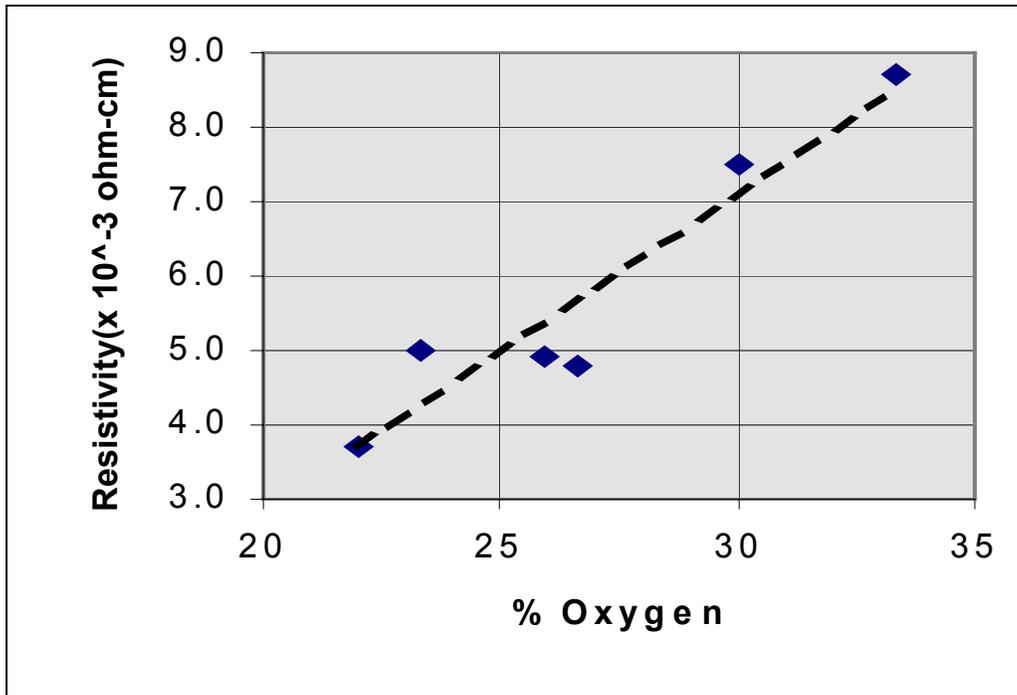
Figure 20. Resistivity versus oxygen content of the sputtering ambient at

T = 200° C.

Although these layers contain no extrinsic dopant, defect conductivity is effective. In figure 20 we show the dependence of conductivity on oxygen flow. We studied the dependence of device performance on the defect controlled conductivity of the ZnO buffer layer and have found the best performance to date when the resistivity is high. This suggests that prevention of dopant migration from the doped layer is not a primary function of the buffer layer. However, it could be argued that the oxygen vacancies, which contribute charge carriers also, provide migration paths for dopants from the doped layer. We hope to sort this out in future studies, but for now we turn our attention to device performance. In the results reported here all devices had an undoped ZnO buffer layer thickness of 1000X

Efforts to fabricate ZnO/CIGS devices using reactive ZnO have generally resulted in poor performance of all three device parameters indicative of deterioration of space charge layer properties as well as interface properties(7). For devices with a band gap of about 1 eV we observed Jsc's of only 32 mA/cm^2 , while our standard CdS devices typically yielded Jsc's of 40 mA/cm^2. Voc's were below 400 mV and FF's in the low .4 range. Our manufacturing-friendly approach to device fabrication has always been based on techniques to determine how to independently optimize surface and bulk properties. In this case we were confronted with low Jsc's which indicated that the effects of the ZnO deposition were being felt deeper than the interface region. This is suggestive of an ion

bombardment issue rather than a reactive environment issue, and indeed the steps that we took to reduce bombardment yielded positive results. In table 2 we show results from

Device	Jsc(mA/cm^2)	Voc(Volts)	FF
7-7	37.8	.37	.48
12-7	41.0	.38	.45
12-9	41.8	.38	.38
26-1		.41	.54
26-6		.39	.56

Table 2. ZnO/CIGS device parameters for reactively sputtered ZnO.

several recent runs in which we systematically controlled the deposition environment. As can be seen, we have achieved Jsc's in excess of 41 mA/cm^2. The current densities are determined by integration of the QE spectral response using NREL calibrated reference cells. The QE response for device 12-7 is shown in figure 21. Also shown are responses for typical CdS devices. As can be seen, the band gaps for the CdS devices differ by a small amount. This is due to the different location of the devices relative to the CIGS source materials. Device 148-12 is closer to the Ga source and is expected to contain more Ga than device 148-4. Its band gap is shifted downward accordingly. The ZnO device 12-7 indicates a smaller band gap which implies that the Ga content in the space charge layer is below the alloying level. Its band gap is 0.95 eV, the same as CIS. Notwithstanding the fact that the ZnO device has the lowest band gap it clearly generates more current than the CdS devices. Some of the increase is due to fortuitous interference fringes at the red end, but the superior optical properties of ZnO can clearly be seen in the increased blue contribution. The improved blue response is also noteworthy because it suggests good collection properties in the interface region as well. This might also be
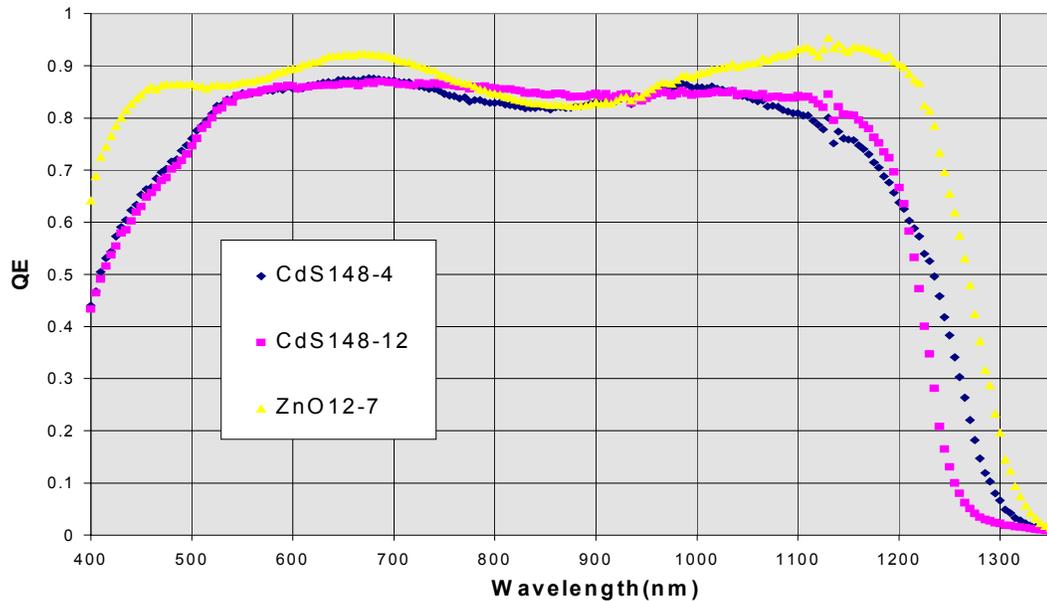
Figure 21. Comparison of QE response for CdS and ZnO devices.

expected to result in improved Voc and FF. However, as seen in Table 2, while these have been improved over our previous efforts, they are far below our benchmark values(Voc =.51, FF = .68) for CdS/CIGS devices with this band gap. In our most recent runs(26) we have further improved the interface properties to result in Voc's of .41 and FF's up to .56. We are thus encouraged that these values can approach those of our benchmark CdS devices.

The issue of the somewhat contradictory performance of the blue response and the surface parameters Voc and FF is one we now turn our attention to. Our phenomenological thinking is that Voc and FF are controlled by electron properties, while blue current is controlled by hole properties. The interface contains states that are determined by the details of both the semiconductor surface as well as the deposition parameters of the ZnO. It is not unreasonable that changes in these may affect hole and electron properties differently. We have just initiated our investigation of this issue and have only preliminary data at this time. One observation that we have made is that the ZnO/CIGS interface seems more susceptible to photoinduced shunting. As seen in figure 22, shunting in the dark is low for some devices. The slope in the light curve near Jsc, however, is suggestive of shunting which limits the FF to a value of .48. This suggests that the light induced shunting is caused by a different entity than dark shunting. As discussed previously (4), we have found capacitance techniques to be very helpful in studying shunting phenomena and have been using these techniques on these as well as CdS devices. There is a correlation between a component of photocapacitance and device performance. Thus the species being formed at the ZnO interface that is responsible for the shunt-like behavior is connected to the poor performance of Voc and FF. With further effort we expect to understand and gain control of this species to allow further advancements in overall device performance.
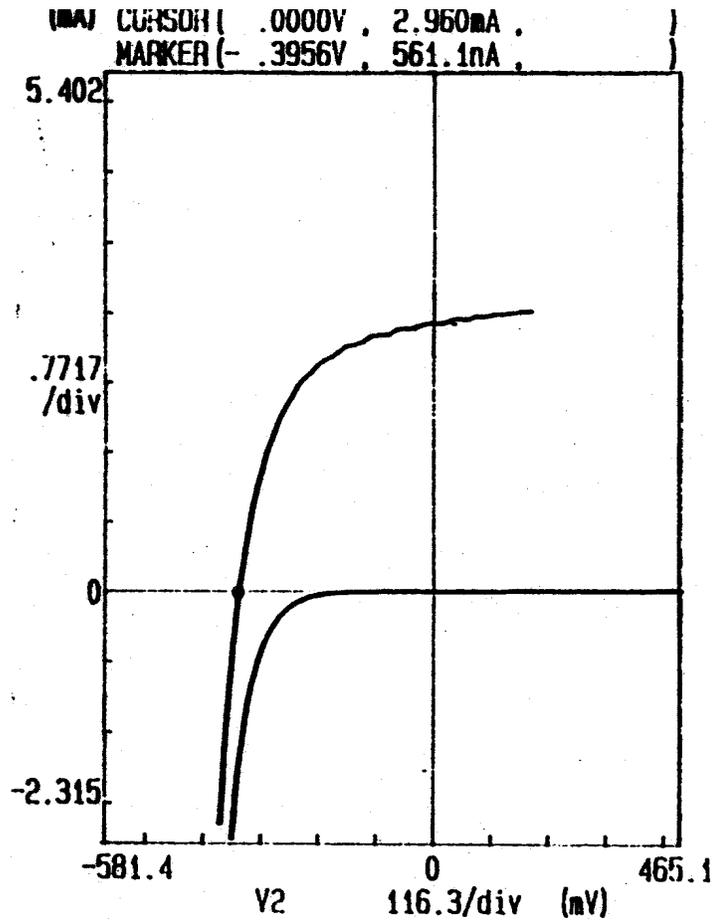

Figure 22. Dark and light IV curves for a ZnO/CIGS device indicating light induced shunting.

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13. ABSTRACT (Maximum 200 words). The main tasks of the cadmium telluride portion of this project include the development of simplified processing for fabricating high-efficiency CdTe solar cells, studies on the long-term stability of CdTe devices, and the development of alternative transparent conducting oxides, window layers, and back contacts.

The second portion of this project focused on CIGS solar cells. The main tasks include the development of a manufacturable process for CIGS devices and the development of high-band-gap alloys for use in tandem cell structures. Additional objectives include development of improved junction formation processing and contributing to the overall understanding of these materials and devices. Because our processing is manufacturing-driven, we use an all solid-state, simplified two-step process that relaxes the level of deposition control required.

14. SUBJECT TERMS
photovoltaics ; CdTe ; solar cell fabrication ; window layers ; back contacts ; transparent conducting oxides; vapor $CdCl_2$ treatment ; low temperature processing ; stability ; CIGS ; low band-gap devices ; high-band gap devices ; ZnO/CIGS junctions

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