



The Calibre tool suite offers a complete design-to-silicon solution to ensure a confident design for manufacturing.

Calibre Offers a Complete Design-to-Silicon Solution

A powerful hierarchical engine is at the heart of the Calibre tool suite, which offers a complete IC and SoC design-to-manufacturing solution. Each tool is an excellent point tool on its own, but the combination of Calibre DRC™, Calibre LVS™ and Calibre RVE™ (results viewing environment) with Calibre xRC™, Calibre RET and Calibre MDP, simplifies and strengthens the design flow.

Calibre xRC parasitic extraction tool accurately models the parasitic effects of passive interconnects that can cause design failure in deep submicron IC designs. Automated interfacing of Calibre LVS to Calibre xRC provides simplicity (one rule file, one invocation) and automated back annotation for accurate parasitic extraction results, and ensures accurate and intentional device extraction with parameter calculation and parasitic device extraction for accurate simulation.

Calibre Interactive™ complements the Calibre physical verification tool suite by enabling designers to perform verification from within Cadence Virtuoso® and Mentor Graphics IC Station™ and Calibre DESIGNrev™. Together with Calibre RVE, Calibre Interactive provides a seamless, push-button interface, enabling designers to use a single platform for cell/block and full-chip physical verification.

The Calibre RET tool suite for Optical and Process Correction (OPC), Phase Shift Mask (PSM), Scatter Bars (SB) and Off-Axis Illumination (OAI) deliver silicon accuracy, fastest turn-around-time and excellent yield.

Calibre MDP allows for seamless continuation of the data manipulations required for RET techniques to the mask data format conversion in one batch run, keeping data hierarchically represented as long as possible.

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