Compact Distributed RLC Interconnect Models—Part IV: Unified Models for Time Delay, Crosstalk, and Repeater Insertion

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***Abstract*—Using a new physical model for the transient response of a distributed resistance-inductance-capacitance (RLC) interconnect with a capacitive load, novel compact expressions have been derived for the 1) time delay, 2) peak crosstalk for coupled lines, 3) optimum number and size of repeaters, and 4) time delay for repeater-inserted distributed resistance–capacitance (RC) and RLC lines. These new models are used to define a design space that illustrates the tradeoff between the number of repeaters and wire cross-section for specified delay and crosstalk constraints.**

***Index Terms*—Crosstalk, delay effects, inductance, interconnections, repeaters, RLC circuits, time domain analysis, transmission line theory.**

I. Introduction

EARLIER work on distributed resistance-inductance-capacitance (RLC) interconnect models [1], [2] is extended in a companion paper [3] that describes a new physical model for the transient output voltage of a distributed RLC interconnect with a step input and a capacitive load. The inclusion of a load capacitance and wire inductance allows application of this model to evaluate effects of repeaters in high-speed global wires. The crosstalk models described in this work focus on modeling state-of-the-art global interconnect structures, where one or two signal interconnects are flanked by shielding power/ground lines and sandwiched between ground planes [3, Fig. 2.].

The comprehensive model for the transient response of a distributed RLC interconnect is derived in [3]. This model has been compared to H-simulation program with integrated circuit emphasis (HSPICE) simulations and is shown to have negligible error for a wide range of line parameters. It has also been extended to describe transient waveforms induced in two-coupled lines. The complete transient model can be expressed using just four normalized ratios (*basis variables*), which are defined as follows:

$$R_{\text{ratio}} = \frac{\text{line resistance}}{\text{characteristic impedance}} = \frac{rL}{Z_o}$$

$$C_{\text{ratio}} = \frac{\text{load capacitance}}{\text{line capacitance}} = \frac{C_L}{cL}$$

$$T_{\text{ratio}} = \frac{\text{time}}{\text{ToF}} = \frac{t}{t_f}$$

$$R_T = \frac{\text{driver output resistance}}{\text{characteristic impedance}} = \frac{R_{tr}}{Z_o} \tag{1}$$

where the time-of-flight (ToF) $t_f = L\sqrt{lc}$ is the time taken by a signal travelling at the speed of light in that medium to cover a distance equal to the length of the line. Interconnects with quite different line parameters such as length, size of driver, load and resistance, capacitance, and inductance per unit length may yet have similar basis variables. Hence, their transient characteristics will also be similar when represented using the normalized ratios. These dimensionless ratios will be used in this paper to describe interconnect properties such as time delay and crosstalk.

II. Unified Time Delay Model

The voltage at the end of a finite line with a capacitive termination for time $t \leq 3t_f$ is given by [3, (75)], and is rewritten as shown in (2) at the bottom of the next page, where

$$P = \frac{B\left(B+\sqrt{B^2+4}\right)}{\sqrt{B^2+4}}, \qquad Q = \frac{-B\left(B-\sqrt{B^2+4}\right)}{\sqrt{B^2+4}}$$

$$M = \frac{B+\sqrt{B^2+4}}{2}, \qquad N = \frac{B-\sqrt{B^2+4}}{2}$$

$$B = \frac{4l}{rC_LZ_o}. \tag{3}$$

Using the simplifications described in the Appendix, (2) can be approximated as

$$V_{fin}(L,\,t) = V_{dd}\frac{2Z_o}{Z_o+R_{tr}}e^{(-rt)/2l} \times \left[1-e^{-(1/C_LZ_o)(t-t_f)}\right]u_o(t-t_f). \tag{4}$$

Setting $t = t_f$ in (4), $V_{fin}(L, t_f) = 0$. This observation validates the theory that the presence of a load capacitance prohibits the voltage at the end of the line from changing instantaneously. The 50% time delay t_d is calculated by solving

$$V_{fin}(L,\,t_d) = \frac{V_{dd}}{2} \tag{5}$$

i.e.,

$$\frac{2Z_o}{Z_o+R_{tr}}e^{(-rt_d)/2l}\left[1-e^{-(1/C_LZ_o)(t_d-t_f)}\right]u_o(t_d-t_f) = \frac{1}{2}. \tag{6}$$

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The expression in (6) is an implicit equation for calculating the 50% time delay. Some special cases and further simplifications of this implicit expression are considered in the following sections.

A. Open Circuit Termination

The open circuit termination time delay $t_{d,\,oc}$ can be calculated by setting $C_L = 0$ in (6)

$$\frac{2Z_o}{Z_o + R_{tr}}\, e^{(-rt_{d,oc})/2l} u_o(t_{d,\,oc} - t_f) \geq \frac{1}{2}. \tag{7}$$

The equality sign in (6) has changed to an inequality in (7) because the absence of a load capacitance does not prevent the voltage from rising instantaneously. Therefore, at $t = t_{d,\,oc}$, $V_{fin}(L,\, t_{d,\,oc}) \geq V_{dd}/2$.

For $t_{d,\,oc} = t_f$, (7) can be simplified to

$$\frac{rL}{Z_o} \leq 2 \ln\left(\frac{4Z_o}{Z_o + R_{tr}}\right). \tag{8}$$

Since the left side of (8) is always non-negative, the following additional constraint is automatically imposed

$$R_{tr} \leq 3Z_o. \tag{9}$$

Equations (8) and (9) are the same conditions derived in [1] for ToF operation of a distributed RLC interconnect with an open-circuit termination.

B. Lossless Line With a Load Capacitance

The time delay of a lossless line $t_{d,\,lc}$ can be calculated by setting $r = 0$ in (6)

$$\frac{2Z_o}{Z_o + R_{tr}}\left[1 - e^{-(1/C_L Z_o)(t_{d,\,lc} - t_f)}\right] u_o(t_{d,\,lc} - t_f) = \frac{1}{2} \tag{10}$$

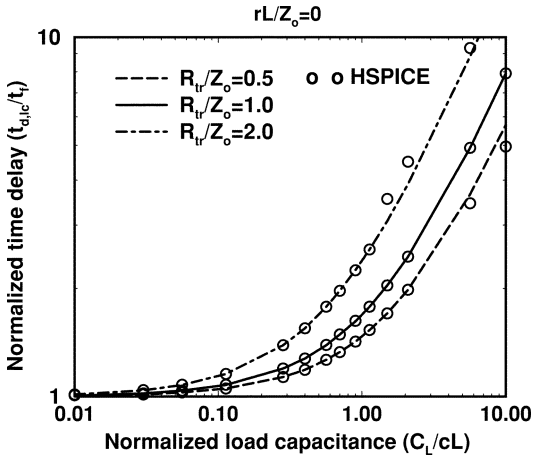

Fig. 1. Normalized time delay (t_d/t_f) versus normalized load capacitance (C_L/cL) for different values of normalized driver impedance (R_{tr}/Z_o) for a lossless line ($rL/Z_o = 0$).

that can be simplified to

$$t_{d,\,lc} = t_f + C_L Z_o \ln\left(\frac{4Z_o}{3Z_o - R_{tr}}\right). \tag{11}$$

Using a linear best-fit curve, (11) can be approximated as

$$t_{d,\,lc} \approx t_f + C_L\,(0.45R_{tr} + 0.25Z_o) \tag{12}$$

that can also be written using the "ratio notation" of (1) as

$$\frac{t_{d,lc}}{t_f} \approx 1 + \frac{C_L}{cL}\left(0.45\,\frac{R_{tr}}{Z_o} + 0.25\right). \tag{13}$$

Equations (12) and (13) give the time delay of a lossless line ("lc" line) with a load capacitance, and they are compared to HSPICE simulations in Fig. 1.

C. Lossy RLC Line With Load Capacitance

The normalized time delay, computed using the complete transient expressions in [3], is plotted against the normalized

$$\begin{aligned}
&V_{fin}(L,\, t_f < t < 3t_f) \\
&\quad = e^{(-rt)/2l} V'_{1A}(t) = V_{dd}\,\frac{Z_o}{Z_o + R_{tr}}\, e^{(-rt)/2l} \\
&\qquad \times \left\{ \begin{array}{l}
P\displaystyle\sum_{i=0}^{\infty}\left[(-M)^i \left(\frac{t - L\sqrt{lc}}{t + L\sqrt{lc}}\right)^{(i+1)/2} I_{i+1}\left(\frac{r}{2l}\sqrt{t^2 - L^2 lc}\right)\right] \\
\quad + Q\displaystyle\sum_{i=0}^{\infty}\left[(-N)^i \left(\frac{t - L\sqrt{lc}}{t + L\sqrt{lc}}\right)^{(i+1)/2} I_{i+1}\left(\frac{r}{2l}\sqrt{t^2 - L^2 lc}\right)\right] \\
\quad + \dfrac{P}{1 - G_s}\displaystyle\sum_{i=0}^{\infty}\sum_{u=1}^{\infty}\left[(-M)^i \left(4 - (1 + G_s)^2 G_s^{u-1}\right)\left(\frac{t - L\sqrt{lc}}{t + L\sqrt{lc}}\right)^{(i+u+1)/2} I_{i+u+1}\left(\frac{r}{2l}\sqrt{t^2 - L^2 lc}\right)\right] \\
\quad + \dfrac{Q}{1 - G_s}\displaystyle\sum_{i=0}^{\infty}\sum_{u=1}^{\infty}\left[(-N)^i \left(4 - (1 + G_s)^2 G_s^{u-1}\right)\left(\frac{t - L\sqrt{lc}}{t + L\sqrt{lc}}\right)^{(i+u+1)/2} I_{i+u+1}\left(\frac{r}{2l}\sqrt{t^2 - L^2 lc}\right)\right]
\end{array} \right\} u_o\left(t - L\sqrt{lc}\right)
\end{aligned} \tag{2}$$

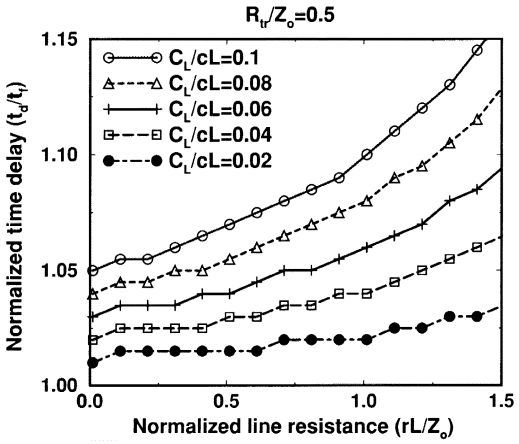

Fig. 2. Normalized time delay versus normalized line resistance for $R_{tr}/Z_o = 0.5$ and different values of C_L/cL, calculated using the complete transient model of [3].

line resistance in Fig. 2, showing an almost linear relationship between the two quantities. Therefore, the time delay expression in (13) can be rewritten for a lossy RLC line as

$$\frac{t_{d,\mathrm{rlc}}}{t_f} = 1 + \frac{C_L}{cL}\left(x\,\frac{rL}{Z_o} + 0.45\,\frac{R_{tr}}{Z_o} + 0.25\right) \tag{14}$$

or

$$t_{d,\,\mathrm{rlc}} = t_f + C_L\,(x\,rL + 0.45R_{tr} + 0.25Z_o) \tag{15}$$

where $x(C_L/cL)$ is the magnitude of the slope of the curves in Fig. 2.

To estimate the value of x, consider the resistance–capacitance (RC) delay model of [4] given by

$$t_{d,\,\mathrm{rc}} = 0.377rcL^2 + 0.693\,(R_{tr}cL + rLC_L + R_{tr}C_L)\,. \tag{16}$$

For a highly resistive line, the distributed RLC line model should give the same time delay as the RC line model, i.e., the models in (15) and (16) should converge to the same result. Assuming

$$rL \gg Z_o, \quad C_L \gg cL, \quad \text{and} \quad rL \gg R_{tr} \tag{17}$$

(15) will reduce to

$$t_{d,\,\mathrm{rlc}} \approx x\,rLC_L \tag{18}$$

and (16) will reduce to

$$t_{d,\,\mathrm{rc}} \approx 0.693rLC_L. \tag{19}$$

Comparing (18) and (19), it can be estimated that $x = 0.693$. Substituting this value in (15) and simplifying gives the approximate model for time delay of a distributed RLC line with load capacitance as

$$t_{d,\,\mathrm{rlc}} = t_f + 0.693C_L\,(rL + 0.65R_{tr} + 0.36Z_o)\,. \tag{20}$$

D. Unified Time Delay Model

In order to get a unified time-delay model for RC and RLC lines, (16) can be modified as

$$t_{d,\,\mathrm{rc}} = 0.377rcL^2 + 0.693R_{tr}cL + 0.693C_L \times\,(rL + 0.65R_{tr} + 0.36Z_o)\,. \tag{21}$$

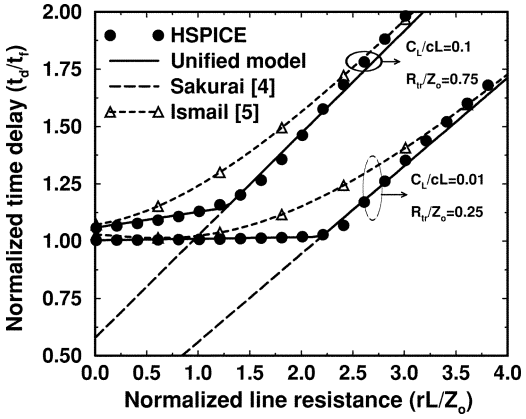

Fig. 3. Normalized time delay versus normalized line resistance for different values of R_{tr}/Z_o and C_L/cL for a step input.

(It was implicitly assumed in [4] that $R_{tr} = Z_o$; the modification in (21) has relaxed this assumption.) The actual time delay for a line is equal to the RC delay if resistance dominates, or is equal to the RLC delay if inductance dominates. Since every interconnect has a distributed inductance associated with it, the terms RC and RLC are only suggestive of whether the line is dominantly resistive or inductive. Hence, the more general case is the time delay model that will reduce to the RC delay if resistance dominates or to the RLC delay if inductance dominates. The time delay of an interconnect is the greater of the RC and RLC model delay i.e.,

$$t_d = \max\,(t_{d,\,\mathrm{rlc}},\, t_{d,\,\mathrm{rc}})\,. \tag{22}$$

Therefore, by comparing (20) and (21), *the unified expression for time delay can be written as*

$$t_d = \max\left(t_f,\ 0.377rcL^2 + 0.693R_{tr}cL\right) + 0.693C_L\,(rL + 0.65R_{tr} + 0.36Z_o)\,. \tag{23}$$

It can be interpreted from (23) that the time delay consists of two parts: a) time for the signal to reach the load end of the line, and b) time to charge up the load capacitance to $V_{dd}/2$. The time for signal propagation through the interconnect is dictated by ToF for RLC lines and by time to charge up the distributed line capacitance in RC lines. Therefore, in the "max" function, if ToF dominates, then the line behavior is inductive. Otherwise, it is a resistive line. The time taken to charge up the load capacitance, given by the second half of (23), is the same for both RC and RLC lines.

Using the ratio notation of (1), (23) can be rewritten as

$$\frac{t_d}{t_f} = \max\left(1,\ 0.377\,\frac{rL}{Z_o} + 0.693\,\frac{R_{tr}}{Z_o}\right) + 0.693\,\frac{C_L}{cL}\left(\frac{rL}{Z_o} + 0.65\,\frac{R_{tr}}{Z_o} + 0.36\right). \tag{24}$$

The normalized unified time-delay model (24) is plotted against the normalized line resistance for two different sets of values for C_L/cL and R_{tr}/Z_o in Fig. 3. It is easily deduced that the new unified time delay model has the best matching to HSPICE simulations compared to time delay models in [4] and [5]. For $0.1 \le rL/Z_o \le 5$, $0 \le C_L/cL \le 0.1$ and $0.25 \le R_{tr}/Z_o \le$

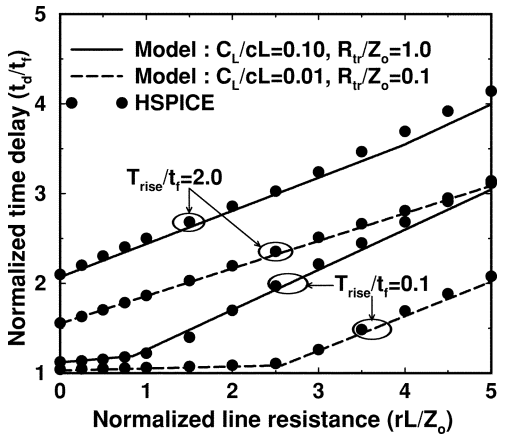

Fig. 4. Normalized time delay versus normalized line resistance for different values of R_{tr}/Z_o, C_L/cL, and $T_{\rm rise}/t_f$ for a ramp input.

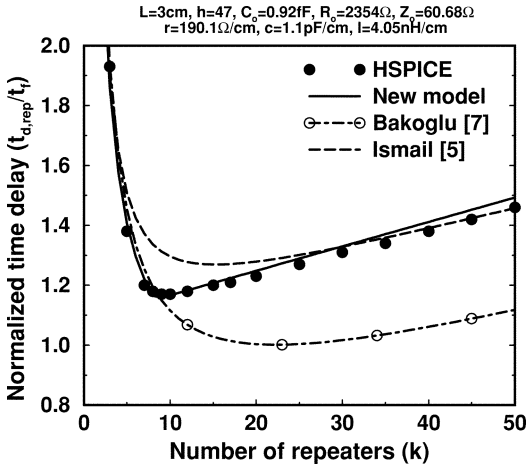

Fig. 5. Normalized delay versus number of repeaters for a 3-cm-long line. The new model has an error of about 2% when compared to HSPICE simulations, which is much better than models in [5] and [7].

1, the error between the unified models of (23) and (24) and HSPICE simulations is about 2%.

When the interconnect circuit is excited by a ramp input waveform with a finite rise time $T_{\rm rise}$, the unified model for the 50% time delay for RC and RLC lines is given by

$$t_d = \max\left(t_f + 0.15\,\frac{rL}{Z_o}\,T_{\rm rise},\ 0.377rcL^2 + 0.693R_{tr}cL\right) + 0.25\left(1+\frac{R_{tr}}{Z_o}\right)T_{\rm rise} + 0.693C_L\left(rL + 0.65R_{tr} + 0.36Z_o\right). \tag{25}$$

When $T_{\rm rise} = 0$ (for a step input), (25) reduces to (23), as expected. The derivation of (25) is described in [6]. Using the ratio notation, (25) can be written as

$$\frac{t_d}{t_f} = \max\left(1 + 0.15\,\frac{rL}{Z_o}\,\frac{T_{\rm rise}}{t_f},\ 0.377\,\frac{rL}{Z_o} + 0.693\,\frac{R_{tr}}{Z_o}\right) + 0.25\left(1+\frac{R_{tr}}{Z_o}\right)\frac{T_{\rm rise}}{t_f} + 0.693\,\frac{C_L}{cL}\left(\frac{rL}{Z_o} + 0.65\,\frac{R_{tr}}{Z_o} + 0.36\right). \tag{26}$$

The unified time-delay model for a ramp input (26) is plotted against normalized line resistance rL/Z_o for different sets of line parameters in Fig. 4. The model in (25) has a 2% error when compared with HSPICE simulations for $0.1 \le rL/Z_o \le 5$, $0 \le C_L/cL \le 0.1$, and $0.25 \le R_{tr}/Z_o \le 1$.

III. Repeater Insertion Models

Based on an analysis similar to [7], expressions for repeater insertion in distributed RLC lines are derived in this section.

A. Unified Time Delay Model for Repeater Insertion

Assume that k repeaters are inserted in a line of length L, and that the width of each repeater is h times minimum feature size. Also, let the output resistance and input capacitance of a minimum-sized repeater be R_o and C_o, respectively. Using (20), the time delay (RLC model) of the line is given by

$$t_{d,\,\rm rlc\_rep} = k\left[\frac{t_f}{k} + 0.693hC_o\left(\frac{rL}{k} + 0.65\,\frac{R_o}{h} + 0.36Z_o\right)\right]. \tag{27}$$

Simplifying

$$t_{d,\,\rm rlc\_rep} = t_f + 0.693C_o\left(hrL + 0.65kR_o + 0.36hkZ_o\right). \tag{28}$$

Similarly, the RC time delay model for a repeater-inserted line can be written using (21) as

$$t_{d,\,\rm rc\_rep} = \left(0.377\,\frac{rcL^2}{k} + 0.693\,\frac{R_ocL}{h}\right) + 0.693C_o\left(hrL + 0.65kR_o + 0.36hkZ_o\right). \tag{29}$$

Comparing (28) and (29), *the unified time delay expression for a line with repeaters can be written as*

$$t_{d,\,rep} = \max\left(t_{d,\,\rm rlc\_rep},\ t_{d,\,\rm rc\_rep}\right) \tag{30}$$

or

$$t_{d,\,rep} = \max\left(t_f,\ 0.377\,\frac{rcL^2}{k} + 0.693\,\frac{R_ocL}{h}\right) + 0.693C_o\left(hrL + 0.65kR_o + 0.36hkZ_o\right). \tag{31}$$

The "max" function in (31) can be used to distinguish between the RC and the RLC regions. Therefore, if the ToF for an interconnect segment is greater than the RC charging time for its distributed line capacitance, i.e.,

$$0.377\,\frac{rcL^2}{k} + 0.693\,\frac{R_ocL}{h} \le t_f \tag{32}$$

or

$$0.377\,\frac{rL}{kZ_o} + 0.693\,\frac{R_o}{hZ_o} \le 1 \tag{33}$$

the line behavior is inductive; otherwise, it is resistive, as is borne out by the "max" function in (31).

The unified time-delay model in (31) is compared to the delay models in [5] and [7] in Fig. 5, in which the normalized time delay is plotted against number of repeaters for a 3-cm-long in-

terconnect. The delay calculated by HSPICE simulations is also shown in Fig. 5. The "knee" in the curves of Fig. 5 is the transition from the RC to the RLC region, which is determined by the inequality in (33). In the region where RLC models are to be used, Bakoglu's models [7] severely underestimate the actual delay, due to violation of ToF constraint. Ismail and Friedman's model [5] for time delay has a good fit to HSPICE simulations only at the extremities, since it is a curve-fitted model. The best fit to the HSPICE simulations is given by the new unified model for repeater insertion in RC and RLC lines, which has a maximum error of about 2%. It is evident from Fig. 5 that the delay is minimized at the boundary between the RC and RLC regions. This is the "optimal" repeater insertion design, and it is investigated in the next section.

B. Optimal Repeater Insertion

It can be interpreted from (31) that for a constant size of repeaters, it is not desirable to insert a greater number of repeaters than necessary for ToF operation of the interconnect segments between each pair of repeaters. This is because adding more repeaters increases total time delay by increasing repeater delay without decreasing interconnect delay. Similarly, it is not desirable to increase the size of repeaters for a constant repeater count once ToF operation is achieved for the interconnect segments. *Therefore, optimal repeater insertion would entail inserting just the sufficient number (and size) of repeaters to operate at the boundary of RC and RLC regions.* This implies that the condition for RC and RLC regions of operation (33) should be satisfied in the equality, i.e.,

$$0.377\,\frac{rL}{kZ_o} + 0.693\,\frac{R_o}{hZ_o} = 1. \tag{34}$$

Solving (34) for h, one gets

$$h = \frac{0.693kR_o}{kZ_o - 0.377rL}. \tag{35}$$

Substituting (35) in (31) and setting the derivative of time delay with respect to k equal to 0 gives the optimum number of repeaters $k_{opt,\,\mathrm{rlc}}$. Substituting this value in (35) gives the optimum size of repeaters $h_{opt,\,\mathrm{rlc}}$

$$k_{opt,\,\mathrm{rlc}} = 0.9513\,\frac{rL}{Z_o} \quad \text{and} \quad h_{opt,\,\mathrm{rlc}} = 1.1479\,\frac{R_o}{Z_o}. \tag{36}$$

Substituting (36) into (31) gives the optimum time delay as

$$t_{d\_opt,\,\mathrm{rlc}} = t_f + 1.496\,\frac{rLR_oC_o}{Z_o}. \tag{37}$$

Using the ratio notation of (1), the optimum time delay in (37) can be written as

$$\frac{t_{d\_opt,\mathrm{rlc}}}{t_f} = 1.0 + 1.496\,\frac{rL}{Z_o}\cdot\frac{C_o}{cL}\cdot\frac{R_o}{Z_o}. \tag{38}$$

The optimum number and size of repeaters derived using RC models in [7] are given by

$$k_{opt,\,\mathrm{rc}} = \sqrt{\frac{0.377rcL^2}{0.693R_oC_o}} \quad \text{and} \quad h_{opt,\,\mathrm{rc}} = \sqrt{\frac{R_oc}{C_or}} \tag{39}$$

and the corresponding optimum time delay is

$$t_{d\_opt,\,\mathrm{rc}} = 2.5\sqrt{R_oC_orcL^2}. \tag{40}$$

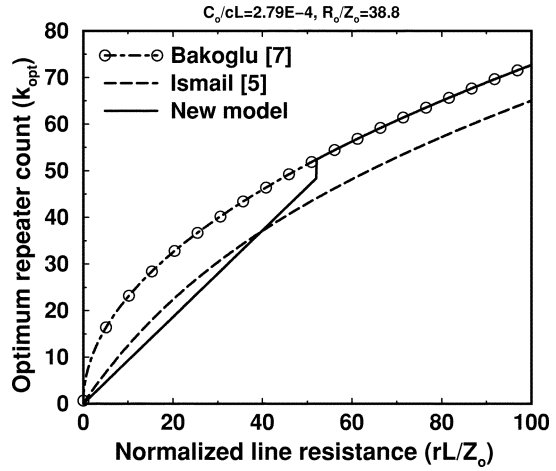

Fig. 6. Optimum number of repeaters versus normalized line resistance rL/Z_o. The smaller number of repeaters predicted by the new model reduces via blockage and repeater power dissipation.

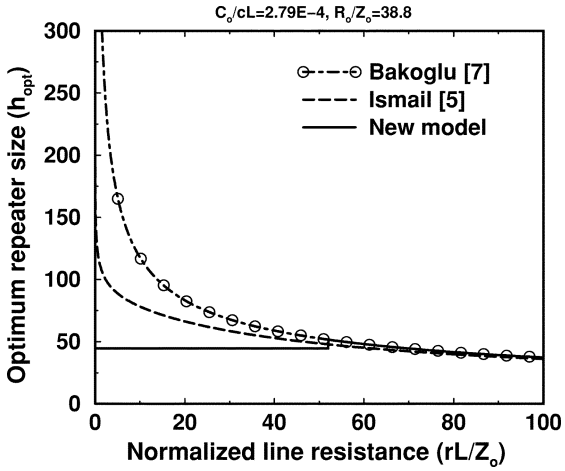

Fig. 7. Optimum size of repeaters versus normalized line resistance rL/Z_o. The smaller size of repeaters predicted by the new model leads to considerable saving in on-chip repeater area.

If the repeaters are designed using the optimum RC models in (39), there is a possibility of violating the ToF constraint—in which case the optimum time delay in (40) will underestimate the actual delay of the line. The boundary condition for the validity of the repeater models is obtained by substituting (39) in (33), giving the following condition for optimum repeater insertion

Condition I: "If $1.332\sqrt{rlR_oC_o/Z_o} \leq 1$ *use optimum RLC repeater insertion equations in (36) and (37); otherwise, use optimum RC repeater insertion equations in (39) and (40)."*

Condition I implies that the number and size of repeaters that will minimize total delay of the interconnect and its repeaters is either the optimum RC design, or the optimum RLC design, depending on the line characteristics such as length and resistance per unit length. For example, the optimal RLC design may result in a greater delay compared to the optimum RC design for a long and highly resistive line, because of the delay of the large number of repeaters required to achieve ToF operation for the interconnect segments. The optimum number of repeaters and size of repeaters is plotted against normalized line resistance rL/Z_o in Figs. 6 and 7, respectively. The new model ad-

vocates a smaller optimum number and size of repeaters, which leads to considerable reduction in on-chip repeater area, repeater power dissipation and via blockage. On the other hand, using the Bakoglu (RC) optimum size and number for the repeaters might result in a greater time delay, compared to using the RLC optimum size and number of repeaters.

IV. Crosstalk in Two Coupled Lines

A novel combination of the distributed RLC line analysis for the transient voltage induced in the quiescent line, and a lumped element circuit representation for the charge up of the load capacitance is used to derive a compact crosstalk model.

For a simple RC charging circuit [Fig. 8(a)], the output voltage (V_o) and 50% rise time ($t_{d,\,50\%}$) are given by

$$V_o(t) = V_{dd}\left(1 - e^{-(t/RC)}\right) \tag{41}$$

and

$$t_{d,\,50\%} = 0.693RC. \tag{42}$$

Comparing (20) and (42), the transients induced in the quiescent distributed RLC line can be approximated as an RC charging of the load capacitance. The equivalent lumped element circuit model of the quiescent RLC line can be represented by Fig. 8(b), where the effective impedance in the current path is

$$R = rL + 0.65R_{tr} + 0.36Z_o \tag{43}$$

and the magnitude of the voltage source (V_{fin}) is equal to the voltage induced at a point on the quiescent distributed RLC line that is just before the load capacitance. This voltage can be modeled as $V_{inf}(x = L, t = t_f)$, the voltage induced at $x = L$ in an infinitely long quiescent line at $t = t_f$ [2]. It is the difference between the common and differential mode solutions to the decoupled partial differential equation system. Therefore, V_{fin} can be written as

$$\begin{aligned} V_{fin} &= V_{inf}(x = L, t = t_f) \\ &= V_{dd}\left(\frac{e^{-(rL/2Z_o^+)}}{1 + \frac{R_{tr}}{Z_o^+}} - \frac{e^{-(rL/2Z_o^-)}}{1 + \frac{R_{tr}}{Z_o^-}}\right). \end{aligned} \tag{44}$$

Therefore, the voltage across the load capacitor of the quiescent line can be written as

$$V_Q(t) = V_{fin}\left(1 - \exp\left(-\frac{t - t_f}{C_L(rL + 0.65R_{tr} + 0.36Z_o)}\right)\right) \times u_o(t - t_f). \tag{45}$$

Assume that the peak crosstalk occurs at $t = t_{\rm peak}$, when the derivative of (45) with respect to t is equal to slope S. It was observed experimentally that the error is minimal for $|S| = |0.5/t_f|$. Solving

$$\left|\frac{\partial V_Q(t)}{\partial t}\right| = \left|\frac{0.5V}{t_f}\right| \tag{46}$$

for $t_{\rm peak}$ gives

$$t_{\rm peak} = t_f + C_L\,(rL + 0.65R_{tr} + 0.36Z_o) \times \ln\left(\frac{V_{fin}}{\frac{0.5}{t_f}\,C_L\,(rL + 0.65R_{tr} + 0.36Z_o)}\right). \tag{47}$$

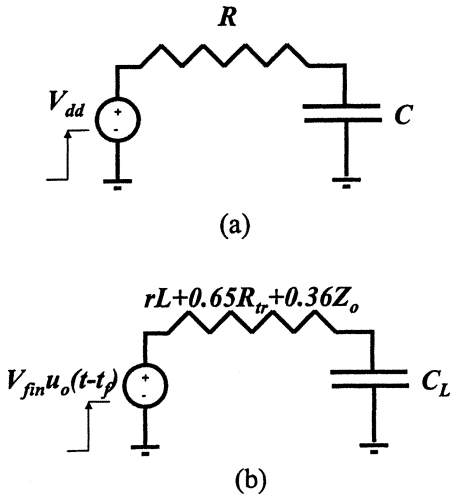

Fig. 8. (a) Typical RC charging circuit (b) equivalent circuit representation used for approximate crosstalk model.

Substituting (47) in (45) gives the peak crosstalk $V_{p,\,\rm rlc}$

$$V_{p,\,\rm rlc} = V_{fin} - \frac{0.5}{t_f}\,C_L\,(rL + 0.65R_{tr} + 0.36Z_o). \tag{48}$$

For distributed RC lines with a load capacitance, Sakurai [4] provides the following expression for peak crosstalk

$$V_{p,\,\rm rc} = -K_1 V_{dd}\left(\frac{1}{1 + 2\eta}\right)^{1/2\eta}\left(\frac{\eta}{1 + 2\eta}\right) \tag{49}$$

where

$$K_1 = -1.01\,\frac{R_T + C_T + 1}{R_T + C_T + \pi/4} \tag{50}$$

and

$$R_T = \frac{R_{tr}}{rL}, \quad C_T = \frac{C_L}{cL} \quad \text{and} \quad \eta = \frac{c_c}{c} \tag{51}$$

where c_c is the coupling or mutual capacitance per unit length. (Note that the negative sign in (49) is missing in the model in [4].) However, this expression is not very accurate for RC lines with large load capacitance. In order to get a more accurate expression, we will use the same method used to get the compact crosstalk expression for RLC lines, but base it on Sakurai's models for RC lines. From this analysis, the new RC expression for crosstalk can be written as

$$\begin{aligned} V_{p,\,\rm rc} = &-0.58V_{dd}\,\frac{R_T + C_T + 1}{R_T + C_T + \pi/4} \\ &\times \left[\begin{array}{l} \exp\left(-\dfrac{1.04}{R_TC_T + R_T + C_T + (2/\pi)^2}\right) \\ -\exp\left(-\dfrac{1.04}{R_TC_T + R_T + C_T + (2/\pi)^2}\,\dfrac{1}{1 + 2\eta}\right) \end{array}\right] \\ &- \frac{0.05}{t_f}\,C_L\,(rL + 0.65R_{tr} + 0.36Z_o). \end{aligned} \tag{52}$$

The RLC (48) and RC (52) crosstalk models are unified by the following condition:

Condition II: "*If* $L \le L_{\max}$, $V_{\rm peak} = V_{p,\,\rm rlc}$, *else* $V_{\rm peak} = \max(V_{p,\,\rm rlc},\, V_{p,\,\rm rc})$ *where* $L_{\max}$ *is the solution of* $\partial V_{p,\,\rm rlc}/\partial L = 0$".The normalized peak crosstalk is plotted against the normalized line resistance for different values of R_{tr}/Z_o and C_L/cL

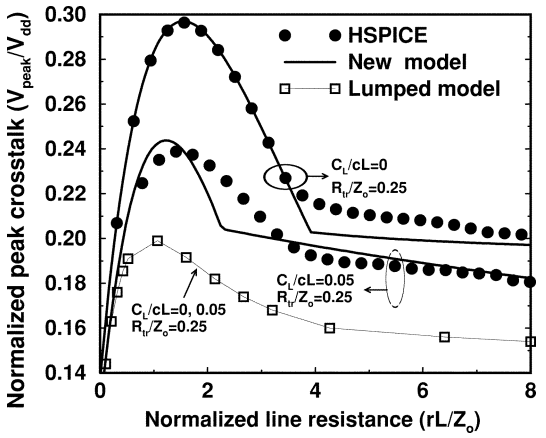

Fig. 9. Normalized peak crosstalk versus normalized line resistance for different values of R_{tr}/Z_o and C_L/Z_o.

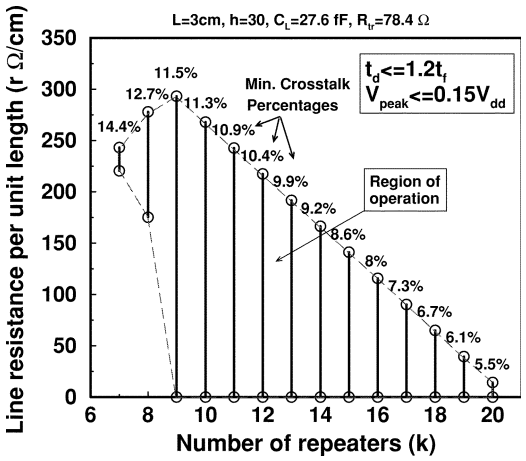

Fig. 10. Design plane—line resistance versus number of repeaters—for delay $<=1.2t_f$ and peak crosstalk $<=$ 15% of V_{dd}. For any particular number of repeaters, there is a range of line resistances that satisfy the delay and crosstalk constraints. The region of operation is enclosed by an envelope.

in Fig. 9, which compares Condition II with HSPICE simulations of a distributed RLC line, as well as with a lumped element model similar to [8]. The error between Condition II and HSPICE is less than 10% for practical values of $0.1 \leq rL/Z_o \leq 5$, $0 \leq C_L/cL \leq 0.1$, and $0.25 \leq R_{tr}/Z_o \leq 1$.

V. Delay-Crosstalk Design Space

Inserting repeaters in global interconnects can cause 1) an increase in C_L/cL for each interconnect segment by adding load capacitance and decreasing the line capacitance (because the segment length is shorter than total wire length) and 2) reduce propagation delay. By reducing wire cross-sectional area (increasing wire resistance), the inductive effects can be mitigated resulting in a decrease in inductive crosstalk. However, the higher line resistance causes propagation delay to increase. An optimal combination of repeater insertion and reduced wire cross-sectional area would decrease inductive crosstalk and wiring area, while maintaining constant delay. In fact, for a target delay and peak crosstalk, there is a range of permissible wire resistances (cross-sectional areas) for each number of repeaters (Fig. 10). The upper limit of each range, determined by the delay constraint, maximizes wiring density and minimizes crosstalk, while the lower limit, determined by the crosstalk constraint, minimizes propagation delay. Thus, the specified design constraints on maximum permissible time delay and crosstalk delineate a feasible region in the "per unit length line resistance—repeater count" design plane in Fig. 10.

The other design decision that can be aided by Fig. 10 is determining how many repeaters to use to balance crosstalk and time delay, if the interconnect geometries are fixed. Fig. 11 shows the tradeoff between crosstalk and time delay versus number of repeaters for a fixed r (or wire cross-sectional area). For a 3-cm-long line, inserting two repeaters would decrease time delay but increase crosstalk (point A). This illustrates the fact that unless interconnect repeater circuits are carefully designed, inserting repeaters to reduce delay could increase crosstalk. However, when ten repeaters are inserted (point B), then the peak crosstalk decreases by 48% with only a 6% delay penalty, compared to point A. Table I illustrates a carefully planned repeater circuit design that inserts eight repeaters in a 3-cm-long global interconnect, thereby reducing peak crosstalk by 51%,

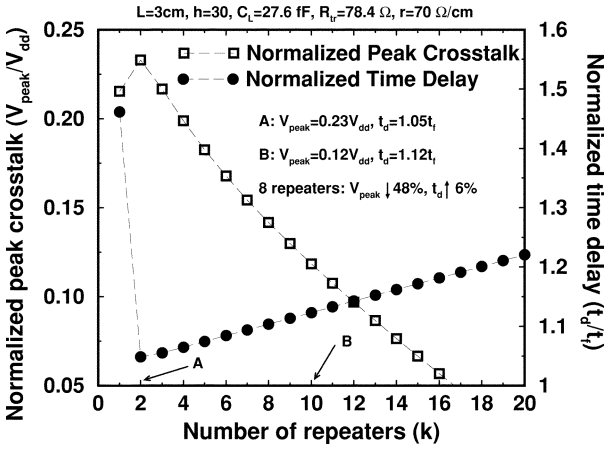

Fig. 11. Crosstalk and delay versus number of repeaters, for fixed r = 70 Ω/cm. Inserting eight repeaters (B) decreases crosstalk by 48% and increases time delay by 6%, compared to inserting two repeaters (A).

TABLE I
Using Repeaters Decreases Crosstalk (and Increases Wiring Density) Without Penalizing Time Delay

# of rep + driver	r (Ω/cm)	Time delay	Peak crosstalk
1	48.9	$1.2t_f$	23.4%
9	293.5	$1.2t_f$	11.5%

and wiring cross-sectional area by 83% without any additional delay penalty, when compared to a line without repeaters.

VI. Conclusion

New compact expressions for time delay, repeater insertion and crosstalk in distributed RLC lines with capacitive load have been presented. For some practical ranges of the line parameters, the error is approximately 2%, 2%, and 10% for time delay, repeater insertion and crosstalk, respectively, when compared to HSPICE simulations. In addition, it is shown that intelligent

repeater insertion, with the aid of these new physical models, can reduce crosstalk by 51% and wiring cross-sectional area by 83% without increasing delay compared to a reverse-scaled, single-driver circuit.

APPENDIX
EXPRESSION FOR 50% TIME DELAY MODEL

Let $V_{fin}(L,\, t_d) = V_{dd}/2$, i.e., $t = t_d$ is the 50% time delay. Since t_d is close to t_f, $t_d - t_f \ll t_f$. For small arguments $x \ll n$, the modified Bessel function can be approximated as [9]

$$I_n(x) \approx \frac{1}{n!}\left(\frac{x}{2}\right)^n, \qquad n > 0. \tag{53}$$

Using (53) and exponential series expansion, the first term in the parenthesis in (2) can be approximated as

$$P\sum_{i=0}^{\infty}\left[(-M)^i\left(\frac{t-L\sqrt{lc}}{t+L\sqrt{lc}}\right)^{(i+1)/2} I_{i+1}\left(\frac{r}{2l}\sqrt{t^2-L^2lc}\right)\right] \approx \frac{-P}{M}\left[e^{-M(r/4l)(t-L\sqrt{lc})}-1\right]. \tag{54}$$

Similarly, the remaining terms in parenthesis in (2) can be approximated as

$$Q\sum_{i=0}^{\infty}\left[(-N)^i\left(\frac{t-L\sqrt{lc}}{t+L\sqrt{lc}}\right)^{(i+1)/2} I_{i+1}\left(\frac{r}{2l}\sqrt{t^2-L^2lc}\right)\right] \approx \frac{-Q}{N}\left[e^{-N(r/4l)(t-L\sqrt{lc})}-1\right] \tag{55}$$

$$\frac{P}{1-G_s}\sum_{i=0}^{\infty}\sum_{u=1}^{\infty}\left[(-M)^i\left(4-(1+G_s)^2G_s^{u-1}\right)\times\left(\frac{t-L\sqrt{lc}}{t+L\sqrt{lc}}\right)^{(i+u+1)/2} I_{i+u+1}\left(\frac{r}{2l}\sqrt{t^2-L^2lc}\right)\right] \approx \frac{P(3+G_s)}{M^2}\left[e^{-M(r/4l)(t-t_f)}-1+M\frac{r}{4l}(t-t_f)\right] \tag{56}$$

and

$$\frac{Q}{1-G_s}\sum_{i=0}^{\infty}\sum_{u=1}^{\infty}\left[(-N)^i\left(4-(1+G_s)^2G_s^{u-1}\right)\times\left(\frac{t-L\sqrt{lc}}{t+L\sqrt{lc}}\right)^{(i+u+1)/2} I_{i+u+1}\left(\frac{r}{2l}\sqrt{t^2-L^2lc}\right)\right] \approx \frac{Q}{(1-G_s)}\left[4\left(e^{(r/4l)(t-t_f)}-1-\frac{r}{4l}(t-t_f)\right)-\left(\frac{1+G_s}{G_s}\right)^2\left(e^{G_s(r/4l)(t-t_f)}-1-G_s\frac{r}{4l}(t-t_f)\right)\right]. \tag{57}$$

Typically, $B \gg 1$. Therefore, from (3), $P \approx 2B$, $M \approx B$, $Q \approx 2/B$ and $N \approx -1/B$. Since $P \gg 1$, $M >> 1$, $Q \ll 1$ and $N \ll 1$, the approximations in (55)–(57) can be neglected in comparison to (54). Also, $P/M \approx 2$. Setting $t_f = L\sqrt{lc}$ and $M = 4l/rC_LZ_o$, (54) can be used to approximate (2) as

$$V_{fin}(L,\, t) = V_{dd}\frac{2Z_o}{Z_o+R_{tr}}e^{(-rt)/2l}\left[1-e^{-(1/C_LZ_o)(t-t_f)}\right]\times u_o(t-t_f). \tag{58}$$

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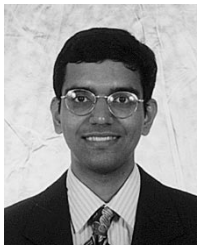

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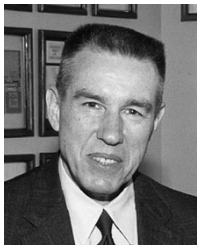

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